

# DESIGN AND CONSTRUCTION OF A CONFIGURABLE FULL-FIELD RANGE IMAGING SYSTEM FOR MOBILE ROBOTIC APPLICATIONS

D.A. Carnegie<sup>1</sup>, J.R.K. McClymont<sup>1</sup>, A.P.P. Jongenelen<sup>1</sup>, B. Drayton<sup>1</sup>,  
A.A. Dorrington<sup>2</sup> and A.D. Payne<sup>2</sup>

<sup>1</sup>School of Engineering and Computer Science,  
Victoria University of Wellington, Wellington, New Zealand,

<sup>2</sup>Department of Engineering,  
University of Waikato, Hamilton, New Zealand.

## ABSTRACT

Mobile robotic devices rely critically on extrospection sensors to determine the range to objects in the robot's operating environment. This provides the robot with the ability both to navigate safely around obstacles and to map its environment and hence facilitate path planning and navigation. There is a requirement for a full-field range imaging system that can determine the range to any obstacle in a camera lens' field of view accurately and in real-time. This paper details the development of a portable full-field ranging system whose bench-top version has demonstrated sub-millimetre precision. However, this precision required non-real-time acquisition rates and expensive hardware. By iterative replacement of components, a portable, modular and inexpensive version of this full-field ranger has been constructed, capable of real-time operation with some (user-defined) trade-off with precision.

## 1. INTRODUCTION

Mobile robotic devices are critically dependent upon extrospective sensors in order to be able to operate in an environment. Specifically, accurate range finding is required in order to be able to negotiate around obstacles, map the environment and implement efficient path planning. Such ranging needs to not only be accurate, but also able to be acquired in real-time with a high field-of-view coverage.

Infrared ranging is often used for close-range obstacle avoidance and has become increasingly popular with the development of the inexpensive Sharp GP2 range of analogue and digital detectors [1]. However, such sensors are limited in range and are seldom reliable past 3 metres or so. Ultrasonic techniques are often employed when ranging to ~10 metres (dependent upon the carrier frequency) however they suffer significantly from the broadness of the transmitted

beam, exacerbated by the comparative difficulty in focussing an acoustic rather than an EM wave. Subsequently for this technique to be of use in mobile robotic ranging and mapping, considerable software processing is often required to counter the multiple path reflections. Furthermore, because of the inherent dead-band, ultrasound must often be augmented by an IR sensor for close range obstacle detection.

The limited range of these techniques is a significant impediment to mobile operation in a large open environment, and hence laser-based ranging using a projected dot or line is often employed. Sick [2] (for example) are a major supplier of such laser based systems and produce a variety of devices with fields of view ranging from 70° through to 360°. The wider fields of view are achieved at the expense of lower acquisition rates or significantly greater cost. Whilst precision to the millimetre level is obtainable, this is normally only achievable if range is significantly compromised. Consequently, laser scanning systems that provide an acceptable compromise between long range, good precision, wide field of view and low acquisition times are typically extremely expensive and outside the budget of many mobile robot projects. Certainly this expense often precludes their incorporation into commercial devices.

A niche exists for the development of a ranging system that provides a wide field of view, high precision, and a short acquisition time. Furthermore, such a system would ideally be able to alter its field of view simply by changing the lens or incorporating a telephoto system adjustable by the user (or autonomously by the robot) during range acquisition.

These requirements can be satisfied by a Full-Field Range Imaging System (FFRIS), whereby the range to every object in a field of view (determined by an optical lens) can be obtained simultaneously. A specific requirement by the authors is to obtain a FFRIS that can be mounted on robots in their mobile robotic fleet, three of which are pictured in Figure 1. Ideally this FFRIS could be used in both an indoor and an outdoor environment.



Figure 1. Robotic platforms requiring extrospective sensors, (a) MARVIN an indoor security robot, (b) two robots designed for urban search and rescue applications

The authors believe it is instructive to relate the development of our successful FFRIS in terms of the successive design iterations that addressed particular problems or limitations that were identified at each stage in the development process. We hope that such a description will aid the reader in appreciating the problems inherent in the development of full-field ranging

systems and hence understand the justification of the techniques and components selected for this particular implementation. In the process, we hope that the reader gains an added appreciation of full-field ranging techniques, image capture devices, high frequency modulatable illumination sources and drivers, FPGAs as embedded control systems, external memory requirements and interfacing, and power supply issues. This list is too exhaustive to cover any one topic in much detail given these space constraints, but the integration of these into a complete functional system forms the basis of this work.

To begin the discussion, the next section will outline the theory behind FFRIS operation. Section 3 details the requirements of a FFRIS that would make such a device useful for mobile robotics. Section 4 discusses an initial design solution that successfully implemented full-field ranging but could not be employed on mobile robots because of its cost, bulk, power requirements and long acquisition times. Section 5 provides a solution to many of these problems, but still resulted in a system that had to be bench-mounted. The successful device is presented in detail in section 6, where a modular, robust, compact and inexpensive FFRIS is constructed. The chapter concludes with the results of this new device.

## 2. PRINCIPLES OF FULL-FIELD IMAGE RANGING

Many techniques exist for determining the distance to an object using an optical source, including:

- passive stereo and photogrammetry,
- active triangulation and structured light,
- interferometry,
- direct and indirect time-of-flight (ToF)

Space does not permit a full discussion of the merits of each of these techniques and the reader is referred to numerous books and articles which review these techniques. The FFRIS utilises an indirect time-of-flight measurement technique over a field of view determined by the optics of a standard camera lens and therefore the following discussion is limited to an introduction of the ToF method. The images presented in Figures 2 to 4 below are extracted from [4].

A direct time-of-flight system records the time for a pulse of light to be emitted, reflected off an object and returned to a receiver placed adjacent to the illumination source as illustrated in Figure 2. These systems can be point, line, or full-field scanning or full-field non-scanning depending upon the configuration of the source and sensor. Distance  $d$  is simply determined by

$$d = \frac{ct}{2}$$

Equation 1

where  $t$  is the total flight time and  $c$  is the speed of light.

A significant problem with such systems is that the distance resolution is critically dependent on the resolution of the timer. For example, to obtain 1 cm distance resolution the timer must be able to resolve the returned pulse to within 66 ps. The expense and complexity of the electronics required to achieve this resolution renders such systems of questionable value for most range determination applications

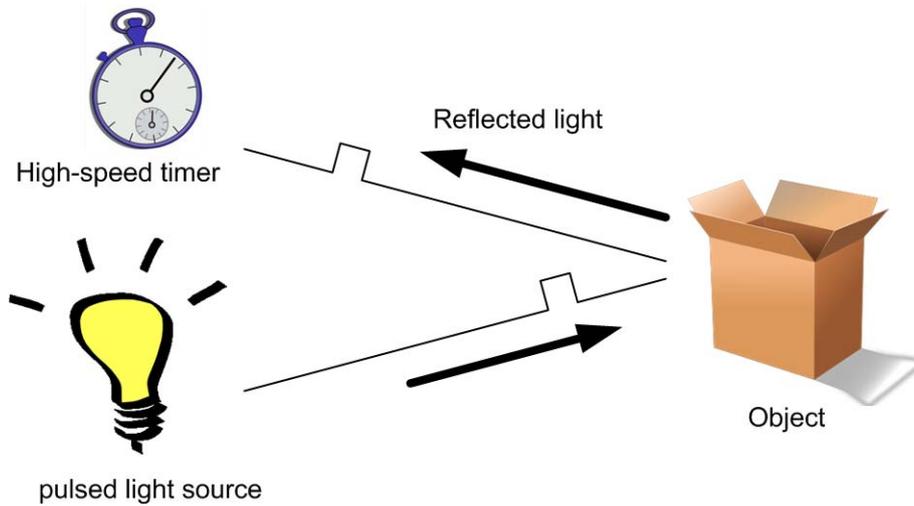


Figure 2. Principle of distance determination using direct time-of-flight.

To overcome the high bandwidth requirements of the direct ToF method, a number of techniques exist that encode the distance information indirectly, often through amplitude or phase. For example in [4] a light source and a high-speed shutter are pulsed at the same frequency as illustrated in Figure 3. There will be a delay in the light reaching the shutter that is proportional to the object's distance. As indicated in Figure 4, objects that are nearer to the illumination/shutter system will have a higher proportion of the reflected pulse pass into the image sensor than objects that are more distant. The intensity of the received light can therefore be used as an indicator of object distance. However this intensity may also be affected by changes in object orientation, reflectivity and ambient lighting, and these effects need to be eliminated by appropriate system normalisation.

An alternative technique is a heterodyne approach where intensity modulated light at frequency  $f_m$  is projected onto a scene and the receiving camera shutter is modulated at a slightly different frequency  $f_s = f_m + \delta$ . The modulation frequency  $f_m$  is in the range 10 MHz – 100 MHz, and  $\delta$  is typically 1 – 5 Hz. These signals are effectively mixed and integrated by the camera system to produce a beat signal of frequency  $\delta$ .

The light received at the camera has a phase offset of the modulation envelope introduced due to the time taken for the light to travel twice the distance from the imaging system to the object. Calculating distance then becomes an issue of accurately determining the phase offset  $\phi$  of the signal at the beat frequency  $\delta$ . Distance is related to the phase offset by:

$$d = \frac{\phi}{4\pi} \frac{c}{f_m} \quad \text{Equation 2}$$

The phase offset  $\phi$  can be determined by a variety of techniques including the Discrete Fourier Transform and an inner-product method. Space constraints restrict a more detailed review of the theory and implementation of full-field ranging systems. The interested reader is referred to reviews of such systems in [5] or the more detailed descriptions of the techniques we employ in [6-10] or further theoretical treatment in [11].

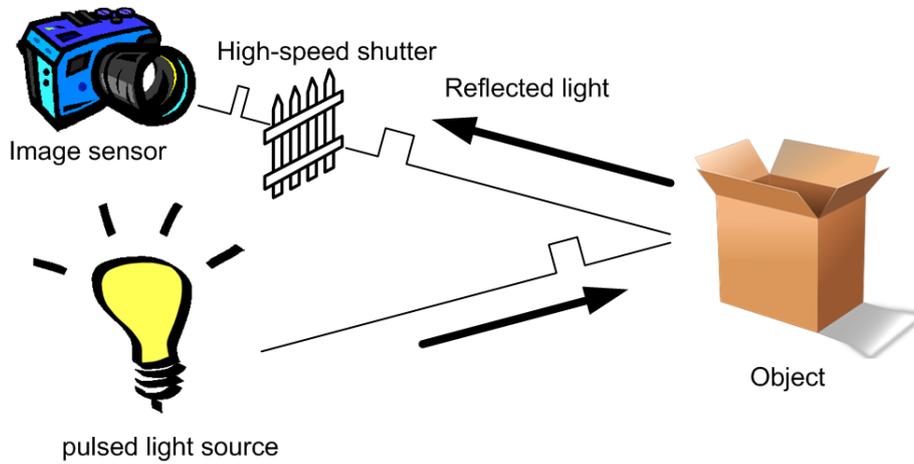


Figure 3. Principle of distance determination using direct time-of-flight.

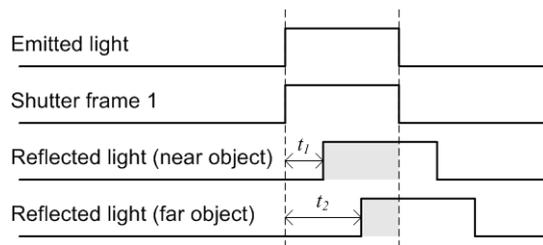


Figure 4. Principle of distance determination using direct time-of-flight.

FFRIS devices currently on the market include systems developed by PMDTechnologies [12], Mesa Imaging [13] and Cantesa [14], with two typical examples illustrated in Figure 5. Our bench-top system has demonstrated several advantages over the offerings from either of these manufacturers particularly in terms of configurability and versatility. This will be explained in subsequent sections.



Figure 5. (Left) Cam Cube 3-D Range Imaging Camera from PMDTechnologies [12] (Right) SR4000 Range Imaging Camera from Mesa Imaging [13]

### **3. FULL FIELD RANGE IMAGING SYSTEM REQUIREMENTS**

As discussed in the introduction, a full-field ranging system is of significant potential use as an extrospective sensor for mobile robots. In order for such a system to implement active ranging using either a homodyne or heterodyne approach, the system must possess the following:

- The ability to precisely modulate an illumination source (preferably at frequencies in excess of 10 MHz)
- A sensor to image the intensity of the received illumination
- The ability to precisely modulate a “shutter”. This will control the timing (and hence the intensity) of light entering the sensor
- The ability to precisely frequency lock the shutter and illumination modulation
- The ability to process the received frames to determine the phase (that encodes the distance)
- An intelligible output of the range to objects within the device’s field of view

Furthermore, it is desirable that the FFRIS also contains:

- The ability to alter the modulation frequencies (both shutter and illumination). This provides the user with the ability to experiment with different configurations. The authors have found this to be invaluable for determining the frequencies that produce the best precision results [15,16]. It would be additionally useful if these frequencies could be changed “on the fly”, in other words be configurable without requiring the downloading of new code.
- The ability to alter the illumination intensity. This permits the range of the system to be increased if required (assuming the user has taken precautions regarding eye safety).
- An embedded processor so that the device can be operated independent of a host PC
- Circuitry to protect the illumination source from over-current or over-heating (which would shorten the lifetime of the illumination source).

Finally, for the device to be useful as an extrospective sensor on a mobile robot, the device should preferably be all of:

- Inexpensive. Due to the low quantity of production this requires use of off-the-shelf components
- Portable. We require the system to be able to run without the need of mains power or attached PC
- Low – or at least variable – acquisition time. The system must be able to operate in real-time even if this incurs a loss of precision.
- Configurable. The system should be configurable for use over a variety of ranges, lighting conditions, object reflectivities and required spatial and range resolutions

Our solution, as mentioned in the introduction, is the result of several development iterations. We initially demonstrated the proof-of-concept of full-field range imaging using a heterodyne technique, and then iteratively solved limitations and problems until arriving at our final design solution that is suitable for mounting on a mobile robot.

## 4. INITIAL DESIGN

Proof of concept of the principle of operation was first obtained using a heterodyne approach [6]. This system utilised AD9852 direct digital synthesizer (DDS) ICs interfaced to a reprogrammable microcontroller to provide the shutter and illumination modulation frequencies. This DDS is a 300 Mega-Samples Per Second (MSPS) device with high frequency resolution provided by a software programmable 48 bit tuning word. The illumination was provided by red Agilent HLMP EL series LEDs that could be successfully driven at up to 20 MHz, and the shutter modulation was provided by a photo-cathode modulated Photek MCP125 Image Intensifier connected to a standard 80 – 200 mm focal length Nikon F-mount zoom lens and an 8-bit monochrome Pulnix TM9701 camera.

This system successfully produced images oscillating at the beat frequency (the difference of the shutter and illumination modulation frequencies, i.e. a heterodyne technique), and a DFT in time was applied to each pixel to provide an estimate of the phase that represents time-of-flight from which the range was determined.

This device, operating at 10 MHz and beat frequencies of 1, 2 and 5 Hz, was successful in producing a highly linear response with a standard deviation of  $\sim 1$  centimetre for objects ranging from 1 metre to 5 metre distance. However, there was a systemic offset error, and the 8-bit limitation of the camera system dramatically depreciated the system's performance. Furthermore, the low modulation frequency also impacted performance as (from Equation 2) the range precision is proportional to the modulation wavelength.

### 4.1 Revised Design

For the next iteration of the design [7], the Pulnix camera was replaced by a 12 bit Pantera TF 1M60 capable of 100 Hz operation at  $512 \times 512$  resolution (i.e.  $2 \times 2$  binning mode) or 200 Hz operation at  $128 \times 128$  resolution (i.e.  $8 \times 8$  binning mode). The image intensifier was replaced by a custom ordered Photek model that had a response almost an order of magnitude faster – the photocathode being capable of being gated down to 1 ns. The slow response LEDs were replaced with four 80 mW Mitsubishi ML120G21 laser-diodes that have a potential modulation frequency of the order of 100 MHz, and the higher speed (400 MSPS) DDS chips, AD9952 were employed to generate the modulation signals up to 200 MHz with a resolution of 0.093 Hz (from the 32 bit tuning word – lower than the AD9852 but still adequate for this application).

In practice, the maximum useable modulation frequency of this improved system was limited to 90 MHz. Sub millimetre precision was obtained at a modulation frequency of 35 MHz, with precision peaking at approximately 0.6 mm at 65 MHz. This system clearly demonstrated the success of our proof of concept.

Subsequent improvements [8] included the introduction of an FPGA to provide laser level control and intensifier gain control. The FPGA was also configured to generate a shuttering signal to gate the photocathode of the intensifier to ensure it turned off during CCD frame transfer in order to limit image smear.

For the phase determination, it was now possible to arrange the drive signals so that the beat signal falls completely within a frequency bin. Hence an inner-product approach could be used in place of the previous DFT. This algorithm was almost an order of magnitude faster and provided essentially the same phase resolution.

This improved system could obtain 0.5 mm resolution for acquisition times  $> 22$  seconds, but even at 10 seconds, a precision of 0.6 mm could be obtained. Employing the  $8 \times 8$  binning, the system could generate range images between 15.7 and 68.5 Hz with a best precision of 2.5 mm [15]. The penalty for this however, was significantly reduced spatial resolution.

The primary remaining acquisition time limitation was the employment of the digital camera attached to the image intensifier. Affordable cameras at the time possessed a slow frames-per-second acquisition rate, typically 50 Hz to 100 Hz, with higher rates only possible with pixel binning.

This system was also severely limited by the utilisation of the image intensifier. This device was costly (~6000 euro) and bulky as can be seen in Figure 6, where the image intensifier is the tube-like device attached to the camera. Furthermore, the intensifier requires three independent voltages, one of the order of -50 to +10 V, another ~700 V, and the third at a level of approximately 6 kV (note the presence of the high voltage power supplies in the foreground of Figure 6). Finally, the range processing was performed off-line by an externally interfaced PC. So whilst successful, this form of the FFRIS was limited to being a bench-top device.

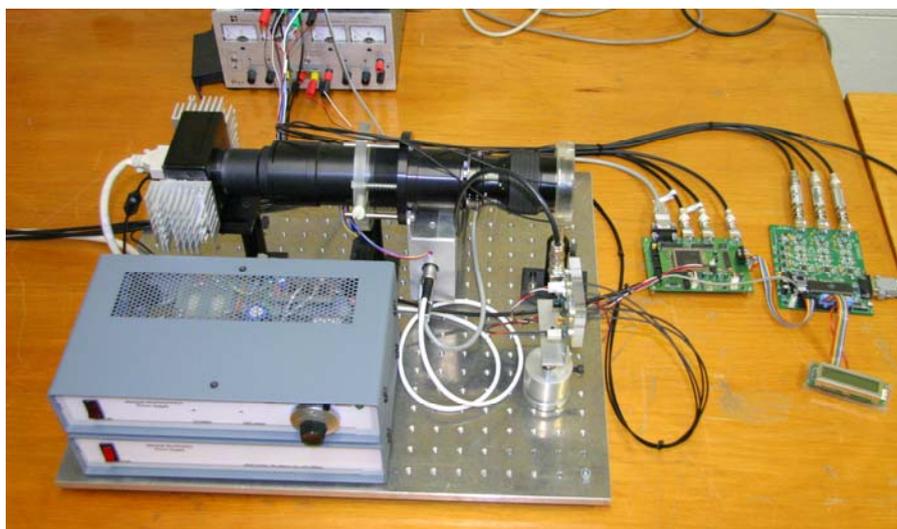


Figure 6. Original FFRIS configuration featuring image intensifier and high-voltage external power supply

## 5. REAL-TIME CAPABLE DESIGN

As mentioned, the primary limitations of the previous systems were the bulk and expense of the image intensifier and the limitations in frame acquisition imposed by the requirement for a commercial digital camera. The next iteration in the system development [9] replaced the Image Intensifier and the digital camera with a PMDTechnologies PMD19k-2 image sensor chip. This CMOS based PMD sensor permits the gain modulation of the imaging pixels to be controlled on-chip, effectively replacing the shuttering function previously performed by the image intensifier and the image acquisition function of the camera. This vastly reduced the bulk and power requirements of the FFRIS, rendering the system potentially portable. Furthermore the component costs of the system were reduced by over 80%! One disadvantage

however, is that the pixel array sizes of these chips are currently limited – although significant improvements are expected in the near future.

At this point, the decision was made to produce a semi-modular system comprising

- an FPGA development board (based on the Stratix III),
- an Illumination board containing the laser diodes and driver circuitry,
- an Imaging Sensor board (with the sensor and lens attached as a daughter board),
- a VGA/Ethernet board for VGA output display and interfacing to a PC.

This is illustrated in Figure 7 [9]. Note the circular arrangement of the illumination diodes on the right. This semi-modular system provided the capability to upgrade or change one of the boards without necessitating a full system redesign, for example the sensor or illumination diodes could be exchanged with little effect on the remaining hardware.

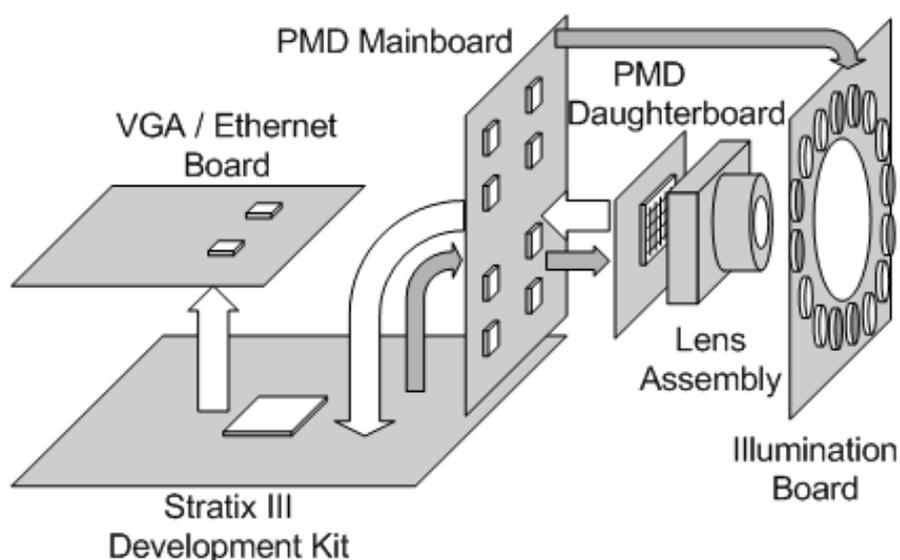


Figure 7. System architecture of modular bench-top full-field imaging system

In the previous design iteration an FPGA controlled the gain of the laser diodes and produced a shuttering signal. Now that an FPGA was embedded in the system, the capability existed to utilise it to generate the modulation frequencies and hence eliminate the requirement of employing the DDS chips. This significantly simplified the FFRIS board design.

Furthermore, by choosing an FPGA with sufficient capacity, the received frames could be stored and processed on-chip to determine the phase and hence the range to objects in those frames. Eliminating the requirement for an external PC is a significant improvement for mobile robotic applications. A Stratix III Development kit hosting an Altera Stratix III EP3SL150 FPGA was employed. This FPGA was chosen primarily for its easily reconfigurable phase-locked-loop resources which provide the ability to reconfigure the phase, frequency and duty cycle of the output channels in real time. This FPGA also has enough on-chip logic and memory resources to buffer the frames and hence calculate the full-field range images in real-time.

The FPGA now incorporated [9] (again change with previous xxx) the tasks of:

- Driving the modulation signals
- Controlling data retrieval from the sensor
- Calculating range images
- Timing and control of signals for VGA display of range image data
- Handling JTAG interface and Ethernet connections to a PC in order to receive and process user commands or transferring data for long-term storage

The Illumination board comprised independently driven infrared (808 nm) and visible red (658 nm) laser diodes employed in two independent banks of 8. These diodes were driven in a controlled current configuration (by the FPGA) with a continuous total optical output power of 800 mW. Lasers of different wavelength were employed to investigate how their different reflectivities affected the performance of the FFRIS. Extra care is required in using the IR lasers however, since eye damage can easily result due to the beam being undetectable by the unassisted retina, preventing a natural blink reflex.

Parallel work by the authors (for example [15,17]) provided a theoretical framework to select optimum frequencies within the achievable system bandwidth.

A problem encountered is that range ambiguity occurs if the phase shift exceeds  $2\pi$  and is a significant issue as the modulation frequency is increased. The maximum unambiguous range  $d_u$  is inversely related to the modulation frequency  $f_m$  as:

$$d_u = \frac{c}{2f_m} \quad \text{Equation 3}$$

Hence for a 10 MHz modulation frequency ranges up to 15 metres can be resolved unambiguously, but at 60 MHz, this reduces to 2.5 metres. In other words, at this modulation frequency the system would not be able to resolve the difference between an object located at 3 metres distance from one located at 5.5 metres. This problem has been resolved [16,18] by employing two modulation frequencies simultaneously, however a discussion of this is outside the scope of this chapter.

The PMD 19K-2 3D Video Sensor Array from PhotonICs is employed as the imaging sensor. This sensor features a  $160 \times 120$  array of pixels grouped into four independently modulated blocks of  $40 \times 120$  pixels. Each modulation block presents a capacitive load of 250 pF at the driver interface. To drive these blocks at modulation frequencies of 10 MHz and above, ultra high current pin drivers (EL7158 from Intersil) are employed.

For this particular sensor, a rise and fall time of 12 ns can be achieved, limiting the maximum modulation frequency (without skew) to 41 MHz. Maximum contrast is achieved with a modulation input of +2.5 V. At a modulation frequency of 41 MHz, the imaging sensor's modulation inputs have an impedance of approximately  $15.5 \Omega$  each and so the current draw per modulation input is 160 mA, with a worst case total current draw of 640 mA. The complete assembled system is illustrated in Figure 8.

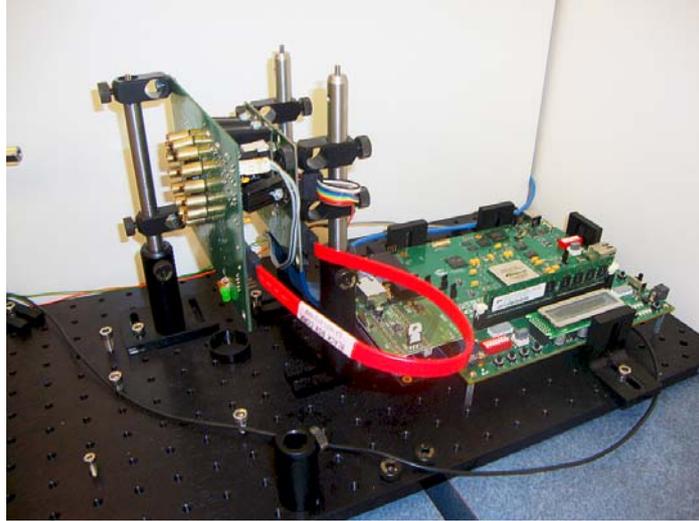


Figure 8. Assembled FFRIS utilising Stratix III FPGA development board

## 6. PORTABLE VERSION

The system described so far demonstrates many of the requirements that we wish for our final system, however its size is constrained by the large physical dimensions (210×180×70 mm) of the Stratix III development board as can be appreciated in Figure 8.

For the portable version, suitable for mounting on a mobile robot, the modular construction of the previous design is retained to allow a versatile system since it can be expected that the FPGA will be replaced in the future with a more powerful version, the illumination diodes may be exchanged for different wavelengths, bandwidth or intensity, and certainly advances are expected in sensor capacity.

The new system has the arrangement of Figure 9 [19] which illustrates how the four boards sandwich against each other to minimise physical dimensions. The boards are separated and attached to each other using M3 PCB standoffs.

Physical sizing is determined in the first instance by the circular cut-out for the Illumination board. This must have a minimum diameter of 35 mm to accommodate the optical lens (diameter 30 mm). The laser diodes of the Illumination board have an 8 mm diameter, and to accommodate 16 requires them to be centred on a circle with a minimum diameter of 43 mm. To accommodate the on-board voltage regulation and laser driving circuitry, and the 6 mm diameter of the standoffs, a board design of 100 mm square is required (considerably smaller than the dimensions of the Stratix III development board).

The system is designed to be generic and flexible in terms of the components it will tolerate. The device is designed to meet the processing requirements of a 1 Mpixel image although we expect it to be some time before such a sensor becomes inexpensively available. Similarly, the current ratings for the components are over-specified which has obvious implications for the power source. Again this is done deliberately to accommodate circuit additions in the future if required. The following sections detail the function of each board and a brief description of how this was implemented.

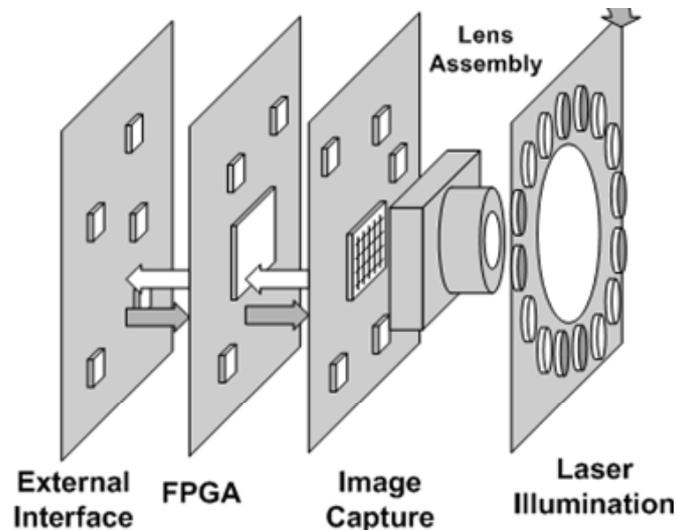


Figure 9. System architecture of portable modular full-field imaging system

Communication between the boards is facilitated by a generic I/O interface that carries 17 differential transmit lines, 17 differential receive lines, a +3.3 V rail spread across 20 pins, a +12 V rail spread across 19 pins, 4 single ended I/O lines, and 4 JTAG lines (TDO, TDI, TMS, TCK). This is implemented with a 172 pin high speed mezzanine male connector. The form of this connector is modelled on the external interfaces provided on the Stratix III development kit.

## 6.1 FPGA Board

This board is the “heart” and “brains” of the entire system. It is configured to internally contain the NIOS processor which performs many of the system control function. The FPGA board connects to the image sensing/capture board via one of the two generic digital I/O ports and via these ports controls the image capture and illumination processes. The FPGA board also connects to the External Interface board to facilitate the FPGA sending captured images to peripheral devices such as a PC or VGA monitor. The FPGA selected has to have sufficient I/O lines to access the generic I/O ports and to interface to external RAM.

As discussed, the prototype version utilised the Altera Stratix III family of FPGAs. For this portable implementation, the Altera Cyclone III EP3C40 is preferred due to the substantially lower cost. This version of the Cyclone family contains 39,600 logic elements, 4 PLLs, ~ 1 Mbit RAM, and 535 User I/Os. This is deemed sufficient for our initial purposes, but should a future iteration require additional processing of the raw images, then the EP3C120 contains three times the number of logic elements and RAM and provides for an easy upgrade path (pins are mostly identical). A 50 MHz oscillator is employed as the system clock.

The design of the full-field range imaging system utilises four discrete blocks of memory for processing and storage of images. The prototype system implements the RAM required for image processing on the FPGA’s internal 5499 Kbit static random access memory. This is sufficient for storage and processing of image frames from the  $160 \times 120$  (19K2) pixel PMD sensor but not for higher resolution sensors and so provision for external memory must be provided.

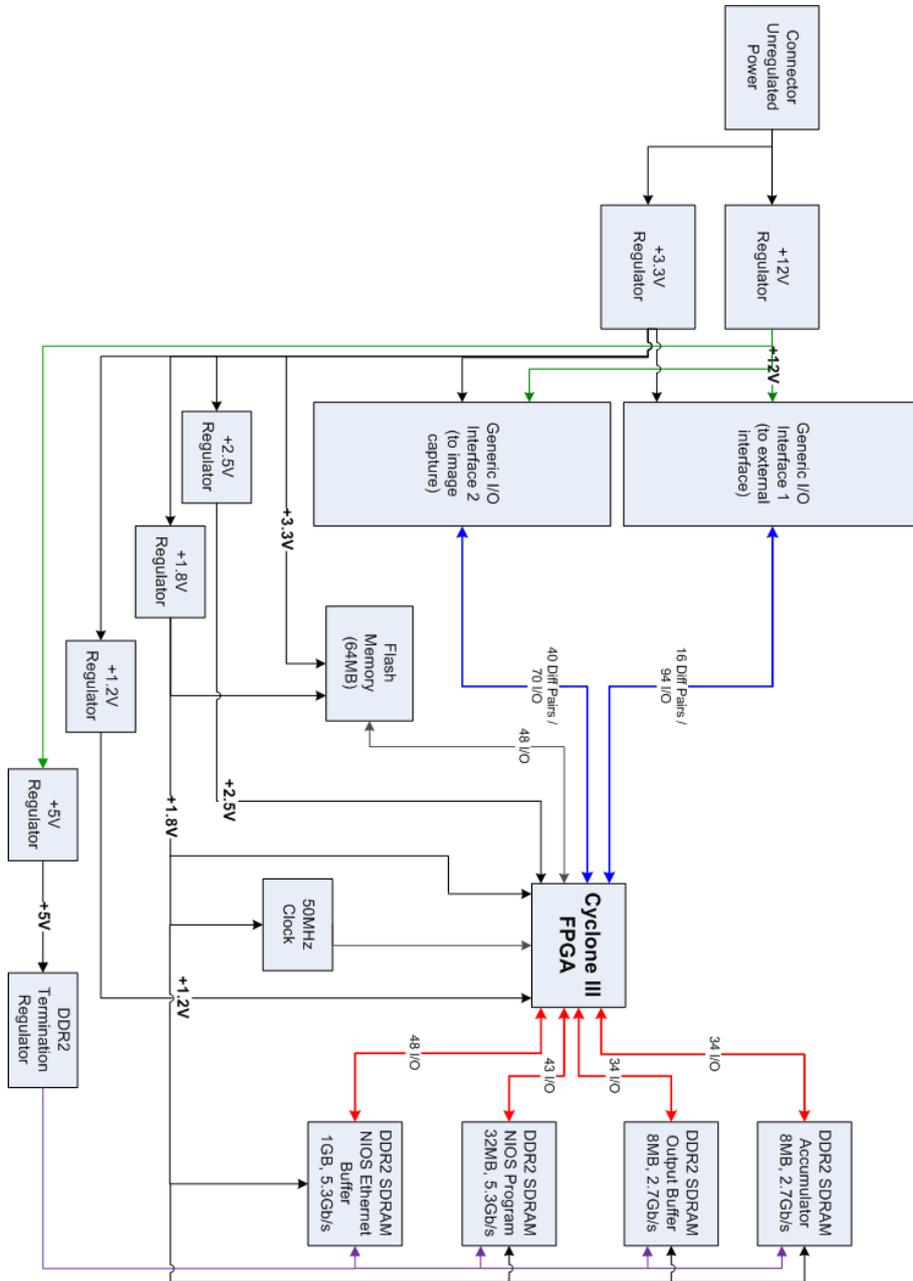


Figure 10. Block diagram of FPGA board

## 6.2 Memory Requirements

Five different types of memory are required for this system:

- Accumulator – required for the storage of images during image processing
- Output buffer – stores the images to be accessed by the NIOS processor, the VGA output and/or the Ethernet output
- NIOS program – stores the firmware of the NIOS processor
- NIOS Ethernet frame buffer – required to store image frames to output to a peripheral computer
- Flash FPGA configuration memory – stores the FPGA configuration to be loaded at start up.

In determining the choice of memory to satisfy the above requirements, it is important to note that the Cyclone III family supports several high speed external memory interfaces to allow external memory to be connected to the FPGA with little customisation of hardware or software. These supported memory devices include DDR, DDR2 and SDR SDRAM. DDR2 SDRAM is preferred over the older memory types for this application.

The accumulator is used to store the accumulated real and imaginary terms (up to 16 bits each) for each pixel needed to calculate the phase [20]. Hence for a 1 Mpixel image this would require 4 MB. For an image processing routine operating at a clock frequency of 10 MHz, the accumulator must operate at a data rate of 320 MBit/s (32 bits/pixel  $\times$  10 MHz). The accumulator must read and write a pixel value each time it performs a mathematical operation. This increases the required data rate of the accumulator to at least 640 MBit/s.

Depending upon the application, the output buffer may be required to hold between 1 and 4 frames at 16 bits per frame. An application that only requires the distance information would simply require 1 frame, if amplitude was also required then 2 frames would be necessary and if the raw pixel data is needed then all 4 frames would need to be stored. Hence for a 1 Mpixel frame, in the worst case, 8 Mbytes are required. This output buffer is accessed by the NIOS processor, the VGA output process and the image processing process. All three accessing processes are clocked at 10 MHz and so the memory must be able to transfer data to each process at a speed of 320 Mbit/s. Time multiplexing is utilised to handle the three accessing processes. This increases the required data transfer speed to 960 Mbit/s (320 Mbit/s by each process).

For the accumulator and output buffer, the Micron MT47H64M8 DDR2 SDRAM is selected. This device has a memory size of 512 Mbit and operates at a clock frequency of 333 MHz. It has an 8-bit wide data bus allowing data transfer rates of 2.7 Gbit/s. For the NIOS program, the Micron MT47H32M16 DDR2 SDRAM is selected, effectively being a 16 bit variant of the H64M8 above.

The NIOS Ethernet buffer RAM stores frames that are to be output to a peripheral computer via the Ethernet connection. We have designed 1 Gbyte of memory, sufficient to buffer 256 1 Mpixel output frames. This is implemented using the M47H512M8 DDR2 SDRAM which has a memory size of 4 Gbit and operates at a frequency of 333 MHz. It has an 8-bit wide data bus allowing data transfer rates of 2.7 Gbit/s. Two of these devices operating in parallel increase the memory density to 8 Gbit (1 Gbyte) and double the data transfer rate to 5.3 Gbit/s.

The Flash configuration is 64 Mbyte which is deemed to be easily sufficient for any current or future sized configuration files.

### 6.3 Illumination Circuit Board

As explained previously, 16 laser diodes are incorporated into the Illumination board and are chosen to be the 130 mW CWML101J27 Mitsubishi devices, operating at 660 nm. These are driven by the iC-HK 155 MHz laser switches to provide up to 150 mA continuous current or 700 mA maximum pulsed current. A block diagram representation of this board is provided in Figure 10. It is important at start-up that the diode current be gradually increased to allow the laser to reach a steady operating temperature since at low temperatures the high currents could potentially cause catastrophic optical damage. The diode current in earlier iterations of the board was controlled by an on-board microcontroller. This functionality is now undertaken by the FPGA, and the diodes are modulated from the FPGA via a control signal marked in Figure 11 in the form of a Two-Wire Interface TWI bus. This control signal feeds into a digital to analogue convertor (DAC) (AD5311 from Analog Devices) and then to the laser switch. A protection circuit has also been included to switch off the laser diodes if the control or modulation signals from FPGA board become disconnected from the Laser Illumination board.

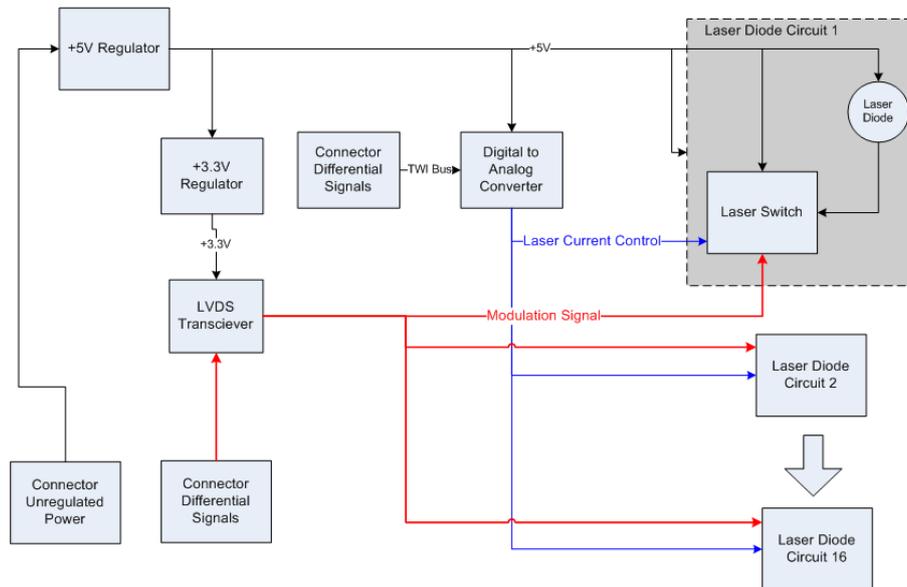


Figure 11. Block diagram for Illuminator Board

A DIP switch allows the user to select between running the laser diodes at maximum power or half power. The half power option operates the laser diodes at a safer optical intensity when output power is not a critical consideration for image ranging a scene.

## 6.4 Image Sensing and Capture Board

This board connects to the FPGA via the generic digital interface. This board handles all the digitising of the captured images from the sensor and all the signal modifications to drive the image sensor. It also buses power and modulation control signals from the FPGA board to the illuminator board. It is illustrated in block diagram form in Figure 12.

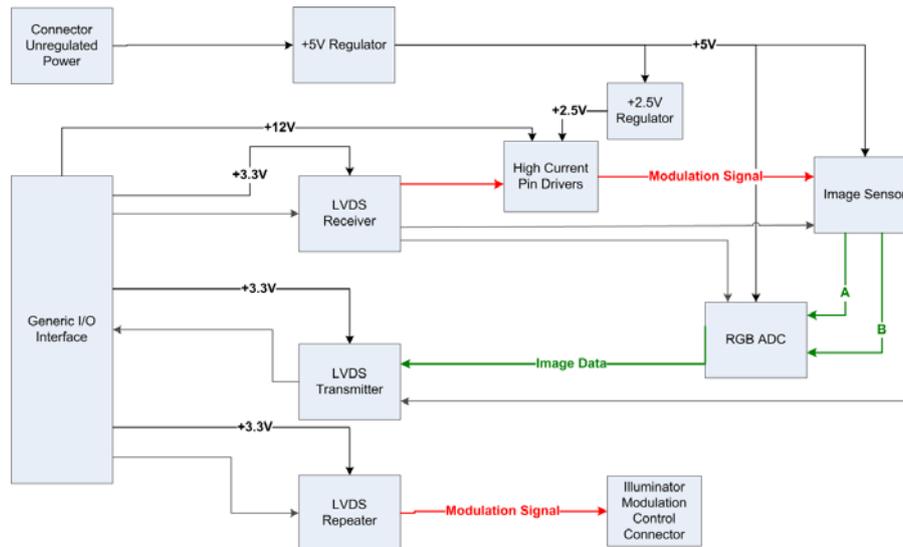


Figure 12. Block diagram for the Image Sensing and Capture Board

The FFRIS requires control over the modulation of the sensor and must be able to access the raw pixel values. These requirements eliminate many of the image sensors currently on the market. We chose not to wait for an improvement over the PMD 19k sensor to become available, and elected instead to design the Image Capture board so that it could immediately host the PMD Daughter board from the previous system incarnation. As this image board is only a sub-system of the complete FFRIS, it will be straight-forward to design a modified board in the future as appropriate sensors become available (this is the motivation behind the modular design – to easily implement hardware changes without incurring a system redesign). The PMD daughter board connects to this board so that the imaging sensor is centred on the board, ensuring that the attached optical lens will be aligned with the circular cut-out of the Laser Illumination board.

The image sensor has two analogue video outputs. A 16-bit Imaging Signal processor ADC (AD9826 from Analog Devices) is provided to convert the two analogue video streams from the image sensor into digital frames to be processed by the FPGA. This ADC can sample the video streams at a maximum rate of 15 million samples per second. Each 16-bit data word is transferred to the FPGA in two sequential bytes on an 8-bit data bus via the generic I/O interface.

The generic I/O interface between the FPGA and Image Capture board utilises LVDS signals to improve the quality of the transmitted signals. LVDS receivers and transmitters convert the LVDS signals to the single-ended CMOS signals required by the image sensor, ADC and high current pin drivers. The LVDS receiver/transmitters are the SN65LVDT388/389 8-way high

speed drivers, and the repeater is the SNLVDS100. The Image Capture board buses the modulation and control signals to the Illumination board via Serial Advanced Technology Attachment (SATA) connections.

## 6.5 External Interface Board

This board provides all the necessary communication drivers to allow the system to connect with peripheral devices such as an external computer or VGA monitor. It also provides communication interfaces to allow configuration and management of the imaging system by an external control computer. Figure 13 presents a block diagram of the main sub-systems of the External Interface board.

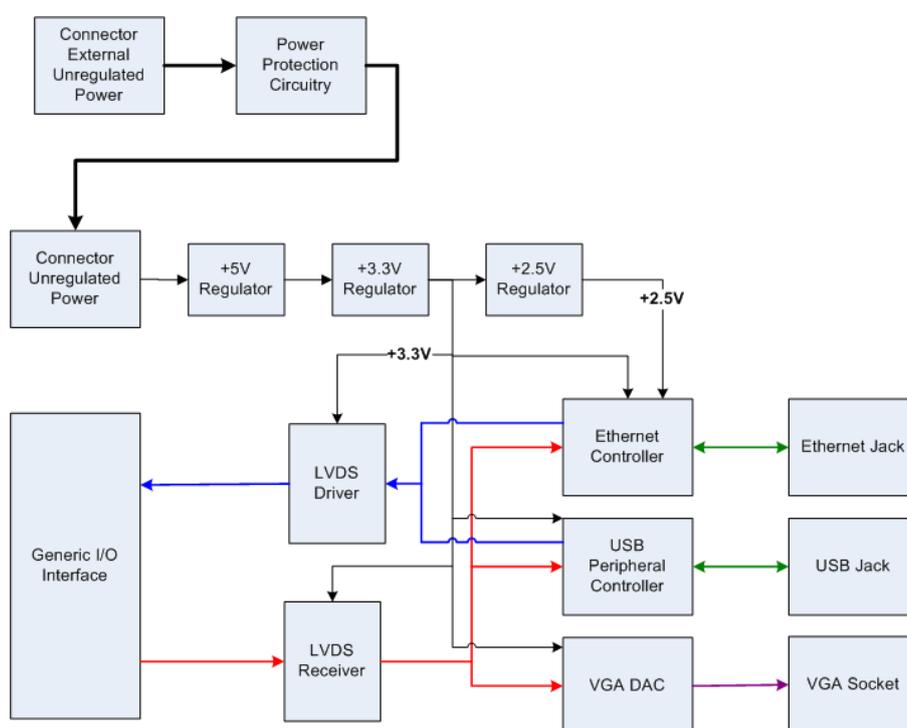


Figure 13. Block diagram of the External Interface board

Image frames can be displayed on an external standard  $640 \times 480$  resolution VGA monitor over a VGA interface allowing users to examine four frames of raw and processed data simultaneously in real time. The VGA output is driven by a triple 10-bit high speed video DAC (ADV7123, from Analog Devices). This DAC has three separate 10-bit input ports that drive three complementary outputs to produce the analogue red, green and blue video streams to display images on a VGA monitor.

All the VGA data and control signals are sent over the generic I/O interface from the FPGA board to the External Interface board. The External Interface board uses a standard VGA jack to allow the connection of any standard VGA monitor.

An 8-bit microcontroller (ATMega32U4 from Atmel) incorporating a USB controller is employed to provide the communication interface between the control computer and the range imaging system (which contains a Mini-B USB connector). The MCU provides full-speed and low-speed USB connections and allows the range imaging system to appear as a USB device to any USB host running on an external computer.

The External Interface board contains a RJ-45 jack with an integrated Ethernet interface to allow long term storage of processed and raw image frames on an external computer. A stand-alone Ethernet controller (DM9000A from Davicom) provides both the MAC and PHY transceiver and is interfaced to the FPGA via a 16-bit data bus over the generic I/O interface. The NIOS processor is responsible for writing image frames to the Ethernet controller chip.

## **7. POWER SUPPLY**

As can be seen from Figures 10 – 13, the component boards require a plethora of voltages, including +1.2, +1.8, +2.5, +3.3, +5.0, +12 V. These are provided on the component boards by an appropriate regulator, but such designs are straight-forward and will not be further described here.

The power consumption of the image ranger sub-systems has been calculated based on the maximum ratings of the components utilised on each board plus a future expansion capacity. The resultant maximum rating of each board is (rounded up to the nearest 5 W):

- FPGA Board – 25 W.
- External Interface Board – 5 W.
- Image Sensing and Capture Board – 10 W.
- Laser Illumination Board – 50 W.

The FPGA board power consumption is primarily set by the configuration of the FPGA, specifically the speed and the number of resources utilised, 20 W being the measured output of the working Stratix as configured in the bench-top system.

Based on the power consumption calculation the input power supply must be able to deliver 90 W of power. The power supply will typically be from a 12 V source and hence the supply must be capable of providing a maximum of 7.5 A. The External Interface board incorporates protection and filter circuits to provide a clean power supply to the unregulated power bus that runs through the entire system. A 40 A rated Schottky diode (48CTQ060SPBF, from Vishay) provides reverse polarity protection on the input voltage and two power-out connectors, fused at 10 A each limit the total current. An inductor-capacitor (LC) filter, rated at 23 A, provides filtering on the input power supply to prevent high frequency noise.

## **8. RESULTS**

The completed and assembled unit is illustrated in Figure 14 [19]. With the modular board arrangement, it has dimensions of 120×200×120 mm (excluding protruding connectors) which is approximately 30% of the size of the bench top system of Figure 8. This comparison is illustrated in Figure 15. Different connectors could be employed to further reduce the device's physical size, but this is not a priority since the current sizing can easily be accommodated on our mobile robots.

With the PMD sensor, 19200 simultaneous range measurements at sampling frequencies of up to 24 Hz to centimetre precision have been achieved. Sub-centimetre acquisition requires

sampling at rates of 0.1 Hz or lower. Range disambiguation has been implemented [16,17] with little loss of precision.

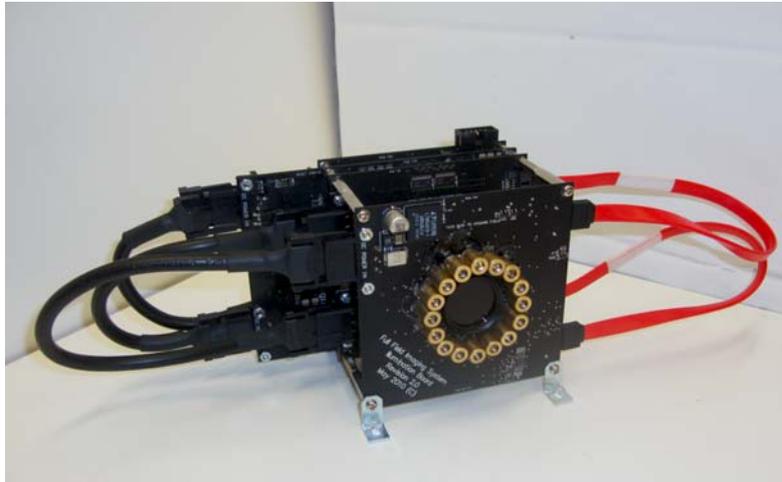


Figure 14. Completed portable FFRIS

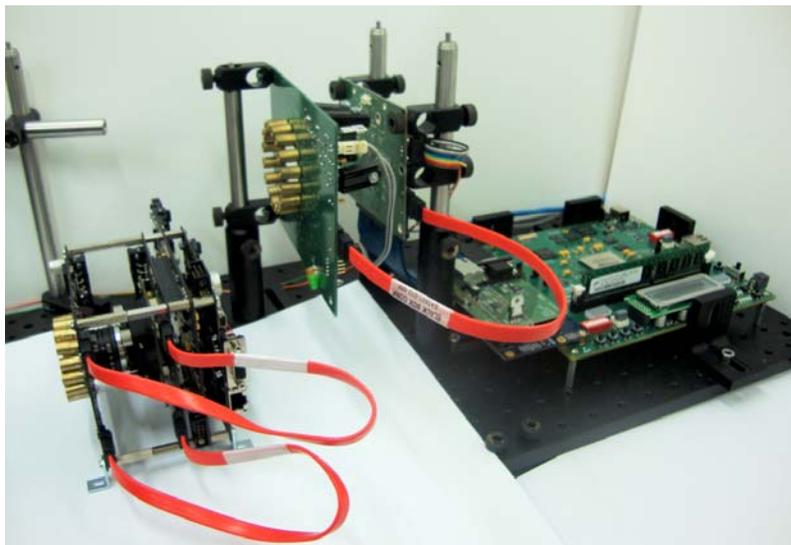


Figure 15. Comparison of portable and bench top FFRIS

The field of view of the system is limited only by the optical hardware. Using a 16 mm focal length lens results in a field of view (horizontal  $\times$  vertical) of  $22.2^\circ \times 16.5^\circ$ . Care must be taken with the selection of lens as wider angle lenses in particular will introduce optical distortion. Calibration of the system for different lens types will mitigate this effect.

Figure 16 displays a sample (face of a mannequin) output from the system where colour has been used to illustrate the range. This image was taken with a modulation frequency of 36 MHz and a frame integration time of 20 ms. As required, changes in acquisition time, laser intensity, and modulation frequencies can easily be made by a user.

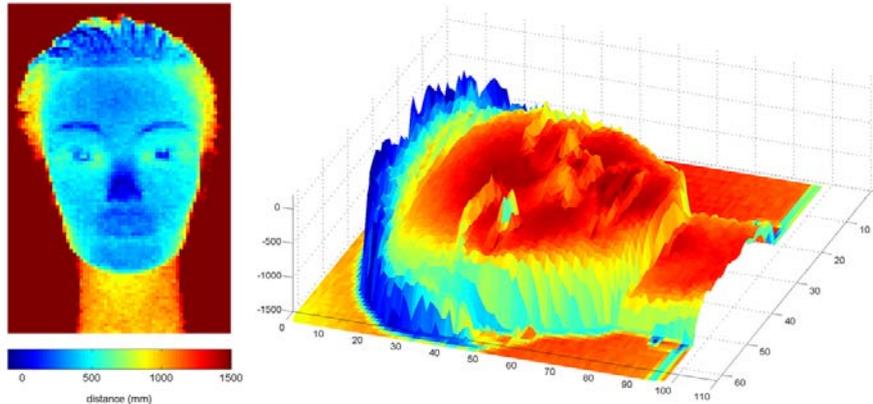


Figure 16. Colour enhanced range full-field range image

## 9. SUMMARY

Reviewing the original specifications, this completed FFRIS satisfies all of the essential and desirable requirements. Specifically:

- The system is able to operate at configurable modulation frequencies up to 40 MHz.
- All modulation and synchronisation frequencies are generated within the FPGA and are precisely frequency locked with each other.
- The illumination intensity of the laser diodes can be easily changed in software.
- Full-field range measurements are calculated by the on-board embedded FPGA. This range can be visually displayed, or provided in numerical form for another processor.
- No external PC is required unless the configuration details are to be altered or the frames transferred for long-term storage or analysis.
- The lasers are protected from over-current during turn-on or in the event of loss of modulation or control signals.
- The device can be entirely powered by the 12 V batteries that power most of the fleet's mobile robots. The system has been currently over-engineered allowing for a maximum power consumption of 90 W. In operation 50 – 60 W is a more typical figure, but this can increase particularly if greater intensity is required from the laser diodes. Regardless, for the mobile robots in our fleet, the robot's locomotive motors easily dominate power requirements.
- The device is inexpensive. The largest cost is the sensor (currently 1000 euro), with the next most expensive component being the FPGA which is of the order of 100 euro. Total component cost of the system is approximately 2000 euro.
- It is compact with the most significant room for improvement being a change of the connectors. Whilst commercial production could further reduce the system size, it is comparable to other systems currently on the market.
- Acquisition time and modulation frequency can be varied in software to provide versatility between real-time operation where precision may not be so critical through to longer acquisition, high precision measurements when greater environmental detail is required.

Whilst other devices on the market may outperform our system in one or more of spatial resolution, frame rate, depth precision or size, none out perform us on all of these criteria. The most significant advantage of our solution is that it is extremely configurable and provides a solution for a greater range of situations than any other systems we have investigated.

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