Analysis on Supercapacitor Assisted Low Dropout (SCALDO) Regulators

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Abstract

State-of-the-art electronic systems employ three fundamental techniques for DC-DC converters: (a) switch-mode power supplies (SMPS); (b) linear power supplies; (c) switched capacitor (charge pump) converters. In practical systems, these three techniques are mixed to provide a complex, but elegant, overall solution, with energy efficiency, effective PCB footprint, noise and transient performance to suit different electronic circuit blocks. Switching regulators have relatively high end-to-end efficiency, in the range of 70 to 93%, but can have issues with output noise and EMI/RFI emissions. Switched capacitor converters use a set of capacitors for energy storage and conversion.

In general, linear regulators have low efficiencies in the range 30 to 60%. However, they have outstanding output characteristics such as low noise, excellent transient response to load current fluctuations, design simplicity and low cost design which are far superior to SMPS. Given the complex situation in switch-mode converters, low dropout (LDO) regulators were introduced to address the requirements of noise-sensitive and fast transient loads in portable devices. A typical commercial off-the-shelf LDO has its input voltage slightly higher than the desired regulated output for optimal efficiency.

The approximate efficiency of a linear regulator, if the power consumed by the control circuits is negligible, can be expressed by the ratio of V_o/V_{in}. A very low frequency supercapacitor circulation technique can be combined with commercial low dropout regulator ICs to significantly increase the end-to-end efficiency by a multiplication factor in the range of 1.33 to 3, compared to the efficiency of a linear regulator circuit with the same input-output voltages. In this patented supercapacitor-assisted low dropout (SCALDO) regulator technique developed by a research team at the University of Waikato, supercapacitors are used as lossless voltage droppers, and the energy reuse occurs at very low frequencies in the range of less than ten hertz, eliminating RFI/EMI concerns.

This SCALDO technique opens up a new approach to design step-down, DC-DC converters suitable for processor power supplies with very high end-to-end efficiency which is closer to the efficiencies of practical switching regulators, while maintaining the superior output specifications of a linear design. Furthermore, it is important to emphasise that the SCALDO technique is not a variation of well-known switched capacitor DC-DC converters.

In this thesis, the basic SCALDO concept is further developed to achieve generalised topologies, with the relevant theory that can be applied to a converter with any input-output step-down voltage combination. For these generalised topologies, some important design parameters, such as the number of supercapacitors, switching matrix details and efficiency improvement factors, are derived to form the basis of designing SCALDO regulators. With the availability of commercial LDO ICs with output current ratings up to 10 A, and thin-profile supercapacitors with DC voltage ratings from 2.3 to 5.5 V, several practically useful, medium-current SCALDO prototypes: 12V-to-5V, 5V-to-2V, 5.5V-to-3.3V have been developed. Experimental studies were carried out on these SCALDO prototypes to quantify performance in terms of line regulation, load regulation, efficiency and transient response.

In order to accurately predict the performance and associated waveforms of the individual phases (charge, discharge and transition) of the SCALDO regulator, Laplace transform-based theory for supercapacitor circulation is developed, and analytical predictions are compared with experimental measurements for a 12V-to-5V prototype. The analytical results tallied well with the practical waveforms observed in a 12V-to-5V converter, indicating that the SCALDO technique can be generalized to other versatile configurations, and confirming that the simplified assumptions used to describe the circuit elements are reasonable and justifiable.

After analysing the performance of several SCALDO prototypes, some practical issues in designing SCALDO regulators have been identified. These relate to power losses and implications for future development of the SCALDO design.

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Acronyms and Abbreviations

AC	Alternating Current
ADC	Ananlog to Digital Converter
AES	Auxiliary Energy System
ARC	Adaptive Reference Control
ASIC	Application-Specific Integrated Circuit
BJT	Bipolar Junction Transistor
BIA	Buffer Impedance Attenuation
CCM	Continuous Conduction Mode
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DC	Direct Current
DCM	Discontinuous Conduction Mode
DCS	Direct Current Sinker
DGB	Dynamic Gate Biasing
DSC	Digital Still Camera
DSP	Digital Signal Processing
EDLC	Electrochemical Double Layer Capacitor
EMI	Electromagnetic Interference
ESD	Energy Storage Device
ESR	Equivalent Series Resistance
ESS	Energy Storage Systems
ETEE	End-to-End Efficiency
FET	Field Effect Transistor
GPRS	General Packet Radio Device
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
IEEE	Institute of Electronics and Electrical Engineers
LDO	Low Dropout Regulator
MOSFET	Metal Oxide Semiconductor Filed Effect Transistor
MES	Main Energy System

NMOS	n-type Metal Oxide Semiconductor
PCB	Printed Circuit Board
PCFC	Pole Control Frequency Compensation
PDA	Personal Digital Assistant
PFC	Power Factor Correction
PIC	Peripheral Interface Controller
PMOS	p-type Metal Oxide Semiconductor
PMS	Power Management System
POL	Point of Load
PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulation
OFRC	Output Fixed Ratio Converter
QSW	Quasi Square Wave
RF	Radio Frequency
RFI	Radio Frequency Interference
RMS	Root Mean Square
RS-SCALDO	Reduced Switched SCALDO
SC	Switch Capacitor
SCALDO	Supercapacitor Assisted Low Dropout Regulator
SEPIC	Single-ended Primary Inductance Converter
SMPS	Switched-Mode Power Supply
SoC	System On-Chip
UPS	Interruptible Power Supply
VLSI	Very Large Scale Integrated Circuits
VRM	Voltage Regulator Module
WSN	Wireless Sensor Nodes
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Chapter 1

Introduction

1.1 Background

Supercapacitor-based solutions for power electronics applications are a key research area at the School of Engineering, the University of Waikato. One important achievement in this research, a patented technique [1, 2] to improve the efficiency in linear regulators- "Supercapacitor Assisted Low Dropout (SCALDO) Regulator " was made in 2008. It has been practically proven that the technique can achieve an end-to-end efficiency improvement factor in the range of 1.33 to 3 which is significant, compared to conventional linear regulators [1–11]. In-depth theoretical analysis of this technique was an essential requirement to check the potential applicability in practical circumstances such as processor power supplies, portable devices and high current discrete power supplies.

1.2 Significance of DC Power Supplies

The reliable operation of virtually any electronic circuit requires a steady, constant voltage DC power supply. This source can be either a battery, a combination of battery and DC-DC converter or a power supply converting AC mains into one or more low voltage DC supplies, suitable for electronic components. A reliable power supply is vital for any successful electronic design, to achieve the specified performance in the worst case scenarios. Such a supply will have (i) specific line and load regulation characteristics; (ii) minimum output impedance; (iii) high efficiency; (iv) predictable transient behaviour; (v) cost effective design [12, 13].

Historically, vacuum tube supplies were well-established and those power supplies were suited for powering equipment with relatively low currents at high voltages. However, for high-current low-voltage applications, vacuum tube supplies became bulky and inefficient, and power supply design has been conveniently replaced with transistors [14–16]. In the 1960s and the early 1970s, power supplies were linear designs with efficiencies in the range of 40 to 50% [12]. These power supplies came with many desirable characteristics, such as simplicity, low output ripple, excellent line and load regulation, fast transient response and low electromagnetic interference (EMI), but they suffered badly from low efficiency. With the introduction of switch mode systems in the mid 1970s, efficiency rose from 60 to 80%

and those power supplies became a popular solution [12]. However, with the evolution of complex VLSI chips and processor-based systems, the demand for fast transient response, lower noise and less complex DC power supplies was a design challenge for power supply designers, which is specially apparent in mobile battery operated products.

Developing power management systems (PMS) for processor based portable products is a complex problem for several reasons such as (i) end-to-end efficiency of the overall PMS affecting the battery run time; (ii) DC power rail specifications for processors with tight voltage margins; (iii) load current slew rate issues, where modern high power processors require high current slew rates in the range of 50 to 1000 A/μs; (iv) RFI/ EMI issues of switch-modes; (v) weight and volume limitations [17].

In modern portable devices, the commonly used techniques for DC-DC converters are (i) linear regulators; (ii) switched-mode power supplies; (iii) switched capacitor converters. In many portable products such as cellular phones, digital cameras, portable computers and smart phones, the PMS is built by mixing these three techniques to suit the overall design requirements and the DC rail specifications of individual circuit blocks. In powering up mixed signal circuit blocks and RF circuits, RFI/EMI issues could be a significant factor, while high current processor blocks may demand a DC rail with high slew rate capability. When both weight and volume are concerns, switch-modes offer compactness and efficiency, but dealing with RFI/EMI and bulky inductors can be a significant issue.

Power supply designs for portable electronic products have become an exponentially growing segment due to the evolutional advancements in both switch-mode and linear voltage regulator designs. With sinking operating voltages and rising current demands, the designer must consider factors such as power wastage, long battery life, small size, and low cost. These design parameters change and rearrange the design priorities for power supplies and makes the choice between linear and switching mode power supplies ambiguous.

Low dropout regulators (LDO) are linear regulator ICs specially designed to work with a low voltage difference between the input and the output. They are frequently used in battery powered portable products such as point of load (POL) power supplies where adaptation of switch-mode power supplies becomes difficult, primarily due to noise performance, slew rate requirements and the complex nature of their output impedance [18,19]. An example of a POL approach in a portable product with a 48 to 8 V intermediate bus converter is given in Fig. 1.1 where all other voltages are derived from the 8 V bus. In this kind of situation, to minimize compound efficiency loss, which can be significant at times, the POL converters should offer efficiency close to or above 90% [20]. The digital still camera (DSC) shown in Fig. 1.2, indicating the combined use of switch-modes and LDOs is another example. Fig. 1.3 depicts the part of power management solution offered for such a case from Texas Instruments TPS65010 IC. In TPS 65010 IC, part of the circuitry allows configuring several switch-mode circuits, while the other part of the silicon is used

to configure LDO circuits. More details are available in [21, 22]. In some portable products where some parts of the load requires very demanding currents, in the orders of tens to few hundreds milliamperes, and with DC power rails higher than the battery voltage or the bulk switching power supply's output rail voltage, switched capacitor converters are also used [23].

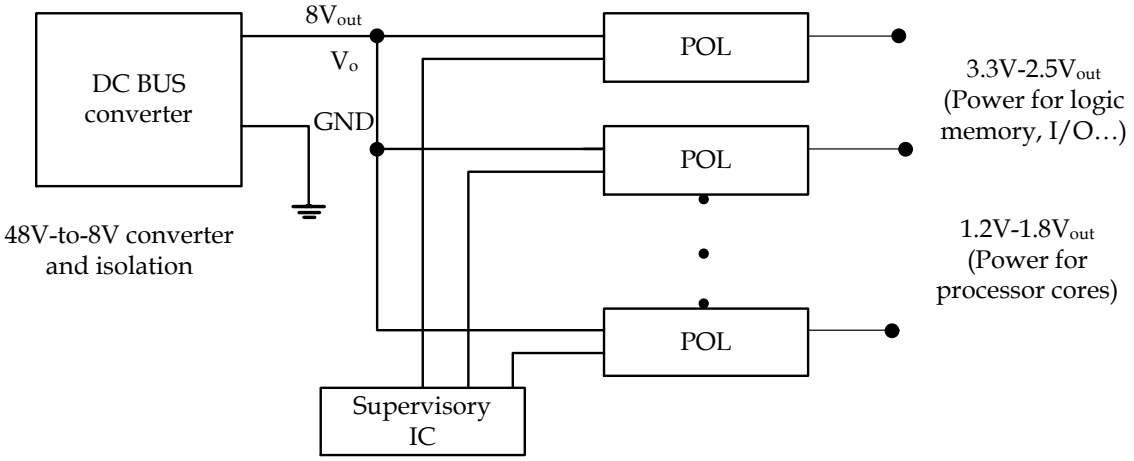


Figure 1.1: An 8 V intermediate bus architecture with 48V-to-8V bulk converter and POL stages [20]

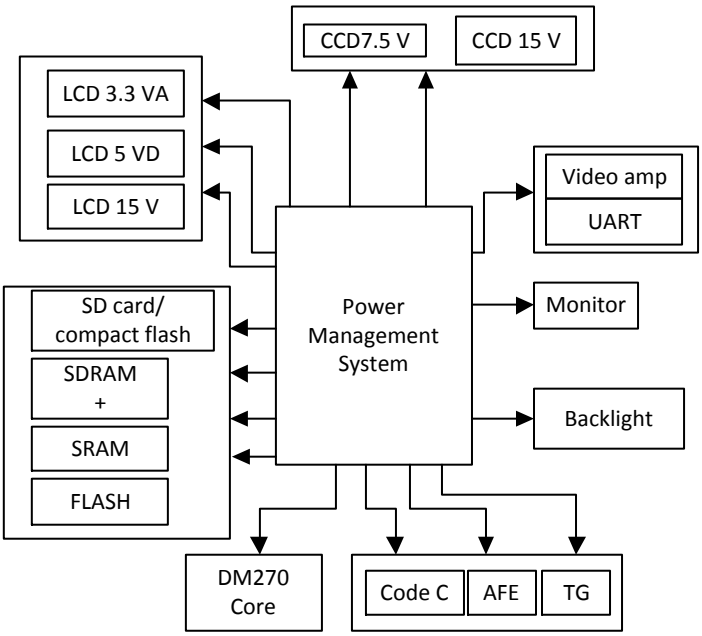


Figure 1.2: An example of a Digital Still Camera (DSC) architecture [21]

Table 1.1 gives a comparison of switch-mode and linear regulator parameters that can affect the design of a power supply of portable devices [18, 24].

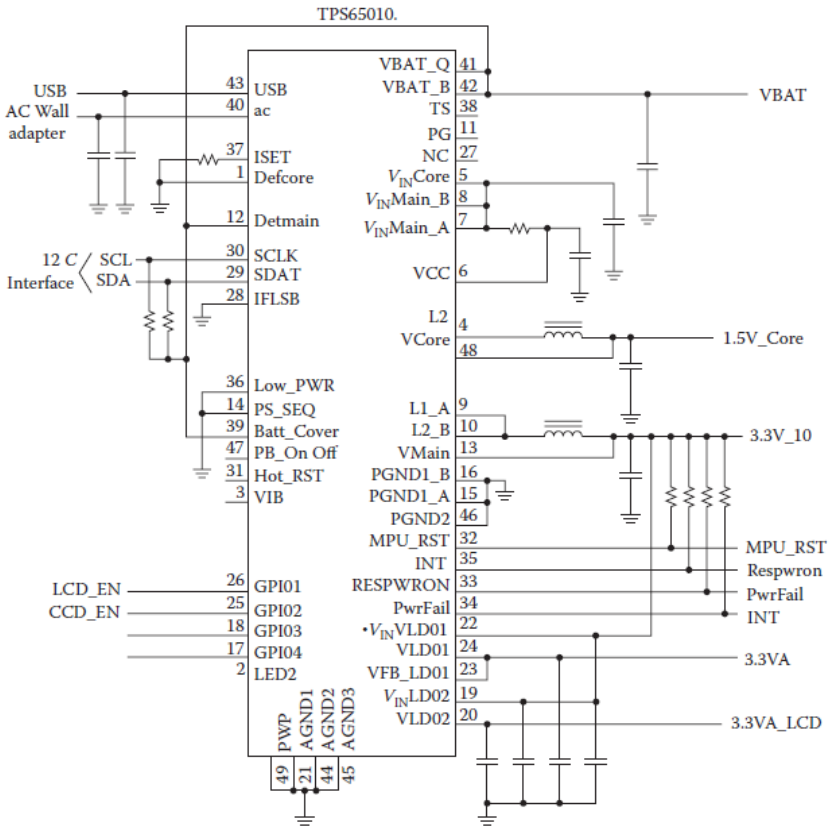


Figure 1.3: Power management solution, Texas Instruments TPS65010 IC [21]

Table 1.1: Comparison Between Linear and Switch-Mode Regulators [18]

Property	Linear Regulator	Switching regulator
Function	Only steps down; input voltage must be greater than output.	Steps up, steps down, or inverts
Efficiency	Low to medium, but actual battery life depends on load current and battery voltage over time; high if V_{in}-V_{out} difference is small.	High, except at very low load currents (μA), where switch-mode quiescent current is usually higher.
Waste Heat	High, if average load and/or input/output voltage difference are high	Low, as components usually run cool for power levels below 10 W
Complexity	Low, which usually requires only the regulator and low-value bypass capacitors	Medium to high, which usually requires inductor, diode, and filter capacitors in addition to the controller IC; for high-power circuits, external FETs are needed
Size	Small to medium in portable designs, but may be larger if heat sinking is needed	Larger than linear at low power, but smaller at power levels for which linear requires a heat sink
Total Cost	Low	Medium to high, largely due to external components
Ripple/Noise	Low; no significant ripple, low noise, better noise rejection.	Medium to high, due to ripple at switching rate

1.3 Requirement of Modern DC Power Supplies

In order to meet expanding data processing demand, many high performance microprocessors and very large scale integrated circuits (VLSI) are being introduced. Today's high-performance processors have very stringent power requirements such that the high performance ICs consume significantly higher power, at lower DC rail voltages with tighter voltage regulation, higher currents and faster transient response for abrupt changes in load current [25–28]. According to the International Technology Roadmap for Semiconductors (ITRS) future VLSI devices of gigahertz capability are expected to have feature sizes below 45 nm with DC power supply requirements with sub 1V and the equivalent noise voltages closer to the DC rail values [29].

During the last decade, power requirements for state of the art microprocessors in computer power supplies have followed the trend shown in Fig. 1.4. The increases in operating frequency and the introduction of new instruction sets lead to increases in supply current requirements while the transition to improve semiconductor processes with smaller geometries reduces operating voltages [30]. The evolution of the lower voltage implementation of microprocessors began with the introduction of a high-performance Pentium processor which was driven by a less than 5 V power supply [27,28]. By the mid-nineties, processor power supplies had decreased to 3.3 V ICs replacing the standard 5 V ICs due to their better speed, lower power consumption and higher integration density. Then the decreasing power supply rails became a trend in processor supplies which kept dropping down to sub 1 V levels, while the current consumption exponentially increased towards 100 to 150 A or even higher creating significant challenges to processor power supplies [27,30,31].

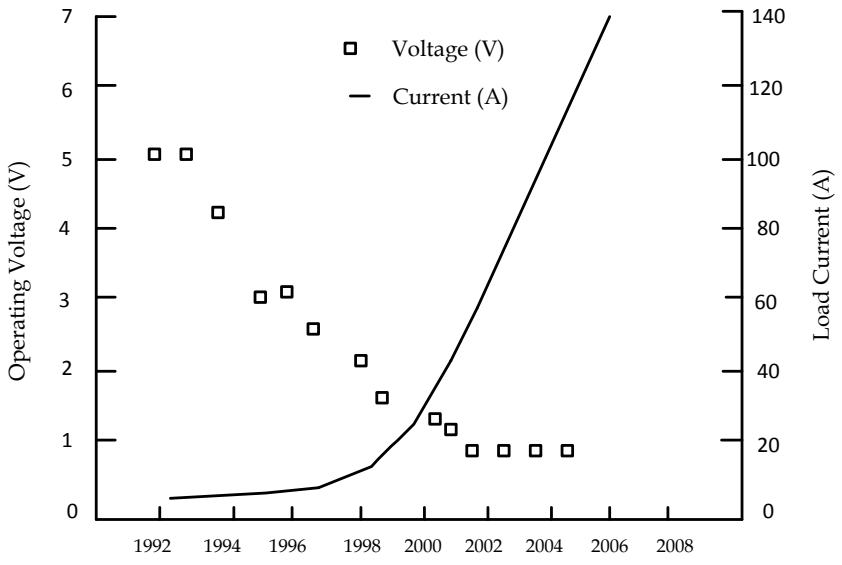


Figure 1.4: Microprocessor Power Trends [30]

Meanwhile, microprocessors need tight power management because the processors are operating at higher frequencies, in the gigahertz (GHz) order clock speeds, and several hundred million transistors are packed on a single silicon chip, where the feature size continues to fall to below 45 nm [27–29]. The development of modern integrated circuits is shown in Fig.1.5, where Moore's law is applied and creates a signal integrity crisis.

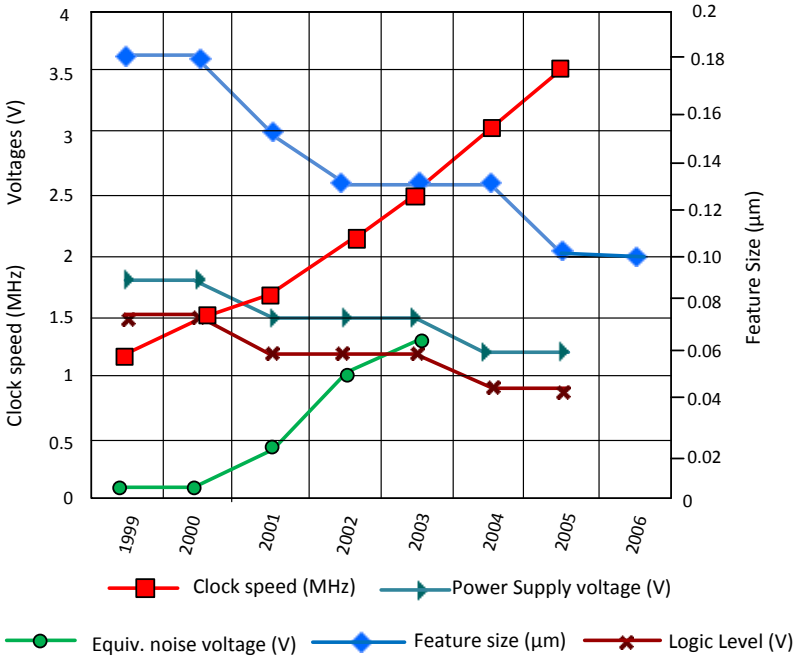


Figure 1.5: Moors law of driving signal integrity crisis [32]

As the speed of the IC's increase, they present more dynamic loads to their power supplies. Some applications, such as high end processors and similar components, now require adequate transient response in the face of fast varying dynamic loads with high current slew rates in the range of 10 to 1000 A/μs. For a small load change, these slew rates do not create significant problems whereas most dramatic load transients occur in processor transition in changing from sleep mode to active mode and vice versa, as shown in Fig. 1.6. The transition between sleep and active modes occurs in a very little time, resulting in extremely high $\frac{di_L}{dt}$ [27, 28].

Modern generation microprocessor chips, high-end servers, and work stations are powered by sub-volt levels of voltages and they require tighter voltage tolerances. Those converters named as "Voltage Regulator Modules" (VRMs) are designed with a tight output voltage regulation range (2.5%), a very fast transient response of (1 A/ns), a high power density and a working efficiency of about 92% as a minimum at rated load [31, 33, 34]. For example, a 1.1 V VRM output, voltage deviation can only be $\pm$ 33 mV. During the sleep-to-active mode transients, it is important to meet this voltage deviation [27].

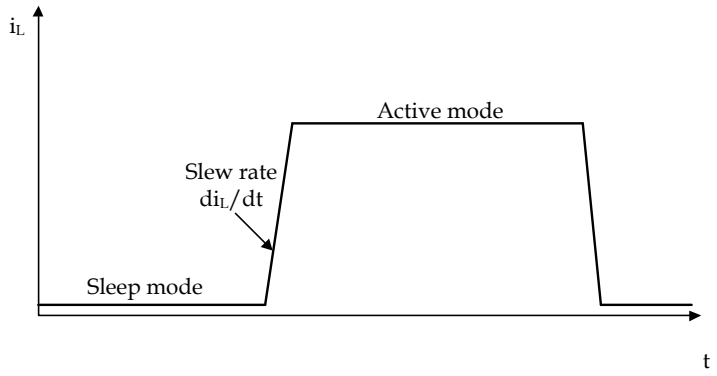


Figure 1.6: Load waveform during transitions

The above requirements of modern microprocessors create serious design challenges in VRM specifications [28, 31, 33–39]. According to [36] three issues have been identified to meet the requirement of future VRMs:

1. VRM topology
2. System integration
3. Low voltage power devices

Most conventional VRMs use the buck topology or the synchronous rectifier approach. According to [27], in such designs, a transient limitation comes from their large output filter inductance. The slew rate of the inductor current is too low and during the transients, this large inductor limits the energy transfer speed. Therefore capacitors have to store or discharge all the energy from the load. With this large output filter inductance, to maintain voltage regulation according to modern transient requirements, more output filter capacitors and decoupling capacitors are required. However, the space constraints of VRM and motherboards make conventional VRM designs, impractical for future microprocessors [27].

Another limitation of the conventional VRM is its lower efficiency [27]. For lower output voltage, it is more difficult to meet the efficiency requirement. Fig. 1.7 illustrates the efficiency of buck and synchronous rectifier VRMs working at 2 V and 1.2 V output respectively. As shown in Fig. 1.7 the efficiency cannot meet the 80% requirement for the entire load range either in the buck topology or the synchronous rectifier approach. Basically this limitation is due to today's power devices being based on vertical power MOSFET technology. More details are available in [27, 36].

In order to meet modern specifications, novel VRM topologies have been introduced. According to [27] with interleaved quasi-square wave (QSW) topology, the transient response can be significantly improved without increasing capacitor numbers. By increasing the switching frequency to multi-megahertz, the output inductance can be significantly reduced, so the decoupling capacitance is also reduced, while the transient performance

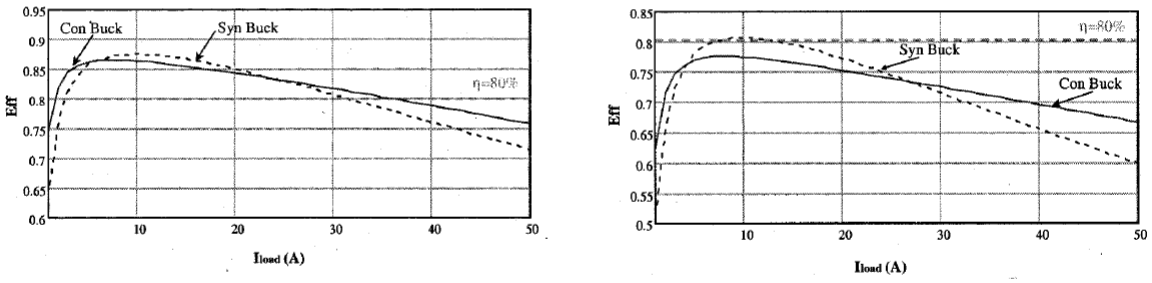


Figure 1.7: Conventional VRM efficiency (a) $V_{in} = 5V, V_o = 2V, f_s = 300kHz$, switches IRL3803 (b) $V_{in} = 5V, V_o = 1.2V, f_s = 300kHz$, switches IRL3803 [27]

is further improved. However, based on the above discussion there is a potential opportunity for an transient enhanced efficiency improved VRM design in the modern processor power supplies.

1.4 DC Power Supply Market Demand

The DC power supply market is experiencing exponential growth due to the evolving need of power consumption in high-tech portable electronics, computer and communication industries. The analog power IC market is a major segment of overall power supply industry, which includes products such as linear regulators, switching regulators, charge pumps and other analog ICs like voltage references and battery management circuits.

In 2002 linear regulator ICs earned the largest dollar volume share of the power management IC market [40]. However, this share was forecast to decline over the next five years. Also SMPS regulator ICs which were widely used as power supplies and the buck regulator ICs accounted for the largest share of unit shipments and dollar volume. Shipment growth was also forecast to be the largest for these regulators, mainly due to decreasing operating voltages [41, 42].

Market research conducted in 2010 by Databeans, Inc., USA [43] on the power management market segment in 2010 gave a good insight into the overall power management market trends from 2010 to 2015. The following discussion is based on these findings which are valid at the time of the submission of this thesis.

In the first half of 2010 semiconductor companies showed a resurgence as the industry rebounded from the recession. Basically the changes of macroeconomic factors such as job growth, rising consumer confidence, and overall economic growth caused this resurgence. According to Databeans estimates [43], the global power management market would reach $21.3 billion in global revenue and 133.6 billion unit shipments in 2010. As shown in Fig. 1.8, they forecast sales of power management ICs growth at an average rate of 8% annually over the following five years, reaching $30.6 billion in total revenue by 2015.

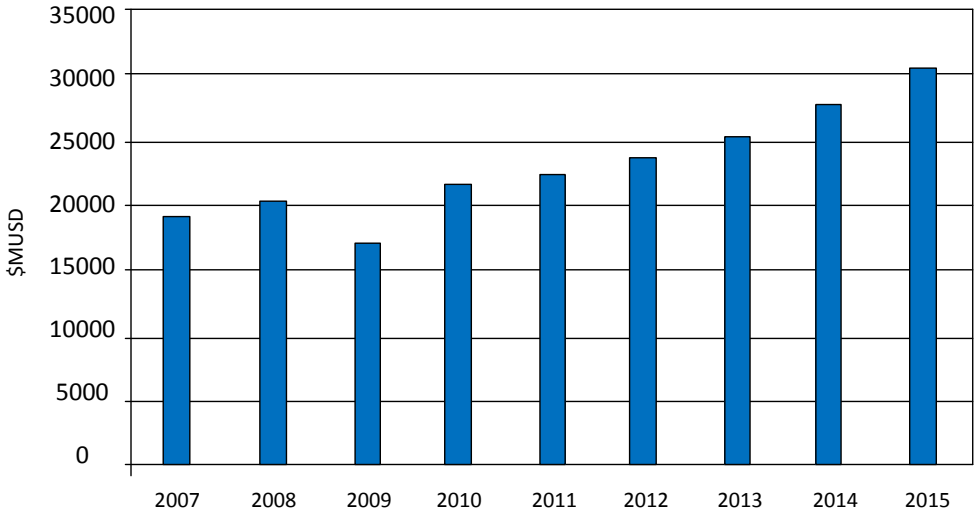


Figure 1.8: Worldwide power management market revenue forecast [43]

Databeans estimates shows the entire industry is fairly well distributed in sales of power management ICs, with no one market segment dominating total sales. As shown in Fig. 1.9, among these segments the communications industry contributes the largest market by revenue, followed closely by the consumer, computer, and industrial segments respectively while automotive segment continued to trail [43]. The communication industry would continue to be the largest of the five market segments, with approximately $5.1 billion in revenue or 24% of the market projected for 2010. This would remain the fastest growing market with annual growth of 10% on average over the next five years. Consumer electronics would be the second largest segment with just over $5 billion. The computer market will be the third largest overall with $4.8 billion, followed by industrial with $4.2 billion. The automotive will remain the smallest of the five segments, with just over $2 billion in sales.

Portable devices have become leading application drivers in the today's market. Most general purpose linear regulators are used in the communications, computing and consumer segments. In 2010 general purpose regulators would account for $479 million in sales and 3.4 billion in total worldwide unit shipments. Advances in technology have made it possible to significantly reduce voltage drop on all linear regulators. Manufacturers today advertise almost all linear regulators as low-dropout. Low dropout regulators are most often used in wired communication systems, where power savings can be less important than the battery-operated devices. Databeans projected that in 2010 total sales of LDOs would reach $2.2 billion with 12.9 billion units shipped [43]. Over the following five years annual sales in this market would grow 10% on average, while unit shipments would grow 11% on average until 2015.

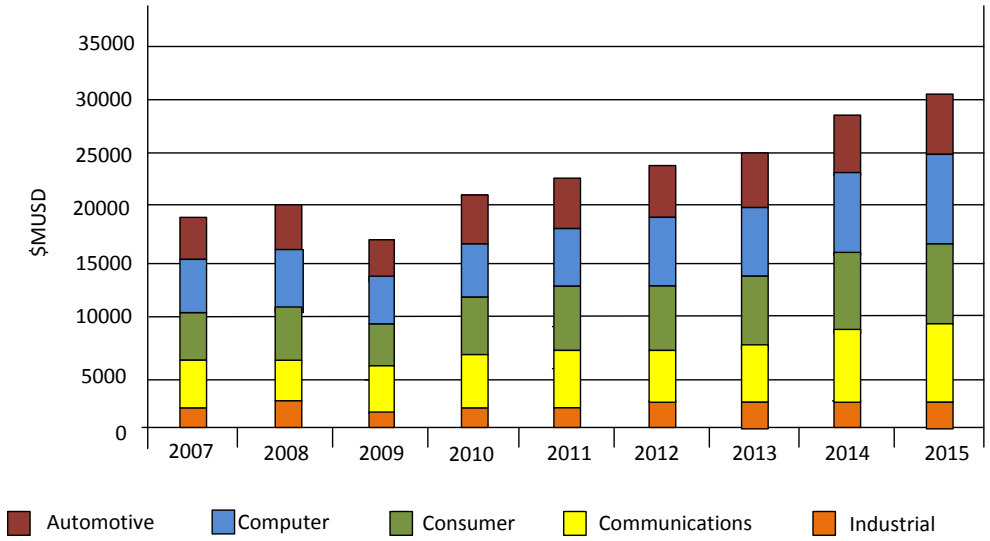


Figure 1.9: Worldwide power management revenue forecast by market segment [43]

There has been a continued trend toward greater integration, wider output voltage capability, higher efficiency and compact size, allowing for low profile circuit implementation in switching regulators. According to Databeans as a whole this market would account for $ 4.7 billion in 2010 sales and strong average growth of 13% annually reaching $ 8.6 billion revenue by 2015 [43].

Fig. 1.10 illustrates the commercial utilization of LDO and switching regulator families with predictions for the future years as per market research reports from Databeans, indicating the total business potential in millions of dollars (lower trace-M), total unit sales in million units (middle trace-MU) and the average selling price (upper trace-ASP) of these components [43].

1.5 New Project Proposal

Taking the requirement of modern power supplies and the demand for LDO regulators in present and future power supply markets into consideration, the need for an efficiency improved LDO regulator was apparent.

In 2008, the basic concept of the patented SCALDO technique [1], was developed by the University of Waikato research team led by Nihal Kularatna. Patented document is available in Appendix A. Basically, it has been practically proven that using supercapacitors and a very low frequency supercapacitor circulation technique in combination with a LDO, provides a way of achieving significantly higher efficiency than the conventional linear regulator. A 12V-to-5V proof of concept circuit was developed with an end-to-end efficiency of approximately 78%, despite the use of a conventional linear regulator, which could provide only about 42% maximum end-to-end efficiency at the same input-output

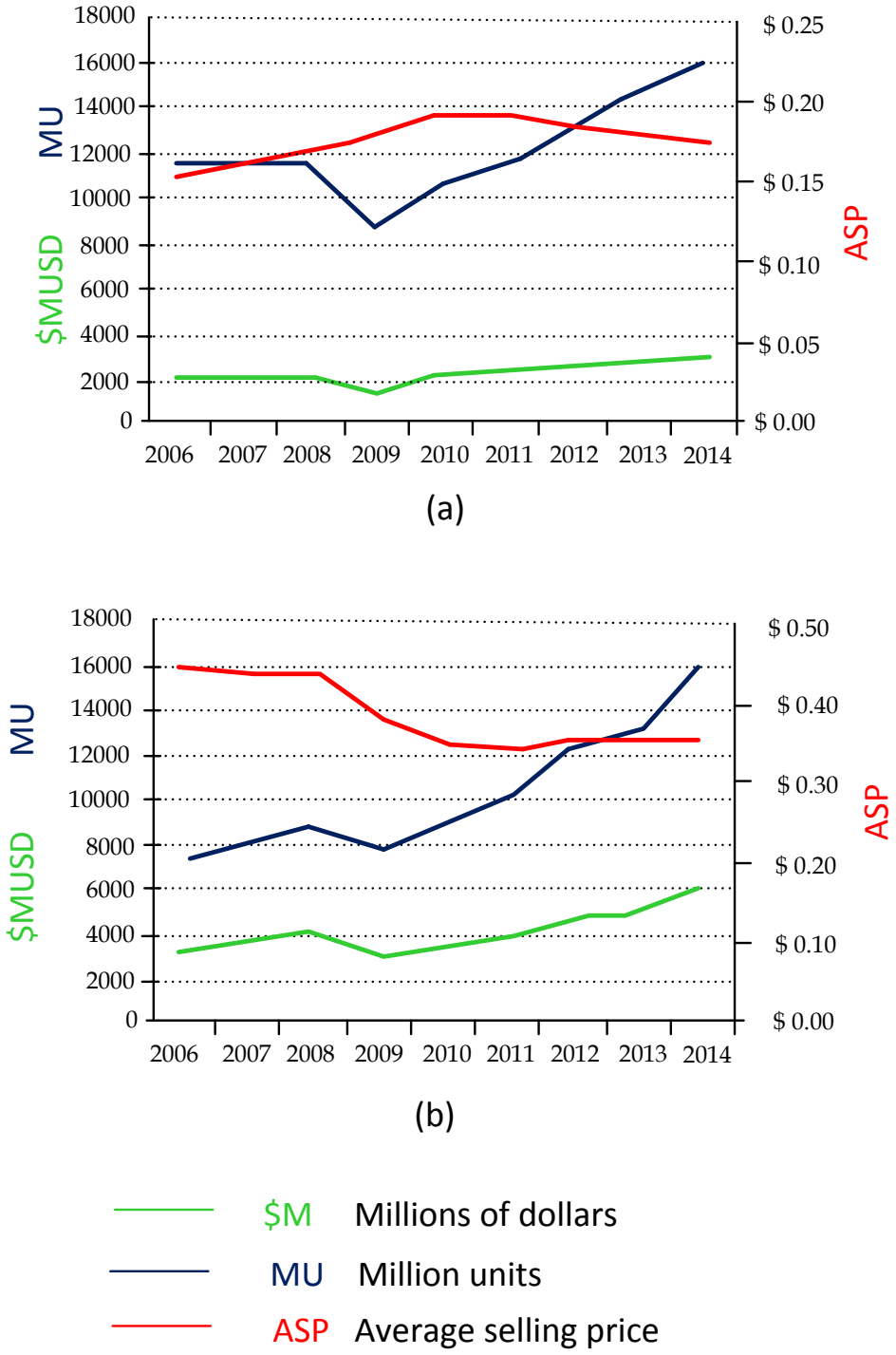


Figure 1.10: Worldwide market forecast (a) switching regulators (b) LDO regulators [43]

voltage combination [2]. The end-to-end efficiency of the overall circuit is improved significantly, while maintaining the useful hallmarks of a linear regulator. The technique is identified as a versatile approach in developing DC-DC converters applicable for processor power supplies with very high end-to-end efficiency, and can be developed further to compete with the higher efficiency switching power supplies. In-depth theoretical analysis and further improvements were identified as essential areas for further research to be carried out to ensure the applicability of SCALDO technique in modern power supply requirements. Based on this, PhD research on "Analysis on Supercapacitor-Assisted Low Dropout (SCALDO) Regulators" was suggested.

The research tasks were carried out along the following lines.

1. Further analyse the theory on SCALDO concept to develop the generalised mathematical models applicable to any DC-DC input-output combination
2. Design and develop various SCALDO prototypes to match the practical requirements based on the generalised theory
3. Identify the practical issues in designing SCALDO regulators
4. Carry out a detailed experimental study on overall system performance on SCALDO technique in terms of line regulation, load regulation, efficiency and transient response for specific practical implementations
5. Analyse essential theory on supercapacitor circulation in SCALDO regulator switching
6. Estimate the power losses of the SCALDO technique
7. Figure out advantages and drawbacks of the novel technique with respect to modern power supply mechanisms and VRM specifications.
8. Outline the areas where tentative further researches can be carried out

1.6 Thesis Structure and Original Work

This thesis is the first comprehensive report of the analysis of the supercapacitor assisted low dropout (SCALDO) regulator technique. Consequently, work done by some of my colleagues of the Power Electronics Research Group has been incorporated in this thesis.

In general terms, my chief supervisor (Nihal Kulatratna) and Jayathu Fernando provided the basic theoretical backbone for the supercapacitor assisted low dropout regulator approach, developing the initial idea of the SCALDO concept which led to filing of a US patent [1]. Lasantha Tilakaratna developed a modification to minimise the loss of paralleling two capacitors at the beginning of the discharge phase. Xu Zhang developed the PCB of the 5.5V-to-3.3V SCALDO prototype and worked with me to take the measurements of line regulation, load regulation, efficiency and transient response.

Assoc. Prof. Alistair Steyn-Ross suggested the use of Laplace transform theory as a better way of analysing the SCALDO operation. He guided me in developing the Laplace

transform based analysis for the SCALDO cycle of the Phase I (supercapacitor charging phase) as an example. Then he improved the MATLAB code that I developed based on the SCALDO cycling in order to get better results.

Thesis Structure

This thesis outlines the design and the analysis of the efficiency enhanced supercapacitor-assisted low dropout (SCALDO) regulator. The chapters of the thesis are laid out as follows.

- Chapter 1 presents the general overview of the project background and the motivation factors detailing the requirement of modern power supply and power supply market demand
- Chapter 2 presents a brief overview on DC-DC converters starting with unregulated power supplies followed by a general discussion on linear regulators with special attention to low dropout regulators performance and applications
- Chapter 3 continues the discussion on DC-DC converters making it specific to high frequency DC-DC converters; switch mode powers supplies and switched capacitor converters
- Chapter 4 discusses the fundamentals of analysing the control loop of DC-DC converters
- Chapter 5 presents basic capacitor theory and the importance of supercapacitors and their applications in various industries, paying specific attention to its use as an energy buffer
- Chapter 6 introduces the basic concept of the SCALDO-patented technique and the generalised theory, and their step-by-step derivations. Comparison of the SCALDO technique with classical switched capacitor technique is also given at the end of the discussion
- Chapter 7 illustrates the experimental results of the overall system performance on the SCALDO technique in terms of line regulation, load regulation, efficiency and transient response for practical implementations
- Chapter 8 explains the essential theory of Laplace transform-based analytical solution developed to predict the performance and associated waveforms of the individual phases of the SCALDO operation
- Chapter 9 discusses the loss estimation of the SCALDO technique with supporting theoretical information
- The conclusion outlines the results of the project and the areas of tentative further research that can be carried out

Original Work

My original contributions include:

- Theoretical analysis of the SCALDO concept to further develop the generalised mathematical models applicable to any DC-DC input-output combination forming the basis of SCALDO regulator design
- Design and development of 5V-to-2V and 12V-to-5V SCALDO prototypes to match the practical requirements and identification of the issues in designing the SCALDO regulators
- Detailed experimental study on overall system performance of 5V-to-2V and 12V-to-5V and 5.5V-to-3.3 V SCALDO prototypes in terms of line regulation, load regulation, efficiency and transient response for several practical implementations
- Development of Laplace transform-based theoretical analysis to predict the performance and associated waveforms of the individual phases of the SCALDO operation
- Power loss estimation and analysis of the SCALDO regulator using the Laplace transform based analytical solution

The following eleven international publications were achieved alongside this thesis.

Journal papers

- K. Kankanamge[1], N. Kularatna, and D.A. Styen-Ross, "Laplace Transform-Based Theoretical Foundations and Experimental Validation-Low Frequency Supercapacitor Circulation for Efficiency Improvements in Linear Regulators", accepted for publication in IET Power Electronics.
- K. Kankanamge and N. Kularatna, "Improving the end-to-end efficiency of DC-DC converters based on a supercapacitor assisted low dropout regulator (SCALDO) technique" Submitted to Transactions on IEEE Industrial Electronics.

Peer-reviewed conference papers

- K. Kankanamge, N. Kularatna, and D. A. Steyn-Ross, "Laplace Transform-Based Theoretical Foundations and Experimental Validation Low Frequency Supercapacitor Circulation Technique for Efficiency Improvements in Linear Regulators" Proc. of IEEE Industrial Electronics Conference 2011, Melbourne, Australia, Nov 2011, pp. 4113-4118.
- K. Kankanamge, and N. Kularatna, "Implementation aspects of a new linear regulator topology based on low frequency supercapacitor circulation", Proc. of Applied Power Electronics Conference 2012, pp. 2340-2344.
- K. Kankanamge, and N. Kularatna, "Supercapacitor assisted LDO (SCALDO) technique- an extra low frequency design approach to high efficiency DC-DC converters and how it compares with the classical switched capacitor converters", Submitted to Proc. of Applied Power Electronics Conferenece 2013.

[1]K. Kankanamge was my maiden name but this thesis is submitted under my married name K. Gunawardane

- N. Kularatna, J. Fernando, K. Kankanamge and L. Tilakaratna, "Very low frequency supercapacitor techniques to improve the end-to-end efficiency of DC-DC converters based on commercial off the shelf LDOs" Proc. of IEEE Industrial Electronics Conference, 2010, pp. 721-726.
- N. Kularatna, J. Fernando, K. Kankanamge and X. Zhang, "A low frequency supercapacitor circulation technique to improve the efficiency of linear regulators based on LDO ICs," Proc. of IEEE Applied Power Electronics Conference, Texas, USA, 2011, pp. 1161-1165.
- J. Fernando, N. Kularatna and K. Kankanamge, "Indirect Applications of Supercapacitor Energy Storage Capabilities and Characterisation Required", Proc. of IEEE 22nd International Symposium on Industrial Electronics, Taiwan, May 2013.

Magazine articles

- N. Kularatna, K. Kankanamge, and J. Fernando, "Supercaps improve LDO efficiency-Part 1: Low noise linear supplies", Power Electronics Technology Magazine, USA, April 2011, pp.14-17.
- N. Kularatna, K. Kankanamge, and J. Fernando, "Supercapacitor enhances LDO efficiency- Part 2: Implementation", Power Electronics Technology Magazine, USA, May 2011, pp.30-33.

Book chapters

- K. Kankanamge-Gunawardane, "Control Loop Design of DC-to-DC Converters", Chapter 5 (Ed) N. Kularatna (2011): DC power supplies, power management and surge protection for power electronics systems, FL, USA, CRC Press., 2011.

Chapter 2

DC-to-DC Converters

2.1 Unregulated Power Supplies

A DC power supply derived from a commercial AC source can be of two fundamental types:

1. Transformer-isolated
2. Non transformer-isolated

A transformer-isolated power supply is bulky due to its line frequency transformer and this type of supply was utilised in older electronic equipment where the compactness of the device was not a major concern. This is still used in some applications where the safety of the device is a critical concern. In the non-transformer-isolated type, the regulatory requirements of electrical isolation are covered by a DC-DC converter followed by an unregulated DC power supply, so that direct rectification and smoothing can be used without having the burden of transformers. A common example is the power supply of a personal (desktop) computer. In such an approach, the incoming line voltage is directly rectified and filtered by a smoothing capacitor where the voltage rating exceeds the peak value of the AC line voltage, which is either 165 V DC (for 120 V, 60 Hz systems) or 325 V DC (for 230 V, 50 Hz). Fig. 2.1 indicates the difference between these two approaches.

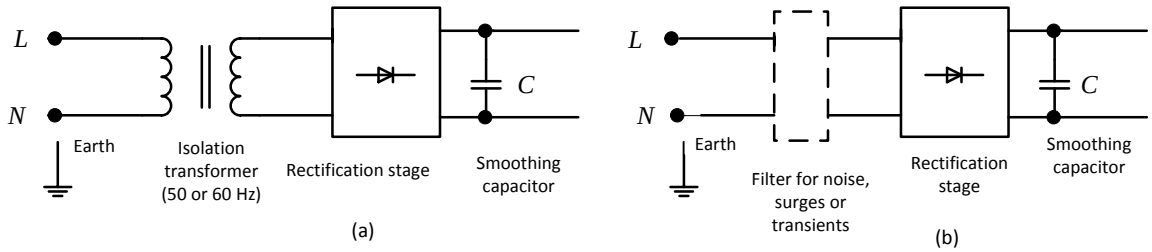


Figure 2.1: Unregulated power supply derived from a commercial AC line (a) transformer isolated (b) non-transformer isolated direct rectification

For the unregulated power supply shown in Fig. 2.2, if the peak voltage of the waveform appearing at the input of the bridge rectifier is V_{pk} and the line frequency is f, the peak-to-peak ripple voltage at the output can be approximated as,

$$\Delta V_{\text{pk-pk}} \approx \frac{I_L}{2fC} \tag{2.1}$$

where C is the smoothing capacitor and I_L is the load current.

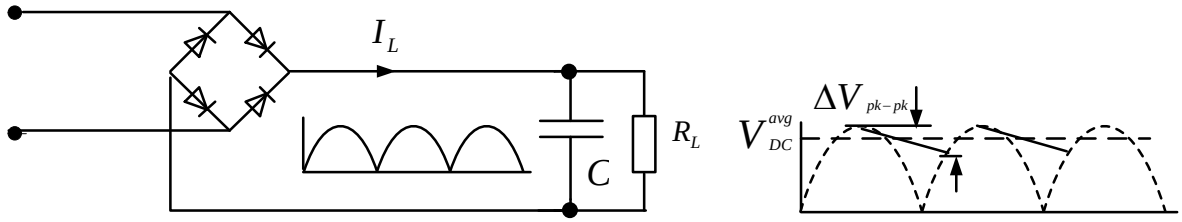


Figure 2.2: Estimating the size of the smoothing capacitor

For an ideal capacitor, if the forward voltage drop across each of diodes is V_D, the approximate output DC voltage, V_{DC} will be,

$$V_{\text{DC}} = V_{\text{pk}} - 2V_D - \frac{I_L}{4fC} \tag{2.2}$$

The approximate design parameters for an unregulated DC power supply can be estimated using the above relationships, either with or without a transformer.

An unregulated DC power supply has a load regulation curve as per Fig. 2.3 due to some practical limitations such as path resistances, diode resistances, equivalent series resistance (ESR) of the smoothing capacitor and transformer losses etc [44].

2.2 Regulated Power Supplies

The operation of every electronic circuit requires a supply voltage, which is usually assumed as a steady, constant voltage DC power supply [45]. Given the scenario of load regulation of the unregulated power supply in Fig. 2.3, design improvements are needed to make the output DC voltage constant at different load currents and input voltages.

Historically, with the availability of vacuum tubes, regulated power supplies were developed to solve this load regulation issue. In the early days vacuum tube supplies were well established and such supplies were suited for powering equipment which used relatively low currents at high voltages. However, for high-current low-voltage applications, vacuum tube supplies became bulky and inefficient, and the design was conveniently implemented with transistors [14–16].

When designing a regulated DC power supply, the designer should consider the output voltage changes with respect to three important parameters [46]:

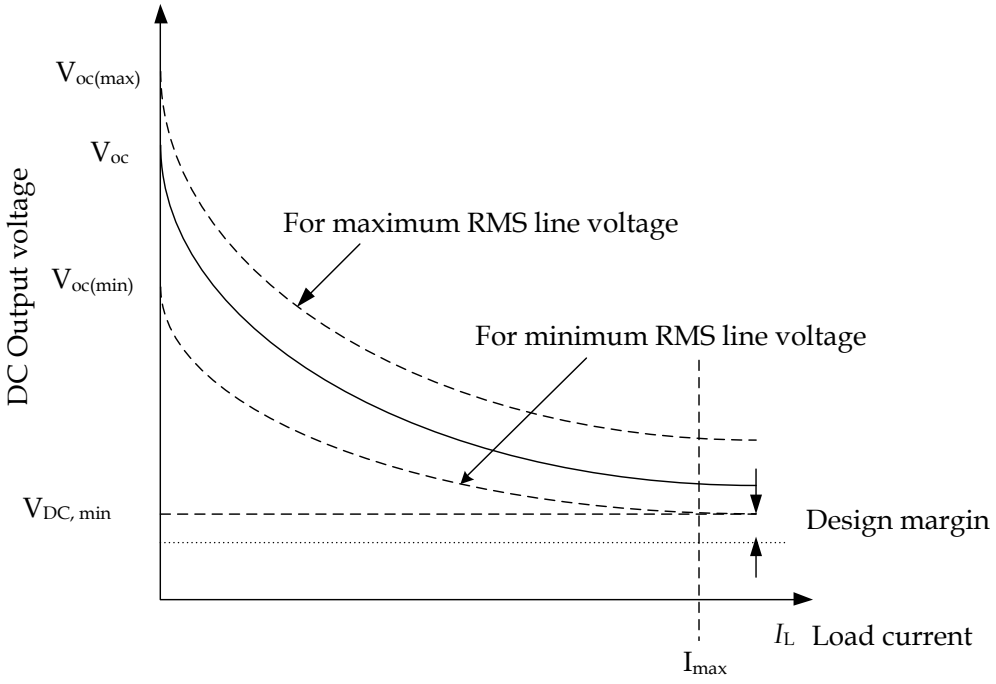


Figure 2.3: Load regulation curve of a typical unregulated DC power supply [44]

1. Variations in load current (load regulation)
2. Fluctuations in input source voltage (line regulation)
3. Variations due to temperature changes

Equation (2.3) shows how these parameters determine the output voltage fluctuations. Here coefficient k_1 represents the Thevenin resistance, which is the output resistance (R_o) of the circuit, k_2 represents the coefficient representing line regulation, and k_3 represents temperature coefficient of the power supply.

$$\Delta V_{\text{reg}} = k_1 \Delta I_L + k_2 \Delta V_S + k_3 \Delta T \tag{2.3}$$

Different types of transistor-based regulators were designed and improvements were made to enhance the performance. More details can be found in [16, 46–48].

To illustrate the above relationship shown in Eqn. (2.3), a simple version of an open-loop linear DC regulator which is based on a single transistor will be considered. In any linear regulator configuration, output voltage is regulated by controlling the voltage drop across the series-pass element. (More details on linear regulators will be discussed later.)

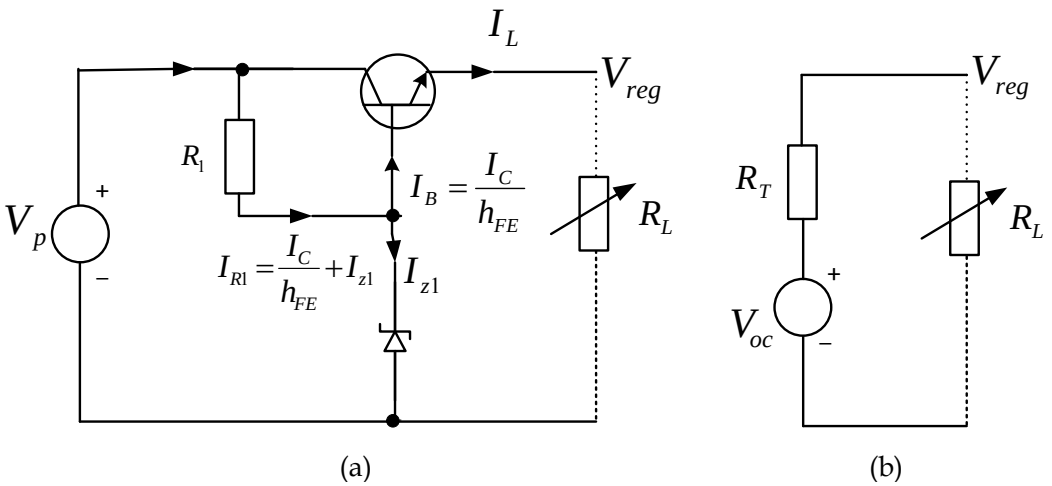


Figure 2.4: The basic linear regulator configuration - an open loop type[1]

Figure 2.4(a)[1] illustrates a very simple open-loop linear regulator. In general, the output regulated voltage, V_{reg} can be approximated by,

$$V_{\text{reg}} = V_z - V_{\text{BE}} \tag{2.4}$$

Under maximum load conditions, if the zener diode voltage is to be maintained at its breakdown value with a minimum current of $I_Z^{\min}$, the current through resistor R_1 under maximum load current is,

$$I_{R_1} \approx \frac{I_L^{\max}}{h_{\text{FE}}} + I_z^{\min} \tag{2.5}$$

If the load is removed, the base current is driven into the zener diode and in that situation, the worst-case current through the resistor R_1 is,

$$I_{R_1}^{\text{worstcase}} \approx \frac{V_{\text{in}}^{\max} - V_Z}{R_1 + r_Z} \approx I_Z^{\max} \tag{2.6}$$

If the zener diode internal resistance is negligible,

$$I_{R_1}^{\text{worstcase}} \approx I_Z^{\max} \approx \frac{I_L^{\max}}{h_{\text{FE}}} + I_Z^{\min} \tag{2.7}$$

In this situation, the approximate Thevenin equivalent circuit parameters are,

$$V_{\text{oc}} \approx \frac{V_Z R_1 - V_{\text{in}} r_Z}{R_1 + r_Z} - V_{\text{BE}} \tag{2.8}$$

$$R_T \approx (R_1 // r_Z) + r_e \tag{2.9}$$

[1]Please note that this circuit cannot be used without including a protection circuit, and having a protection strategy so that in the event of a fault the circuit will protect itself. A generalised discussion on power supply protection strategies is available in section 3.3

where r_e is one of the transistor's T-model circuit parameters.

Considering Thevenin equivalent circuit model of the circuit shown in Fig. 2.4(b),

$$V_{\text{reg}} = V_{\text{oc}} - R_T I_L \tag{2.10}$$

Which gives,

$$V_{\text{reg}} = -\left[\frac{R_1 r_Z}{R_1 + r_Z} + r_e\right] I_L - \left[\frac{r_Z}{R_1 + r_Z}\right] V_{\text{in}} + \left[\frac{R_1}{R_1 + r_Z} V_Z - V_{\text{BE}}\right] \tag{2.11}$$

$$I_E = I_L = \frac{I_S}{\alpha} \exp\left[\frac{V_{\text{BE}}}{V_T}\right] \tag{2.12}$$

which gives,

$$V_{\text{BE}} = V_T \log\left[\alpha \frac{I_L}{I_S}\right] = \frac{kT}{q} \log\left[\alpha \frac{I_L}{I_S}\right] \tag{2.13}$$

where I_S is the saturation current and V_T is the thermal voltage of the B-E junction considering the nominal voltage V_z and temperature coefficient k_T of the zener diode.

$$V_{\text{reg}} = -\left[\frac{R_1 r_Z}{R_1 + r_Z} + r_e\right] I_L - \left[\frac{r_Z}{R_1 + r_Z}\right] V_{\text{in}} + \left[\frac{R_1}{R_1 + r_Z} V_Z \left[1 + k_T T\right] - \frac{kT}{q} \log\left[\alpha \frac{I_L}{I_S}\right]\right] \tag{2.14}$$

Given the above simplified analysis, it is evident that the regulated output has a severe dependency on the value of the V_{BE} and the impact of the base current variations under load conditions. This leads to values of coefficients in Eqn. (2.14) given by,

$$k_1 = -\left[\frac{R_1 r_Z}{R_1 + r_Z} + r_e\right] \tag{2.15}$$

$$k_2 = -\left[\frac{R_1 r_Z}{R_1 + r_Z} + r_e\right] \tag{2.16}$$

$$k_3 = \left[\frac{k_T R_1}{R_1 + r_Z} V_Z - \frac{k}{q} \log\left[\alpha \frac{I_L}{I_S}\right]\right] \tag{2.17}$$

In modern electronics, the following three basic approaches are available for DC-DC conversion:

1. Linear regulators
2. Switched-mode power supplies (SMPS)
3. Switched capacitors (charge pumps)

In a practical system, with a properly designed protection strategy, these three techniques can be combined to provide a complex, but elegant, overall solution with energy efficiency, effective silicon or PCB footprint, and noise and transient performance to suit different parts of an electronic system. Table 2.1 compares the popular DC-DC converter techniques. Detailed discussion on linear regulators is presented in the following section.

Detailed discussion on switch mode power supplies and charge pumps will be available in Chapter 3.

Table 2.1: Comparison of popular DC-DC converter techniques

Feature	Linear regulators	Charge pump converters	Switched-mode power supplies
Design Complexity	Low	Moderate	Moderate-to-High
Cost	Low	Moderate	Moderate
Noise	Lowest	Low	Low-to-Moderate
Efficiency	Low-to-Moderate	Moderate-to-High	High
Thermal Management	Poor-to-Moderate	Good	Best
Output Current Capability	Moderate	Low	High
Requirement of Magnetic Parts	No	No	Yes
Limitations	Cannot Step Up	V_{IN}/V_{OUT} Ratio	Layout Considerations

2.3 Linear Regulators

In order to obtain the desired regulated output voltage, a linear regulator operates using the concept of a voltage-controlled current source. As shown in Fig. 2.5[1], the control circuitry monitors the output voltage, and adjusts the current source as required by the load, to hold the output voltage at the desired value [49]. The specifications of the current source defines the maximum load current the regulator can withstand while maintaining regulation. As discussed in the previous example, the output voltage is controlled using a feedback loop, which requires a compensation to assure loop stability. Most linear regulator topologies have built-in compensation, and are completely stable without external components. Some regulators such as low dropout regulators, require some external components such as output capacitors, to maintain regulator stability. More details about the stability of linear regulators will be discussed in Chapter 4.

In order to keep the output voltage, V_{reg}, constant for the fluctuations of load current or input voltage, the following relationship can be derived.

$$R_S = R_L \frac{V_p - V_{\text{reg}}}{V_{\text{reg}}} \tag{2.18}$$

where V_p, R_S and R_L are input voltage, resistance due to the linear regulator's series pass element and the load resistance respectively.

The same relationship can be represented as,

$$R_S = R_L \frac{V_{\text{d-o}}}{V_{\text{reg}}} \tag{2.19}$$

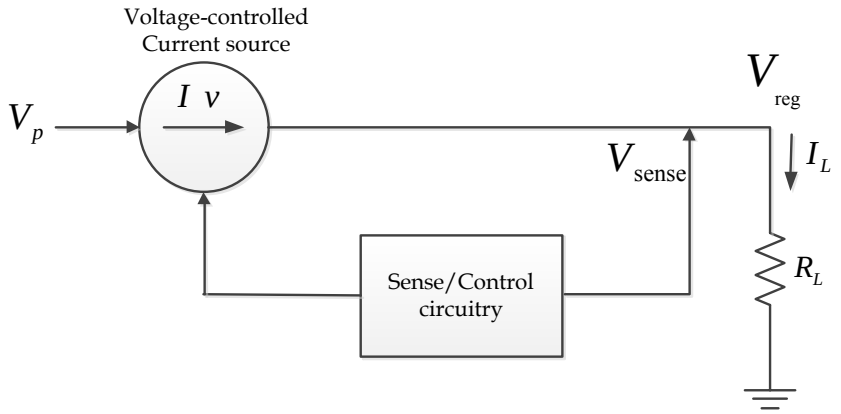


Figure 2.5: Linear regulator functional diagram[1] [49]

where $V_{\text{d-o}}$ is the voltage across the series pass element, which is the same as the dropout voltage. The feedback circuit is expected to control the value R_S for the fluctuations of $V_{\text{d-o}}$.

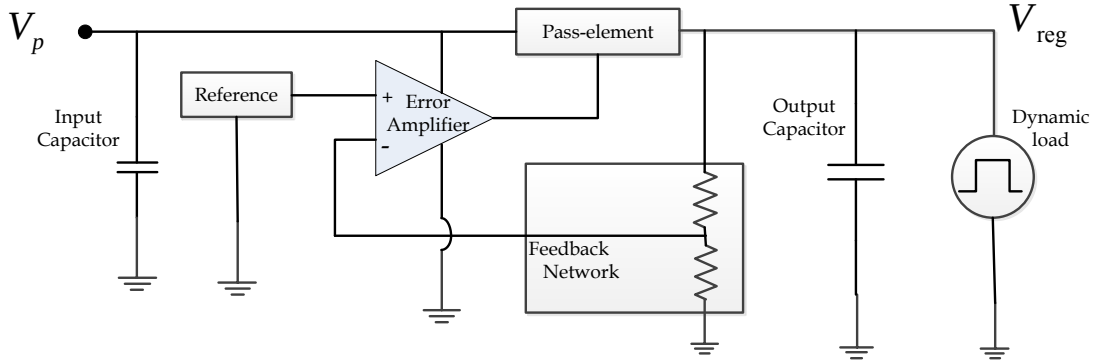


Figure 2.6: Linear regulator block diagram[1]

As shown in Fig. 2.6[1], the major components of a typical linear regulator include the pass element, the precision reference, the feedback network, and the error amplifier. The pass element is a transistor or a combination of transistors whereas the output voltage is regulated by controlling the voltage drop across the series pass element, which is normally a power transistor biased in the linear or saturation region, avoiding any secondary breakdown situations. The voltage-error amplifier with negative feedback given by the fraction of output voltage, forms the feedback signal. The error amplifier continuously amplifies the difference between precision reference and the fraction of output voltage, to control the conductivity of the pass element [24, 45, 49–53].

Figure 2.7[1] illustrates the basic elements of a single transistor-based, closed-loop, linear regulator. As with the open-loop regulator discussed in the example before, the output voltage is regulated by controlling the voltage drop across the series pass-element. If the

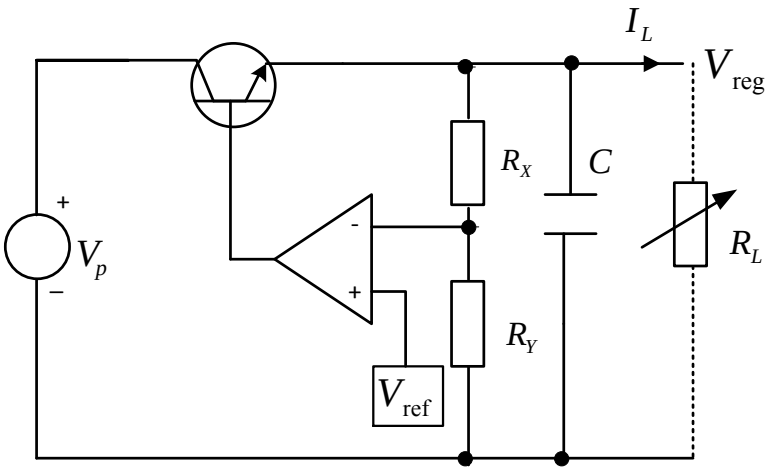


Figure 2.7: The basic linear regulator configuration - closed-loop type[1]

op-amp is ideal, and the reference voltage is fixed at V_{ref}, as far as the opamp can maintain its basic function, V_{reg} can be given by,

$$V_{\text{reg}} = V_{\text{ref}} \left[1 + \frac{R_X}{R_Y} \right] \tag{2.20}$$

In the case where a non-ideal opamp with an open loop gain of A_{OL} and input resistance between the inverting and non-inverting inputs is R_{in}, the following relationship for an output load current of I_L can be developed as,

$$V_{\text{reg}} = \left[1 + \frac{R_Y}{R_X} \right] V_{\text{ref}} - \frac{V_{\text{BE}}}{A_{\text{OL}}} \left[1 + \frac{R_X}{R_Y} \right] \left[\frac{1 + R_X // R_Y}{R_{\text{in}}} \right] \tag{2.21}$$

The power dissipation of a linear regulator is determined by the difference between the input and the output voltage, output load current, and the power consumed by control circuitry. The power dissipation in the series-pass device contributes largely to lower the efficiency of linear regulators compared to switching regulators. The efficiency of a linear regulator can be approximated by,

$$\eta = \frac{V_{\text{reg}} I_L}{V_p I_p} \approx \frac{V_{\text{reg}} I_L}{V_p (I_L + I_q)} \approx \frac{V_{\text{reg}}}{V_p \left[1 + \frac{I_q}{I_L} \right]} \tag{2.22}$$

where I_q is the current drawn by the control circuits which is usually referred to as the ground pin current. If the power consumption of the control circuit is negligible, then the best possible theoretical efficiency of a linear regulator is given by,

$$\eta_{\text{max}} \approx \frac{V_{\text{reg}}}{V_p} \tag{2.23}$$

The major advantages of linear regulators compared to switching regulators are low noise, excellent transient response to load current fluctuations, design simplicity and low cost. However, due to their low efficiency, these circuits are not attractive to high-power requirements with wide differential voltage between the input and output sides [24, 54, 55]. The following section illustrates more details of the essential components of a linear regulator circuit.

Due to the difference in pass elements, in general, there are three basic types of linear regulator topologies:

1. Standard (NPN Darlington) regulator or MOSFET
2. Quasi LDO regulator
3. Low dropout or LDO regulator

In a linear regulator, the minimum possible difference between the input voltage and the output voltage while retaining the regulatory function, is referred to as the dropout voltage. In the above topologies, the dropout voltage shows a remarkable difference across the three. A linear regulator, that operates with the highest dropout voltage, dissipates the most internal power so has the lowest efficiency.

Another important difference between these regulator types is the ground-pin current required by the regulator when driving rated load current. Increased ground-pin current is undesirable as it is a form of wasted power, which must be supplied by the power source.

Another characteristic that describes the performance of a linear regulator is transient response, which is the finite amount of time to correct the output voltage after a change in load current. This characteristic is a measure of how fast the regulator returns to steady-state conditions after a change of the load current.

The topological differences among the above three linear regulator configurations will be discussed in the following section based on the references [24, 45, 49, 53, 56].

2.3.1 NPN Regulator

A standard NPN regulator as shown in Fig. 2.8[1] uses a combination of transistors which consists of an NPN Darlington pass transistor (Q_2 and Q_3) with a PNP base current driver transistor (Q_1), as the pass element. The dropout voltage of this regulator is given by,

$$V_{\mathrm{DROP}} = V_{\mathrm{SAT}}(Q_1) + V_{\mathrm{BE}}(Q_2) + V_{\mathrm{BE}}(Q_3) \tag{2.24}$$

where $V_{\mathrm{SAT}}(Q_1)$ is the saturation voltage across the collector and the emitter (V_{CE}) terminals of the PNP transistor, Q_1 and $V_{\mathrm{BE}}(Q_2)$ and $V_{\mathrm{BE}}(Q_3)$ are the voltages across the base and the emitter terminals of the NPN transistors.

This standard NPN regulator has a very steady ground-pin current which is typically several milliamperes. This regulator configuration is unconditionally stable without any

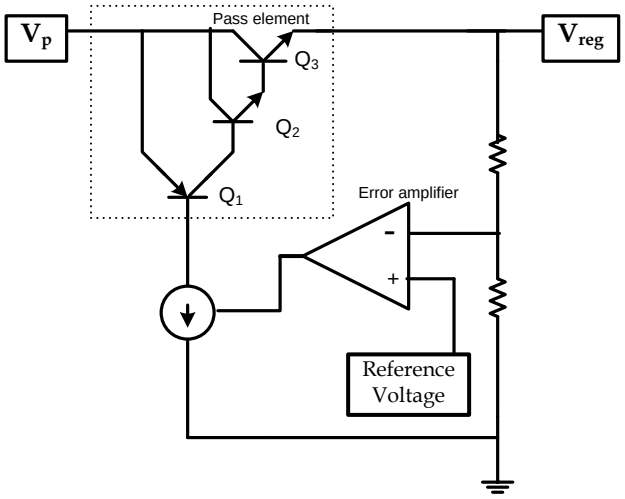


Figure 2.8: A standard NPN regulator configuration[1]

external capacitors and is a better choice for AC-powered applications where the input-output voltage differential is several volts. Standard NPN regulator is not a good choice for powering modern portable electronic devices due to its rather high dropout voltage.

2.3.2 Quasi-NPN Regulator

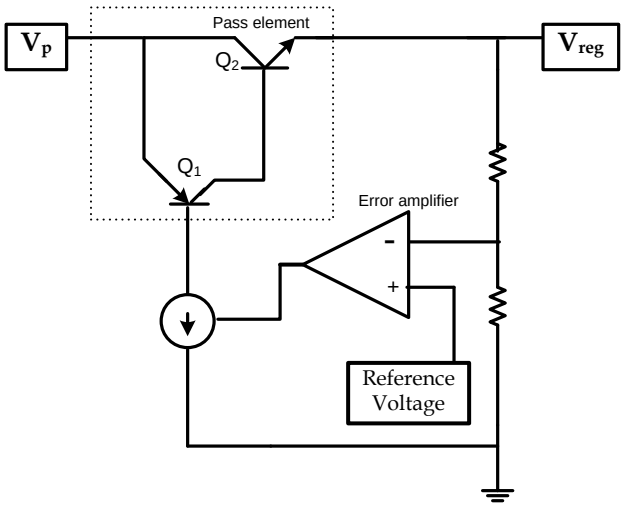


Figure 2.9: Quasi- NPN regulator configuration[1]

As is obvious from the topological differences between the series-pass devices, the dropout voltage of the quasi-NPN regulator is lower than that of the standard NPN regulator. As shown in Fig. 2.9[1], the NPN pass transistor regulator uses the combination of a PNP base current driver transistor (Q_1) and a single NPN power transistor (Q_2), as

the pass element. Therefore the dropout voltage is given by,

$$V_{\mathrm{DROP}} = V_{\mathrm{SAT}}(Q_1) + V_{\mathrm{BE}}(Q_2) \tag{2.25}$$

It has a relatively steady ground pin current which is typically several milliamperes. This configuration requires an output capacitor to sustain stable operation. (More details will discussed in the next chapter). Due to its relatively low dropout voltage, the NPN pass transistor regulator is a good choice for modern battery powered portable electronic devices.

2.3.3 Low Drop-out Regulator

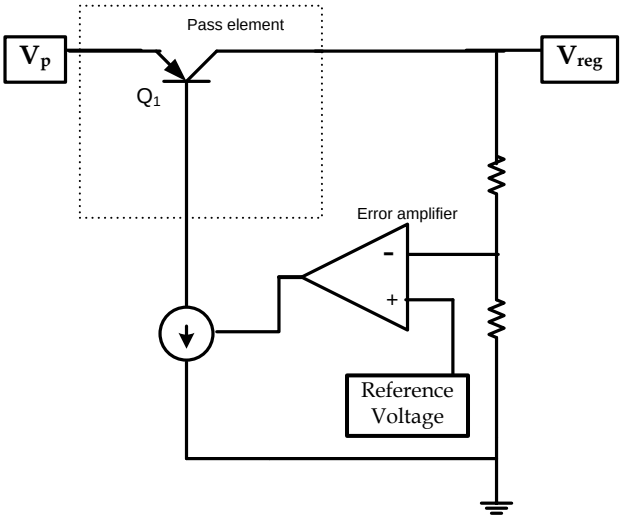


Figure 2.10: Low dropout regulator configuration[1]

As shown in Fig. 2.10[1], an LDO uses a PNP transistor as the pass element. Its dropout voltage is given by,

$$V_{\mathrm{DROP}} = V_{\mathrm{SAT}}(Q_1) \tag{2.26}$$

The dropout voltage of the LDO regulator is typically between 0.1 V and 0.7 V. The LDO regulator offers the best dropout voltage among the three bipolar technology-based linear regulators and it is the best option of the three for modern battery-powered embedded applications.

However, the LDO regulator has an unsteady ground-pin current because of the relatively low gain of the PNP transistor. The PNP transistor is has high output impedance. The LDO regulator's operation requires compensation to sustain a stable operation.

Conventionally, the PNP bipolar transistor has been utilised in LDO applications, due its lower dropout voltage than the NPN transistor. However, this configuration has a relatively high ground-pin current and thus lower efficiency which is not ideal for the applications where high efficiency is important. The high ground-pin current problem associated with the PNP LDO regulator is intrinsic to the bipolar processing technology, but can be easily resolved by replacing the regulator construction with a CMOS device. The ground-pin current of a PMOS regulator can be smaller than that of the PNP pass transistor regulator whereas the NMOS pass element is most advantageous due to its low on-resistance. However, the gate-drive difficulties make it less significant and as a result there are only a few NMOS LDOs available. The PMOS-based LDOs have been highly developed and have performance levels exceeding most bipolar devices [45].

In a typical PMOS construction, as shown in Fig. 2.11[1], the gate impedance is very high which makes the gate current extremely low. Since the gate current in a PMOS regulator no longer influences its total ground-pin current, this current can be extremely low.

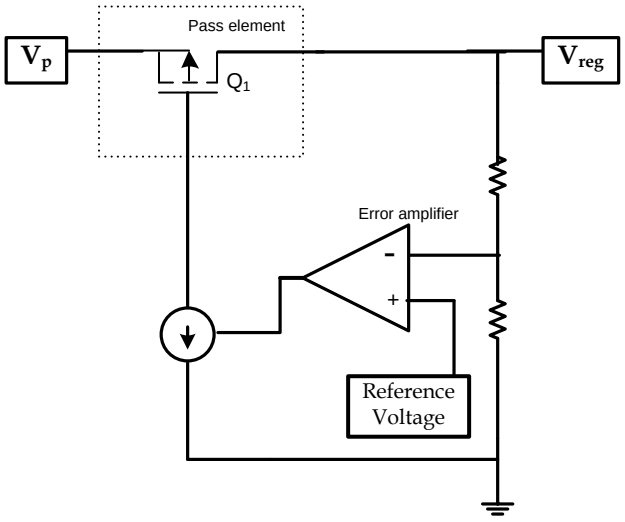


Figure 2.11: P-channel FET low dropout regulator configuration[1]

The PMOS LDO regulator's dropout voltage is given as,

$$V_{\text{DROP}} = R_{\text{DS(ON)}}(Q_1) \times I_L \tag{2.27}$$

where $R_{\text{DS(ON)}}(Q_1)$ is the drain-to-source resistance of the PMOS device when it is fully on, and I_L is the output current to the resistive load.

The dropout voltage can be very low because the $R_{\text{DS(ON)}}$ can be easily adjusted to a very low value by scaling the size of the PMOS. This also means that for a given dropout voltage, the PMOS based LDO is capable of outputting a higher current than the

PNP LDO. The PMOS based LDO creates oscillations without an output capacitor. A carefully selected output capacitor with certain range of capacitance and ESR is required for external compensation. Low dropout voltage and low ground-pin current, make PMOS regulator an excellent choice for battery-powered embedded applications which require extended battery life.

Table 2.2 summarizes the differences of the above discussed linear regulator configurations [45].

Table 2.2: Comparison of Pass Element Structures

Parameter	Standard NPN	Quasi-LDO	LDO-PNP	LDO-NMOS	LDO-PMOS
$I_{\mathrm{L,max}}$	High	High	High	Medium	Medium
I_q	Medium	Medium	Large	Low	Low
$V_{\mathrm{d\text{-}o}}$	$V_{\mathrm{sat}} + 2V_{\mathrm{BE}}$	$V_{\mathrm{sat}} + V_{\mathrm{BE}}$	$V_{\mathrm{CE(sat)}}$	$V_{\mathrm{sat}} + V_{\mathrm{GS}}$	$V_{\mathrm{DS(sat)}}$
Speed	Fast	Fast	Slow	Medium	Medium

2.4 LDO Performance

2.4.1 Efficiency and Power Losses

Usually in linear regulator configurations, most of the energy is dissipated across the pass element. Typical LDO construction does not have any energy storing mechanisms, so the power that is not delivered to the load is dissipated as heat within the LDO.

The power which is dissipated within the regulator (P_D) can be described as follows [45, 55, 57–60]:

$$P_D = [V_p - V_{\mathrm{reg}}]\, I_L + V_p I_q \tag{2.28}$$

The first part of this relationship is the dissipation of the pass device and the second part is the power consumption of the controller portion of the circuit. Linear regulators generate excessive heat if the voltage difference between input and output voltage is high. The larger the difference, the more heat is produced. But, LDOs have extremely low drop-out voltages which can enhance the efficiency of the devices.

As shown in Eqn. (2.22), the efficiency of an LDO regulator is also limited by the ground-pin current of the circuit. To have a high-efficiency LDO, the ground-pin current should be minimised [45, 57]. Modern LDOs have reasonably low I_q, and for simplicity, such a value can be neglected in efficiency calculations if I_q is very small compared to I_L [61, 62].

Fig. 2.12 shows the regulator efficiency as a function of load current (I_L) with different I_q under a particular output voltage (V_{reg}). It shows that the use of very low I_L improves the regulator efficiency at small I_q, which often happens when systems are operating in

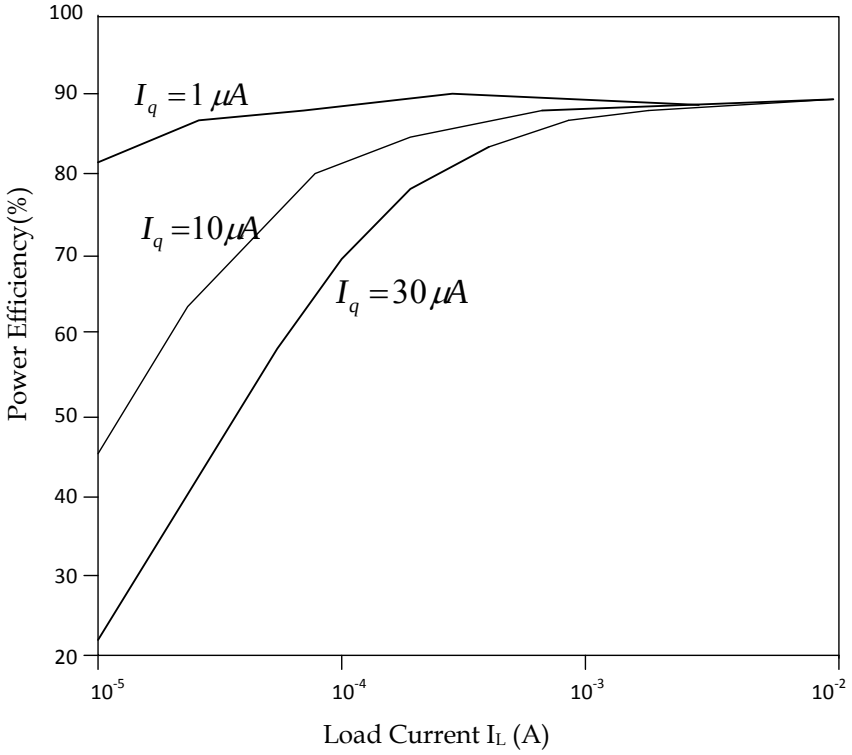


Figure 2.12: Effect of ground-pin current on efficiency of an LDO [61]

standby mode to extend battery life.

Due to its high efficiency, LDO regulator is a well suited popular solution for today's battery-powered portable consumer electronics devices, such as mobile phones, laptops, and game consoles,etc.

2.4.2 Load Regulation

Load regulation is the capability to maintain a constant voltage (or current) level on the output channel of a power supply despite changes in the supply's load (such as a change in resistance value connected across the supply output [63].) The load regulation is defined as,

$$Lo_{\text{reg}} = 100\% \frac{V_{\text{min-load}} - V_{\text{max-load}}}{V_{\text{nom-load}}} \tag{2.29}$$

where, $V_{\text{max-load}}$ is the voltage at maximum load. The maximum load is the one that draws the greatest current, i.e., the lowest specified load resistance (never short circuit); $V_{\text{min-load}}$ is the voltage at minimum load. The minimum load is the one that draws the least current, i.e. the highest specified load resistance (possibly open circuit for some types of linear supplies, usually limited by pass transistor minimum bias levels);

$V_{\text{nom-load}}$ is the voltage at the typical specified load.

Load regulation is a steady-state parameter of a system.Good systems have load regulation of 1% or thereabouts.

Furthermore load regulation can be indirectly represented as output impedance of the power supply. Load regulation is a performance parameter that quantifies the ability to maintain a specified regulated output voltage under varying load conditions [60]. The load regulation can also be denoted as,

$$Lo_{\text{reg}} = \frac{\Delta V_{\text{reg}}}{\Delta I_L} \tag{2.30}$$

A novel topology has been proposed to improve the load regulation with very low quiescent current. The core idea is to operate the pass transistor in its linear region, achieving an area reduction above 90%, reducing the gate capacitance and therefore improving loop response. In addition to this, the Direct Current Sinker (DCS) topology has been combined to improve load regulation without compromising power efficiency, regardless of the maximum output current of the LDO. This improvement can be implemented in any LDO with less efforts to increase the accuracy of the output [64].

2.4.3 Line Regulation

Line regulation is another steady-state performance parameter which is the ability to maintain the specified regulated output voltage under varying input voltages. The line regulation is defined as,

$$Li_{\text{reg}} = \frac{\Delta V_{\text{reg}}}{\Delta V_p} \tag{2.31}$$

2.4.4 Transient Response

The transient response is the maximum allowable output voltage variation for a step change in load current. The transient response is determined by the output capacitor value (C_o), the equivalent series resistance (ESR) of the output capacitor, the bypass capacitor (C_b), and the maximum load current ($I_{\text{L,max}}$) [45, 51, 58, 65]. Fig. 2.13 shows the typical transient response of an LDO regulator for different combinations of input and output capacitors [66]. The maximum transient voltage variation is defined as follows [60, 62].

$$\Delta V_{\text{tr,max}} = \frac{I_{\text{L,max}}}{C_o + C_b}\Delta t_1 + \Delta V_{\text{ESR}} \tag{2.32}$$

where Δt_1 corresponds to the closed-loop bandwidth and ΔV_{ESR} is the voltage variation resulting from the presence of the ESR (R_{ESR}) of the output capacitor. ΔV_{ESR} is proportional to R_{ESR}.

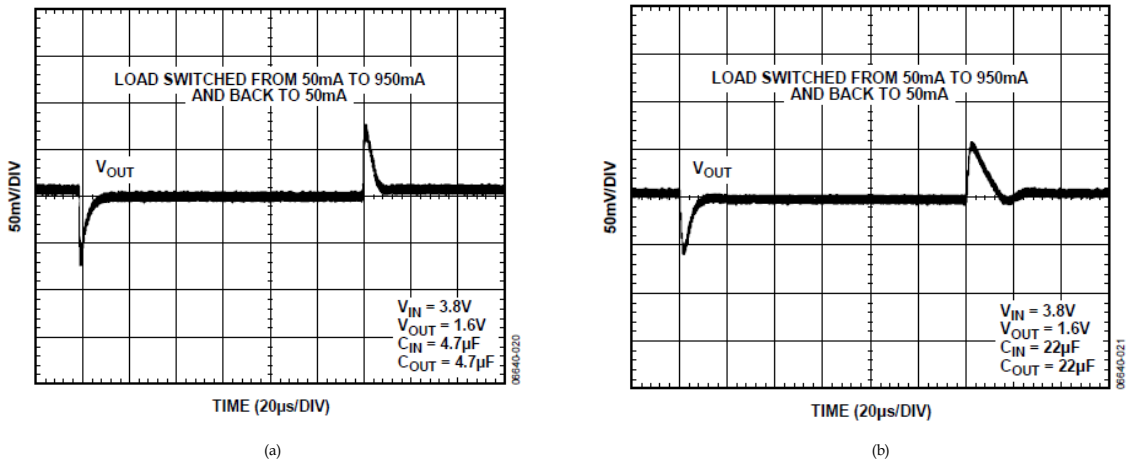


Figure 2.13: Transient response of commercial LDO ADP1708 from Texas Instruments (a) when $C_{\text{IN}} = 4.7\ \mu\text{F}$, $C_{\text{OUT}} = 4.7\ \mu\text{F}$ (b) when $C_{\text{IN}} = 22\ \mu\text{F}$, $C_{\text{OUT}} = 22\ \mu\text{F}$ [66]

Load transient response with small output voltage variation is critical to prevent an accidental turn off or resetting of portable devices. Although reduction of I_q and $V_{\text{d-o}}$ improves efficiency, it slows down the transient response of an LDO regulator. The tail-current in conventional amplifier designs imposes a trade-off between small quiescent current and large slew-rate. A high slew-rate amplifier with pushpull output driving capability is proposed to eliminate this trade-off and enable an ultra-low quiescent current LDO regulator with improved transient response [67].

In order to further improve LDO performance, a buffer impedance attenuation technique (BIA) has been proposed to realize an intermediate stage for driving the PMOS pass device. The proposed BIA technique greatly reduces the output resistance of the buffer through a dynamically-biased shunt feedback. As a result, the pole at the gate of the pass device is pushed far beyond the unity-gain frequency of the LDO regulation loop under the entire load current range even if a huge pass device is used for achieving low dropout voltage and sourcing high load current. The BIA technique thus allows the LDO to dissipate low quiescent current. By employing current-buffer compensation in the LDO, only a single pole is realized within the unity-gain frequency and a good phase margin is achieved for the entire load current range with a small compensation capacitor. Moreover, the LDO can have good transient settling behaviour and small output-voltage variation even if a small output capacitor is used [68].

When a low-voltage IC system is powered by an LDO regulator, it is not easy to suppress the output voltage spikes ΔV_{reg} of the LDO regulator under rapid and large changes of the load transition ΔI_L. A low-voltage fast-response small-voltage-spike LDO regulator with load-tracking impedance adjustment and loop-gain boosting technique has been developed where the stabilization has been achieved by an off-chip, low-ESR, capacitor in the nano farad range [65].

An adaptive reference control (ARC) technique has been proposed for minimizing overshoot-undershoot voltage and settling time of LDOs. This technique is also capable of improving the settling time and load regulation significantly [69].

2.4.5 Power Supply Rejection Ratio (PSRR)

LDOs are used to supply power for portable devices which include RF circuits. In such circuits, a supply that powers the LDO often includes wideband AC ripple superimposed on the DC; the LDO is expected to reject those artefacts.

Power supply ripple rejection ratio (PSRR) is a measure of how well a circuit rejects ripple coming from the input power supply at various frequencies. In the case of an LDO, it is a measure of the output ripple compared to the input ripple over a wide frequency range (10 Hz to 10 MHz is common) and is expressed in decibels (dB) [70–73].
The basic equation for PSRR is,

$$\mathrm{PSRR(dB)} = 20 \log \frac{\text{Voltage ripple output}}{\text{Voltage ripple input}} \tag{2.33}$$

A curve showing PSRR over a wide frequency range for an LDO is shown in Fig. 2.14. PSRR is at a maximum at low frequencies, and begins to fall above 1kHz to 10kHz, depending upon the regulator design.

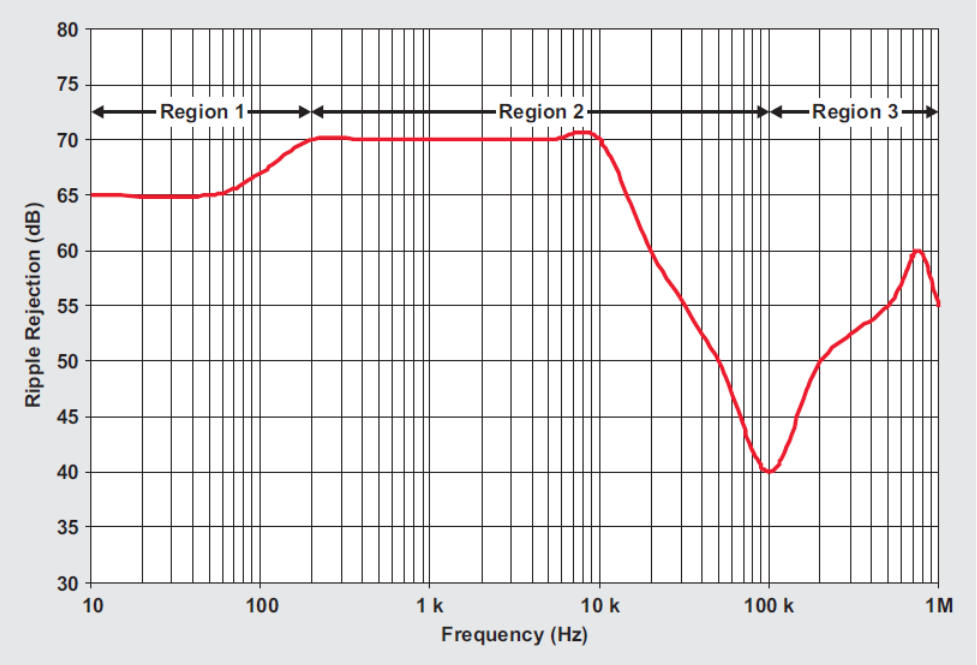


Figure 2.14: LDO PSRR characteristic curve [70]

In general, LDOs have good low-frequency PSRR as the shunt feedback reduces ground impedance at low to moderate frequencies whereas LDOs have poor PSRR performance at high frequencies.

A technique has been proposed inserting a higher frequency current sampling loop without increasing dropout voltage which increases the impedance to the supply at higher frequencies. The aim of the series-sampling loop is to transform the pass transistor into a current source only at higher frequencies. More details can be found in [74].

2.4.6 LDO Noise

In most cases self-generated noise of LDOs is confused with its PSRR. Many times these two are combined and called noise. But more accurately, noise is a physical phenomenon that occurs in transistors and resistors in the LDO's internal circuitry and external components which comprises thermal, flicker and shot noise.

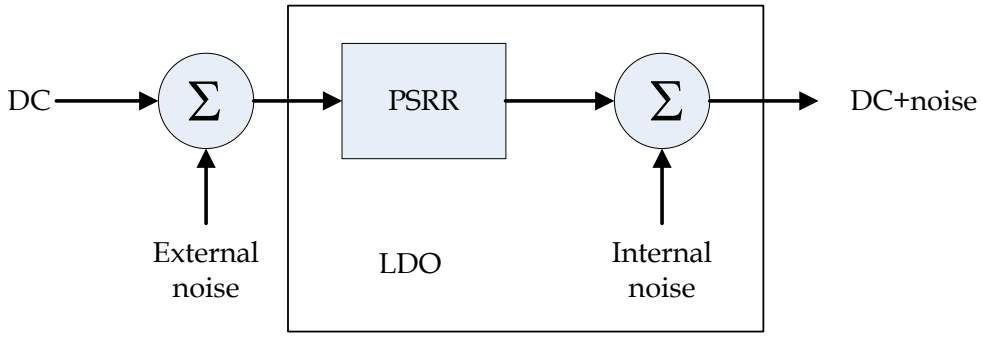


Figure 2.15: Distinction between PSRR and noise in an LDO [75]

Fig. 2.15 illustrates the difference between noise and PSRR. The noise can be either internal or external to the LDO whereas PSRR is an internal parameter of the LDO. LDO users generally concentrate on PSRR and not on the self-generated output noise. PSRR rejects noise coming from outside the LDO but there is always noise generated inside the LDO. So an LDO with high PSRR may not be better for noise rejection [75].

Table 2.3 shows some performance parameters of commercially available LDOs.

2.5 LDO Applications

System-on-chip (SoC) designs that include power management solutions are the modern trend in the portable electronics product industry. With the advancements of portable, hand-held battery-operated devices, improved power efficiency results in prolonged battery life and operating time. A typical power management system contains several subsystems including linear regulators, switching regulators, and control logic. LDO regulators

Table 2.3: Performance comparison for some commercially available LDOs

Model	Output Current (A)	Input Vol. Range (V)	Output Voltage (V)	Dropout voltage	Line Regulation	Load Regulation
Microchip MCP 1827	1.5	2.3–6.0	Fixed 0.8, 1.2, 1.8, 2.5, 3.0, 3.3V and adjustable range of 0.8 V-5.0 V	330 mV at 1.5 A	0.05%/V	0.5%/mA
Texas Instruments TPS75515	5	2.8–5.5	1.5, 1.8, 2.5, 3.3 V fixed and adjustable versions	250 mV at 5 A	0.04%/V	0.35%/mA
National semi LMS1585	3-5	4.75–13	Fixed 1.5 and 3.3 V and adjustable versions	200 mV at 5 A	0.0005%/V	0.05%/mA
Linear Technology LT1581	10	6	Fixed 2.5 V and adjustable versions	430 mV at 10 A	1 mV	1 mA
Analog devices ADP1708	1	2.5–5.5	Fixed 0.75-3.3 V and adjustable versions 0.8 -3.3 V	345 mV at 1 A	0.1%/V	0.001%/mA

are an essential part of the power management system that provides constant voltage supply rails with improved power efficiency [76, 77].

LDO regulators were introduced to address the issues in noise-sensitive and fast transient loads in portable devices. LDO is particularly attractive when compared to a switch-mode design as it can step down an existing supply voltage to a lower value with reasonable efficiency, while achieving the benefits of linear design such as simplicity, low cost, low noise and fast response. As discussed in the previous chapter, a typical LDO has its input voltage slightly higher than the desired output resulting in a higher efficiency than a conventional linear regulator. As shown in Table 2.3, in many situations, the dropout voltage is of the order of 0.1 V to 2 V with the control circuits using extremely low power, providing efficiencies around 65% and even higher for lower dropout voltages, while providing adequate transient response for applications with fast-varying loads [19, 57, 78].

The suppliers of low-voltage LDO regulators are competing to deliver high-performance LDOs in smaller packages with excellent load transient response and stability with the growing power needs of wireless handsets, PDAs, laptops, and other portable, hand-held electronic products [78]. The number of low-voltage LDO suppliers is increasing to meet the power demands of new-generation microprocessors, DSPs and ASICs used in these applications. Furthermore, the space-constraints of the battery-powered products is forcing

manufacturers to pack two or more low-voltage LDOs in an improved package [79,80]. As a result, these low-voltage LDOs are becoming an attractive choice to power low-voltage ICs in portable applications, giving power supply designers various power management options. These LDOs come with optimal combinations of low dropout voltage, quiescent current, transient response, noise and ripple rejection, shutdown mode, and external capacitor requirements [19,57].

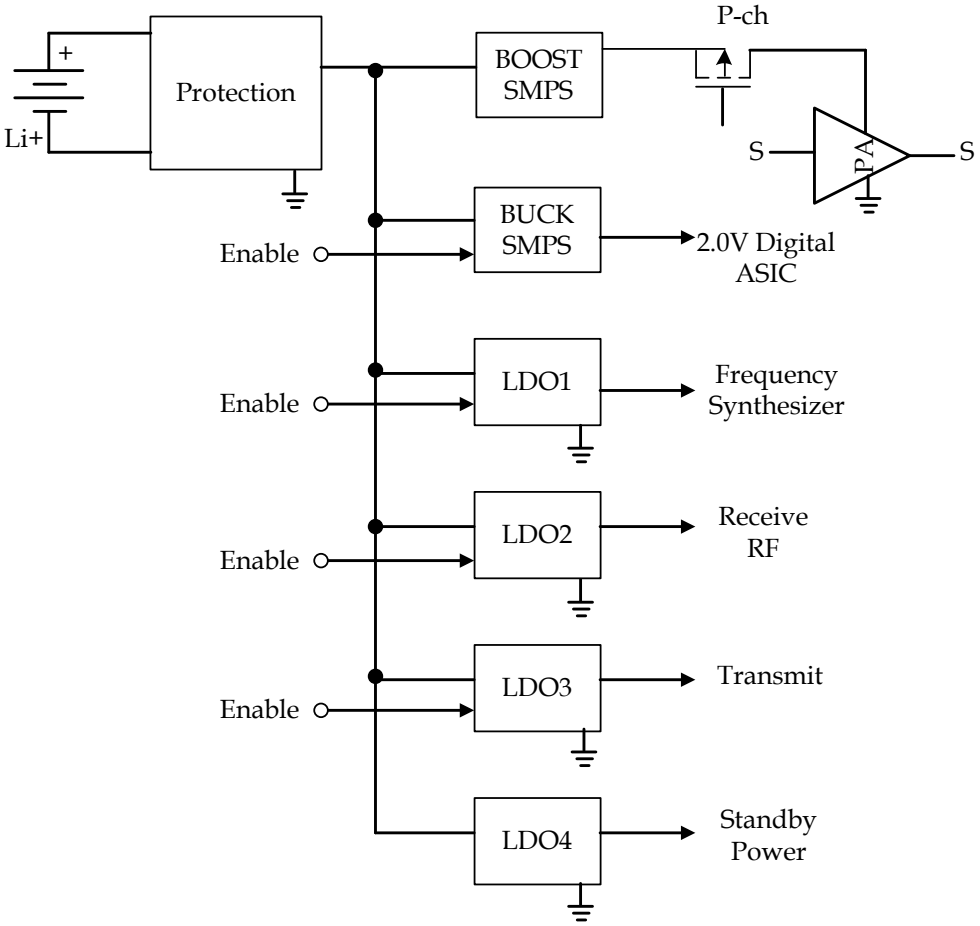


Figure 2.16: Switch-mode and linear regulators distribute power cleanly and efficiently[1] [81]

As analog circuits are more sensitive to noise than digital circuits with their low noise and high PSRR. LDOs are well suited for analog environments such as wireless interfaces [82]. LDOs are used to power the baseband chipsets, RF circuitry, and audio sections of cellular phones which all have different power requirements. The various cell phone blocks are best powered by LDOs with different performance characteristics. In general these cellular phone designs require linear regulators with low-dropout, low-noise, high PSRR, low quiescent current, and low-cost and stable output. More specific cellphone power supply requirements for LDO regulators are available in [81]. To handle the problem of cell-phone noise, the noise-sensitive circuit nodes are powered by LDOs

and other nodes are powered by SMPS. An example of such a design is shown in Fig 2.16[1].

2.6 Chapter Summary

Commercially utilized DC-DC converter techniques can be summarized by three fundamental configurations (i) linear regulators (ii) switch-mode converters (iii) switched capacitor converters. A linear regulator is a zero frequency DC-DC conversion approach, which is usually used for step-down applications where efficiency is not a prime concern, but, low-noise performance, high load-current slew-rate capability, design simplicity and low cost are of prime importance. Due to the difference in pass elements, in general, there are three basic types of linear regulator topologies. Low dropout regulator topology is designed to work with a low voltage difference between the input and the output, and is commonly used in battery-powered portable products. More details on performance and applications of LDOs have been described in this chapter.

The discussion on DC-DC converters continues in the next chapter focusing on high frequency DC-DC converters, switch-mode power supplies and switched capacitor converters.

Chapter 3

High Frequency DC-to-DC Converter Techniques

3.1 Switched-Mode Power Supplies (SMPS)

Switched-mode power supplies (SMPS), are a versatile way of achieving DC power supply requirements of energy efficient, compact and portable systems. One remarkable advantage of switching regulators is the ability to convert a given input voltage to any desired output voltage, regardless of whether the output voltage is higher or lower than the input voltage, or the same or the opposite polarity. Basically, Switch-mode supplies can be divided into two basic types, non-transformer isolated and transformer isolated. Non-transformer isolated versions are used when there is no necessity to have electrical isolation from the primary energy source, especially in lower power systems. Several commonly used non-transformer isolated topologies include (i) buck or step-down converters; (ii) boost or step-up converters; (iii) buck-boost or inverting type converters. Transformer isolated topologies are used in higher power systems which require electrical isolation from the primary supply side. Topologies such as forward mode, flyback, and bridge types are generally used for applications where higher power, galvanic isolation, and multiple output rails are required.

The following sections illustrate the fundamentals of simple and common non-transformer isolated SMPS topologies. A generalised discussion is available and deeper theoretical and design considerations can be referred from the many cited references [24, 44, 83].

3.1.1 Buck Converter

The buck (step-down) converter is used to down-convert an input DC voltage to a lower output DC voltage of the same polarity. Figure 3.2(a) depicts the basic arrangement of a buck converter which comprises four basic elements in the power stage: switch, inductor, capacitor and diode. A transistor is used as a switch which alternately connects and disconnects the input voltage to the inductor.

A switching control signal has a switching frequency of f_c where the total cycle time T_s is comprised of an on time t_{on} and an off duration t_{off}. Figure 3.1(a) illustrates the

basic concept of generating the switch control signal using an amplifier and comparator. Fig. 3.1(b) depicts the comparator signals that generate a pulse-width modulated (PWM) signal as shown in the lower trace of the Fig. 3.1(b). In this situation, the duty ratio can be expressed as,

$$D = \frac{t_{\text{on}}}{T_s} \tag{3.1}$$

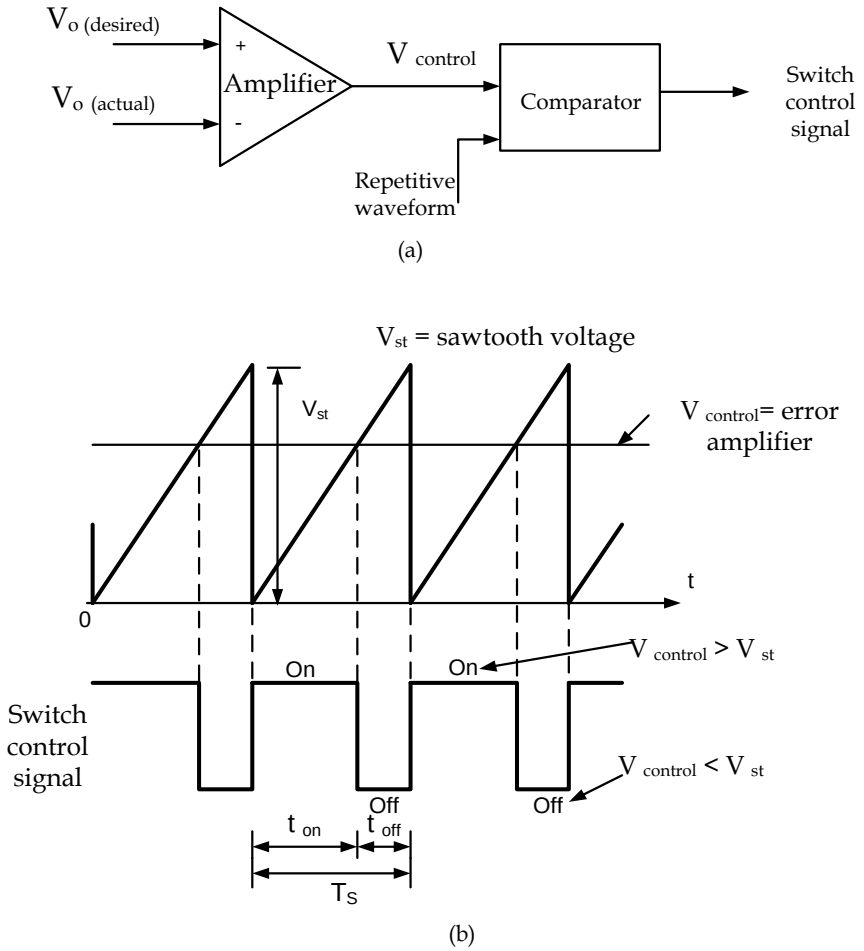


Figure 3.1: Pulse Width Modulation (PWM) (a) Block diagram of a pulse width modulator (b) PWM switch control signal

As shown in Fig. 3.2(b), when the switch is turned on, the input voltage is connected to the inductor. The difference between the input and output voltages ($V_{\text{in}} - V_o$) is applied across the inductor, causing the current through the inductor to increase. During that time, t_{on}, the inductor current flows into both the load and the output capacitor. As a result, the capacitor charges during that time.

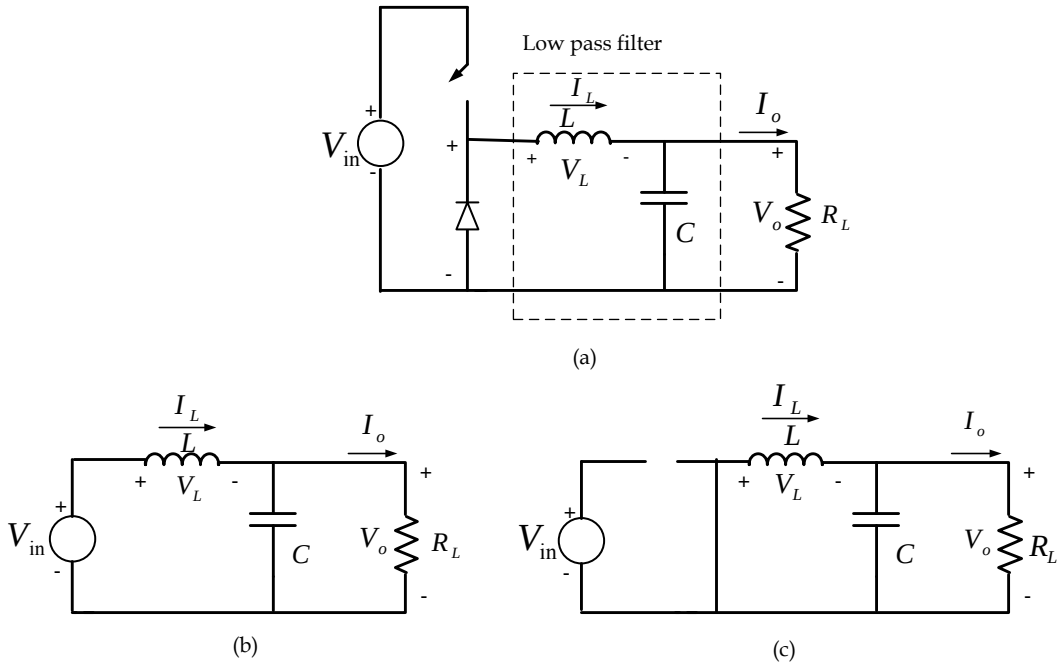


Figure 3.2: Buck converter: (a) basic power stage (b) switch on state (c) switch off state

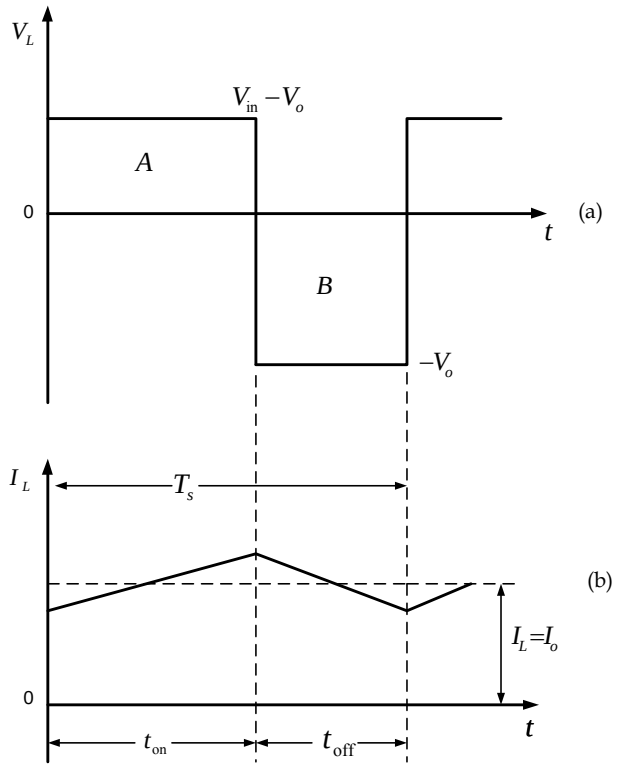


Figure 3.3: Buck converter: waveforms (a) Voltage across the inductor (b) Current through the inductor

As shown in Fig. 3.2(c), when the switch is turned off, the input voltage applied to the inductor is removed. However, as the current in an inductor cannot change instantly, the voltage across the inductor adjusts to hold the current constant. The input end of the inductor is forced to negative in voltage by the decreasing current, eventually reaching the point where the diode is turned on. The inductor current then flows through the load and back through the diode. The capacitor discharges into the load during the off time t_{off}, supplying the total load current. Fig. 3.3(a) and (b) show the voltage and current through the inductor respectively, during switch on and off times.

As explained, the current through the inductor gradually increases when the switch is on, and gradually decreases when the switch is off. The DC load current from the regulated output is the average value of this inductor current. In buck regulator applications, when the switch is turned off, the inductor current does not reach zero. This is known as the continuous conduction mode (CCM). Overall performance is usually better using CCM, and it allows maximum output power to be obtained from a given input voltage and switch-current rating. Discontinuous conduction mode (DCM) operation at lower load current values is generally harmless, and even converters designed for CCM mode operation at full load will become discontinuous as the load current is decreased.

The transfer function of an ideal CCM buck converter is defined as:

$$\frac{V_o}{V_{\text{in}}} = D \tag{3.2}$$

where $D = \dfrac{t_{\text{on}}}{T_s}$

3.1.2 Boost Converter

The boost (step-up) converter circuit is shown in Fig. 3.4. When the switch is on, the input voltage, V_{in} appears across the inductor, and the inductor current also ramps up. When the switch is open, the energy stored in the inductor is transferred to the load through the diode, a voltage equal to $V_o - V_{\text{in}}$ appears across the inductor, and the current ramps down. The corresponding inductor voltage and current waveforms are shown in Fig. 3.5 (a) and (b) respectively. Note that in the boost converter, the input current is continuous, while the output current is pulsating which implies that filtering the output of a boost converter is more difficult than for a buck converter.

The transfer function of a CCM boost converter under ideal conditions is,

$$\frac{V_o}{V_{\text{in}}} = \frac{1}{1-D} \tag{3.3}$$

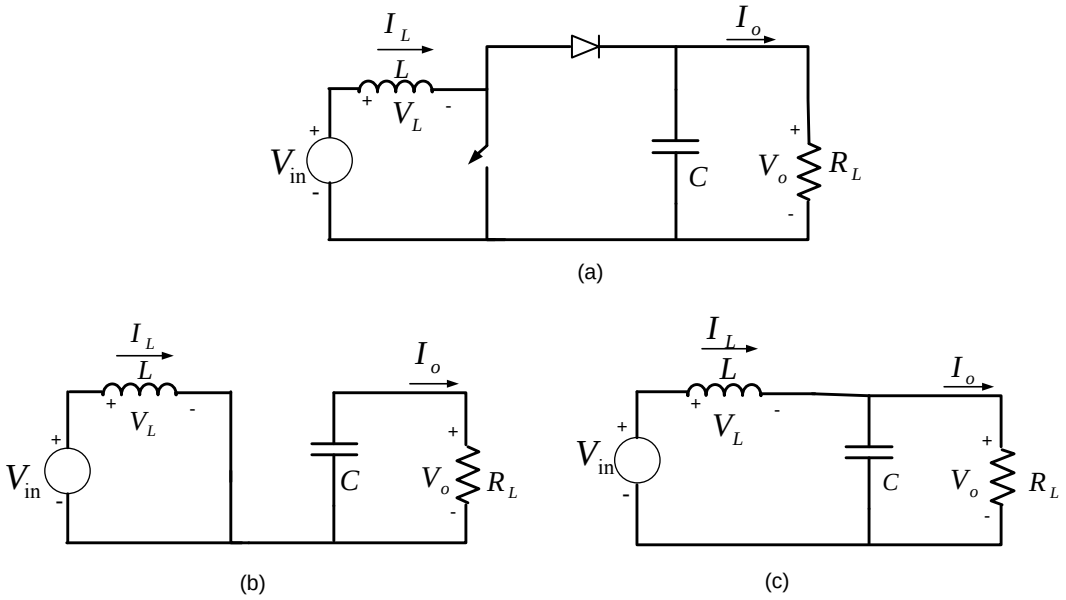


Figure 3.4: Boost converter (a) basic power stage (b) switch on state (c) switch off state

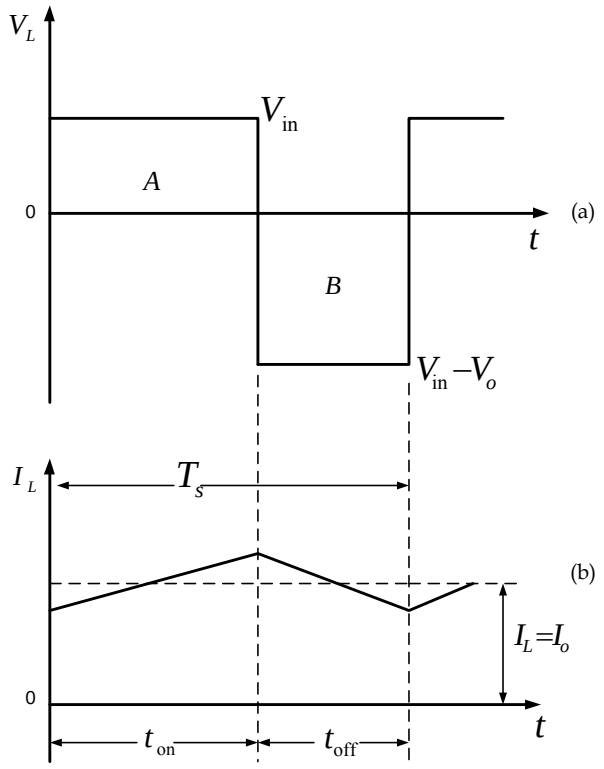


Figure 3.5: Boost converter: waveforms (a) Voltage across the inductor (b) Current through the inductor

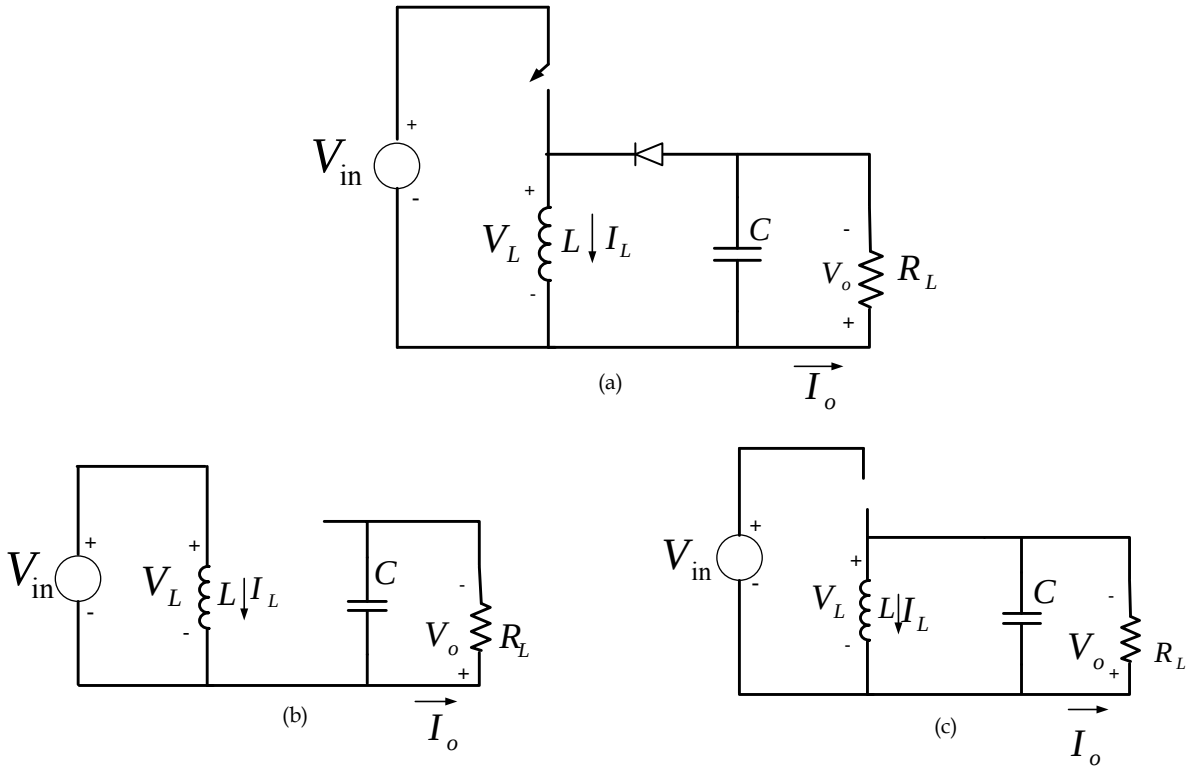


Figure 3.6: Buck-boost converter (a) basic power stage (b) switch on state (c) switch off state

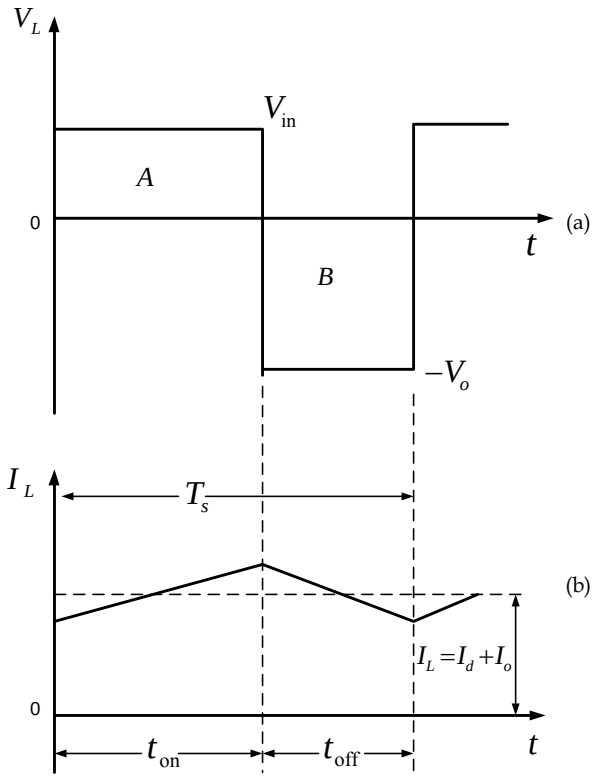


Figure 3.7: Buck-Boost converter: waveforms

3.1.3 Buck-Boost Converter

Another topology called buck-boost converter has more flexibility in output voltage. It can be derived by reconfiguring the same four elements used in the two previous topologies. This topology is capable of step-up or step-down of the input DC voltage. Furthermore the output DC voltage has a reverse polarity compared to the input. As a result, this topology is sometimes referred as the inverting configuration. A simple buck-boost converter topology is shown in Fig. 3.6 where the input voltage is positive, and the output voltage is negative.

The transfer function of an ideal CCM buck-boost converter is,

$$\frac{V_o}{V_{\text{in}}} = \frac{-D}{1-D} \tag{3.4}$$

3.1.4 Forward Mode Converter

The forward mode converter is a transformer isolated topology which has the capability to provide step-up or step-down function. Fig. 3.8 shows the block diagram of a forward mode converter. The power switch in this topology is ground referenced which is called a low-side switch, whereas in buck topology the switch source terminal floats on the switching node.

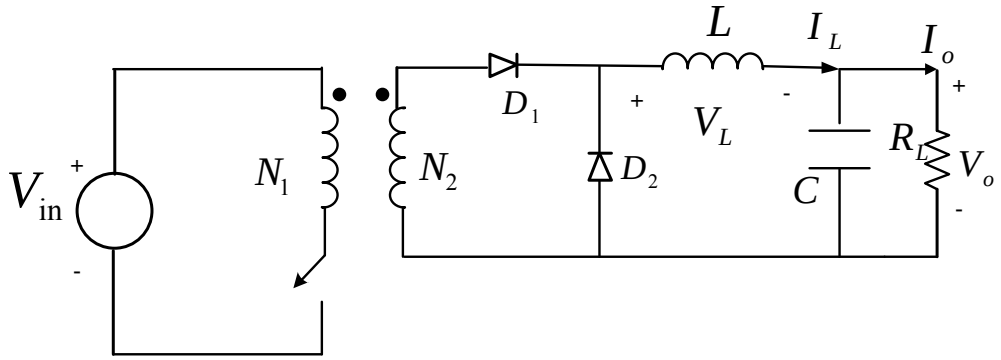


Figure 3.8: Forward mode converter

For $t_{\text{on}} < t < T_s$, the transfer function of an ideal CCM forward mode mode converter is given by,

$$\frac{V_o}{V_{\text{in}}} = \frac{N_2}{N_1} D \tag{3.5}$$

According to Eqn. (3.5), the forward mode converter is similar to the buck converter but modified by the transformer turns ratio.

There are other commonly used transformer-isolated topologies such as (i) Flyback converters; (ii) Half-bridge and full-bridge converters; (iii) Push-pull converters, etc. A summary of characteristics of the SMPS topologies in terms of their relative merits and

demerits, is available in Table 3.1. More details and mathematical derivations of these topologies can be found in [24, 44, 83].

3.1.5 SEPIC Converter

Another popular DC-DC converter which is used in battery-powered applications is called single-ended primary inductance converter (SEPIC). This converter provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage. The typical SEPIC converter shown in Fig. 3.9 uses a transformer and a capacitor to couple additional energy to the load [84, 85].

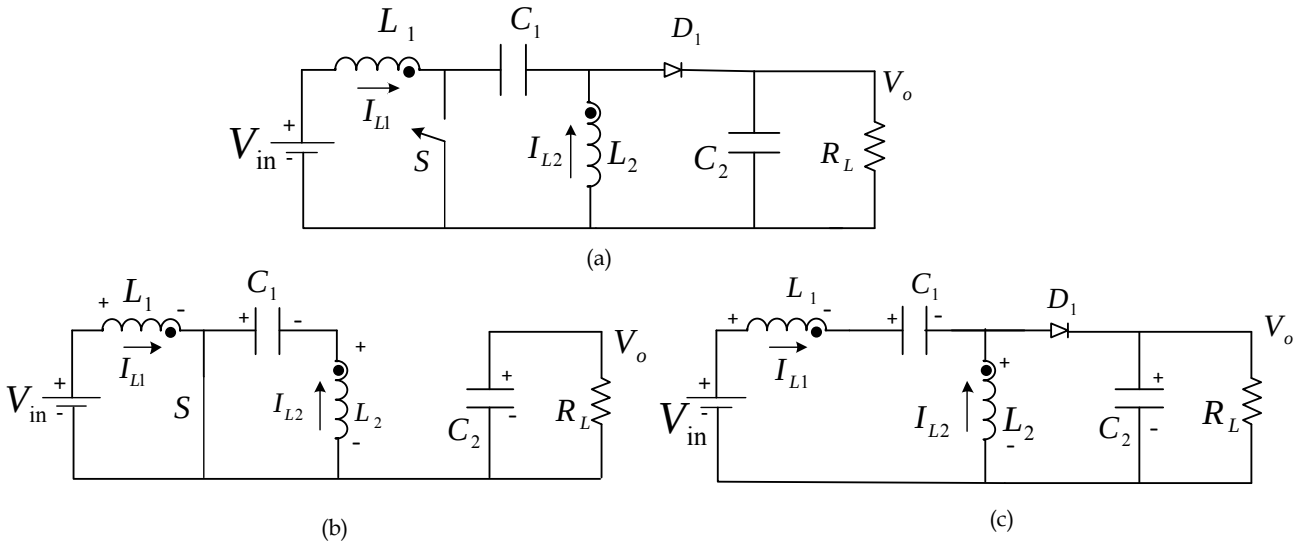


Figure 3.9: SEPIC converter (a) basic power stage (b) switch on state (c) switch off state

When the switch S is on, current I_{L1} flows into common rail via the inductor L_1. Similarly at that time current I_{L2} flows through L_2 where the capacitor C_1 acts as a voltage source. When S_1 goes off, I_{L1} flows through C_1 and D into C_2 and R_L (load resistor). I_{L2} flows through diode into C_2. Both currents ramp down as the capacitors are charged, and the load current flows from C_2 to the load.

The transfer function of a CCM SEPIC converter under ideal conditions is,

$$\frac{V_o}{V_{\text{in}}} = \frac{D}{1-D} \tag{3.6}$$

The operation of this converter is similar to the buck-boost converter, but without any voltage inversion. A more detailed analysis with design approach can be found in [84–87].

This topology allows the operation with fewer cells in the battery, where the cost of extra components is compensated by the savings in the battery.

The main advantages and disadvantages of this design are [44, 87]:

Advantages

- Single switch
- Continuous input current (similar to boost)
- Any output voltage (as for buck-boost)
- Ripple current can be steered away from the input, reducing the need for input noise filtering
- Inrush/overload current limiting capability
- Switch location is a simple low-side case, hence easier gate drive circuits
- Outer loop control scheme is similar to a boost converter

Disadvantages

- Higher switch/diode peak voltages and currents compared to boost topology
- Bulk capacitor size/cost will be greater if operated at lower voltage than boost

The SEPIC converter integrates the best characteristics of the boost and flyback topologies making it especially advantageous in high power-factor preregulator applications [88–90]. Some trends of SEPIC applications and advancements are indicated in [88–97].

3.1.6 Resonant Converters

In conventional hard switching techniques such as PWM, during the switch turn-on and turn-off stages, the power device has to withstand high voltage and current simultaneously. This results in high switching losses. In addition to this, the switching loss is increased proportionally with the switching frequency, thus limiting the maximum switching frequency of the power converters.

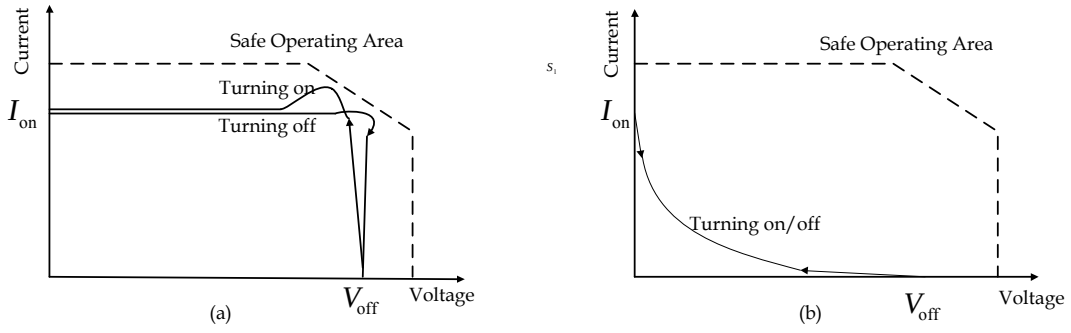


Figure 3.10: Comparison of voltage-current trajectories of (a) hard-switching and (b) soft-switching techniques [44]

Resonant converters are based on soft switching techniques, which turn on and off semiconductor switches in a switch power supply at either zero voltage or zero current crossings called zero voltage switching (ZVS) and zero current switching (ZCS). During

Table 3.1: Characteristics of SMPS topologies [44]

SMPS Configuration	Advantages	Disadvantages	Typical Efficiency
Buck Converter	Simple Higher efficiency No transformers Low switch stresses Small output filter Low ripple	No isolation	78%
Boost Converter	Simple Higher efficiency No transformers Low-input ripple current	No isolation High peak drain current Complexity in control loop design High output ripple Unable to control short circuit current	80%
Buck-Boost Converter	Voltage inversion Simple	No isolation High side switch required Complexity in control loop design High output ripple current	80%
SEPIC converter	Low input ripple current Buck and boost with no inversion No transformers Capacitive isolation against a switch failure	No isolation Switch has high RMS/peak currents Capacitor have high ripple currents High output ripple Complexity in control loop design	80%

the switching period making either voltage or current to zero, the power loss can be set to zero. The reduction of switching loss and the continual improvement of power switches allow the switching frequency of the resonant converters to reach hundreds of kilohertz eliminating the drawback of conventional hard switching topologies [44,98–100]. Fig. 3.10 (a) and (b) show a comparison of voltage-current trajectories of hard switching and soft switching respectively.

As there is no natural zero crossing in a DC power supply, zero voltage and zero current have to be implemented using some additional circuitry to enable soft switching. Generally circuit resonance based on an LC circuit is commonly used for this purpose. There is little difference in the basic structure and the operating principles of resonant converters from conventional hard switching converters. The only difference is that LC circuits are used to resonate at certain period to achieve ZCS and ZVS conditions for the semiconductor switches. Fig. 3.11(a) and (b) show two typical ZCS and ZVS buck converter circuits respectively.

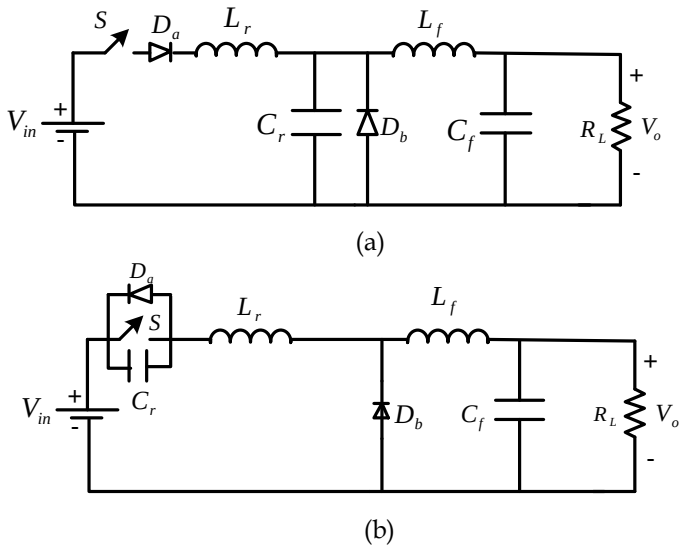


Figure 3.11: Resonant-switch buck converters (a) ZCS (b) ZVS

3.1.7 SMPS Performance

An important advantage of switching regulators is their relatively high power efficiency. Assuming the use of ideal energy storage elements such as capacitors and inductors with perfect lossless switches theoretically 100% efficiency can be achieved. But, in practical situations, inductors, capacitors and transistor switches do not show their ideal characteristics and thus deviate much from the theoretical maximum efficiency. Therefore, in practice the range of efficiencies could be in the range of 80% to 90% for the DC-DC converter stage [101]. If the AC-DC conversion stage is included as is required in a typical off-the-line power supply, end-to-end efficiencies will be much lower. The following example illustrates this practical scenario.

There can be various sources of loss within a typical SMPS, depending on its power level, topology and circuit complexity. The approximate loss contribution range of each is shown in Fig. 3.12, as a percentage of the input power, for a typical supply that delivers 10 W of load power [44, 102].

In general, the major loss contributors in a switching power supply are:

1. Static losses in diodes and switching transistors. In diodes, the forward loss contributes in a major way, whereas in BJTs and MOSFETs collector-emitter saturation voltage and drain-source on resistance are the primary contributors respectively.
2. Dynamic losses in switching transistors and diodes occurring at high frequency due to the charging and discharging of different parasitic capacitances. These losses increase linearly with the switching frequency.
3. In capacitors, ESR contributes a significant share of the overall losses, in addition to the core losses occurring in magnetic components.

4. Control circuits can also contribute a share of the losses, but by suitable selection of control ICs this can be minimized.

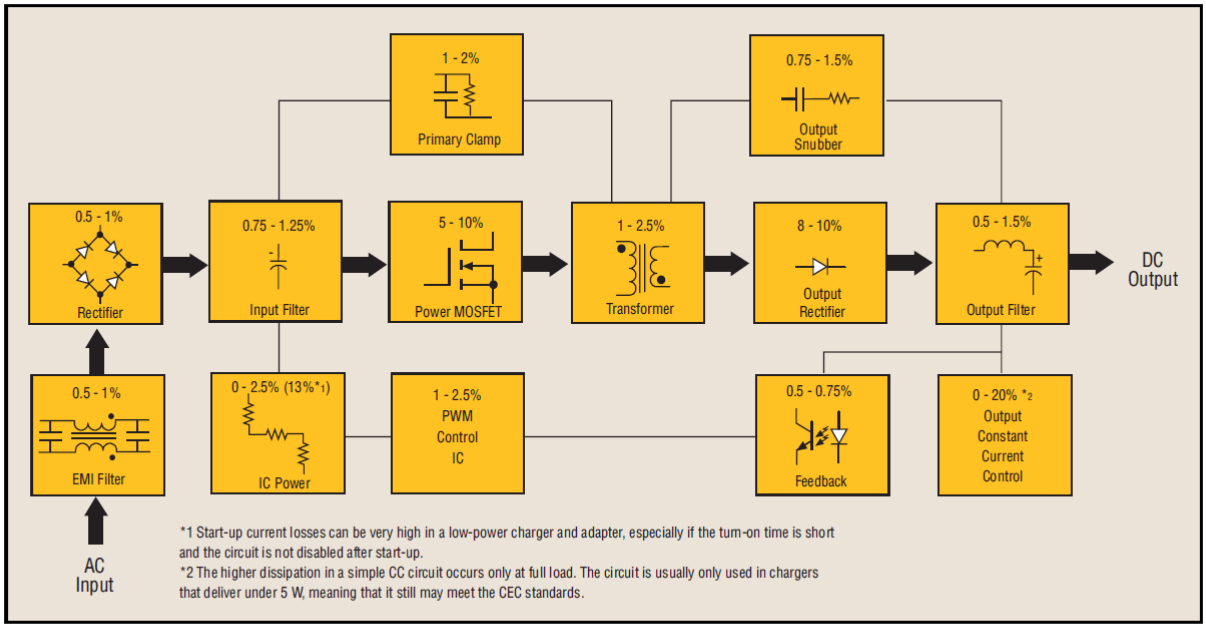


Figure 3.12: Block diagram of the power-consuming circuits within a SMPS [102]

The primary drawback of switching regulators, when compared to linear regulators, is their output noise and EMI/RFI emissions. Due to the resistance, inductance, and finite capacitance of the capacitors used in the input and output terminals of an SMPS converter, voltage ripples and noises are generated leading to conducted noise [101]. An inductor which creates a magnetic field which it cannot perfectly contain within its core contributes to radiated noise. There are also ringing voltages in the converter, parasitic inductances in components and PCB traces. Noise is an inherent property of switching regulators and must be controlled by proper component selection, PCB layout and input or output filtering.

3.1.8 SMPS Applications

Characteristics such as weight, efficiency and size make switch mode power supplies the design of choice for many applications. In industrial applications particularly, the non-transformer isolated basic converters are generally used for lower-power converter circuits whereas transformer isolated topologies, such as forward mode, flyback and bridge types, are generally used for applications where higher power, galvanic isolation and multiple output rails are required. Fig. 3.13 depicts the approximate range of usage in several primary SMPS topologies [44].

Voltage regulator modules (VRM) are used in the power supplies of most modern desktop and laptop computers. These VRMs are used to step down the voltage from the

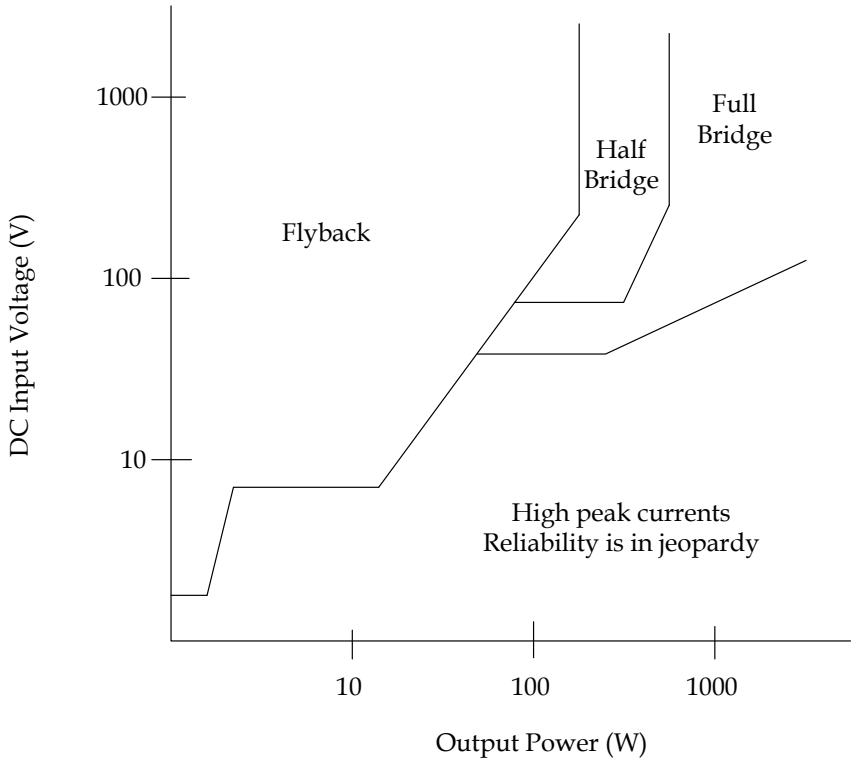


Figure 3.13: Approximate range of usage in several primary SMPS topologies [44]

power supply or the battery to the CPU core voltage [103, 104]. Low voltage and multiple output voltage requirements complicate the design of power supplies, sometimes making it harder to build efficient power supplies.

In the processor power supplies, parallel connected VRMs are used to ensure a sufficient transient response for the increased loading conditions. Such topologies are advantageous in higher power applications as well, due to the ability to reduce the size of the necessary filter elements by interleaving the power modules. Giildner [105] proposed a general purpose four-module 100 kW interleaved buck converter VRM power supply to supply demanding loads in the higher power range. The efficiency of such modular DC-DC converters is much higher than in comparable single stage topologies.

The importance of the power factor correction (PFC) has been recognised due to the growing use of the SMPS in electronics equipments. Taking this requirement into account, a 150 W SMPS experimental prototype with PFC included for personal computer applications has been developed [106].

The losses of standard hard-switched converters are relatively high in the MHz switching frequencies. Reduction of the switching losses and stresses on the switching devices in the power supply is a good way to increase their efficiency. The very low switching losses of resonant converters make them superior compared to traditional hard-switching converters because of their soft-switching behaviour. These converters use the resonance

of an LC circuit with adequate switching strategies, which results in both low EMI and soft-switching. Nakhost and Munk-Nielsen [107] proposed a 50 W half-bridge LLC/LLCC resonant SMPS topology with coreless transformer for AM radio applications above the AM band (1.7 MHz), to avoid switching disturbances and radio signal interference.

Digital control techniques for SMPS supplies have been receiving particular attention over the last few years. Characteristics of low-power SMPS can be significantly enhanced using digital control techniques [108–112]. Advantages of digital control include compensator versatility and programmability without the need for space-consuming, tolerance-affected passive components. Further advantages include integration enhancements and the possibility of extending the role of the digital system to more complex functions such as diagnostics, health monitoring, auto-tuning and communication features thus implementing intelligent systems for power management.

An integrated digital controller for a DC-DC SMPS converters that can be used in portable applications has been developed by Lukic et al. [111]. The controller has very low power consumption, fast dynamic response, and can operate at programmable constant switching frequencies exceeding 10 MHz. In steady state, to minimize power consumption, the controller is clocked at a frequency lower than SMPS switching frequency.

Corradini and Mattavelli have investigated the steady-state and small-signal behaviour of multi-sampled digital pulse width modulators employed in the control of DC-DC switching converters [110].

3.2 Switched Capacitor Regulators (Charge Pumps)

3.2.1 Basic Concept

Switch capacitor (SC) converters are popular DC-DC converting circuits which are used to obtain a DC voltage higher than the supply voltage, or a DC voltage with reverse polarity. Switched capacitor converters accomplish energy transfer and voltage conversion using capacitors [113–117] and high frequency switching to achieve voltage conversion. SCs are only made of capacitors and switches, thereby allowing integration on silicon. The capacitors needed by this circuit could be small enough such that the entire switch capacitor circuit can be integrated on an IC, particularly when the power required is small, reducing the cost of the system [113]. In general, the two most common switched capacitor voltage converters are the voltage inverter and the voltage doubler circuit.

In the voltage doubler, the simple circuit consists of a single capacitor and four switches. Fig. 3.14 indicates the basic concept of the switch capacitor converter, which is commonly known as a charge pump. The charge pump capacitor, C, is charged to the input voltage during the first half of the switching cycle. During this phase, switches S_1 and S_3 are closed; S_2 and S_4 are open and the capacitor C is connected in parallel to the

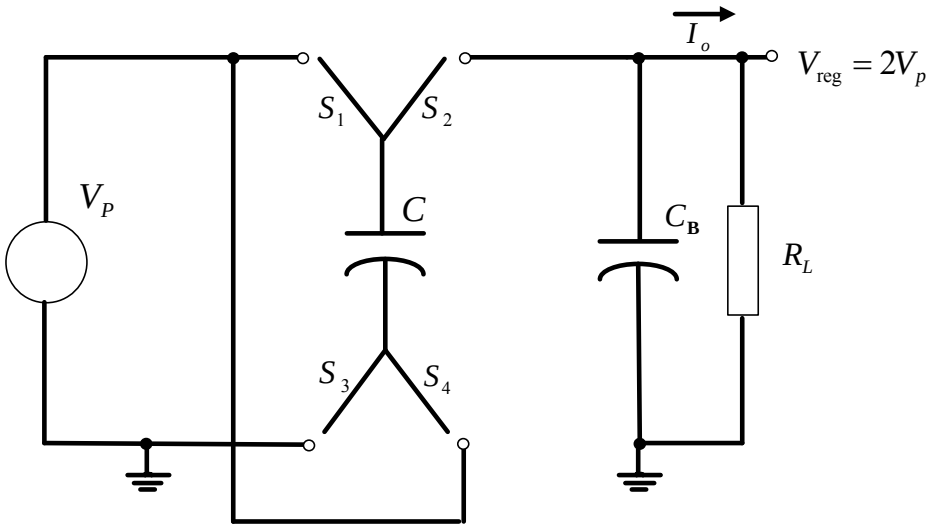


Figure 3.14: Switch capacitor voltage doubler

supply voltage V_p and it is charged to V_p. During the second half of the switching cycle, switches S_2 and S_4 are closed; S_1 and S_3 are open and C, the pump capacitor is placed in series with the input voltage, thereby accomplishing the voltage doubling function. The capacitor maintains its charge of V_pC from the previous phase. This means that during the release phase of circuit operation the following relationship can be derived.

$$[V_{\text{reg}} - V_p]\, C = V_p C \tag{3.7}$$

$$V_{\text{reg}} = 2V_p \tag{3.8}$$

A voltage multiplication factor of greater than two can be achieved by cascading more than one capacitor in parallel in the charging phase, and discharging them in series in the next phase, using an appropriate switching arrangement. This voltage multiplication technique was proposed by Cockcroft and Walton and used to generate steady potentials near 800,000 volts in connection with studying the atomic structure of matter [117]. However, in practice, the Cockcroft-Walton multiplier became somewhat inefficient when implemented in monolithic integrated form because of the relatively large on-chip stray capacitance. In order to overcome these limitations, a new voltage multiplier circuit was derived by Dickson [114] that is suitable for integration in monolithic form. This new configuration achieves more efficient multiplication even in the presence of stray capacitance and its drive capability is independent of the number of multiplier stages.

As shown in Fig. 3.15, in the switch capacitor voltage inverter, during the first half of the switching cycle, switches S_1 and S_3 are closed; S_2 and S_4 are open, so the charge pump capacitor, C, is charged to the input voltage. During the second half of the switching cycle, switches S_1 and S_3 are open; S_2 and S_4 are closed and its voltage is inverted and

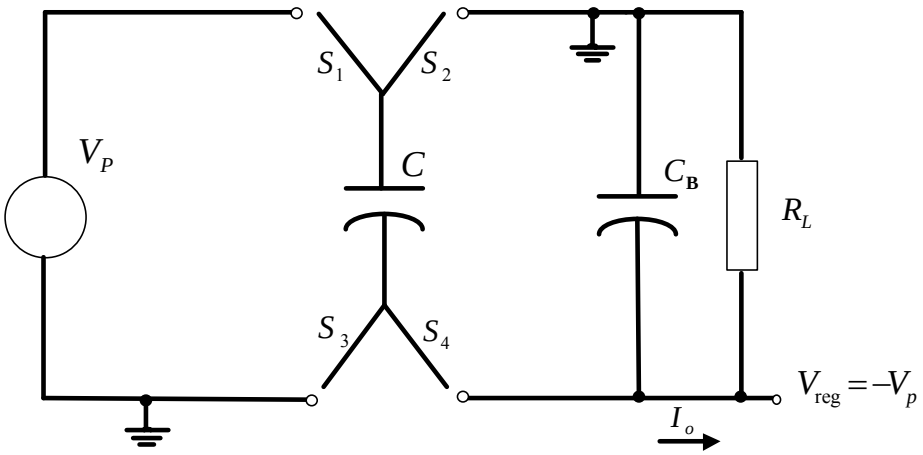


Figure 3.15: Switch capacitor inverter

applied to capacitor C_B and the load. The output voltage is the negative of the input voltage, V_p.

In switch capacitor regulators, when a steady-state condition is reached after initial start-up transients, the charge pump capacitor only has to supply a small amount of charge to the output capacitor in each switching cycle. The amount of charge that has to be transferred depends upon the load current and the switching frequency. While the pump capacitor is charged by the input voltage, the output capacitor C_B must supply the load current. The load current flowing out of C_B causes a drop in the output voltage which creates ripples. The switching frequency impacts the size of the external capacitors required: higher switching frequencies allow the use of smaller capacitors. In general, switching frequencies are generally limited to a few hundred kHz.

3.2.2 Switch Capacitor Performance and Losses

Elimination of the inductor and the related magnetic design issues is a unique advantage of switch capacitor regulators which enables integration of the regulator on a monolithic IC with a few external capacitors. The inductor-less approach makes the regulator smaller in size which is important in many applications where there are space-constraints.

Switched capacitor converters are capable of achieving efficiencies greater than 90%. However, these converters are not suitable to maintain high efficiency for a wide range of ratios of input to output voltages, unlike the case for switching and low dropout regulators. The load current capability is limited by the size of the capacitors and the current-carrying capacity of the switches. In practice, typical IC switched capacitor inverters are available with 10 mA to 500 mA load currents [118].

The conventional charge pump circuits are designed to operate at a fixed switching frequency with a rated output load current and voltage. The input-to-output current

ratio is scaled according to the voltage conversion topology (i.e., doubled for a doubler, inverted for an inverter) regardless of whether or not regulation is used to reduce the doubled or inverted voltage. Any output voltage magnitude less than $2V_p$ for a voltage doubler or less than $|V_p|$ for an inverter, result in additional power dissipation within the converter, thus the efficiency will be degraded proportionally [118].

However, one remarkable downside of most switched capacitor applications is noise. Usually, the noise that is generated at the power input can interfere with RF transmission and reception in wireless applications, whereas the noise that is at the output can couple into sensitive circuits or even create audible noise. The new LTC3200 family of boost charge pumps employs a new architecture designed to minimize noise at the input and output to mitigate such unwanted behaviour [119]. To eliminate the noise in switched capacitor regulators due to switching losses, soft switching feature is added to the converter by adding small inductance to create resonance [120]. Hsiao et al [121] have designed a new converter topology using the resonant switched-capacitor technology in the zero-current switching (ZCS) condition to reduce the switching losses.

Even with ideal components, the SC converter has a non-zero output resistance, and losses in the SC power stage increase with load current. Due to practical limitations on the size of capacitors and switches, applications of SC converters are limited mainly to low and medium power levels of several tens of milliwatts.

Recently, switch capacitor converters have been modified to resolve the problems of increased cost and space to deliver power through multiple voltage rails in a computing platform. Triple Output Fixed Ratio Converter (OFRC), a triple output topology based on a combination of a switched capacitor converter and a buck converter [122] is such an example.

3.2.3 Switched Capacitor Applications

The switched capacitor voltage inverter is useful to maintain a negative voltage in addition to the primary positive voltage in a multi rail power supply, where only a few parts of the circuitry require the negative voltage. Switched capacitor voltage multipliers are also useful in low current applications where a voltage greater than the primary supply voltage is required [118]

In small power applications, the system cost can be reduced by implementing the entire circuit in an integrated chip [123]. No use of magnetic components make them well suited for monolithic integration. Dickson proposed the first integrated version of a charge pump [114]. Monolithic charge pump converters are widely used in non-volatile memory circuits, dynamic random access memory circuits, low voltage circuits, continuous time filters and RS-232C transceivers etc [114], [123]. On-chip charge pumps can be used

to generate the higher than normal voltages required to write or erase information in non-volatile memory circuits [117, 124].

In Dynamic Gate Biasing (DGB), controllable charge pump circuits are used for the stable biasing of MOSFET gates [117, 125–127].

With the increasing demand for longer battery operating time in the power management of portable device designs, switched capacitor converters play an important role in both on-chip and off-chip designs [128]. In switched capacitor designs, operation down to zero load is possible with no need for dummy loads or complex control techniques. When completely unloaded, output voltage of these converters assumes a value uniquely determined by the converter topology [129]. Furthermore, by reducing the switching frequency, the total power losses can be minimised. Moreover, switched-capacitor converters offer a significant size advantage, especially in mobile applications [128].

In the future, as analog designers look for new ways to meet the challenge of reduced supply voltages, on-chip switched capacitors will become an integral part of low-voltage analog and digital circuit designs.

3.3 Power Supply Protection

This section is a extraction of section 7.9 of Chapter 7 of Kularatna [44].

Safety and reliability should be important aspects of power supply operation. Not only the load but also the power supply and its input source should be safe under all operating conditions. The following are a few important items to consider:

- Over voltage protection
- Over current protection
- Protection against transients
- Thermal design

3.3.1 Over Voltage Protection

A power supply should not generate any steady or transient over voltages under all operating conditions, particularly in low-voltage, high-current power supplies. Sometimes an unexpected component failure, such as a shorted power transistor in a buck converter, can generate a disastrous high output voltage. Under a very peculiar and unwarranted load current transient, the power supply may generate a transient over voltage condition. In most situations, the easiest way to protect the load from over voltage is to use crowbar circuits, which detect the over voltage situation quickly and activate a short circuit across a fuse. To enable reliable protection, the over voltage protection must be independent from the rest of the systems circuits; it must have its own voltage reference source and an independent power source. Figure 3.16(a) indicates a simple implementation of a crowbar

circuit in a non-isolated synchronous buck converter. Figure 3.16(b) indicates a case of diode-ORed redundant supplies with independent crowbar circuits. In isolated power supplies, the transformer provides inherent protection against a switch failure; if any of the components in the feedback path opens accidentally, it can create a dangerous situation. Even in such situations, by using optoisolators, one can design crowbar protection circuits using parts similar to the case in Fig. 3.16(a).

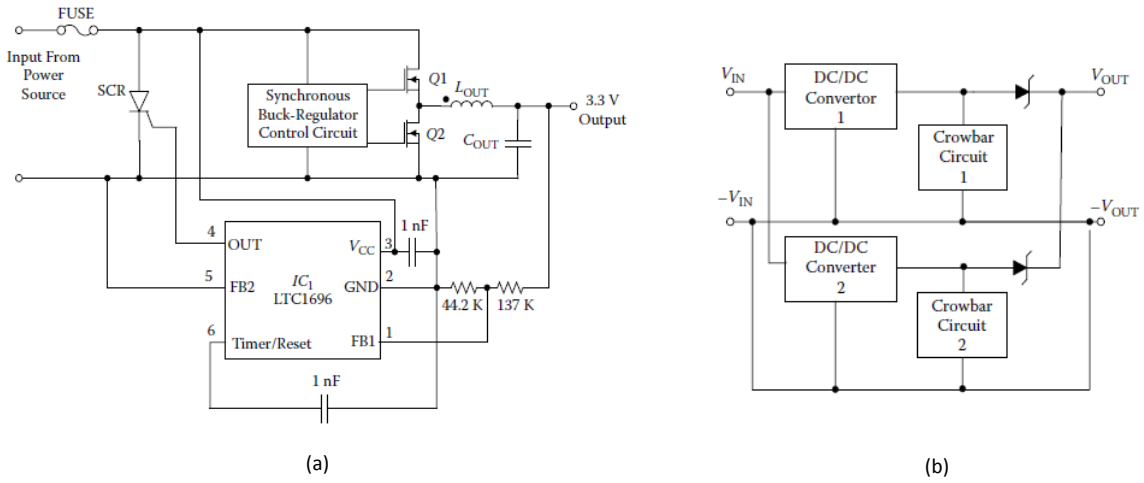


Figure 3.16: Crowbar protection for over voltage conditions: (a) implementation of a simple crowbar circuit using limited components; (b) independent crowbar units in an ORed redundant power supply system. (Source: Courtesy of EDN Magazine)

3.3.2 Over Current Protection

One of the most important protection features in the power supply is current limiting. When designing a current limiter, one should think of two main aspects: measure the current and develop a limiting circuit using the current signal. Current limiter design necessitates trade-offs among cost, complexity, reliability, and performance. There are several possible current-limiting schemes, as shown in Fig. 3.17. In constant current limiting (Fig. 3.17(a)), the output voltage drops sharply beyond the limit of the current. In an LDO or a common linear regulator, if such a scheme is applied at the limit, the voltage across the pass element will exceed the normal operation value (from $[V_{\text{in}} - V_O]$ to $[V_{\text{in}}]$) and the dissipation limit of the transistor and the heat sink can be exceeded, and the designer should allow for such excess dissipation. Figure 3.17 shows fold back technique. An advantage in this scheme over the constant current-limiting method is that dissipation within the regulator circuits is minimized. The ratio of $I_{\text{SC}}/I_{\text{max}}$ is an important parameter for this scheme, where a smaller value means better performance. However, unless the circuit is designed to reset automatically on removal of excess load, this scheme may need manual intervention at over current. Figure 3.17(c) shows the

concept of hiccup current limiting. It incorporates over current shut down but adds an automatic restart mechanism. The power supply shuts down for a limited period of time and automatically restarts after a time out.

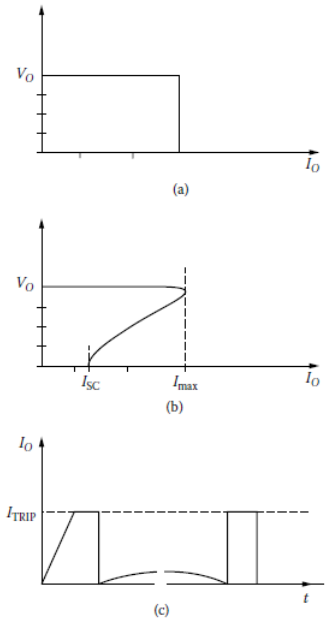


Figure 3.17: Current-limiting methods: (a) constant current limiting; (b) foldback limiting; (c) hiccup current limiting

3.3.3 Protection Against Transients

Due to lightning or inductive load dumps on the AC input power supply, severe surge voltages may occur, and these transients are of very short duration, such as from 50 to 200 μs total. Almost all off-the-line power supplies need to be protected against such events where both common-mode and differential- (or transverse) mode transients can occur. In such situations, non-linear devices such as metal oxide varistors and avalanche diodes can be combined with small inductors and capacitors, as per the representative schemes in Fig. 3.18.

3.3.4 Thermal Design

In any electronic design, semiconductors, as well as the passive parts, have thermal limits for operation. For example, most manufacturers of silicon ICs specify the maximum junction temperature at about 150°C. Similarly, passive parts also have maximum temperature limits. Given such limits, the maximum power dissipation of an IC or a power semiconductor package is given by,

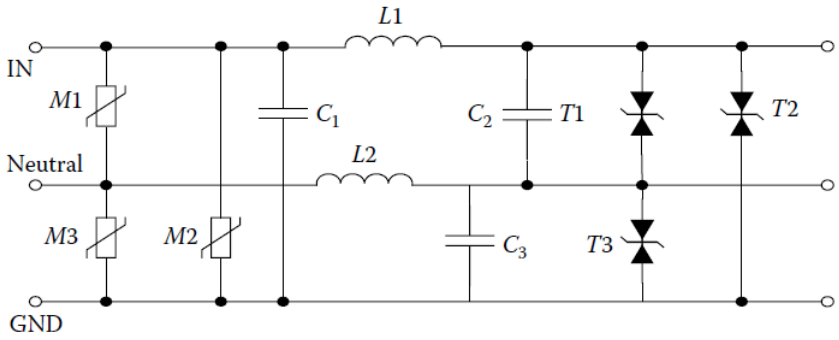


Figure 3.18: Transient protection for common- and differential-mode surges: multi-stage surge suppressor with MOVs ($M1$ to $M3$), avalanche diodes ($T1$ to $T3$), and passive parts

$$P_{D(max)} = \frac{T_{\mathrm{J(max)}} - T_{\mathrm{A(max)}}}{R_{\theta JA}} \tag{3.9}$$

where $T_{\mathrm{J(max)}}$ is the maximum recommended junction temperature, $T_{\mathrm{A(max)}}$ is the worst case ambient temperature of the application, and $R_{\theta JA}$ is the junction-to-ambient thermal resistance of the package in degrees Celsius per watt (°C/W). A semiconductor's package determines its $R_{\theta JA}$ and quantifies how much the junction temperature will rise for each watt the device dissipates into still air.

3.4 Chapter Summary

Switched-mode power supplies, which are based on energy storage components and semiconductor switches, allow buck, boost and buck-boost (with or without inversion) configurations with significant efficiencies, but generate high frequency noise and are limited in load-current slew-rate performances. Switched -capacitor converters use capacitor switching to boost or invert the input voltage. However, they have limited output current capability.

The next chapter discusses the fundamentals of control loop theory for linear regulators.

Chapter 4

Control Loop Design of DC-to-DC Converters

4.1 Introduction

In the previous chapters on linear and switching regulators, discussions did not consider the detailed aspects of the feedback loop used in the topology. In a well-designed DC-DC converter, irrespective of the load behaviour, under all load currents the power supply should be free of any stray oscillations, and the DC rails should not fluctuate beyond specified margins. In a practical power supply design, the design of the control loop becomes a challenge because of the non-ideal components such as op-amps, capacitors, inductors and transformers. This is further complicated by the finite frequency response properties of BJTs and MOSFETS, which have junction capacitances and other complex secondary elements. The subject of stability of a power supply that pertains to the closed-loop frequency response of the DC-DC converter has received much attention during the past quarter century. This chapter provides a summary of essential theory of designing the control loop of linear regulators based on available literature[1].

4.2 Feedback Control and Frequency Response

For most designers, feedback control loop stability is shrouded in a cloud of mystery. In this section, feedback loop stability and the basic concepts with some practical insights into the theory are discussed and some useful practical procedures for refining the process are suggested.

A system that maintains a prescribed relationship between the output and the reference input by comparing them and using the difference as a means of control, is called a feedback control system. Feedback control systems are often referred to as closed loop control systems which use a feedback control action in order to reduce the system error. A typical block diagram of a closed-loop system is shown in Fig. 4.1.

[1]This chapter has been published as a book chapter - K. Kankanamge-Gunawardane, Control Loop Design of DC-to-DC Converters, Chapter 5 (Ed) N. Kularatna (2011): DC power supplies, power management and surge protection for power electronics systems, FL, USA, CRC Press

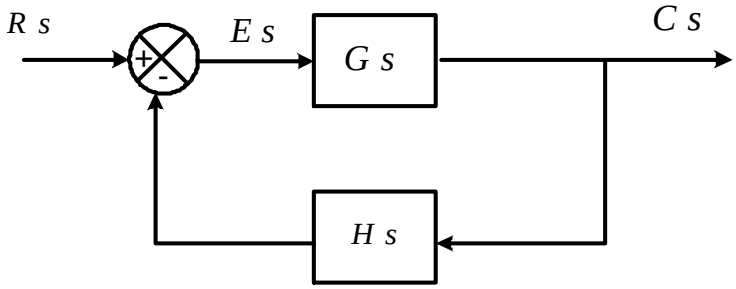


Figure 4.1: Closed-loop system

where $R(s)$, $C(s)$ and $H(s)$ are the input, the output and the feedback element from the output respectively.

In this system $G(s)$, $\frac{C(s)}{R(s)}$, $H(s)$ and $G(s)H(s)$are called the open loop transfer function, closed loop transfer function, feedback loop transfer function and loop gain respectively. More details can be found in Ogata [130].

For the system shown in Fig. 4.1, the closed-loop transfer function is given by

$$\frac{C(s)}{R(s)} = \frac{G(s)}{1 + G(s)H(s)} \tag{4.1}$$

Frequency response is the steady-state response of a system to sinusoidal inputs. In frequency response analysis, the frequency of the input signal is varied over a certain range and the resulting performance is studied.

4.3 Poles, Zeros, and S-Domain

The frequency response can be analysed by representing the transfer function as a function of the complex frequency 's'. The relationship between the input, $V_i(s)$, and output, $V_o(s)$ of a system, which is called the transfer function $T(s)$, is defined as,

$$T(s) = \frac{V_o(s)}{V_i(s)} \tag{4.2}$$

Once this function is derived, by replacing 's' with '$j\omega$' we can evaluate its frequency behaviour. In general, the transfer function $T(s)$ in its own form (without substituting $s = j\omega$) can reveal many useful details about the stability of the circuit. The important thing here is to recognize that this function has a gain and phase associated with it. In general, function $T(s)$ is expressed as a ratio of polynomials in 's' in different forms, including:

$$T(s) = \frac{a_m s^m + a_{m-1} s^{m-1} + \cdots + a_0}{s^n + b_{n-1} s^{n-1} + \cdots + b_0} \tag{4.3}$$

and

$$T(s) = a_m \frac{(s - z_1)(s - z_2) \cdots (s - z_n)}{(s - p_1)(s - p_2) \cdots (s - p_n)} \tag{4.4}$$

In Eqn. 4.4, z_1, z_2, $\cdots$, z_n are called transfer function zeros or transmission zeros, and p_1, p_2, $\cdots$, p_n are called transfer function poles or the natural modes of the network. The n of the transfer function is called the order of the network.
For example a first-order transfer function, which has a single pole, can be written as,

$$T(s) = \frac{a_0}{s - p_0} \tag{4.5}$$

where p_0 is called the pole frequency. (Sometimes first-order systems may involve one zero as well.) A second-order transfer function, which has two poles, can be written as,

$$T(s) = \frac{a_0}{(s - p_0)(s - p_1)} \tag{4.6}$$

where p_0 and p_1 are the pole frequencies. (Sometimes second-order systems may involve one or two zeros.) For example, a low-dropout regulator has three poles and one zero, which has a third-order transfer function, this will be discussed later.

4.4 Bode Plots

This section on Bode plots is based on the reference Sedra [131]. More details in constructing Bode plots can be found in Ogata [130], Chryssis [132], [56,133], and Sedra [131].

Bode plots are convenient tools because they contain all the information necessary to determine if a closed-loop system is stable. Bode plots are graphs of the magnitude and phase of a transfer function, versus frequency. The format is a log frequency scale on the horizontal axis and, on the vertical axis, phase on a linear scale and magnitude on a logarithmic scale. Phase can be expressed in degrees or radians whereas magnitude can be expressed as a proper magnitude or as dB. In order to construct the Bode plot, first determine the transfer function and arrange the equation in the form of Eqn. 4.4.

A transfer function of the form depicted in Eqn. 4.4 consists of a product of factors of the form $(s + a)$, where such a factor appears in the numerator if it corresponds to a zero and in the denominator if it corresponds to a pole.

Based on the transfer function, magnitude response in decibels of the network can be obtained by summing together terms of the form, $20\log_{10}\sqrt{1 + \left(\frac{\omega}{a}\right)^2}$ (if the magnitude is to be expressed in dB) and the phase response can be obtained by summing terms of the form, $\tan^{-1}\left(\frac{\omega}{a}\right)$.

Figure 4.2 shows a typical Bode magnitude (gain) plot where the curve shown in this figure corresponds to the case of a zero. As well as the magnitude response calculated

as in the last paragraph being shown in Fig. 4.2 as the 'actual curve', the curve is also shown as straight line asymptotes which is commonly used as a simplification.

On a plot of decibels versus log frequency magnitude term gives rise to the curve and straight-line asymptotes shown in Figure 4.2. Here the low-frequency asymptote is a horizontal straight line at 0-dB level and the high-frequency asymptote is a straight line with a slope of 20 dB/decade or, equivalently, 6 dB/octave. The two asymptotes meet at the frequency $\omega = |a|$, which is called the corner frequency. As shown in Fig. 4.2, the actual magnitude plot differs slightly from the value given by the asymptotes. The maximum difference is 3 dB and occurs at the corner frequency.

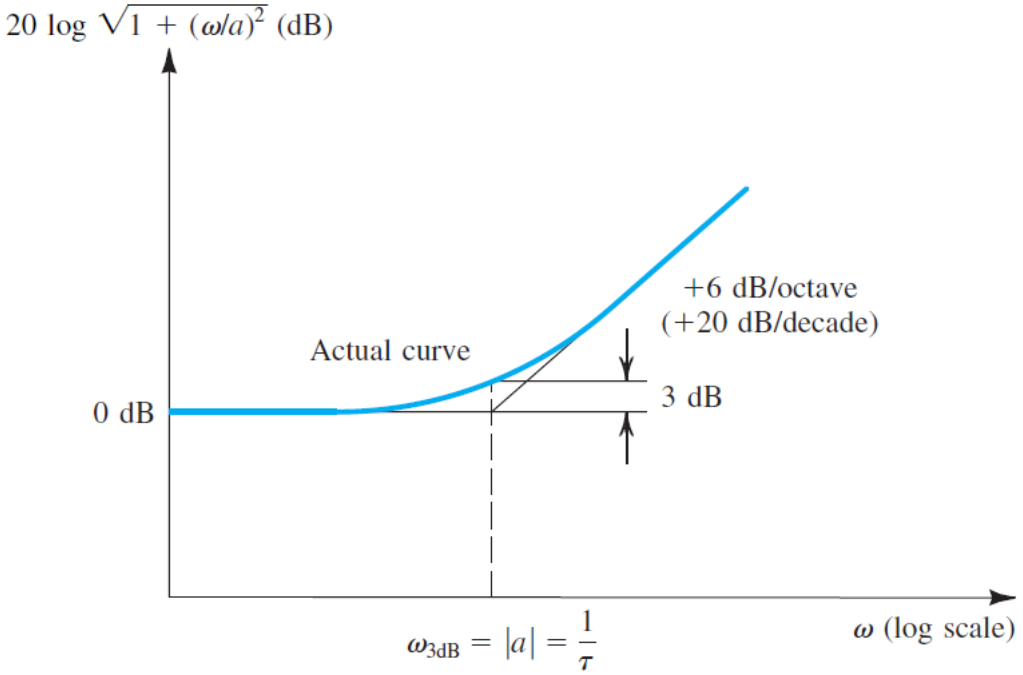


Figure 4.2: Typical Bode magnitude plot of a zero [131]

The magnitude curve corresponds to the case of a pole, the high-frequency asymptote should be drawn with a −20 dB/decade slope after the corner frequency.

In summary, to obtain the Bode plot for the magnitude of a transfer function, the asymptotic plot for each pole and zero is first drawn. The slope of the high-frequency asymptote of the curve corresponding to a zero is +20 dB/decade, while that for a pole is −20 dB/decade. The various plots are then added together, and the overall curve is shifted vertically by an amount determined by the multiplicative constant of the transfer function.

Figure 4.3 shows a typical phase plot representation $\tan^{-1}(\frac{\omega}{a})$, assuming that a is negative. Also shown is an asymptotic straight-line approximation of the arctan function. The asymptotic plot consists of three straight lines. The first is horizontal at $\phi = 0°$ and extends up to $\omega = 10^{-1}|a|$. The second line has a slope of −45 deg/decade and extends

from $\omega = 10^{-1}|a|$ to $\omega = 10^{1}|a|$. The third line has a zero slope and a level of $\phi = -90°$. In order to get the phase plot, the phase shift at each frequency point was calculated by up adding the contributions of every pole and zero at that frequency.

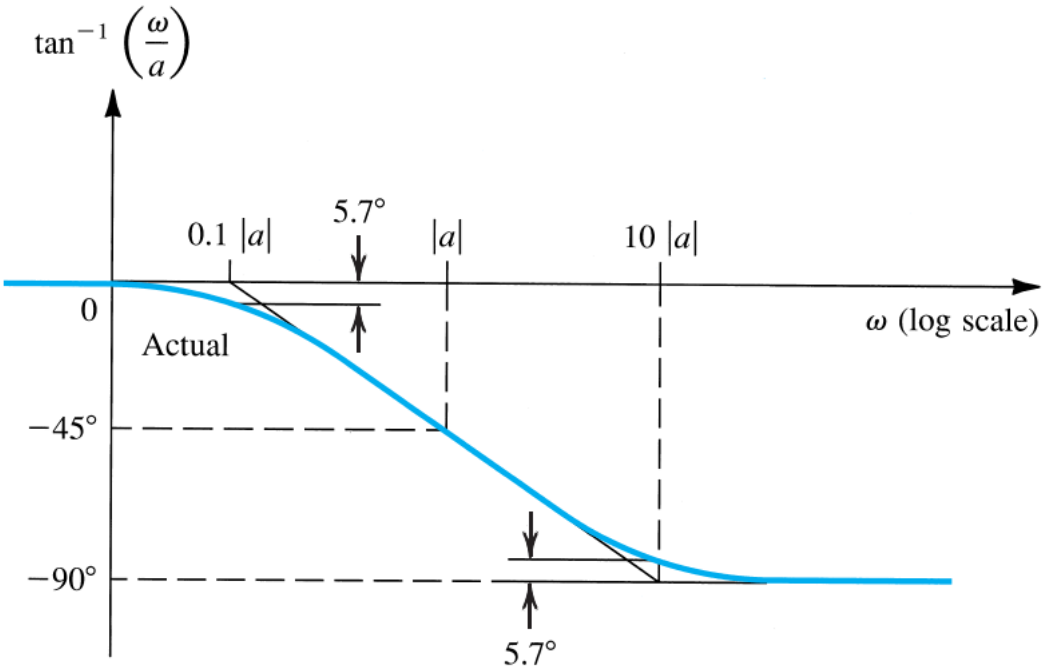


Figure 4.3: Bode plot of the typical phase term $\tan^{-1}(\frac{\omega}{a})$ when a is negative [131]

More details in constructing Bode plots can be found in Ogata [130], Chryssis [132], [56, 133], and Sedra [131].

4.5 Linear Regulators' Feedback Control Loop

Linear regulators' feedback control loop will be discussed in the following sections based on the references [51, 56, 62, 133–142].

4.5.1 Feedback Control

As discussed in Chapter 2, all closed-loop-type linear regulator configurations use a feedback loop to hold the output voltage constant. In analysing linear regulators, loop gain will be mentioned as the magnitude of the voltage gain that the feedback signal experiences as it travels around the loop. In order to maintain a correctly regulated output voltage and a stable loop response, it is important to note that negative feedback must be used for a linear regulator. Fig. 4.4(a) illustrates a block diagram of a typical linear regulator that applies this concept. The resistor divider, error amplifier, and pass device form a closed loop. The output voltage, V_{out}, provides a feedback voltage through the

resistor divider, to the inverting input of the error amplifier. The bandgap reference output (V_{ref}) is a high-precision, fixed voltage that is tied to the non-inverting input of the error amplifier. The error amplifier, essentially an op-amp, then creates a fraction of the feedback signal as output, which is equal to V_{ref}, by sourcing a ground current to the base of the pass device. The pass element, in turn, supplies sufficient output current to keep V_{out} at a certain value.

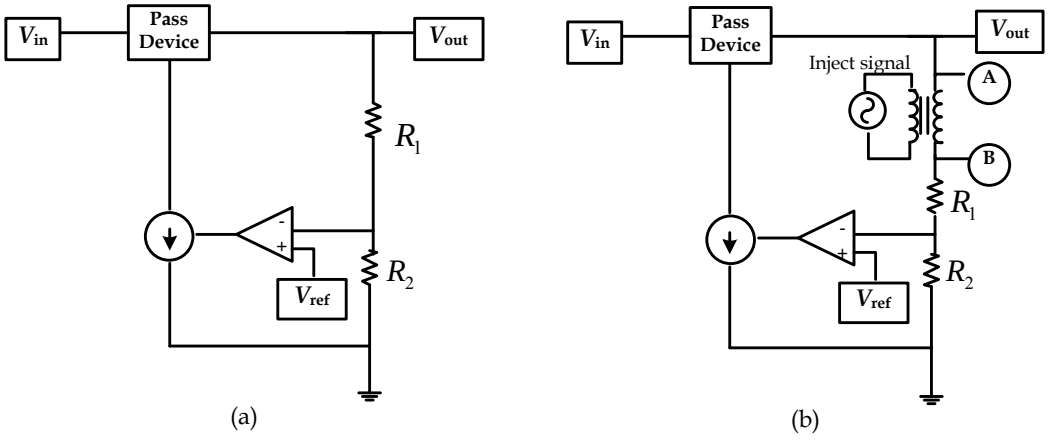


Figure 4.4: (a) Simplified case of a linear regulator; (b) modelling technique to determine the loop gain of a linear regulator [56]

If the op-amp is ideal, and the reference voltage is fixed at V_{ref}, the regulated output voltage will be,

$$V_{\text{out}} = V_{\text{ref}} \left[1 + \frac{R_1}{R_2} \right] \tag{4.7}$$

Eqn. 4.7 illustrates that the feedback is negative, and the adjustment of the output voltage resulting from the feedback is in opposite polarity to the "original" change to the output voltage. This means when there are certain fluctuations in the output voltage by means of a rising or a falling of the output voltage (due to the changes in input voltage), the negative-feedback loop will respond to force it back to the nominal value. In the analysis of feedback response, in order to model the actual fluctuations on the output voltage through a transformer, a small sinusoidal signal is coupled to the feedback path. This small-signal sine wave is injected into the feedback path between points A and B and is used to modulate the feedback signal as shown in Fig. 4.4(b). The AC voltages at A and B are measured and used to calculate the loop gain. Initially, the small signal has a value of $\triangle V_A$ at point A, and a value of $\triangle V_B$ at point B with respect to ground. The signal at point B then travels through the loop and eventually arrives at point A, with a value of $\triangle V_{B'}$. Although $\triangle V_A$ and $\triangle V_{B'}$ have the same magnitude (unity gain), there is a difference in phase (in degrees) between the two [56].

If the error amplifier creates an ideal negative feedback to the loop, $\triangle V_A$ would lag $\triangle V_{B'}$ by $-180°$ as shown in Fig. 4.5(a). However, because of the built-in capacitance of the pass element, it introduces a phase shift that reduces the perfect $-180°$ phase difference by a value between $0°$ and $-180°$ (counterclockwise, with $-180°$ as the starting point) as shown in Figs. 4.5(b), (c), and (d). The difference between the phase and $-180°$ when the loop gain is unity is called the phase margin. When system's phase margin becomes zero, it starts to become unstable. A conservative policy is to ensure that the phase margin is more than $45°$. If a $45°$ phase margin cannot be achieved by the intrinsic architecture of the linear regulator, some form of compensation, either internal or external, is required.

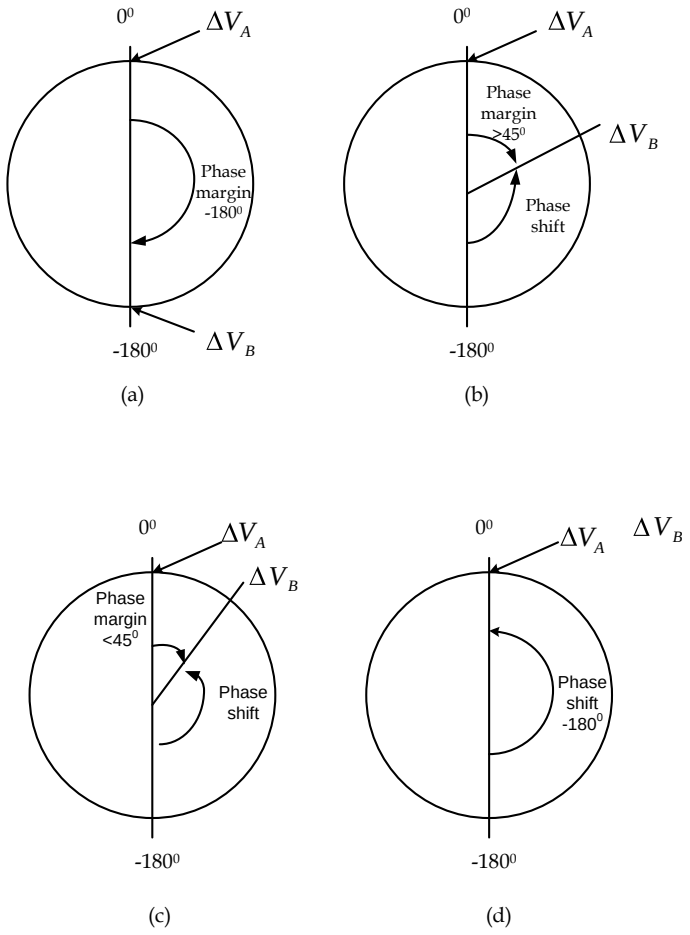


Figure 4.5: Phase map: (a) perfect negative feedback–loop stable; (b) phase margin $> 45°$– loop stable; (c) phase margin $< 45°$– loop needs compensation; (d) perfect positive feedback – loop needs compensation [141]

4.5.2 Frequency Response

To illustrate, a system model of a low dropout regulator (LDO) will be considered as an example. For this configuration, considering the intrinsic factors which determine the

stability of the system, namely, an error amplifier, pass element, feedback resistor, output capacitor and its ESR and bypass capacitors, the small signal equivalent circuit can be drawn as in Fig. 4.6 [62]. The feedback loop shown in Fig. 4.6 can be broken at point A

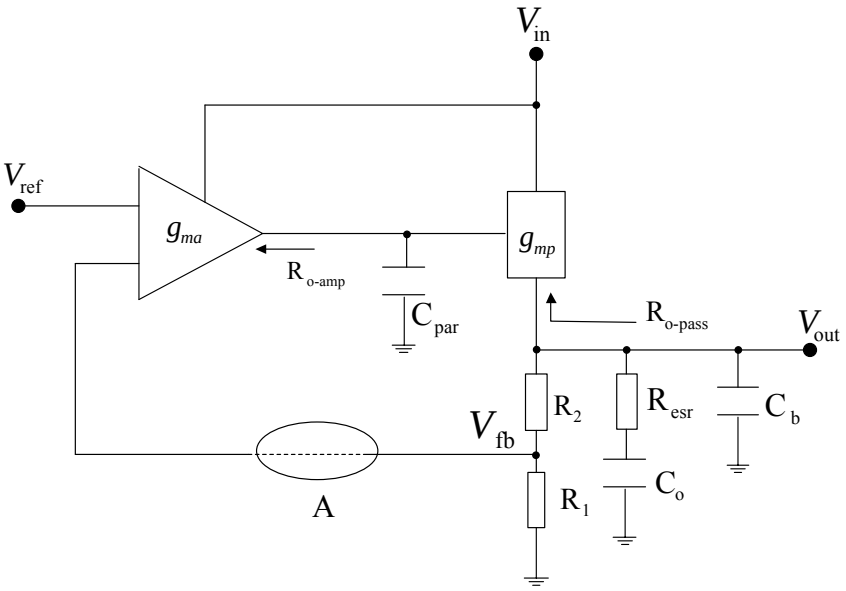


Figure 4.6: LDO AC model [62]

for the analysis. Therefore the input-to-feedback gain can be written as,

$$|A_v| = \frac{V_{fb}}{V_{ref}} \tag{4.8}$$

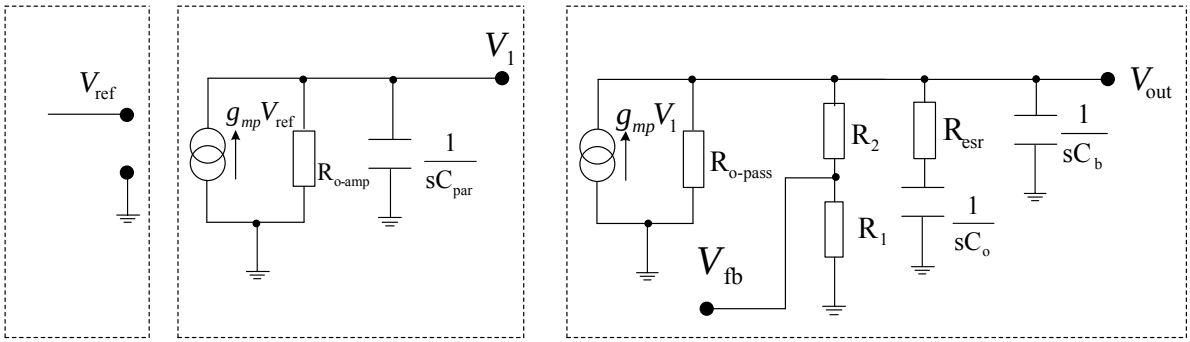


Figure 4.7: LDO AC model Laplace Domain

Based on Fig. 4.7, where the model has been broken up into three parts, the following relationships can be derived:

$$g_{ma}V_{\text{ref}} = \frac{V_1}{R_{\text{o-amp}} // \dfrac{1}{sC_{\text{par}}}} \tag{4.9}$$

$$g_{\text{mp}}V_1 = \frac{V_{\text{out}}}{R_{\text{o-pass}} // \left[R_1 + R_2\right] // \left[R_{\text{esr}} + \frac{1}{sC_o}\right] // \frac{1}{sC_b}} \tag{4.10}$$

$$V_{\text{fb}} = \frac{R_1}{R_1 + R_2} V_{\text{out}} \tag{4.11}$$

Using Eqn. 4.9,

$$\frac{V_1}{V_{\text{ref}}} = g_{\text{ma}} \frac{R_{\text{o-amp}}}{1 + sC_{\text{par}}R_{\text{oa}}} \tag{4.12}$$

Let Z be the impedance seen at V_{out},

$$Z = R_{\text{o-pass}} // \left[R_1 + R_2\right] // \left[R_{\text{esr}} + \frac{1}{sC_o}\right] // \frac{1}{sC_b} \tag{4.13}$$

Therefore Eqn. 4.10 can be written as,

$$\frac{V_{\text{out}}}{V_1} = g_{\text{ma}} Z \tag{4.14}$$

Using Eqn. 4.11,

$$\frac{V_{\text{fb}}}{V_1} = g_{\text{mp}} Z \frac{R_1}{R_1 + R_2} \tag{4.15}$$

Using Eqns. 4.12,4.14 and 4.15

$$\frac{V_{\text{fb}}}{V_{\text{ref}}} = \frac{g_{\text{ma}} g_{\text{mp}} R_{\text{o-amp}} Z}{1 + sR_{\text{o-amp}}C_{\text{par}}} \frac{R_1}{R_1 + R_2} \tag{4.16}$$

Letting,

$$R_x = R_{\text{o-pass}} // \left[R_1 + R_2\right] \tag{4.17}$$

Then Z can be rearranged as

$$Z = R_x // \left[R_{\text{esr}} + \frac{1}{sC_o}\right] // \frac{1}{sC_b} \tag{4.18}$$

$$Z = \frac{R_x \left[1 + sC_o R_{\text{esr}}\right]}{1 + sC_o R_{\text{ESR}} + sC_o R_x + sC_b R_x + s^2 C_o C_b R_x R_{\text{esr}}} \tag{4.19}$$

The following approximations can be made on the resistive parameters.

$$R_x \approx R_{\text{o-pass}} \text{ , } R_{\text{o-pass}} \lll R_{\text{esr}}$$
$$\text{Therefore } R_x + R_{\text{esr}} \approx R_{\text{o-pass}}$$
$$\text{and } R_x // \ R_{\text{esr}} \approx R\text{esr}$$

Using these approximations, Z can be further arranged as,

$$Z \approx \frac{R_x \left[1 + sC_o R_{\text{esr}}\right]}{\left[1 + sC_o(R_x + R_{\text{esr}})\right] + sC_b(R_x // R_{\text{esr}}) \left[1 + sC_o(R_x + R_{\text{esr}})\right]} \tag{4.20}$$

$$Z \approx \frac{R_x \left[1 + sC_o R_{\text{esr}}\right]}{\left[1 + sC_o(R_x + R_{\text{esr}})\right]\left[1 + sC_b(R_x // R_{\text{esr}})\right]} \tag{4.21}$$

$$Z \approx \frac{R_x \left[1 + sC_o R_{\text{esr}}\right]}{\left[1 + sC_o R_{\text{o-pass}}\right]\left[1 + sC_b R_{\text{esr}}\right]} \tag{4.22}$$

Therefore the overall open loop transfer function of the system is given by,

$$\frac{V_{\text{fb}}}{V_{ref}} = \frac{g_{\text{ma}} g_{mp} R_{\text{o-amp}} R_1 R_x}{R_1 + R_2} \frac{\left[1 + sC_o R_{\text{esr}}\right]}{\left[1 + sR_{\text{o-amp}} C_{\text{par}}\right]\left[1 + sC_o R_{\text{o-pass}}\right]\left[1 + sC_b R_{\text{esr}}\right]} \tag{4.23}$$

It can be observed from Eqn. 4.23 the overall transfer function of the system consists three poles and one zero. The poles and the zero approximated to the following;

$$p_1 = \frac{-1}{2\pi C_b R_{\text{esr}}} \tag{4.24}$$

$$p_2 = \frac{-1}{2\pi C_{\text{par}} R_{\text{o-amp}}} \tag{4.25}$$

$$p_3 = \frac{-1}{2\pi C_o R_{\text{o-pass}}} \tag{4.26}$$

$$z_1 = \frac{-1}{2\pi C_o R_{\text{esr}}} \tag{4.27}$$

4.5.3 Control Loop Analysis

The following discussion shows a stability analysis for some practically available linear regulator configurations. The derivations are based on a similar approach to the above LDO's frequency response analysis and transfer function derivation.

(a) Standard NPN Linear Regulator

The standard NPN regulator is based on a NPN Darlington pass transistor with PNP driver as shown in Fig. 2.8. As the pass transistor of the NPN regulator is connected in a circuit configuration known as the common collector, it inherits a low output impedance, which is an important characteristic of all common collector circuits. Therefore a power pole (p_{pwr}), created by the pass element, occurs at a higher frequency because of the relatively low output impedance of the pass element.

$$p_{\text{pwr}} = \frac{-1}{2\pi R_{\text{pwr}} C_{\text{pwr}}} \tag{4.28}$$

where R_{pwr} and C_{pwr} are the resistance and capacitance of the pass element.

The dominant pole (p_{int}), created by the intrinsic elements of the regulator, occurs at a very low frequency due to the very high output impedance of the regulator, especially due to the relatively high capacitance:

$$p_{\text{int}} = \frac{-1}{2\pi R_{\text{int}} C_{\text{int}}} \tag{4.29}$$

where R_{int} and C_{int} are the intrinsic resistance and capacitance of the regulator. According to the Bode plot analysis as shown in Fig. 4.8, there are two poles in the standard NPN regulator. Still, p_{pwr} can occur at a frequency below the 0 dB crossover point, which may create a less than 45° phase margin. As discussed before, in order to keep the conservative policy of phase margin above 45° this needs some compensation (Fig. 4.8). In such

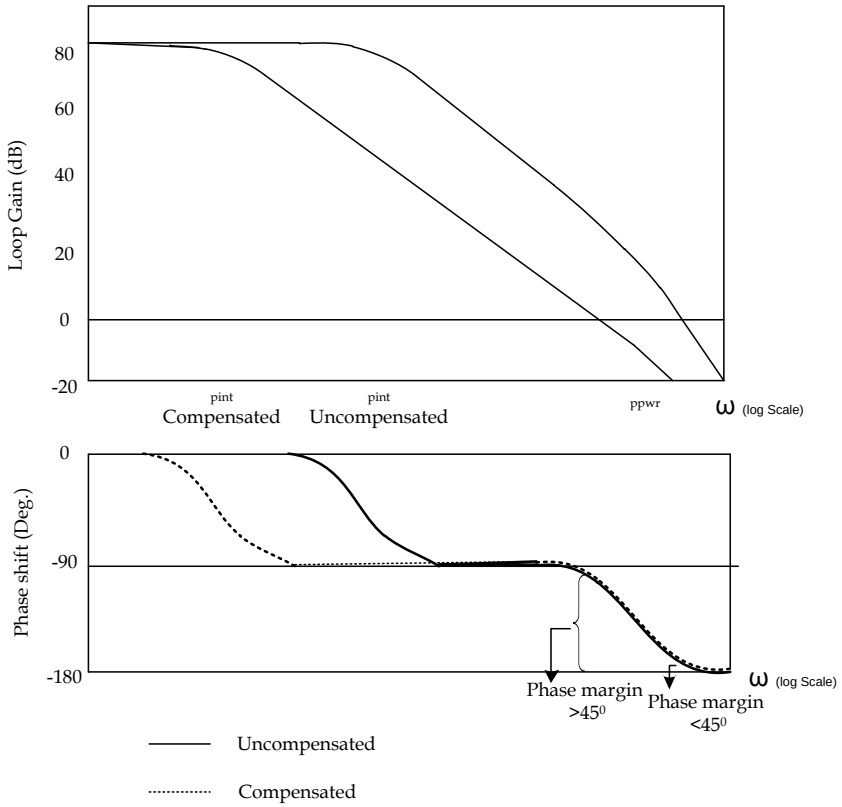


Figure 4.8: Standard NPN regulator Bode plot (uncompensated and dominant pole compensation) [141]

a case, the standard NPN regulator employs an internal compensation known as dominant pole compensation, which is achieved by adding intrinsic capacitance to the regulator so that p_{int} moves to an even lower frequency. Therefore the standard NPN regulator does not need an external compensation due to the superior frequency response of the NPN pass device.

(b) Quasi NPN Linear Regulator

The quasi-NPN regulator uses an NPN pass device, and it is in the common-collector configuration, which means its output impedance is relatively low. However, because the base of the NPN is being driven from a high-impedance PNP current source as shown in Fig. 2.9, the regulator output impedance of a quasi-LDO is not as low as the standard NPN regulator with an NPN Darlington pass device. Therefore p_{pwr} occurs at a frequency lower than that of the standard NPN regulator, and usually below the 0 dB crossover point. The result is a less than 45° phase margin, where compensation is required (Fig. 4.9).

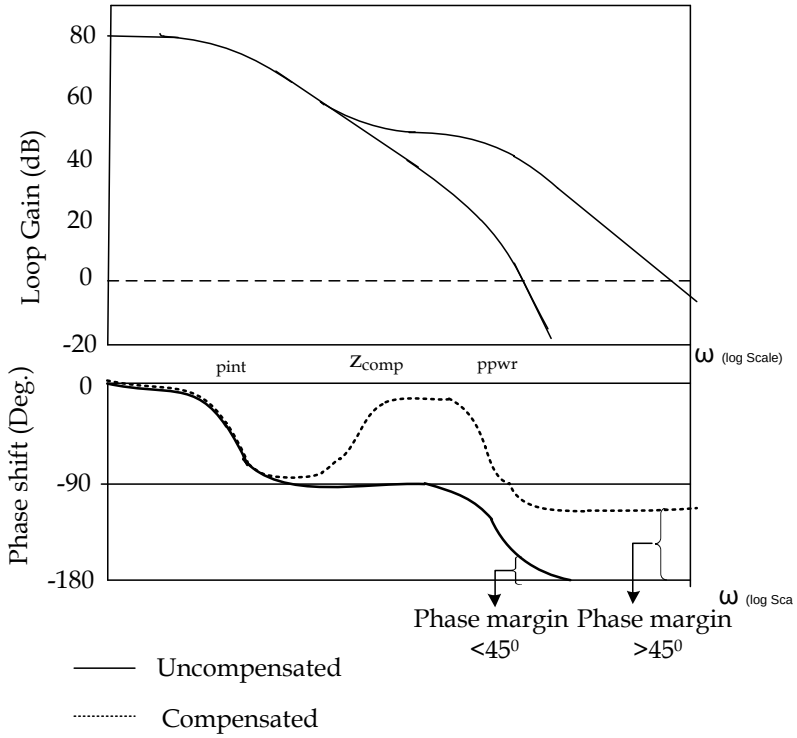


Figure 4.9: Quasi- NPN regulator Bode plot [141]

Because of the relatively low frequency of p_{pwr}, the NPN pass transistor regulator cannot be stabilized by using only dominant pole compensation. Instead, a zero must be placed between p_{int} and p_{pwr} to increase the phase margin to at least 45° (Fig. 4.9). This is accomplished by using an external compensation method, such as the addition of an output capacitor next to V_{out}. The frequency of the added zero (z_{comp}) is defined by,

$$z_{\text{comp}} = \frac{-1}{2\pi R_{\text{esr}} C_o} \tag{4.30}$$

where R_{esr} is the equivalent series resistance of the output capacitor. Because p_{pwr} of the NPN pass transistor regulator still occurs at a relatively higher frequency, output

capacitor selection is relatively easy. As long as z_{comp} is lower than p_{pwr}, C_{out} can be small, and R_{esr} is not critical.

(c) LDO Regulator

Compared to other linear regulator configurations, PNP pass transistor regulators require a more careful selection of the output capacitor. Its pass element, the PNP transistor as shown in Fig. 2.10, exhibits a high output impedance, so p_{pwr} occurs at a frequency lower than in the other linear regulator configurations. Furthermore the impedance of the load, created by load resistance and output capacitance, becomes a significant contributor to loop stability by adding another low-frequency load pole (p_L) to the Bode plot. The frequency of p_L is expressed as,

$$p_L = \frac{-1}{2\pi R_{\text{load}} C_{\text{out}}} \tag{4.31}$$

Typically, R_{load} and C_{out} are higher than the intrinsic resistance (R_{int}) and capacitance (C_{int}) of the regulator, which makes f(p_L) have a frequency lower than f(p_{int}). With three poles the PNP pass transistor regulator needs further compensation, even with dominant pole compensation. A zero must be added to compensate, which can be accomplished by the addition of an output capacitor next to V_{out}. The location of the zero in the frequency space is particularly critical, because it translates to a careful matching of the capacitance and ESR of the output capacitors.

The zero must occur somewhere between p_{int} and p_{pwr}(Fig. 4.10). Because p_{pwr} occurs at a relatively low frequency, the "space" between p_{int} and p_{pwr} is narrow; hence, the choice of z_{comp} is narrow and is demonstrated as,

$$p_{\text{int}} < z_{\text{comp}} < \frac{p_{\text{pwr}}}{10} \tag{4.32}$$

Eqn. 4.32 shows that z_{comp}) must occur above p_{int}), and at least one decade below p_{pwr}. This is because Z_{comp} needs the full one decade above z_{comp} to fully realize its +90° phase shift. Based on Eqn (5.12) in order to maintain loop stability at any given capacitance value, the ESR must satisfy the following:

$$\frac{R_{\text{int}} C_{\text{int}}}{C_{\text{out}}} > R_{\text{esr}} > 10\frac{R_{\text{pwr}} C_{\text{pwr}}}{C_{\text{out}}} \tag{4.33}$$

If the R_{esr} is either too high or too low, it is out of range. The R_{esr} is too high when the following condition exists:

$$R_{\text{esr}} > \frac{R_{\text{int}} C_{\text{int}}}{C_{\text{out}}} \tag{4.34}$$

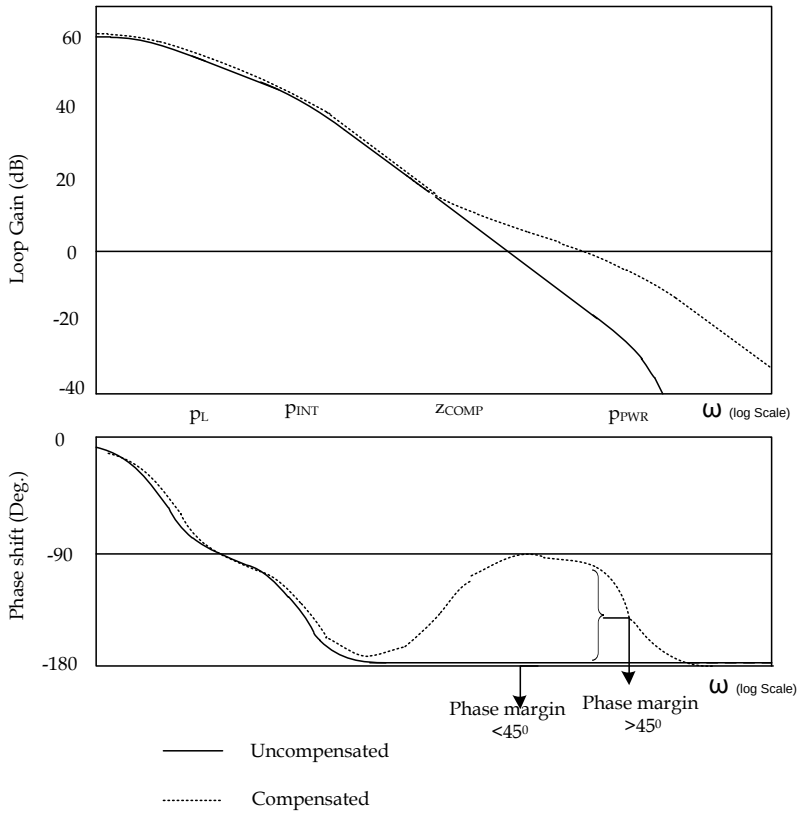


Figure 4.10: LDO regulator Bode plot (uncompensated and dominant pole compensation) [141]

Under these conditions, z_{comp} occurs at a frequency below p_{int}). Additionally, because of the narrow space between p_L, p_{int} and z_{comp} can be within one decade of p_{int}. This prevents z_{comp} from realizing its full $+90°$ phase shift. As a result, the phase margin may not rise above $45°$ and, hence, the loop needs compensation. On the other hand, the ESR is too low when the following is true:

$$R_{\text{esr}} < 10\frac{R_{\text{pwr}}C_{\text{pwr}}}{C_{\text{out}}} \tag{4.35}$$

Here, z_{comp} occurs within one decade below p_{pwr}, which prevents it from realizing its full $+90°$phase shift. Therefore the phase margin will not rise above $45°$, and the loop needs compensation.

Please note that p_L, p_{int}, p_{pwr} and z_{comp} are represented as p_1, p_2, p_3 and z_1 respectively in the section 4.5.2 frequency response discussion with reasonable approximations.
The LDO manufacturer provides a set of curves that define the boundaries of the stable region, plotted as a function of load current (Fig. 4.11). Fig. 4.12 shows typical aluminium electrolytic capacitor characteristics over frequency and temperature.

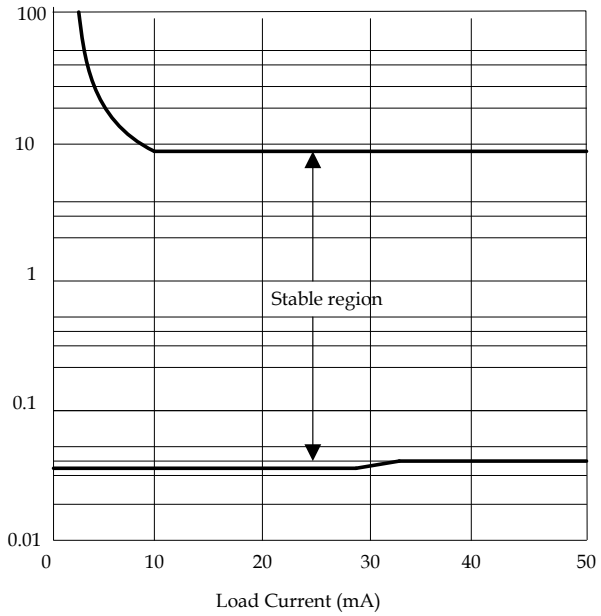


Figure 4.11: ESR range of a typical LDO. (From C. Simpson, National Semiconductor, Application Note 1148, May 2000.)

4.5.4 Enhancements for the LDO Compensation

There are novel modifications to the basic LDO architecture from Analog Devices ADP330X series LDO regulator family in which careful selection of output capacitor is important [143]. Leung et al. [144] have analysed and shown that conventional frequency compensation cannot effectively stabilize a low-voltage LDO with a two-stage error amplifier. Furthermore they emphasized that the conventional technique is parameter dependent and very sensitive to external effects, so it is limited to certain operation conditions and not the optimum. In order to stabilize low-voltage LDOs, they have developed a novel approach based on nested Miller compensation, called pole control frequency compensation (PCFC), which is a systematic approach and improves the stability of the low-voltage LDO under load current and temperature.
Conventional ESR frequency compensation is not an optimal method to maintain stability for a wide range of loading current as the pole at the output node changes significantly with different loading conditions. Kwok and Mok [136] have introduced a tracking zero to cancel the output pole so that the frequency response becomes independent of current.

4.6 Chapter Summary

In a practical DC-DC converter, the design of the control loop becomes a challenge because of non-ideal behaviour in components such as op-amps, capacitors, inductors and transformers, and the finite frequency response properties of BJTs and MOSFETS. The Bode plot is a convenient tool to determine if a closed-loop system is stable.

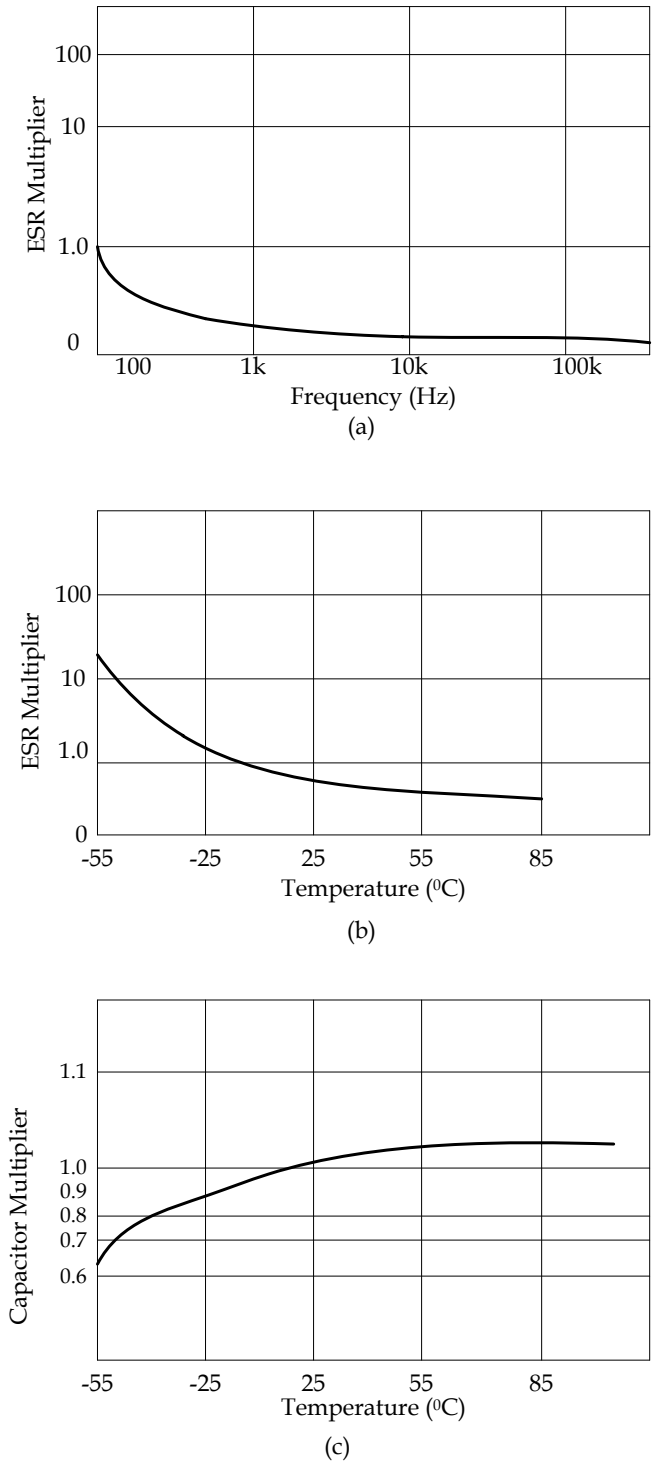


Figure 4.12: Behavior of typical aluminum electrolytic capacitors at different frequencies and temperatures: (a) frequency behavior; (b) ESR change with temperature; (c) capacitance change with temperature. (From ON Semiconductor, Application Note SR003AN/D.

The next chapter discusses the basics of capacitors and supercapacitors and the properties, performance, reliability and applications supercapacitors.

Chapter 5

Supercapacitors and Applicable Theory

5.1 Capacitor Fundamentals

A capacitor is a device that stores electrical charge and releases it when it is required by the circuit. The arrangement shown in Fig. 5.1 illustrates the simplest configuration of a capacitor: two parallel conducting plates separated by a dielectric material (electric insulator) where the parallel plates have an area A and separation d.

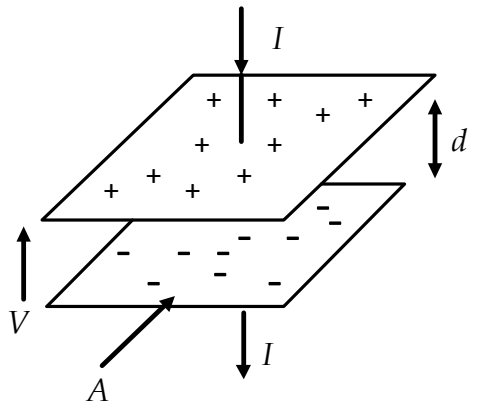


Figure 5.1: Construction of a parallel-plate capacitor

The charge on either one of the parallel conductors in the capacitor is zero in the uncharged state. When a DC voltage, V, is applied to the capacitor electrodes, an electrical charge builds up on the capacitor plates with electrons producing a positive charge ($+Q$) on one plate and an equal and opposite negative charge ($-Q$) on the other plate. Current, I, flow continues until the potential difference between the two electrodes becomes equal to the supply voltage, in a fully-charged capacitor.

The ratio $\frac{Q}{V}$ is defined as the capacitance,

$$C = \frac{Q}{V} \tag{5.1}$$

with capacitance units of farad (F).

The behaviour of a capacitor is described by the equation,

$$i(t) = \frac{\mathrm{d}q}{\mathrm{d}t} = C\frac{\mathrm{d}v}{\mathrm{d}t} \tag{5.2}$$

where t is time, i is current through the capacitor at time t, and v is the voltage across the capacitor leads at time t.Integrating Eqn. (5.2), capacitor voltage can be obtained as,

$$v = \frac{1}{C}\int_0^t i(t)^{'}\,\mathrm{d}t^{'} + v(0) \tag{5.3}$$

where $v(0)$ is the initial voltage of the capacitor at the beginning of the charging process.

As shown in Fig. 5.1, the simplest form of a capacitor consists of two conducting plates of area, A, which are parallel to each other and separated by distance d by a dielectric material such as ceramic, polymer or aluminium oxide. In such a parallel-plate capacitor, the electric energy is stored statically in the electric field between two electrodes.

The capacitance formula for a parallel-plate capacitors is given by,

$$C = \frac{\epsilon A}{d} \tag{5.4}$$

Thus capacitance, increases with electrode area (A) and increases with permittivity, ϵ, of the dielectric material, but decreases with the electrode separation, d. Conventional capacitors yield capacitance values in the range of 5 pF to 1 F with a voltage range of 10 to over 400 V.

5.1.1 Capacitor Charging

A typical charging circuit of a capacitor is shown in Fig. 5.2 using constant DC voltage V_{in} and a series resistance R. This resistor represents the resistance of the capacitor, resistance of external leads and connections, and any deliberately introduced resistance. Assume that the initial voltage of the capacitor, $V(0)$, is zero.

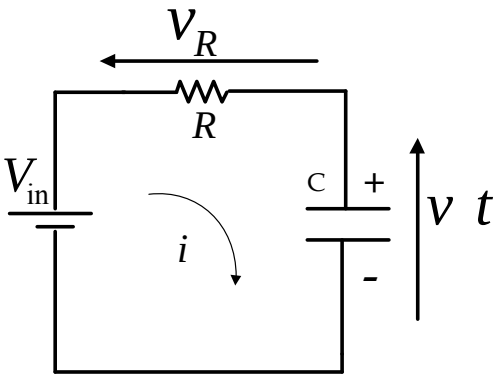


Figure 5.2: Charging a capacitor from a voltage source

Using Kirchoff's voltage law,

$$V_{\text{in}} = i(t)R + \frac{1}{C}\int_0^t i(t)'\,\mathrm{d}t' \tag{5.5}$$

Solving Eqn. (5.5) for current we obtain,

$$i(t) = \frac{V_{\text{in}}}{R}\exp\left[\frac{-t}{RC}\right] \tag{5.6}$$

Using Eqn. (5.6), the capacitor voltage at a given time during the charging process is,

$$v(t) = V_{\text{in}}\left[1 - \exp\left[\frac{-t}{RC}\right]\right] \tag{5.7}$$

Fig. 5.3(a) shows the voltage and current behaviour of the capacitor during the charging process.

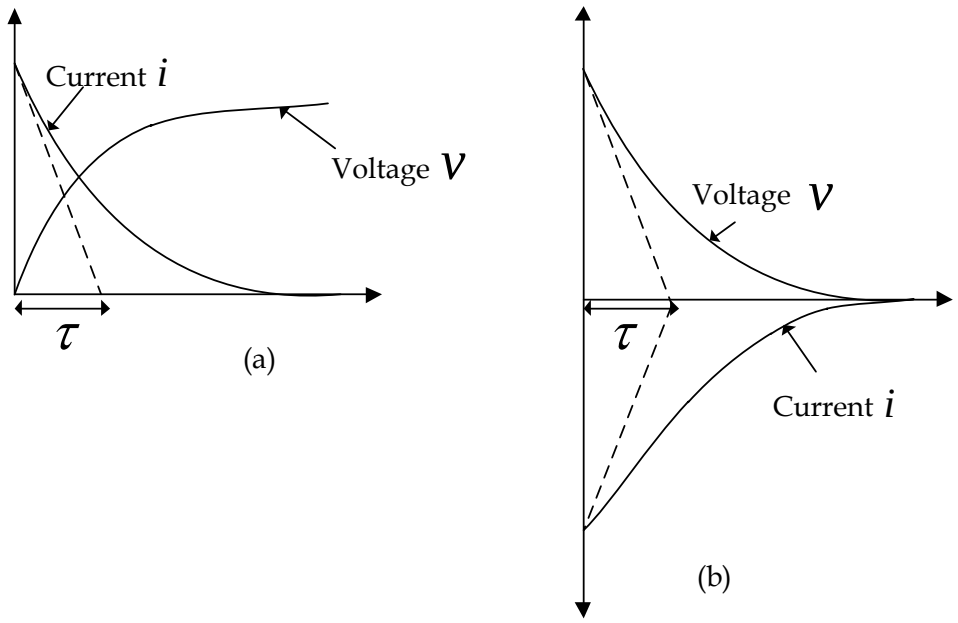


Figure 5.3: Capacitor voltage-current behaviour (a) Charging process (b) Discharging process

The rate of charge of the capacitor depends on the product of R and C. This is usually called the time constant, τ,

$$\tau = RC \tag{5.8}$$

5.1.2 Capacitor Discharging

If the DC supply is replaced with a short circuit, the capacitor will discharge through the load resistance R. When discharging, the current behaves the same as for charging, but

flows in the opposite direction. Voltage across the capacitor will decay exponentially to zero. Equations for both voltage and current discharge are given by,

$$v(t) = V_f \exp\left[\frac{-t}{RC}\right] \tag{5.9}$$

$$i(t) = \frac{V_f}{R} \exp\left[\frac{-t}{RC}\right] \tag{5.10}$$

where V_f is the voltage at the starting of capacitor discharge. See Fig. 5.3(b).

5.1.3 Capacitor Energy Storage

The total energy stored in a capacitor, E, can be shown as the product of the capacitance, C, and the square of the voltage, V.

$$E = \frac{1}{2}CV^2 \tag{5.11}$$

According to the the law of conservation of charge, if two pre-charged capacitors are connected together as shown in Fig. 5.4, the total charge on the parallel combination is equal to the sum of the original charges on the capacitors.

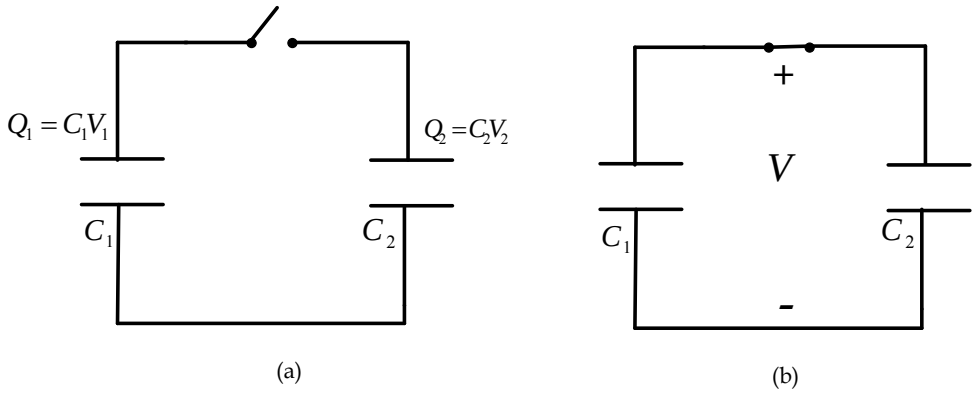


Figure 5.4: Charge distribution between capacitors

The two capacitors shown in Fig. 5.4, C_1 and C_2,are charged to voltages V_1 and V_2, respectively. When the switch is closed, an impulse of current flows, and the charge is redistributed between the two capacitors. The total charge at the beginning of the parallel combination of the two capacitors is,

$$Q_T = C_1V_1 + C_2V_2 \tag{5.12}$$

This charge is distributed between the two capacitors, so that the total charge across the two capacitors remains the same.

$$Q_T = C_1V + C_2V = (C_1 + C_2)V \tag{5.13}$$

where V is the new voltage across the parallel combination.

$$V = \frac{C_1V_1 + C_2V_2}{C_1 + C_2} \tag{5.14}$$

The total energy loss E_L due to paralleling is,

$$E_L = \left[\frac{1}{2}C_1V_1^2 + \frac{1}{2}C_2V_2^2\right] - \frac{1}{2}(C_1 + C_2)V^2 \tag{5.15}$$

which gives,

$$E_L = \frac{1}{2}\frac{C_1C_2}{C_1 + C_2}(V_1 - V_2)^2 \tag{5.16}$$

If C_2 is very much smaller than C_1 the relationship in Eqn. (5.16) can be simplified as,

$$E_L \approx \frac{1}{2}C_2(V_1 - V_2)^2 \tag{5.17}$$

According to the approximation in Eqn. (5.17), if C_1 is a supercapacitor of 1 F and C_2 is an electrolytic capacitor of 10 μ F, the total energy loss is dominated by the small capacitor.

5.1.4 Capacitor Models

In practical circumstances, the actual capacitor model is more complex as in Fig. 5.5(a). Fig. 5.5(b) shows a simplified version of this equivalent circuit model.

ESR and ESL indicate the equivalent series resistance (composed of the lead resistances, electrodes, and terminating resistances) and equivalent series inductance respectively. These two parameters are important design parameters when the capacitor is used at higher frequencies or in high-voltage situations. R_{ac} and R_{dc} represent the equivalent resistance due to AC dielectric losses and leakage resistance due to DC dielectric losses, respectively [100]. In certain circuits such as precision integrators or sample/hold circuits, the dielectric absorption of the capacitor is an important parameter. Dielectric absorption is a property, in which the dielectric material does not become polarized instantly. This causes a memory effect and is represented by R_d and C_d in Fig. 5.5(a). The dielectric absorption property prevents a capacitor from totally discharging, even when short-circuited

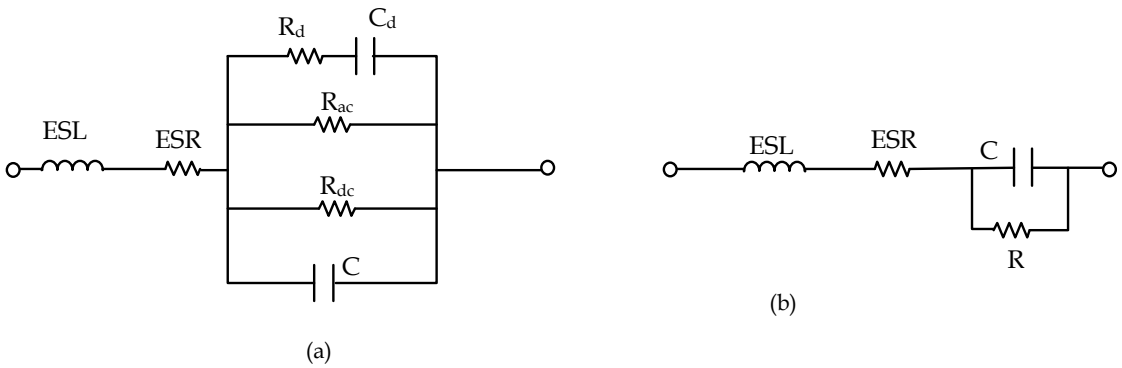


Figure 5.5: Capacitor models (a) a comprehensive equivalent circuit (b) a simplified version [100]

for a short period of time [145]. In such a situation, if the capacitor is charged and then discharged, and left open, it will recover some of its charge which will gradually reappear as a small amount of DC voltage at the terminals of the capacitor due to the parasitic effect of R_d and C_d. Figure 5.6 shows the effect of dielectric absorption when a capacitor is fully charged and then discharged by a short circuit [100, 145].

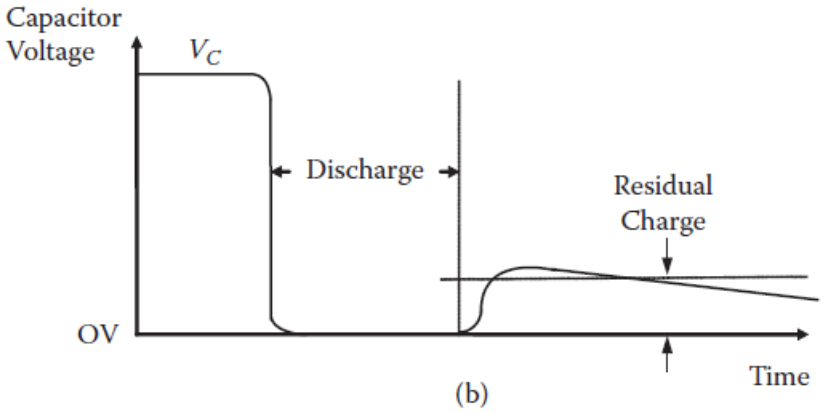


Figure 5.6: Effect of dielectric absorption [100]

In ideal conditions, the capacitor is simply represented as the capacitance, C, as shown in Fig. 5.7(a). However a simplified first-order model of the capacitor which has capacitance and equivalent series resistance (ESR) as shown in Fig. 5.7(b) is used in most DC applications.

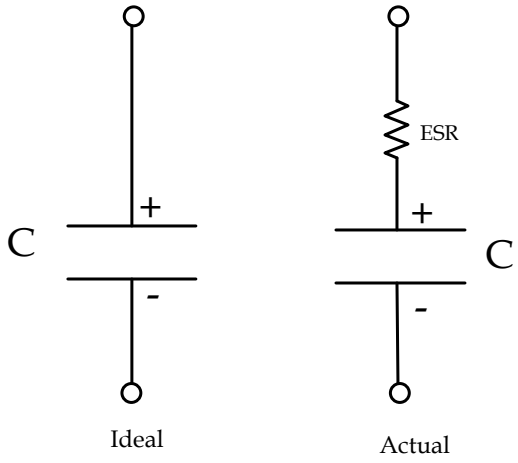


Figure 5.7: (a) Ideal capacitor (b) Simplest first-order model

5.2 Capacitor Types and Their Properties

The capacitor is one of the most critical passive components used in electronic circuits to provide smoothing, buffering, filtering, bypassing, DC blocking etc. Capacitors have the capability of storing electrical charge and releasing it when required by the circuit. There is a wide variety of capacitor types, based on the capacitor construction and the technology used. The most commonly used capacitor types are,

1. Film capacitors
2. Ceramic capacitors
3. Electrolytic capacitors

Film capacitors are general-purpose capacitors that are used in applications requiring tight capacitance tolerances and very low leakage currents. They have very low ESR and ESL values and much more stable electrical parameters. Film capacitors have relatively large sizes and weights, but have much higher surge or pulse load capabilities. [146]. Film capacitors are not polarized, so they can be used in AC voltage applications [147].

Ceramic capacitors are also fixed value capacitors that are suited for AC applications as they are non-polarised [147]. Electrical behaviour of the capacitor is defined by the composition of the ceramic material. Applications of ceramic capacitors are divided into two stability classes [148]:

- Class 1 ceramic capacitors have high stability and low losses for resonant circuit application
- Class 2 ceramic capacitors have high volumetric efficiency for buffer, by-pass and coupling applications

Electrolytic capacitors are available in several types as aluminium, tantalum and niobium versions.

Aluminum electrolytic capacitors are available in the range of less than 1 μF to 1 F with working voltages up to several hundred DC volts, resulting in more capacitance and energy storage per unit volume [147–149]. Aluminium electrolytic capacitors are polar devices having distinct positive and negative terminals. They are capable of providing high ripple current capability together with high reliability.

Tantalum capacitors are generally available in low-voltage versions up to several hundred microfarads. Because of their smaller size for a given capacitance and lower impedance at high frequencies they are popular in miniature applications [148]. This capacitor category has a lower energy density and is produced to tighter tolerances than Aluminum electrolytics [148]. Self-healing spontaneous short circuits are a problem of Tantalum capacitors.

Niobium capacitor were first introduced as cheaper alternative to tantalum capacitors. But, the materials suppliers could not make a capacitor-grade niobium powder that matched the capacitance/voltage (CV) values required to compete with tantalum. Limitations of niobium capacitors include lower volumetric efficiency (CV in a given capacitor size), lower voltage range and higher DC leakage compared to tantalum capacitors [150].

Each capacitor type is suitable for some applications but not adequate for others. A summary of essential features that is given in Table 5.1 [151].

Table 5.1: Characteristics of various capacitor types [151]

	Aluminium	Tantalum	Niobium	Ceramic	Film
Dielectric	aluminium oxide	tantalum pentoxide	niobium pentoxide	Based on barium titanate, etc.	polyester, polypropylene, etc.
Shape	Screw terminal type, snap-in type, lead terminal type, chip type	Chip type, Dip type	Chip type	Chip type, Dip type	Dip type, case type for SMD
Advantages	Cheap, small-size and large-capacity	Small size and comparatively large capacitance, semi-permanent service life	Small size and comparatively large capacitance, semi-permanent service life	Small-size, no polarity	Good characteristics, can be made for low- to high-voltage applications, high reliability
Disadv.	Short service life in hot environment, large tolerance, polarized	Can be used with some voltage leeway, Polarity	Can be used with some voltage leeway, Polarity	Large changes in capacitance due to changes in temperature and DC voltage	Large outside dimensions

Figure 5.8 shows some common capacitor types. Figure 5.9 depicts a summary of ranges of capacitance and rated voltage of various types of capacitors [151].

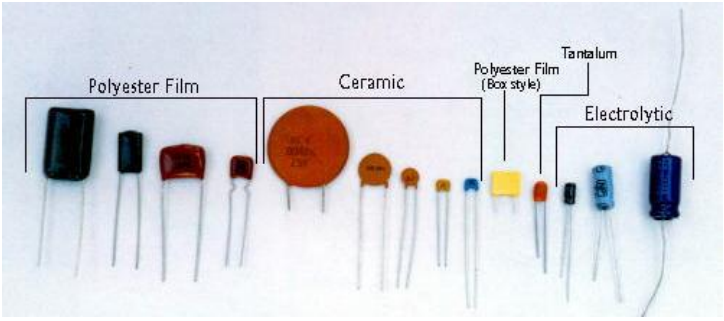


Figure 5.8: A sample of some commercially available capacitors

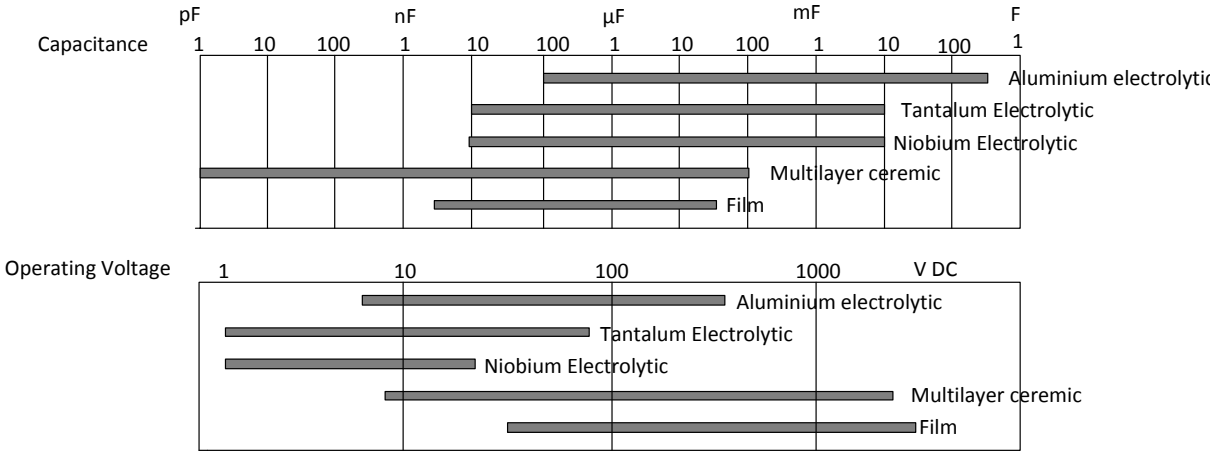


Figure 5.9: Ranges of capacitance and operating voltage of various capacitors [151]

Some typical capacitor applications in the electronics industry are [152]:

- DC-blocking capacitor: When fully-charged, the capacitor blocks the flow of DC current between two parts of a circuit
- Capacitor as an energy (charge) buffer: Capacitors are used as a charging unit and the energy is stored and released when required by the circuit
- Bypass capacitor: The reactance of a capacitor decreases as the frequency increases. In certain applications this property is utilised by placing a capacitor in parallel with other components to bypass a specified frequency and higher values.
- Capacitor as a filter: In filter circuits such as, low-pass, high-pass and band-pass capacitors are used as the main filter elements
- Coupling capacitor: The ability of a capacitor to pass AC signals, allows it to couple sections of an electronic circuit that require DC isolation.
- Decoupling capacitor: A capacitor is used to minimize noise and disturbances to the logic signal. Typically in such applications, the capacitor is placed very close to the IC output and serves as a local energy source to provide some extra current.

- Snubber capacitor: A snubber capacitor is used to limit high voltage transient across the circuit, and is frequently used in power electronic circuits.

In real-time applications, capacitors do not show their ideal characteristics due to the effect of factors such as parasitic resistance, inductance and capacitance variations over temperature and voltage. Choosing the wrong capacitor can lead to unpredictable circuit behaviour, circuit instability, excessive power dissipation or noise [153]. A capacitor has a rated capacitance, and a tolerance which is expressed as a percentage decrease or increase of the rated capacitance. The standard capacitance tolerance is $\pm 20\%$. In general, capacitors can have a tolerance in the range of -20% to as high as +80% [147, 154, 155].

The capacitance of a capacitor varies with temperature as the changes in temperature affects the dielectric properties. Furthermore, this variation is dependent to a small degree on the rated voltage and capacitor size. The normal working range for most capacitors is -30 °C to +125 °C with nominal voltage ratings [147, 154]. The ESR of a capacitor also increases with temperature.

The effective capacitance decreases as the frequency increases. The impedance of an ideal capacitor is expected to drop with the inverse of the frequency, based on the relationship given in Eqn. 5.18. However, the impedance of a non-ideal capacitor model takes a dip at self-resonance, f_0 and then begins to increase with frequency as illustrated in Fig. 5.10. The inductive component (ESL) takes over at frequencies greater than f_0 [100, 156].

$$X_c = \frac{1}{2\pi f C} \tag{5.18}$$

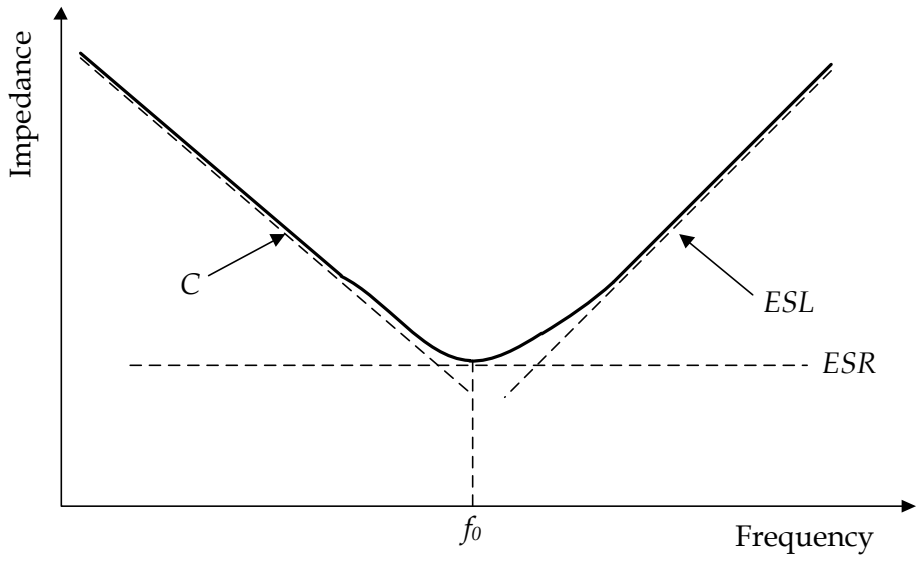


Figure 5.10: Frequency dependency of a non-ideal capacitor [100]

The dielectric material of the capacitor is not an ideal insulator, as it results in a very small current flowing through the dielectric due to the influence of the powerful electric fields built up by the charge on the plates [154]. This small DC current flow, in the range of nanoamperes, is called the leakage current. However, electrolytic capacitors may have very high leakage currents typically in the order of about 5 to 20 μA [154]. Leakage can be represented as equivalent to a resistor in parallel with the capacitor as shown in Fig. 5.11. Furthermore, the capacitor leakage current is also dependent upon the charging period, applied voltage and temperature.

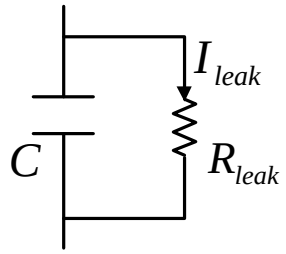


Figure 5.11: Leakage model of a capacitor

5.3 Ragone Plot

Energy storage devices (ESD) are characterized by the energy and the available power for a load [157]. The Ragone plot is a chart used for performance comparison of various energy storing devices where the values of energy density (in Wh/kg) are plotted versus power density (in W/kg) [158]. ESDs such as batteries, capacitors, supercapacitors, flywheels, magnetic energy storage devices etc., are located in characteristic regions in the power-energy plane in the Ragone plot. Both axes are usually presented on a logarithmic scale, which allows comparing performance of very different devices. As shown in Fig. 5.12, this plot compares the performances of various energy storage devices like batteries, supercapacitors and conventional capacitors [159]. The choice of the ESD depends particularly on the power density required by the application.

The sloping lines (isotherms of characteristic time constant) on the Ragone plot indicate the relative time taken to get the charge in or out of the device [157]. At one extreme, capacitor can pump power in and out within microseconds; whereas at the other extreme, battery cells which have a poor dynamic performance take a few hours to generate and deliver their energy. Supercapaciotrs are somewhere in between and provide a reasonable compromise between the two.

Portable devices, have a wide range of energy-storage needs. Some portable devices require high-power, high-energy for hours of run-time, whereas others require only a few seconds of operation before recharging [161]. As illustrated in the Ragone plot, batteries

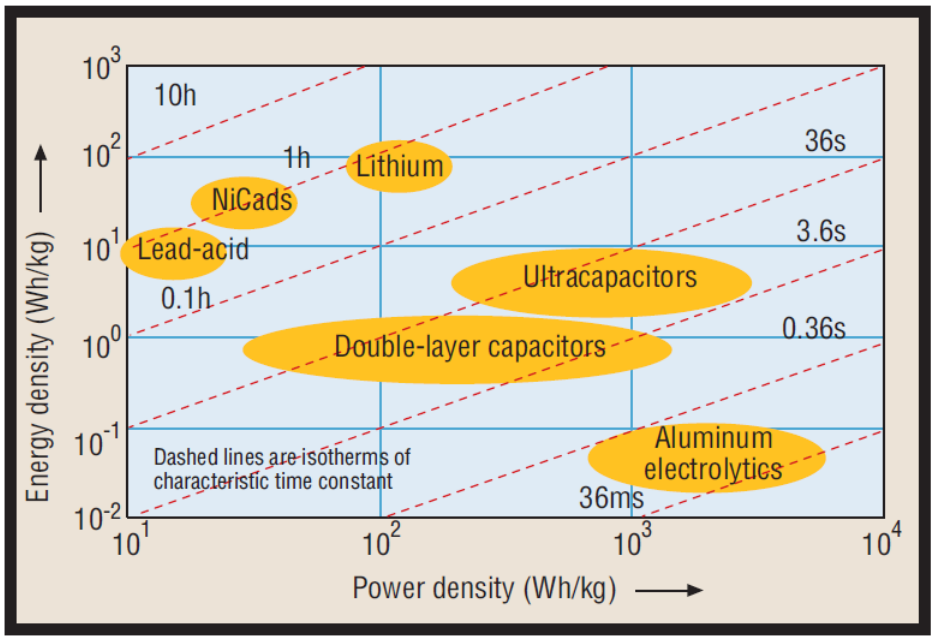


Figure 5.12: The Ragone plot showing energy density vs. power density [160]

have high energy densities but low power densities making them suitable for applications which need longer runtimes. Batteries suffer from several drawbacks, such as limited lifetime and expensive maintenance. In contrast, capacitors have rather high power densities but, low energy densities with much longer lifetimes and cycle life [157] .

5.4 Supercapacitors

As shown in Fig. 5.12 the Ragone plot, supercapacitors, also known as ultracapacitors or electrochemical double-layer capacitors (EDLC), are unique electrical storage devices, which have a higher energy density than conventional capacitors and a greater power density than batteries [159–161]. Also supercapacitors have other important properties such as extremely long cycle life, mechanical robustness and low internal resistance. Recent developments in technology, materials and manufacture have made supercapacitors an essential component for short-term energy storage in power electronic and industrial storage applications.

Because of their extraordinary power density and energy density, supercapacitors fill the gap between batteries and classical capacitors, allowing new applications. A comparison of the properties of these three energy storage devices is shown in Table 5.2.

As shown in Fig. 5.13(a) and (b), the construction of a supercapacitor consists of two electrodes, immersed in an ionic electrolyte with a separator located between the two electrodes. When the electrodes are electrically charged, the ions of the electrolyte

Table 5.2: A comparison of storage technologies [159]

Performance	Capacitors	Supercapacitors	Batteries
Energy density [Wh/kg]	0.1	3	30-210
Power density [W/kg]	10^7	3000	100
Time of charge [s]	$10^{-3} - 10^{-6}$	0.3–30	> 1000
Time of discharge [s]	$10^{-3} - 10^{-6}$	0.3–30	1000–10000
Cycle life	10^{10}	10^6	1000
Typical lifetime [years]	30	30	5

move toward the electrodes of opposite charge [159, 162–167]. As shown in Fig. 5.13(c), in the charged state, the anions and the cations are located in the electrolyte next to the electrode such that they balance the excess charge on the electrically conducting side of the phase boundary. Thus, there are two layers of excess charge of opposite polarity across each phase boundary. Therefore each electrode−electrolyte interface represents a capacitor so the complete cell can be considered as two capacitors in series as shown in Fig. 5.13(d) [165]. Due to the micropores in the carbon-based electrode material, the surface area can reach up to 3000 m^2/g [168]. This property combined with the short distance between the opposite charges results in a very high capacitance up to 5000 F per cell [162] .

For a symmetrical capacitor, the cell capacitance is given by,

$$\frac{1}{C_{\text{cell}}} = \frac{1}{C_1} + \frac{1}{C_2} \tag{5.19}$$

where C_1 and C_2 represent the capacitance of the first and second electrodes, respectively.

The capacitance of a supercapacitor can be very large, in the order of farads to thousands of farads, due to the very small distance which separates the opposite charges at the interfaces between the electrolyte and the electrodes, and the huge surface area of the electrodes.

Supercapacitor technology has matured over the last few years with supercapacitors now available from fractional farads to a few thousands of farads, power densities around 4300 W/kg, maximum energy storage density around 2.8 Wh/kg and ESR ranges from 0.3 to 130 mΩ [169]. Because of high-tech manufacturing processes and state-of-the-art materials which allow high capacitances, the maximum allowable voltage across a single cell supercapacitor is limited and is typically less than 4 V. In some applications, several supercapacitors are connected in series to form a bank to achieve higher voltage ratings [162, 170, 171], but as a result, the total capacitance of the capacitor bank decreases, and the internal resistance increases. Furthermore, supercapacitors show large deviations

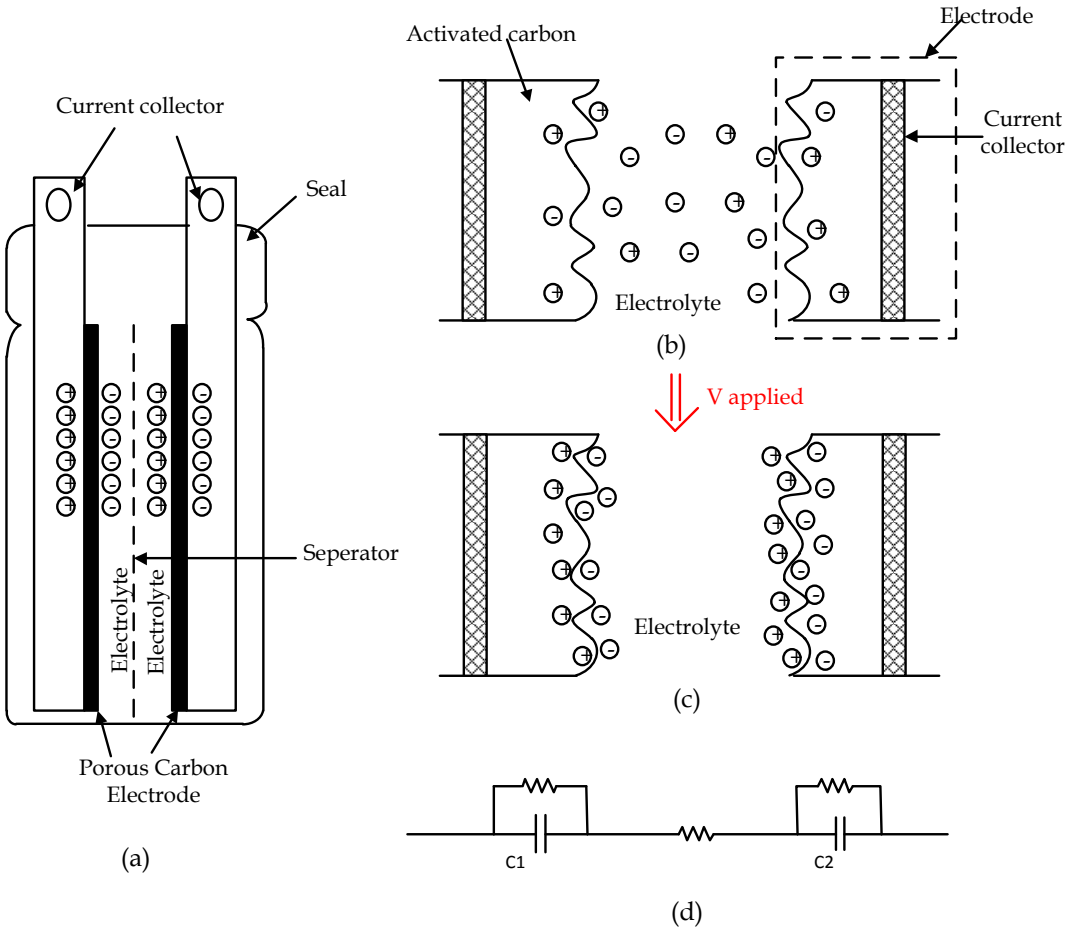
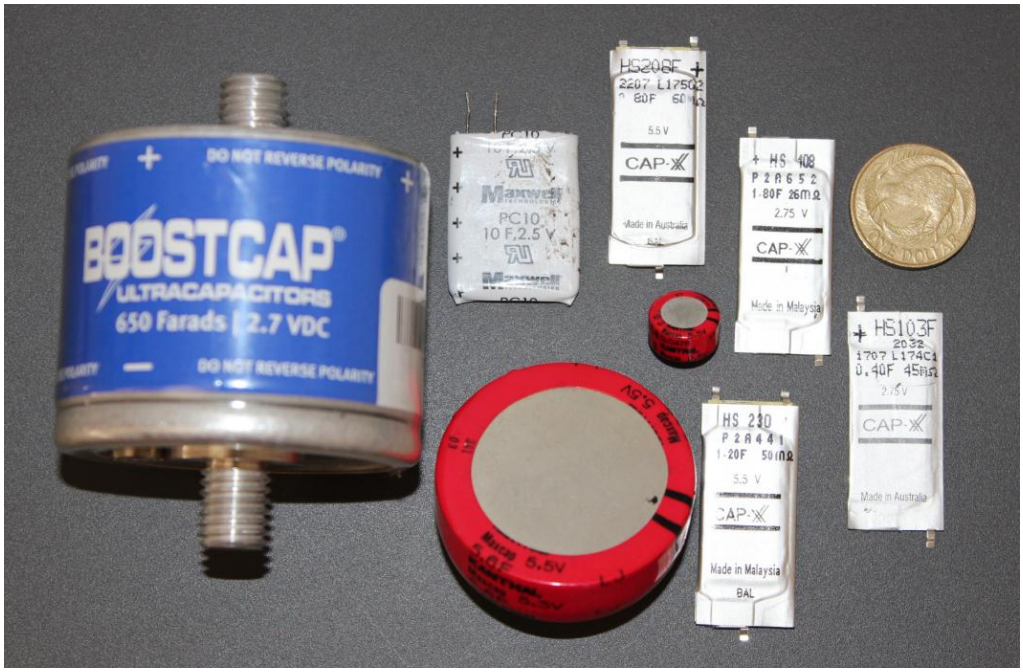


Figure 5.13: Construction of a supercapacitor

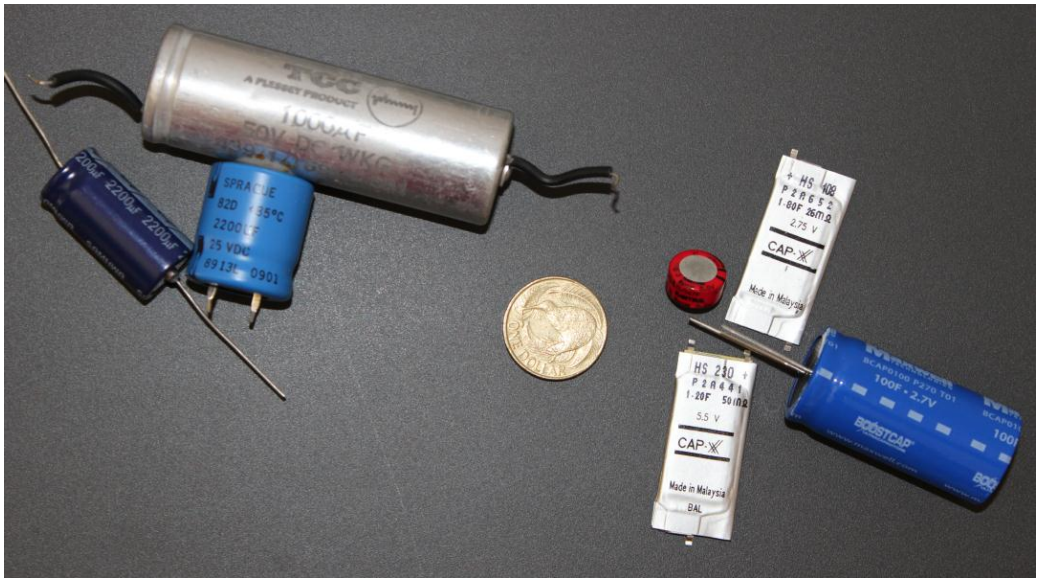
in their capacitance which can be as high as 20% of the nominal cell capacitance value. Because of these differences in the capacitances in a bank, the total voltage over a series connection of supercapacitors will not be equally distributed among the capacitors,leading to over-voltage conditions appearing over one or more capacitors. This can result in individual cells being overcharged. For this reason, an active or passive voltage-balancing circuit is employed to regulate the cell voltage. To improve the supercapacitor working voltage, hybrid supercapacitor units have been constructed by combining an anode of tantalum electrolytic capacitors with a cathode of electrochemical capacitors. These hybrid supercapacitors meet the requirements of larger capacitance while maintaining a high working voltage of about 100 V and a smaller internal resistance and size [170].

As shown in Table G.1 in Appendix G, a large number of high-performance supercapacitors are commercially available from a range of manufacturers and distributors around the world [172–177].

Table G.2 shown in Appendix G compares supercapacitors and electrolytic capacitors from a few suppliers, and clearly indicates that the ESR of new generation supercapacitors



(a)



(b)

Figure 5.14: Illustration of small physical dimensions of supercapacitors(a) commercially available supercapcitors (b) commercial supercapacitors and electrolytic capacitors together

are relatively small compared to common electrolytic caps [172–177]

5.5 Supercapacitor Models

Various equivalent circuit models have been proposed to characterise supercapcitors. Because of the complex nature of the construction, they are best described by a distributed parameter model. More frequently, lumped-parameter equivalent circuit models similar to Fig. 5.15 are utilised in analysing supercapacitors [178]. The equivalent circuit shown in this figure contains a resistance for the ion permeable separator and resistances and capacitances for individual activated carbons fibres in the electrodes. Various other equivalent circuit models for supercapacitors are available in [164, 179–182].

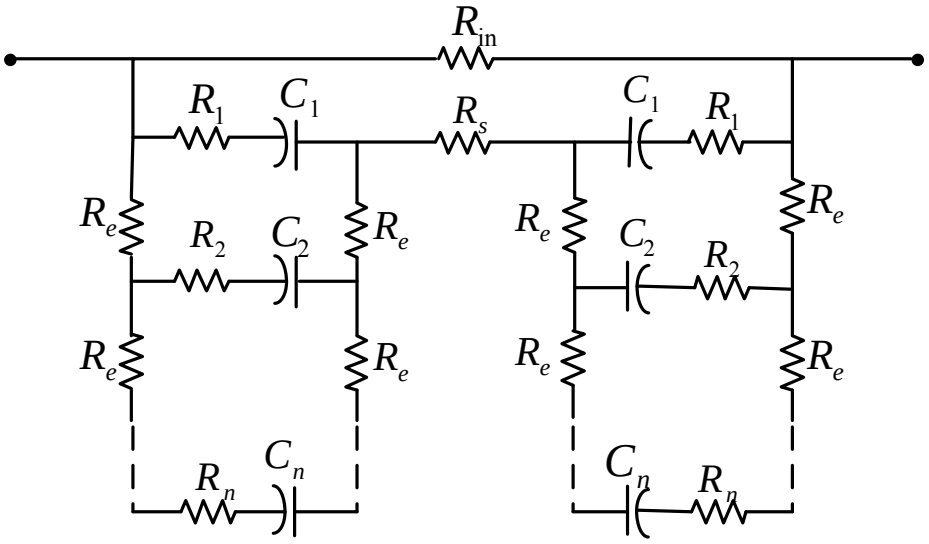


Figure 5.15: Lumped-parameter equivalent circuit model of a supercapacitor [178]

Fig. 5.16(a) represents the first-order model of a supercapacitor [159, 178, 183–185]. This model comprises four basic elements: C, capacitance, R_s, equivalent series resistance (ESR), R_p, parallel resistance and L, series inductor. R_s causes some energy loss during capacitor charging and discharging, and R_p simulates energy loss due to capacitor self-discharge. R_p is always much greater than R_s, so R_p is neglected in high-power applications. L results from the physical construction of the capacitor and is usually a small value which can be ignored in constant-current charging/discharging applications.

Supercapacitor behaviour can be approximated by the simplified version of the first-order as in Fig. 5.16(b) [186]. This model comprises an equivalent series resistance (ESR) and an ideal capacitance C. ESR is the term used for the loss that causes internal heating in the capacitor and is more important during charging and discharging processes.

The type of model that can be employed for analysis is determined by the application in which the supercapacitor is utilized. High-order models give more accurate analysis on

circuit performance. However, utilising a higher-order supercapacitor model tends to complicate analysis, calculations and simulations. The simplified classical equivalent circuit shown in Fig. 5.16(b) can be employed to predict system performance in slow discharge applications [178]. However, for devices with dynamic current profiles, the simplified model is not a reliable guide to explain the voltage behaviour and energy efficiency. In battery life time prediction, prognostics, fast charge/ discharge situations, more complex models are required.

Buller et al. [187] have come up with a new approach of modelling the dynamic behaviour of supercapacitors using impedance spectroscopy. Their MATLAB/Simulink model can be used to simulate the voltage response and energy efficiency [187]. Riu et al. [188] have derived a new approach to modelling supercapacitors to increase accuracy. This modelling allows modelling of supercapacitors accurately in the frequency domain, with a significant reduction of parameters, using measurements easily deduced from Electrochemical Impedance Spectroscopy (EIS). These simulation-based test results of dynamic charge and discharge profiles of half-order modelling have shown a good agreement with higher order ladder models.

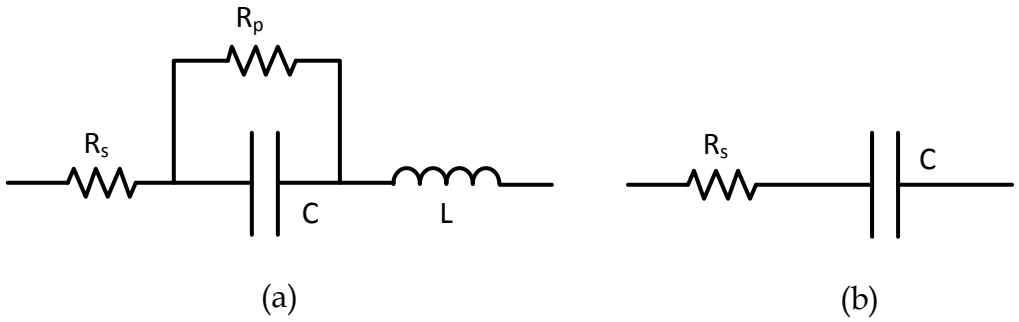


Figure 5.16: (a) First-order model of a supercapacitor (b) Simplified first-order model

Voltage profile of a supercapacitor (voltage vs. time) has two components; a capacitive component, and a resistive component. The capacitive component represents the voltage change due to the change in energy within the supercapacitor. The resistive component represents the voltage change due to the equivalent series resistance (ESR). Figure 5.17 illustrates these two components for a constant current discharge.

The capacitive component is governed by the equation,

$$I = C\frac{dv}{dt} \tag{5.20}$$

and the resistive component is governed by the equation,

$$V = IR \tag{5.21}$$

where dv is the change in capacitor voltage, I is the constant current through the supercapacitor, R is the ESR, dt is the charge or discharge time and C is the capacitance.

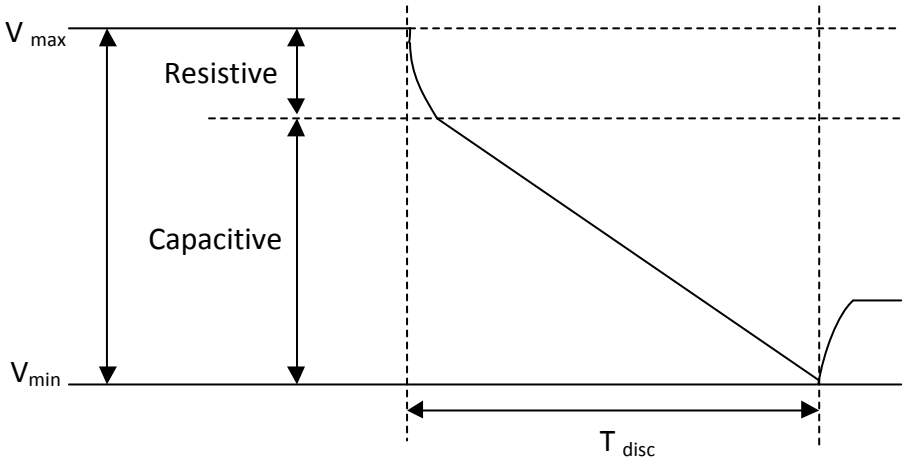


Figure 5.17: Constant-current discharge profile of a supercapacitor

5.6 Supercapacitor Performance and Reliability

During the last decade, there have been many attempts to predict the performance and reliability of supercapcitors. In contrast to electrochemical batteries, supercapcitors are capable of undergoing several thousands of deep charge and discharge cycles, as there is no chemical reaction which takes place at the carbon electrodes. Carbon electrodes are chemically and electrochemically inert, and the electrostatic nature of the charge-storage mechanism is highly reversible. This theoretically assures an infinite shelf life [162, 189]. However, in a real time application, supercapacitor cells exhibit performance fading when they are used for thousands of many charge-discharge cycles for a prolonged period of time [189].

For the reliability and safety of supercapacitor applications, it is important to identify their ageing behaviour and their modes of failure. Methods of characterising supercapacitors are based on the international standard IEC 62391 [190], in which the ageing behaviour of a supercapcitor is determined by the decrease in capacitance and by the increase in internal resistance [191, 192]. The end-of-life criteria is defined as either 20% capacitance reduction or 100% increase in internal resistance [193]. According to Kotz et. al. [193], measurements of the performance of three supercapacitors of the type BCAP0350 from Maxwell technologies under nominal working conditions at 2.5 V cell voltage and

30 °C, for the time period of 2 months, the capacitance dropped by about 10% and the internal resistance increased by about 4%.

It has been identified that the temperature and the operating voltage are the main contributors to the ageing of supercapacitors [193–201]. High temperature accelerates the process of ageing in supercapaciotrs by the higher reactivity of the chemical components. At higher voltages, more impurities undergo a redox reaction and the decomposition of the electrolyte is accelerated [193,194]. These two factors lead to an increase in internal series resistance and to a decrease in capacitance over time and as a result the performance of the supercapacitor diminishes. In general, deep charge-discharge cycling has a negligible effect on the ageing process as opposed to operating voltage and temperature. [193].

A comparison using commercial LS Mtron and Maxwell supercapciotrs on ageing/life cycle test of supercapacitors at 25 °C and 65 °C temperatures in terms of capacitance is shown in Table 5.3. This table clearly shows the effect of increasing temperature on capacitance. Larger currents in high-power applications cause a temperature increase because of the heat generated, which results in temperature-dependent degradation [197].

Table 5.3: A comparison of capacitance behaviour of LS Mtron and Maxwell supercapcitors

	Capacitance							
	LS Mtron				Maxwell			
	at 25 °C		at 65 °C		at 25 °C		at 65 °C	
No. of cycles	(F)	Ratio (%)	(F)	Ratio (%)	(F)	Ratio (%)	(F)	Ratio (%)
Initial	3 115	100	3061	100	3187	100	3145	100
After 10k cycles	2 704	87	2598	85	2581	81	2458	78
After 20k cycles	2 486	80	2401	78	2382	75	2286	73

Another comparison using commercial LS Mtron and Maxwell supercapciotrs on ageing/life cycle tests of supercapacitors in terms of ESR at 25 °C is shown in Table 5.4.

Table 5.4: A comparison of ESR behaviour of LS Mtron and Maxwell supercapcitors

	DC ESR			
	LS Mtron		Maxwell	
No. of cycles	(mΩ)	Ratio (%)	(mΩ)	Ratio (%)
Initial	0 .132	100	0.270	100
After 5k cycles	0 .214	162	0.417	154
After 10k cycles	0 .246	186	0.605	224
After 15k cycles	0 .286	217	0.783	290
After 20k cycles	0 .320	242	0.953	353

The cell voltage of supercapacitors depends on various factors, such as the application-specific current profile, the cell capacitance, the manufacturing tolerance of capacitance and self-discharge rate, the number of cells connected in series and the voltage equalization electronics [162]. In practical supercapacitor systems, the statistical distribution

of the capacitance and ESR lead to an unequal voltage distribution and thus, to different life expectancies of the cells, which diminishes the reliability of the entire system. Since lifetime of supercapacitors is mostly driven by the cell voltage and temperature, charge-balancing circuits are employed to improve the performance, reliability and lifetime. Linzen et. al. [162] have analysed and evaluated different equalization concepts for the supercapacitor charge balancing.

Cheng [192] has developed an enhanced method of characterising supercapacitors using fast charge-discharge cycles to precisely represent the energy capacity at different voltage levels and to estimate the power losses at different power levels.

5.7 Supercapacitor Applications

Enhanced power density and energy density in supercapacitors have made them a reliable energy storage candidate for industrial and consumer applications, easing power constraints on energy sources. Modern supercapacitor families find application in electric vehicles, renewable energy sources, UPS systems, battery-supercapacitor hybrids, portable electronic devices and energy backups in electronic systems. Specifically, some supercapacitor manufacturers promote their product range in various consumer, portable electronics and industrial applications. For example, an Australian manufacturer Cap-XX, which supplies thin-profile supercapacitors ranging from 0.1 F to over 1 F, aims at applications such as high brightness cellular phone or digital camera flash systems, instantaneous power requirements in general packet radio service (GPRS), and transient power requirements in class D audio amps [175]. Another manufacturer, Maxwell Technologies from USA, supplies higher capacity single-cell elements up to about 4000 F (2.3 V), and modules up to about 100 F (voltage rated up to 125 V) aiming their products at interruptible power supplies, telecom network systems, wind turbine pitch systems, peak power for drive systems and actuators, peak shaving and graceful power-down of robotic systems, augmenting the primary energy source for portable devices such as power tools, renewable energy storage sources, and high-power pulse forming in power generators [176]. The following section discusses various supercapacitor applications.

In many battery-powered portables such as mobile phones, GPRS devices and digital still cameras, pulse loads are a common scenario. Usually, pulse currents are many times higher than the steady-state current which could result in a system failure. At very low temperatures, the situation becomes even worse, as batteries (Alkaline, Lithium-ion and NiMH), exhibit vastly reduced capacity and increased internal resistance [202]. The battery-supercapacitor combination utilising low ESR, Cap-XX supercapacitors, [202–204] is designed to deliver the current demand during such load pulses, without the terminal voltage dropping to unacceptable levels, allowing it to function properly in cold conditions. Low ESR provides cap-XX supercapacitors with an unprecedented ability to deliver high

currents and also helps to protect the battery from potentially damaging voltage drops and current peaks [202, 203].

GPRS and GSM modems are now being designed into Compact Flash (CF) cards in order to be used in portable products. The CF card specification limits the current drain of the card to much lower value than a typical transmitter requires. A solution that was developed using a cap-XX supercapacitor to power the transmitter without exceeding the maximum input current requirement, resolved this issue, resulting in improved efficiency, while reducing design costs [205].

Continuous operation of a portable device while batteries are changed, or power is interrupted suddenly for a short while, is important to eliminate the inconvenience and the risk of damaging data loss. Cap-XX supercapacitors with very high capacitance, from a few mF to several Farads, low ESR and low leakage currents ensure the supply of power requirement of a device for a short time [206]. The cap-XX Hot Swap technology [207] in a notebook keeps its memory data in sleep mode while the battery is being changed with no need of rebooting.

Very high currents in notebook computers and other portable products create high ripple currents which can cause premature shutdown, reduced efficiency, lower battery run-time and battery life. This issue of high ripples can be drastically reduced by the use of a cap-XX supercapacitor in parallel with the supply voltage [208]. In such designs, the supercapcitor needs to be charged at power up which can be achieved by a current-limiting charging circuit with low-voltage lockout and reverse-current protection [208].

In mobile applications, the supercapacitor-battery combination improves device performance as the battery supplies the energy and the supercapacitor delivers short-term power. Palma et. al. [169] have proposed three approaches for battery-runtime extension combining battery and supercapacitors:

1. Direct connection of the supercapacitors to the battery terminals
2. Battery-inductor-supercapacitor combination (an inductor connected in series with the a parallel combination of a battery and a supercapacitor)
3. DC-DC converter along with supercapacitors interfacing with the battery

During the last decade the performance of electric and hybrid vehicles has been improved drastically, making them suitable for commercial and personal use. The fuel efficiency and performance of these modern vehicles with electric propulsion capability are largely limited by the characteristics of the energy storage systems (ESS) such as batteries, flywheels and fuel cells [209–212]. When selecting an ESS, there are inevitable trade-offs among the characteristics such as energy, power, cost and life cycle [210]. A hybrid model with improved performance can be constructed by combining two or more options which have complementary characteristics. For example, combining batteries with supercapacitors improves the life and performance of the system [210, 213, 214].

Typically, two ESSs are used in most hybrid vehicles: the main energy system (MES) with high-energy storage capability, and the auxiliary energy system (AES) with high power capability and reversibility. The MES-AES combination has enhanced characteristics such as extended range, good power, high regenerative braking capability, and better efficiency [215]. Ortzar et.al. [215] have designed and evaluated an auxiliary energy system for electric vehicles based on supercapacitors and a DC-DC converter. Another very efficient energy-management system for hybrid electric vehicles, using supercapacitors and neural networks, was developed and tested by Moreno et. al. [211].

ESSs can improve the energy efficiency of common transportation systems such as trains, tramways, and subways. Supercapacitors, new batteries and flywheels have been tested in achieving the goal to recover, store and reuse energy for the next traction operation. A new subway without a supply rail has been developed to enable a more efficient subway traction system. This subway uses an on-board supercapacitor bank for autonomous operation. The supercapacitor bank is charged at each station. When the engine accelerates, the supercapacitor bank is discharged and when it decelerates, the regenerative braking charges the supercapacitor bank. In this way, energy wastage is minimised [212].

Batteries are the primary power source in wireless sensor nodes (WSN), but due to the limited number of recharge cycles and the inability to hold full charge for long periods of time, the battery must eventually be replaced. Such recurring maintenance costs are likely to become very expensive if it must be done for thousands of deeply embedded nodes. Therefore, battery life-span has become a primary limiting factor in WSNs. A viable option for achieving longer-life operation is to replace the battery and with supercapacitors. An efficient charging method for a supercapacitor-operated, solar-powered wireless sensor node called Everlast has been developed [216]. Unlike traditional wireless sensors that store energy in batteries, Everlast's use of supercapacitors enables the system to operate for an estimated lifetime of 20 years without maintenance.

The uninterruptible Power Supply (UPS) is a reliable solution to enhance power quality and protect critical loads from disturbances such as sags, outages and surges [217–220]. Modern UPSs are capable of providing instantaneous access to guaranteed back-up power for up to several minutes. The ESS of a conventional UPS relies on lead-acid batteries, but there are many drawbacks associated with them such as low-power density and limited number of charge-discharge cycles. A power sharing between supercapacitors, fuel cells and batteries has been tested as a promising solution for improving system performance [210, 213, 214]. Lahyani et. al. [218] describes an example of power-sharing between supercapacitors and a lead-acid battery in a 500-kVA rated UPS, with special attention to the optimal supercapacitors-battery combination versus the supercapacitor cost.

Khan et al [221] have reviewed the possibility of storing transient surges using supercapacitors. They analysed transient behaviour by mathematically modelling the equivalent

series RC circuit of the supercapacitor. Kulatana et al [222] have presented details of a measurement system to test the surge endurance capability of supercapacitor families using three different commercial supercapacitors.

5.8 Chapter Summary

The capacitor is one of the most critical passive components used in electronic circuits to provide smoothing, buffering, filtering, bypassing and DC blocking. There are wide variety of capacitor types, based on the capacitor construction and the technology used. Supercapacitors are unique electrical storage devices with a higher energy density than conventional capacitors and a greater power density than batteries. Enhanced power density and energy density in supercapacitors have made them a desirable energy storage candidate for industrial and consumer applications, easing power constraints on energy sources.

The next chapter introduces the fundamentals of the supercapacitor-assisted low dropout (SCALDO) regulator technique and generalised SCALDO theory and step-by-step mathematical derivations.

Chapter 6

Supercapacitor Assisted Low Dropout (SCALDO) Regulator

6.1 Essential Fundamentals

As explained in Chapter 2, if the control circuit consumes only a negligible amount of power the best possible theoretical efficiency of a linear regulator is given by,

$$\eta = \frac{V_{\text{reg}}}{V_p} \times 100\% \tag{6.1}$$

where V_{reg} and V_p are the regulated output voltage and the input voltage respectively.

Usually in a linear regulator configuration, most of the energy is dissipated across the pass-element or the series power semiconductor. Introducing a voltage dropper in series with the pass element will make the dissipation across the pass element lower.

Placing a resistor in series with the pass element as shown in Fig. 6.1 would move some of the energy to the resistor, but this will not improve the overall end-to-end efficiency.

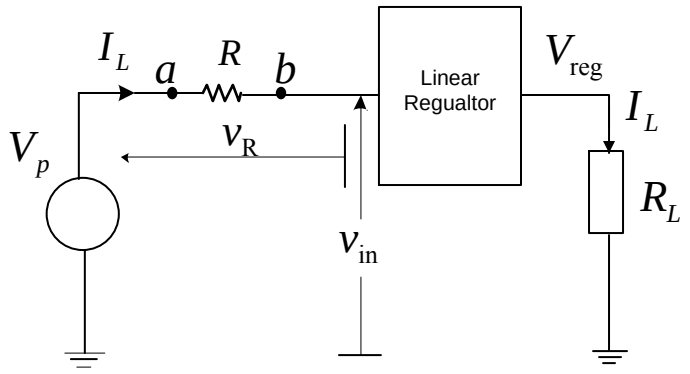


Figure 6.1: An arrangement of placing a resistor in series with the pass element to make the dissipation lower

For this purpose as the series dropper, a hypothetical circuit element which provides a voltage drop without any losses in the element can be utilised. An inductor cannot be placed in the series path, as it cannot supply a constant load current to the regulator.

A capacitor is the matching candidate as a series dropper element, but in such a case if the capacitance is very small it will block the circuit quickly, stopping the current in a negligible period of time. A supercapacitor, which is commercially available, is the ideal candidate as a series dropper element. The fundamental concept of choosing a supercapacitor as the series dropper element is as follows.

The voltage change (dv) across a very large capacitance C such as a supercapacitor is very small when a finite charge (or discharge) current $i(t)$ flows during a finite time t.

$$dv = \int_0^t \frac{1}{C} i(t)\,\mathrm{d}t \tag{6.2}$$

If a large capacitor is used as a voltage dropper in a circuit, then the effect of the voltage change (dv) due to charging the capacitor for a finite amount of time, can be neglected in terms of the operational principles applicable to that particular circuit. For example, when a large capacitor is connected in series to a circuit for a finite time, the capacitor will not act as a blocking element to that circuit due to charging during that time. Based on this simple principle, using a single supercapacitor or an array of supercapacitors in the series path to store and release the energy, the supercapacitor based efficiency improvement technique suitable for linear regulators was developed [1, 2].

6.2 Basic Concept

Fig 6.2 illustrates the concept: a supercapacitor C_{SC} is placed in series with the input of the LDO. Since the series capacitor is large (of the order of farads), it will pass current as it charges for a reasonable period of time. Based on this simple principle, a single supercapacitor can cyclically store and release energy. As per Fig 6.2(a) in the first phase of the operation, the supercapacitor is charged from the unregulated power supply. When the value of LDO input voltage, V_{in} drops to the minimum allowable voltage $V_{\mathrm{in}}^{\mathrm{min}}$ the operation is switched to the next phase. In this phase, disconnecting the unregulated power supply, the supercapacitor is connected in parallel with the input of the LDO as shown in Fig 6.2(b), to release the stored energy in the supercapacitor.

Assuming the initial voltage across the supercapacitor (C_{SC}) is $V_{\mathrm{SC}}(0)$ after charging for a period t, the instantaneous voltage across the capacitor V_{SC} is given by,

$$V_{\mathrm{SC}} = V_{\mathrm{SC}}(0) + \frac{I_L t}{C_{\mathrm{SC}}} \tag{6.3}$$

where I_L is the load current entering the capacitor from the unregulated power supply. (We can assume that the load acts as a constant-current sink, and that the bypass current from the LDO to ground can be neglected.)

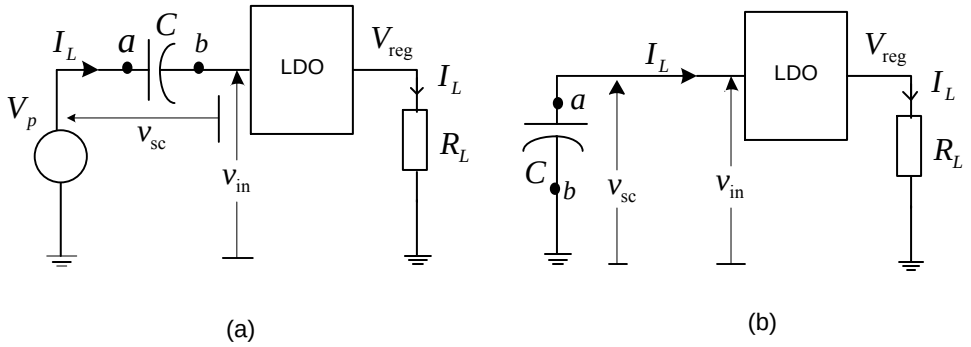


Figure 6.2: The concept of supercapacitor energy storage and recovery (a) Minimizing the series element dissipation and (b) Releasing stored energy

The unregulated source voltage V_p, equals the sum of the supercapacitor voltage and the LDO input voltage,

$$V_p = V_{\mathrm{SC}}(t) + V_{\mathrm{in}}(t) \tag{6.4}$$

The supercapacitor charges until V_{in} reaches $V_{\mathrm{in}}^{\mathrm{min}}$ while the voltage across the capacitor reaches $V_p - V_{\mathrm{in}}^{\mathrm{min}}$ at the end of the charging time. In order to discharge this supercapacitor at the next stage down to $V_{\mathrm{in}}^{\mathrm{min}}$, the criterion $V_p - V_{\mathrm{in}}^{\mathrm{min}} > V_{\mathrm{in}}^{\mathrm{min}}$ must be satisfied. This creates the condition $V_p > 2V_{\mathrm{in}}^{\mathrm{min}}$.

At the end of the charging cycle, the stored energy can be released as shown in Fig 6.2(b). Discharging continues until the LDO input voltage drops back to $V_{\mathrm{in}}^{\mathrm{min}}$ satisfying the following equation,

$$V_p - 2V_{\mathrm{in}}^{\mathrm{min}} = \frac{I_L \triangle t}{C_{\mathrm{SC}}} \tag{6.5}$$

The circuit draws power from the unregulated input only during half the time of its operating period: during the supercapacitor charging phase, the supercapacitor draws current from the unregulated supply, whereas during the discharging, the supercapacitor delivers power to the LDO keeping the unregulated power supply disconnected from the system.

Considering the charge balance of the supercapacitor during the charge-discharge cycle,

$$I_L t_{\mathrm{ch}} = I_L t_{\mathrm{dch}} \tag{6.6}$$

where t_{ch} and t_{dch} are charge time and discharge time respectively.

This gives,

$$t_{\text{ch}} = t_{\text{dch}} \tag{6.7}$$

So that the average input current drawn from the unregulated power supply is,

$$I_{\text{avg}} = \frac{I_L t_{\text{ch}}}{t_{\text{ch}} + t_{\text{dch}}} = \frac{I_L}{2} \tag{6.8}$$

Assuming that the capacitors and switching elements are ideal and neglecting the power consumed by the control circuits, the approximate end-to-end efficiency overall efficiency of the whole system) is given by,

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{V_{\text{reg}} I_L}{V_p \dfrac{I_L}{2}} = \frac{2V_{\text{reg}}}{V_p} \tag{6.9}$$

6.3 Generalised Concept

6.3.1 Series to Parallel SC Array

As shown in Fig 6.3 an array of n ideal series supercapacitors, C_{SC} each, is placed in series with the input of the LDO. This configuration is applicable to a SCALDO regulator, when it satisfies the criterion $V_p > 2V_{\text{in}}^{\text{min}}$. Basically, this is the extended version of the single supercapacitor, $n = 1$ case. The number of supercapacitors, n, can be determined using the following formula.

$$n < \frac{V_p - V_{\text{in}}^{\text{min}}}{V_{\text{in}}^{\text{min}}} \tag{6.10}$$

As the equivalent capacitance of the series capacitor array is large (in the order of farads), it will pass current as it charges for a reasonable period of time. As per Fig 6.3(a) in the first phase of the operation, the series capacitor array is charged until the value of the LDO input voltage, V_{in} is dropped down to its minimum possible input voltage, $V_{\text{in}}^{\text{min}}$.

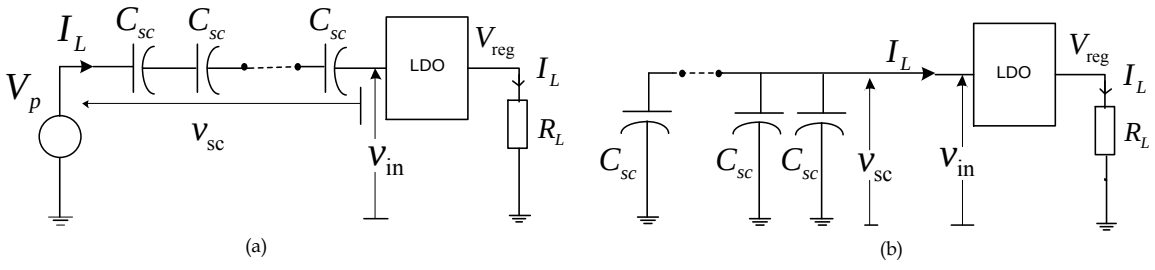


Figure 6.3: The concept of SCALDO regulator for $V_p > 2V_{\text{in}}^{\text{min}}$ (a) Charging n capacitors series minimizing the series element dissipation and (b) Discharging n capacitors parallel releasing stored energy

Assuming the initial voltage across a supercapacitor (C_{SC}) is $V_{\mathrm{SC}}(0)$, after charging for a period t, the instantaneous voltage across the capacitor V_{SC} is given by,

$$V_{\mathrm{SC}} = V_{\mathrm{SC}}(0) + \frac{I_L t}{C_{\mathrm{SC}}} \tag{6.11}$$

where I_L is the load current entering each capacitor from the power supply during the charging process assuming the ground pin current is negligible.

The voltage across a single capacitor at the end of the charging is,

$$V_{\mathrm{sc}}^{\max} = \frac{V_p - V_{\mathrm{in}}^{\min}}{n} \tag{6.12}$$

At the end of this phase, the array of supercapacitors is connected to the input of the LDO as an array of parallel capacitor as shown in Fig. 6.3(b) to release the stored energy. This discharging process continues until the LDO input voltage drops back to $V_{\mathrm{in}}^{\min}$.

The circuit draws power from the unregulated supply during the supercapacitor charging phase (t_{ch}), whereas during the discharge phase (t_{dch}) the supercapacitor delivers power to the LDO keeping the unregulated power supply disconnected from the system.

Considering the charge balance of a single capacitor during charge-discharge cycles,

$$I_L t_{\mathrm{ch}} = \frac{I_L}{n} t_{\mathrm{dch}} \tag{6.13}$$

which gives,

$$t_{\mathrm{dch}} = n t_{\mathrm{ch}} \tag{6.14}$$

The average input current taken from the unregulated power supply is,

$$I_{\mathrm{avg}} = \frac{I_L t_{\mathrm{ch}} + 0 \times t_{\mathrm{dch}}}{t_{\mathrm{ch}} + t_{\mathrm{dch}}} = \frac{I_L}{n+1} \tag{6.15}$$

Assuming that the capacitors and switching elements are ideal and neglecting the power consumed by control circuits, approximate end-to-end efficiency for this configuration is given by,

$$\eta = \frac{P_{\mathrm{out}}}{P_{in}} = \frac{I_L V_{\mathrm{reg}}}{V_p I_{\mathrm{avg}}} = \frac{I_L V_{\mathrm{reg}}}{V_p \dfrac{I_L}{n+1}} = (n+1)\frac{V_{\mathrm{reg}}}{V_p} \tag{6.16}$$

6.3.2 Parallel to Series SC Array

As shown in Fig 6.4(a) an array of n ideal parallel supercapacitors C_{SC} each, is placed in the input of the LDO. This is applicable to a SCALDO regulator when $V_p < 2V_{\mathrm{in}}^{\min}$. The number of supercapacitors, n, can be determined using the following formula.

$$n > \frac{V_{\text{in}}^{\min}}{V_p - V_{\text{in}}^{\min}} \tag{6.17}$$

As the resultant of the parallel capacitor array is large (in the order of farads), it will pass current as it charges for a reasonable period of time. As per Fig 6.4(a) in the first phase of the operation, the parallel capacitor array is charged until the value of the LDO input voltage, V_{in} drops to $V_{\text{in}}^{\min}$.

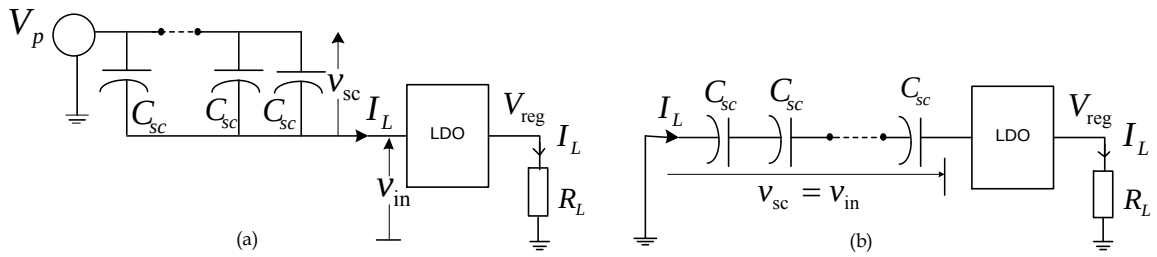


Figure 6.4: The concept of SCALDO regulator for $V_p < 2V_{\text{in}}^{\min}$ (a) Charging n parallel capacitor array minimizing the series element dissipation and (b) Discharging n capacitors series releasing stored energy

Assuming the initial voltage across a supercapacitor (C_{SC}) is $V_{\text{SC}}(0)$, after charging for a period t, the instantaneous voltage across each capacitor V_{SC} is given by,

$$V_{SC} = V_{\text{SC}}(0) + \frac{I_L t}{nC_{\text{SC}}} \tag{6.18}$$

where I_L/n is the portion of load current entering each capacitor from the power supply during the charging process assuming the ground pin current is negligible.

The voltage across a single capacitor at the end of charging is,

$$V_{\text{sc}}^{\max} = V_p - V_{\text{in}}^{\min} \tag{6.19}$$

As shown in Fig 6.4(b), in the next phase of operation, using an array of series capacitors, the stored energy is released until the LDO input voltage drops back to $V_{\text{in}}^{\min}$. The arrangement of supercapacitors in the charge and discharge phases of the operation is showed a remarkable difference with compared to $V_p > 2V_{\text{in}}^{\min}$ configuration.

Considering the charge balance of a single capacitor during charge discharge cycles,

$$\frac{I_L}{n} t_{\text{ch}} = I_L t_{\text{dch}} \tag{6.20}$$

which gives,

$$t_{\text{dch}} = \frac{t_{\text{ch}}}{n} \tag{6.21}$$

Therefore, the average input current drawn from the unregulated power supply is,

$$I_{\text{avg}} = \frac{I_L t_{\text{ch}} + 0 \times t_{\text{dch}}}{t_{\text{ch}} + t_{\text{dch}}} = \frac{I_L}{1 + \frac{1}{n}} \tag{6.22}$$

Similar to $V_p > 2V_{\text{in}}^{\text{min}}$ case, under ideal conditions, the approximate end-to-end efficiency is given by,

$$\eta = \frac{P_{out}}{P_{in}} = \frac{I_L V_{\text{reg}}}{V_p I_{\text{avg}}} = \frac{I_L V_{\text{reg}}}{V_p \frac{I_L}{1 + \frac{1}{n}}} = (1 + \frac{1}{n}) \frac{V_{\text{reg}}}{V_p} \tag{6.23}$$

6.4 Possible Implementation Scenarios

6.4.1 A Simple Case of a Single Supercapacitor

As described in the basic concept, in the simple case ($n = 1$) which satisfies $V_p > 2V_{\text{in}}^{\text{min}}$ criterion, the single supercapacitor is charged by the input current of the LDO and the stored energy in the capacitor is released to the LDO in the next stage. In this approach, the end-to-end efficiency of the overall circuit has been improved significantly, theoretically, by a factor of 2 as shown in Eqn. 6.9, while maintaining the useful characteristics of a linear regulator. The linear regulator in Fig 6.5 is designed with an LDO which operates with a low voltage difference between the input and output sides of the series pass element. As shown in Fig 6.5, four switches (k) are used to switch between charge and discharge phases. The switches, S_1 and S_3 are closed at the start, placing the pre-charged supercapacitor in series with the LDO. The switches, S_0 and S_2 are kept open at this time. The current drawn by the load flows through the supercapacitor, charging it until V_{in} meets the voltage level $V_{\text{in}}^{\text{min}}$.

In the next stage, by setting the switches the other way, the stored energy in the supercapacitor discharges to the linear regulator's input terminal. When the LDO input terminal reaches the value $V_{\text{in}}^{\text{min}}$ of the regulator, S_0 and S_2 go off and S_1 and S_3 are closed again. This cycle repeats to keep the overall regulator circuit working continuously.

In the charging phase, the instantaneous supercapacitor voltage is given by,

$$V_{\text{sc}} = V_p - V_{\text{in}} - I_L(2r + r_{\text{sc}}) \tag{6.24}$$

where ESR of a supercapacitor is r_{sc} and the on-resistance of a switch is r.

In charging, when V_{in} reaches $V_{\text{in}}^{\text{min}}$ for the LDO, the supercapacitor reaches its maximum voltage, $V_{\text{sc}}^{\text{max}}$. Therefore, the supercapacitor voltage rating can be chosen using $V_{\text{sc(max)}}$ given as in the following equation.

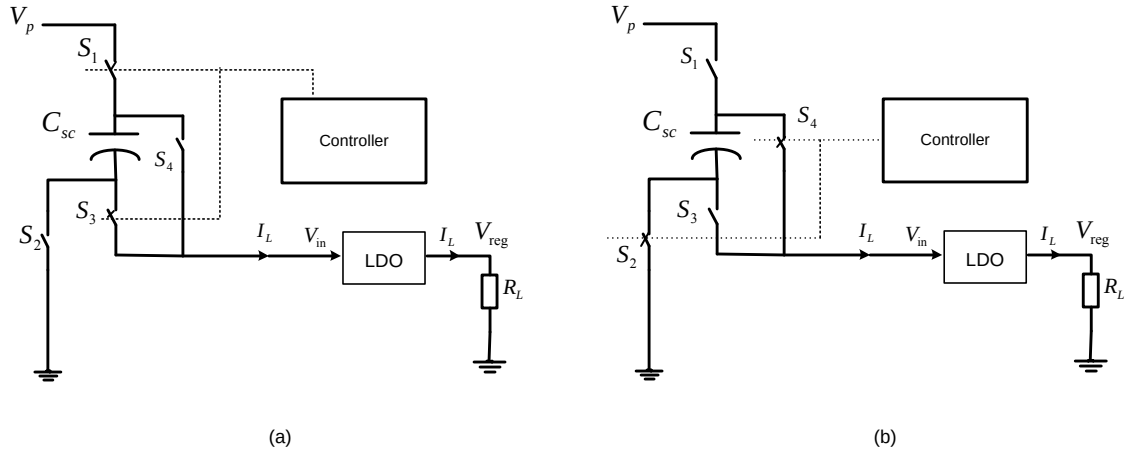


Figure 6.5: The configuration suitable for basic configuration, $V_p > 2V_{\text{in}}^{\min}$(a) Charging process (b) Discharging process

$$V_{\text{sc}}^{\max} = V_p - V_{\text{in}}^{\min} - I_L(2r + r_{\text{sc}}) \tag{6.25}$$

At the beginning of the discharging phase, the voltage at the input of the LDO is at its maximum value. The value of $V_{\text{in}}^{\max}$ is given by,

$$V_{\text{in}}^{\max} = V_p - V_{\text{in}}^{\min} - I_L(2r + r_{\text{sc}}) - I_L(2r + r_{\text{sc}}) \tag{6.26}$$

Discharging phase continues until the value of $V_{\text{in}}^{\max}$ drops down to $V_{\text{in}}^{\min}$.

The discharge time of a supercapacitor is,

$$t_{\text{dch}} = \frac{C}{I_L}\left[V_{\text{in}}^{\max} - V_{\text{in}}^{\min}\right] \tag{6.27}$$

$$t_{\text{dch}} = C\left[\frac{V_p - 2V_{\text{in}}^{\min}}{I_L} - (4r + 2r_{\text{sc}})\right] = T_1 \tag{6.28}$$

It is assumed that the net accumulation of charges in the supercapacitor during a full charge-discharge cycle is zero. Therefore, due to symmetry, the charge time for a supercapacitor is equal to the discharging time.

which gives,

$$t_{\text{ch}} = T_1 \tag{6.29}$$

Theoretically, this results in an efficiency improvement factor (η_r) of 2 compared to the conventional linear regulator.

6.4.2 Other Possible Configurations

This technique can be easily adapted to other practical requirements, if the LDO satisfies the input-output requirements to regulate the output.

(a) Series to Parallel SC Array

Here a group of n (identical) series supercapacitors are connected in series with the LDO as shown in Fig 6.6(a). When V_{in} reaches $V_{\text{in}}^{\min}$, the controller transfers the switches to the parallel capacitor configuration as in Fig 6.6(b), reusing the accumulated charge in the supercapacitors until LDO input voltage drops back to $V_{\text{in}}^{\min}$. Here the number of supercapacitors, n, determines the number of switches, k, required to keep the same set of supercapacitors in series and parallel for charging and discharging respectively.

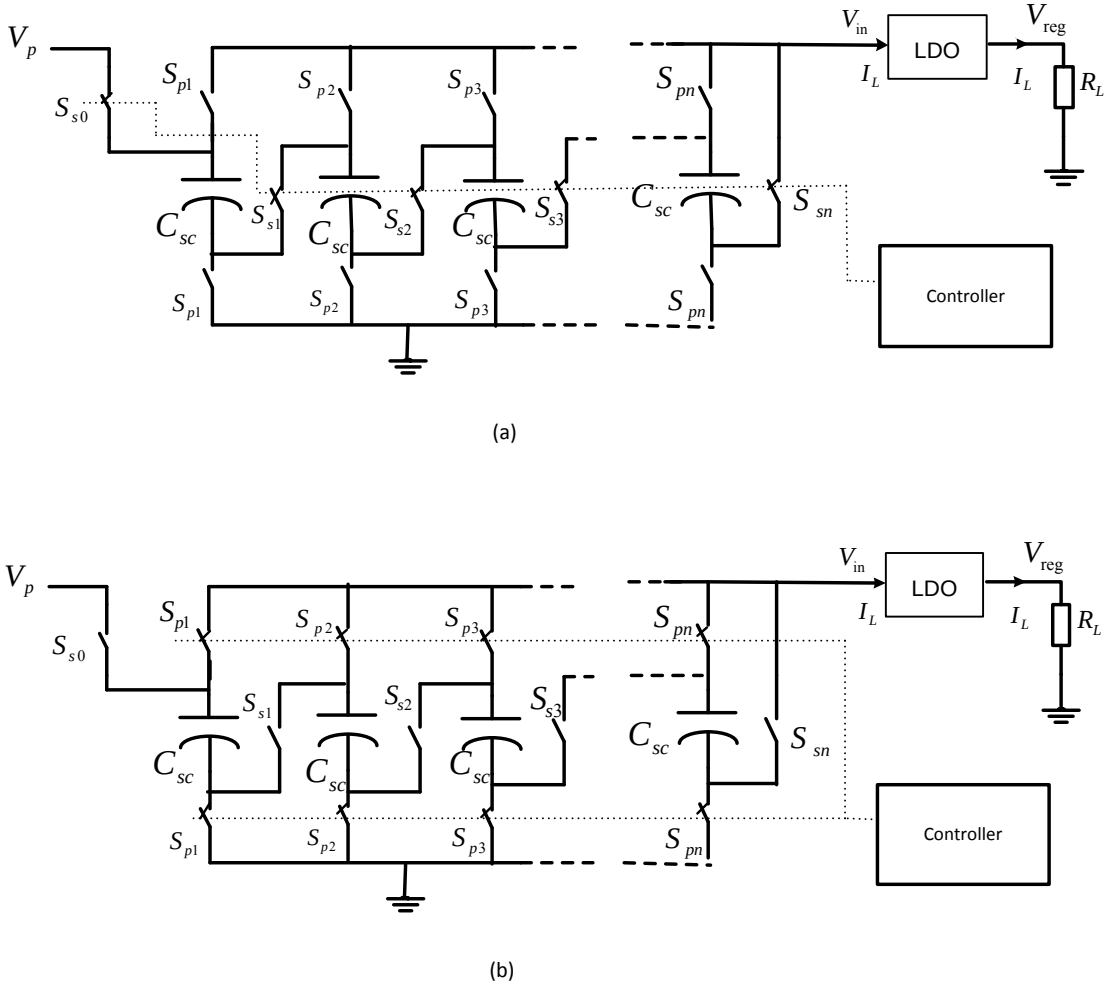


Figure 6.6: The generalised concept of $V_p > 2V_{\text{in}}^{\min}$ configuration (a) Charging process - supercapacitors in a series array (b) Discharging process - supercapacitors in a parallel array

In charging, when V_{in} reaches $V_{\text{in}}^{\min}$ for the LDO, series capacitors reach their maximum voltage, $V_{\text{sc}}^{\max}$. Therefore the supercapacitor voltage rating can be chosen using $V_{\text{sc}}^{\max}$ as given in the following equation.

$$V_{\text{sc}}^{\max} = \frac{1}{n}\left[V_p - V_{\text{in}}^{\min} - I_L\left[(n+1)r + nr_{\text{sc}}\right]\right] \tag{6.30}$$

In the discharging configuration, when the supercapacitors are switched to the parallel arrangement as shown in Fig 6.6(b), each capacitor starts to discharge from $V_{\text{in}}^{\max}$. so that at the beginning of discharge phase the voltage at the input of the LDO is given by,

$$V_{\text{in}}^{\max} = \frac{1}{n}\left[V_p - V_{\text{in}}^{\min} - I_L\left[(n+1)r + nr_{\text{sc}}\right]\right] - \frac{I_L}{n}\left[2r + r_{\text{sc}}\right] \tag{6.31}$$

The discharging phase continues until the LDO input voltage reaches $V_{\text{in}}^{\min}$.

Considering a single supercapacitor from the array, the discharge time for a supercapacitor is given by,

$$t_{\text{dch}} = \frac{nC}{I_L}\left[V_{\text{in}}^{\max} - V_{\text{in}}^{\min}\right] \tag{6.32}$$

$$t_{\text{dch}} = C\left[\frac{V_p - (n+1)V_{\text{in}}^{\min}}{I_L} - (n+3)r - (n+1)r_{\text{sc}}\right] = T_n \tag{6.33}$$

The charging time of a single supercapacitor is given by,

$$t_{\text{ch}} = \frac{t_{\text{dch}}}{n} = \frac{T_n}{n} \tag{6.34}$$

The end-to-end efficiency improvement factor η_r with respect to a standard linear regulator is given by,

$$\eta_r = \frac{\eta}{\eta_{\text{std}}} = \frac{\dfrac{I_L V_{\text{reg}}}{\dfrac{I_L}{[1+n]}V_p}}{\dfrac{I_L V_{\text{reg}}}{I_L V_p}} = 1 + n \tag{6.35}$$

(b) Parallel to Series SC Array

In this case, a group of n parallel (identical) supercapacitors are connected to the input of the LDO as shown in Fig 6.7(a), to keep the supercapacitors charging from the unregulated power supply, while maintaining the LDO regulation. During the charging, when $V_{\text{in}}^{\min}$ for the LDO is reached, the controller transfers the switches to keep the group of supercapacitors in the series configuration, as shown in Fig 6.7(b), to release the stored energy into the LDO, in order to keep the LDO regulating. The stored energy will be released until the $V_{\text{in}}^{\min}$ condition for the LDO is met and then switched back to the charging configuration again.

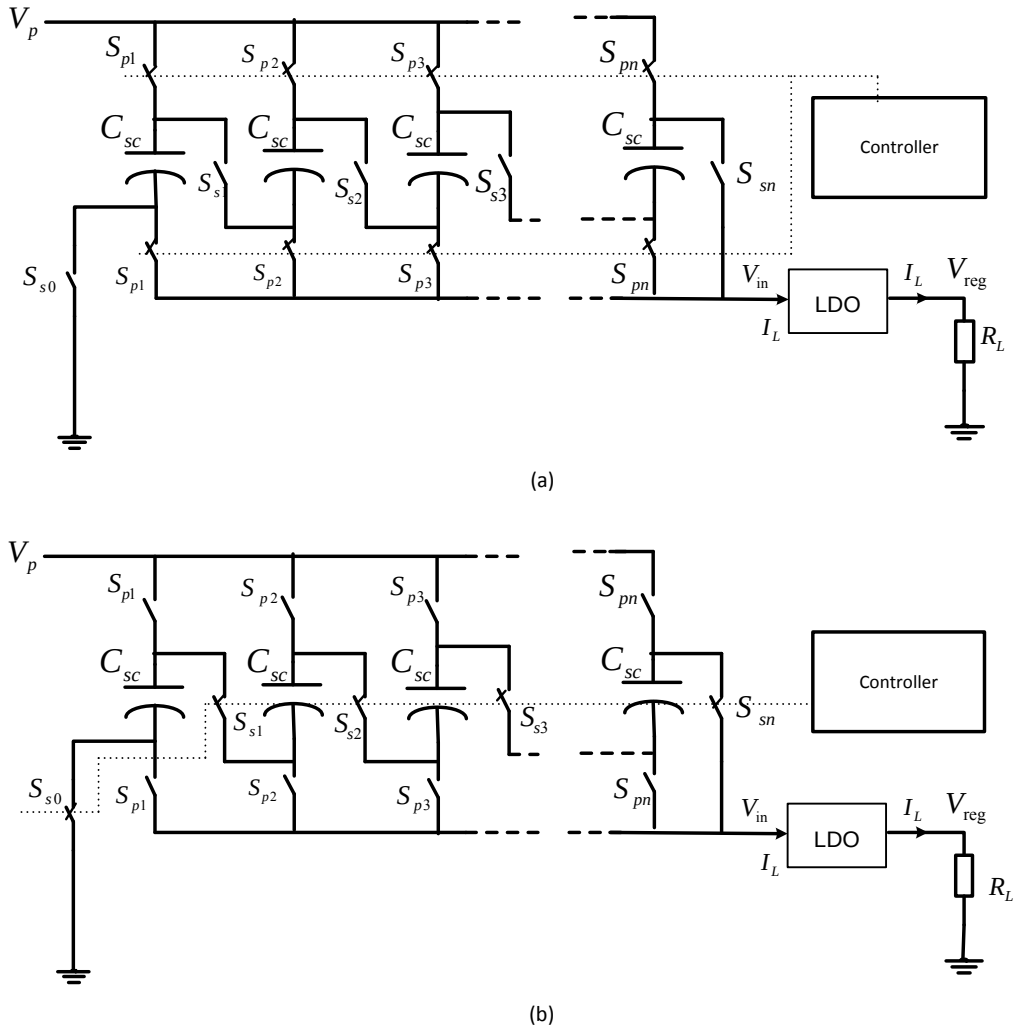


Figure 6.7: The generalised concept of $V_p < 2V_{\text{in}}^{\min}$ configuration (a) Charging process - supercapacitors in a parallel array (b) Discharging process - supercapacitors in a series array

For the generalized case, it is assumed that all the supercapacitors and switches are identical and the ESR of a supercapacitor is r_{sc} and the on-resistance of a switch is r. With the use of a very low power switch controller, we can neglect its power consumption for approximate efficiency calculations. During the supercapacitors' charging, each capacitor leg carries a current of I_L/n, where n is the number of identical supercapacitors in the group.

In the charging phase, the instantaneous supercapacitor voltage is given by,

$$V_{\text{sc}} = V_p - V_{\text{in}} - \frac{I_L}{n}(2r + r_{\text{sc}}) \tag{6.36}$$

In charging, when V_{in} reaches $V_{\text{in}}^{\min}$ for the LDO, the parallel capacitors reach their maximum voltage, $V_{\text{sc}}^{\max}$. Therefore, the supercapacitor voltage rating can be chosen using $V_{\text{sc}}^{\max}$ given in the following equation.

$$V_{\text{sc}}^{\max} = V_p - V_{\text{in}}^{\min} - \frac{I_L}{n}(2r + r_{\text{sc}}) \tag{6.37}$$

In the discharging configuration, when the supercapacitors are switched to the series arrangement as shown in Fig 6.7(b), each capacitor starts to discharge from $V_{\text{sc}}^{\max}$.

Similar to the previous case, considering a single capacitor from the array, the charge and discharge time for a supercapacitor are respectively given by,

$$t_{ch} = T_n \tag{6.38}$$

and

$$t_{\text{dch}} = \frac{T_n}{n} \tag{6.39}$$

The end-to-end efficiency improvement factor η_r with respect to a standard linear regulator is given by,

$$\eta_r = \frac{\eta}{\eta_{\text{std}}} = \frac{\dfrac{I_L V_{\text{reg}}}{\dfrac{I_L}{\left[1 + \dfrac{1}{n}\right]} V_p}}{\dfrac{I_L V_{\text{reg}}}{I_L V_p}} = 1 + \frac{1}{n} \tag{6.40}$$

Table 6.1 summarizes the characteristics of the basic configuration which satisfy $V_p > 2V_{\text{in}}^{\min}$ criterion using a single supercapacitor and the two general configurations which satisfy $V_p > 2V_{\text{in}}^{\min}$ and $V_p > 2V_{\text{in}}^{\min}$ criteria using an array of supercapaciotrs.

6.5 Practical Examples

The SCALDO technique can be easily configured for common DC-DC converters such as 12V-to-5V, 5V-to-3.3V and 5V-to-1.5 V and the technique provides efficiency improvement factors of 2, 1.33 and 3 respectively, compared with linear converters with the same input-output combinations [2–5, 10, 11]. For example, in a 5V-to-1.5V SCALDO regulator, using thin profile supercapacitors in the range of fractional farads to a few farads, this translates to an approximate end-to-end efficiency of nearly 90%. Table 6.2 indicates the efficiencies at each transfer stage, assuming that LDO is not abruptly disconnected. This table gives a clear overview of how this novel topology can assist with increasing the end-to-end efficiency of a linear regulator, with a view to getting the best out of linear-regulator-based DC-DC converters. Practical implementations of these topologies will be discussed in the next chapter. In the practical SCALDO implementations discussed in the next chapter, there is no direct discussion on protection strategies that can be applicable to the SCALDO prototypes. However, it is important to SCALDO based circuits to

Table 6.1: The parameters; n-number of supercapacitors, k- number of switches, V_{sc}^{max}- Max voltage across the supercapacitor, t_{ch}- Supercapacitor charge time t_{dch}- Supercapacitor discharge time and η_r- Efficiency improvement factor for the three different cases of SCALDO topologies

Param	$V_p > 2V_{in}^{min}$, Basic config	$V_p > 2V_{in}^{min}$ Gen. config	$V_p < 2V_{in}^{min}$ Gen. config
n	1	$n < \frac{V_p - V_{in}^{min}}{V_{in}^{min}}$	$n > \frac{V_{in}^{min}}{V_p - V_{in}^{min}}$
k	4	$3n+1$	$3n+1$
V_{sc}^{max}	$V_p - V_{in}^{min} - I_L(2r + r_{sc})$	$\frac{1}{n}\left[V_p - V_{in}^{min} - I_L\left[(n+1)r + nr_{sc}\right]\right]$	$V_p - V_{in}^{min} - \frac{I_L}{n}(2r + r_{sc})$
t_{ch}	T_1	$\frac{T_n}{n}$	T_n
t_{dch}	T_1	T_n	$\frac{T_n}{n}$
η_r	2	$1+n$	$1+\frac{1}{n}$

should consider the power supply protection aspects discussed in section 3.3 in the future stages of implementations.

6.6 Comparison between SCALDO Regulators and Charge Pumps

Supercapacitor-assisted low dropout regulators (SCALDO) were proposed as an alternative design approach to DC-DC converters, where a very low frequency supercapacitor circulation technique is combined with a commercial low dropout regulator IC to achieve significantly high end-to-end efficiency. In this technique the supercapacitor is used as a lossless voltage dropper, and the energy reuse occurs at very low frequencies such as from a few hertz to a few hundred hertz, eliminating any RFI/EMI issues. The efficiency advantage of this approach is very much closer to the efficiencies of practical switching regulators and also eliminates the utilization of bulky inductors. However, at the early stages of this project, there were some concerns raised that this patented technique is merely a variation of well-known switched-capacitor (charge pump) converters. This section is aimed at providing a broad overview of the capability of SCALDO technique, indicating its capabilities and limitations, and comparing the practical performance with a typical switched capacitor converter of similar current capability.

It is important to note that the SCALDO technique does not use supercapacitors for any DC-DC conversion purpose, as in the case of switched-capacitor type DC-DC

Table 6.2: Some useful parameters: number of capacitors, capacitor voltages and approximate efficiencies of SCALDO regulators at transfer times for a few useful converter requirements

Configuration	End- to end Regulation re uirement	LDO min. input voltage	Capacitor re uirements				Appro imate Efficiency at different stages of operation in discharging			Efficiency improvement factor		a theoretical efficiency of a standard regulator
			Number of Caps n	Voltage across a single cap in discharging V								
				a .	id	in	a Voltage	id Voltage	in Voltage			
$V_p < 2V_{in\ \min}$	5 -3.3 V	3.5	3	1.50	1.40	1.20	3		2	1 1/n	1.33	66
$V_p > 2V_{in\ \min}$	12-5 V	5.3	1	6.50	6. 00	5.30		3	3	2	2	42
$V_p > 2V_{in\ \min}$	5-1.5 V	1.6	2	1. 0	1.65	1.60		1	4	1 n	3	30

converters (charge pumps) such as voltage doublers, multipliers and inverters. Charge pumps utilize microfarad-order capacitors to achieve a voltage conversion using switching frequencies in the order of hundreds of kHz. The SCALDO technique utilizes the supercapacitor as a voltage dropper only, and the very small ESR in modern supercapacitors allows the capacitor losses in the series path to be minimised, well approximating a lossless voltage dropper. This SCALDO technique can be extended to provide high output currents in the order of 5 A - 50 A at DC rail voltages suitable for modern processors. Given the low leakage currents in new families of supercapacitors, usually within a range of 5 to about 50 μA [175, 223], compared to their high charge /discharge current capabilities in the range of tens to several hundred amperes, leakage current related losses are negligible. Also the supercapacitor is the best candidate for this new application, as the ESR values (in the range of fractional milliohm to less than 100 mΩ) are less than or comparable to $R_{\mathrm{DS(on)}}$ values of low voltage MOSFETs. Given that the new technique works in the range of fractional hertz to few 100 Hz order frequencies, and with the new supercapacitor families having very low leakage currents, dynamic losses will be significantly lower than a charge pump. Compared to linear or switching regulators, the output voltages of charge pump circuits are usually not regulated and are designed to operate at a fixed switching frequency of few 100 kHz with a rated output load current and voltage. Because of practical limitations on the size of capacitors and switches, applications of charge pumps are

limited mainly to low and medium power levels of several tens of milliwatts.

The following table provides capabilities and limitations of SCALDO technique comparing the practical performance with typical switched-capacitor converters.(This table shows the basic topological differences of the two approaches and is not a quantitative comparison of the two techniques.)

Table 6.3: A comparison summary of SCALDO technique and switched capacitor converters

SCALDO technique	Switched-capacitor techniques
A modified version of a linear regulator with an enormously large capacitor in the series path as a lossless voltage dropper. The capacitor and the switches do not convert the voltage.	Basically a high frequency switching technique for voltage conversion.
Always a step-down configuration	Practically used to step-up or invert a DC voltage.
Enormously large capacitance capacitors (supercapacitors) are used.	Capacitors used are in the range of a few nanofarads to a few tens of microfarads.
Operation frequency is variable and depends on the load current. Switching operation is based on the case of a maximum/minimum voltage detected across the input of the LDO.	Circuit design starts with a fixed oscillator supplying the switching frequency
Very low frequency (10Hz to few 100Hz) switching used for energy storage and reuse in capacitors.	Switching frequency is in the range of ten kilohertz to several hundred kilohertz.
Load always sees the precise output of a linear/low drop out regulator	Load regulation is not precise and requires a another voltage regulator (linear/low drop out type) for precise output voltage.
Capacitor never comes parallel to the input unregulated supply.	In one part of the cycle capacitor comes in parallel to the unregulated supply.
Technique is applicable to very large load currents. [High current capable LDO is required.]	Technique is suitable only for very low load currents.
Negligible minimum dynamic losses in switches.	Significantly high dynamic losses in switches.
Theoretically an efficiency multiplication factor is defined for a given configuration.	Theoretically a voltage conversion factor applies to a given configuration.

Given the above simple summary, it is very clear to see that the SCALDO technique is quite different to the operation of charge pumps, for three primary reasons:

1. SCALDO technique uses a capacitor as a lossless voltage dropper, together with a linear low dropout regulator for precise output regulation
2. Extremely low switching frequency is variable, and it depends on the load current. (In this technique, supercapacitor value is fixed and switching frequency varies with the load current. This is a characteristic behaviour of the SCALDO technique.)
3. If an ultra LDO can be developed for the required output current, there is no limit to precise output regulation at high load currents. [This is due to the availability

of single cell supercapacitors (commercially available) which are in the range of fractional farads to a few thousand farads.]

6.7 Chapter Summary

The Supercapacitor-assisted low dropout (SCALDO) regulator technique opens up a new approach to design DC-DC converters with very high end-to-end efficiencies. In this approach, one or more supercapacitors are used as series voltage droppers in combination with a commercial LDO IC. The supercapacitors are cycled at a very low frequency to release the stored energy to increase the end-to-end efficiency by a gearter-than-unity multiplication factor compared to that of a linear regulator circuit with the same input-output voltages. Generalised mathematical models and derivations of the SCALDO technique are detailed in this chapter. It is important to emphasis that the SCALDO technique is not a variation of well-known switched capacitor DC-DC converter.

The next chapter illustrates the implementation details of the SCALDO regulator technique for 5V-to-2V, 12V-to-5V and 5.5V-to-3.3V prototypes.

Chapter 7

Implementation Aspects of the SCALDO Regulator

7.1 5V-to-2V SCALDO Regulator

Fig. 7.1 shows the schematic implementation of the 5V-to-2V SCALDO regulator which satisfies the criteria, $V_p > 2V_{\text{in}}^{\min}$, in the form of its basic configuration, $n = 1$. This configuration was particularly chosen to show the compactness of the SCALDO technique. A compact prototype version designed utilising a single supercapacitor, is shown in Fig. 7.2.

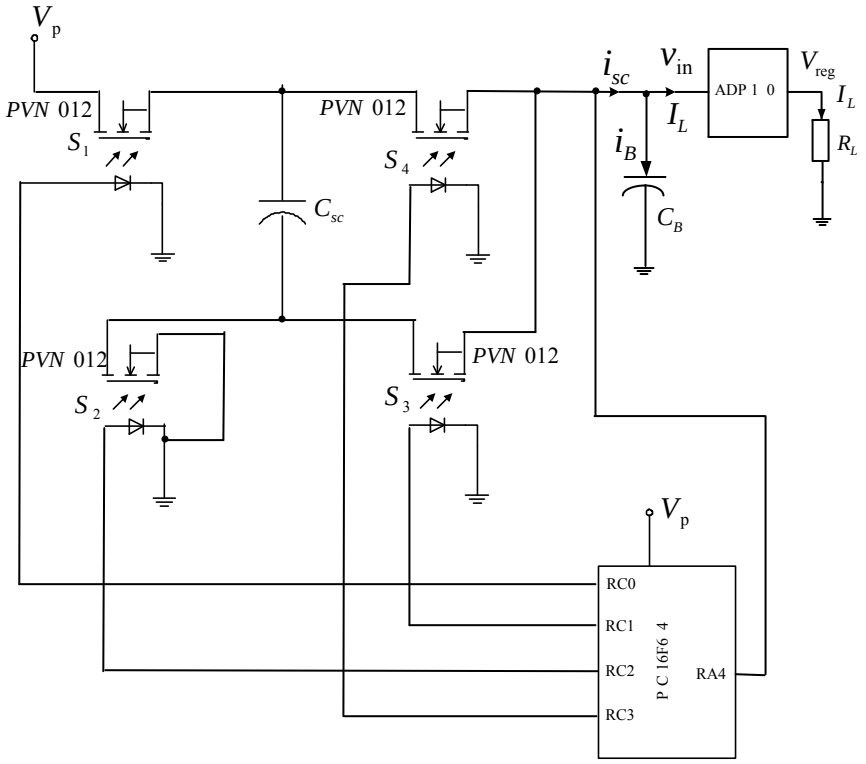


Figure 7.1: The schematic of the 5V-to-2V SCALDO regulator

In designing this prototype, LDO ADP1708 from Analog Devices, which has the specifications shown in Table 7.1, was used as the main Low Dropout regulator. For higher-efficiency LDO operation, an approximate LDO input voltage of 0.4 V above the regulated

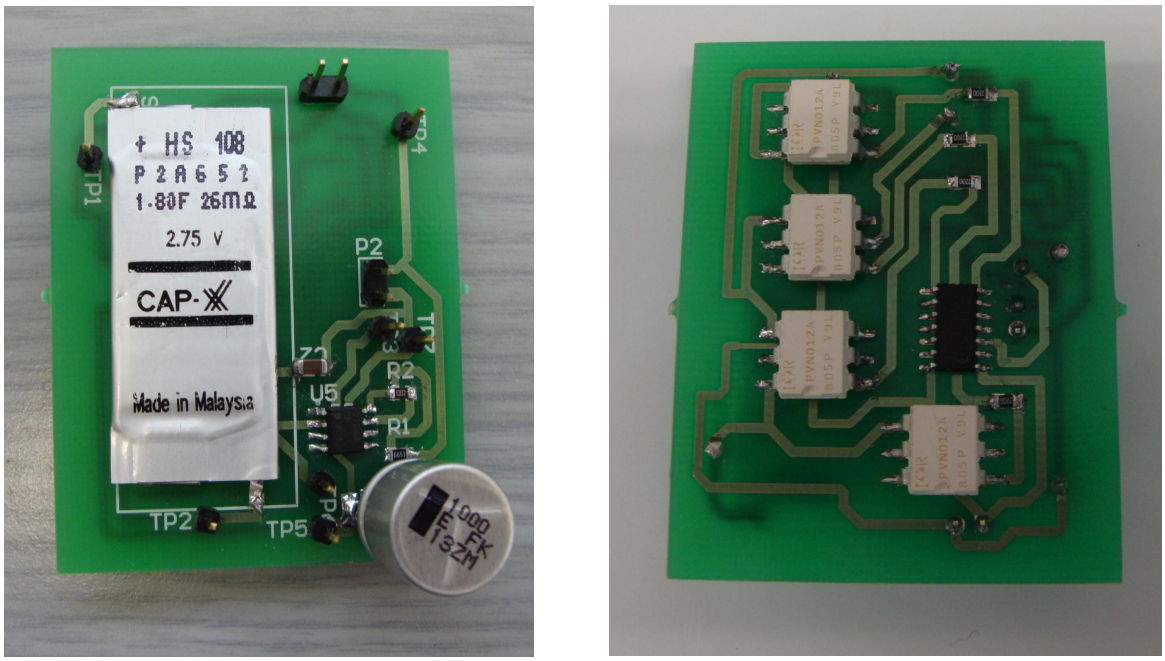


Figure 7.2: A compact version of 5V-to-2V SCALDO regulator

output voltage (2 V) was chosen, so that $V_{\text{in}}^{\text{min}}$ was maintained at 2.4 V. Since the input voltage from the unregulated power supply was around 5 V and the regulated output was 2 V, a single supercapacitor of 1.80 F/2.75 V of the type Cap-XX, was connected in series to maintain the required voltage level of the series dropper element.

Table 7.1: Important specifications of the LDOs used for the SCALDO prototypes

Specification	ADP1708	MCP1827
Maximum output current	1 A	1.5 A
Low dropout voltage	345 mV at 1 A load	330 mV at 1.5 A load
Adjustable output voltage range	0.8 V to 5.0 V	0.8 V to 5.0 V
Transient response	Excellent load/line transient response	Fast response to load transients
Stability	Stable with 4.7 μF ceramic output capacitor	Stable with 1.0 μF Ceramic output capacitor

Solid state relays of the type PVN012 from International Rectifier were used as S_1, S_2, S_3 and S_4 switches. Switches S_1 and S_3 control supercapacitor charging, while S_2 and S_4 control the discharge phase. Solid state relays were used in this proof-of-concept prototype to avoid complications arising from the body diode of common power MOSFETS. A PIC16F684 microcontroller from Microchip Technologies was used to drive the solid state relays. The S_1, S_2, S_3 and S_4 switches were controlled through the RC0, RC1, RC2 and RC3 port pins of the microcontroller respectively. As the unregulated power supply was around +5 V, it was connected to power the microcontroller directly. The LDO input voltage was monitored through the RA4 port pin. The voltage level at this pin is converted to digital format using 10-bit Analog to Digital converter (ADC) of the PIC which operates

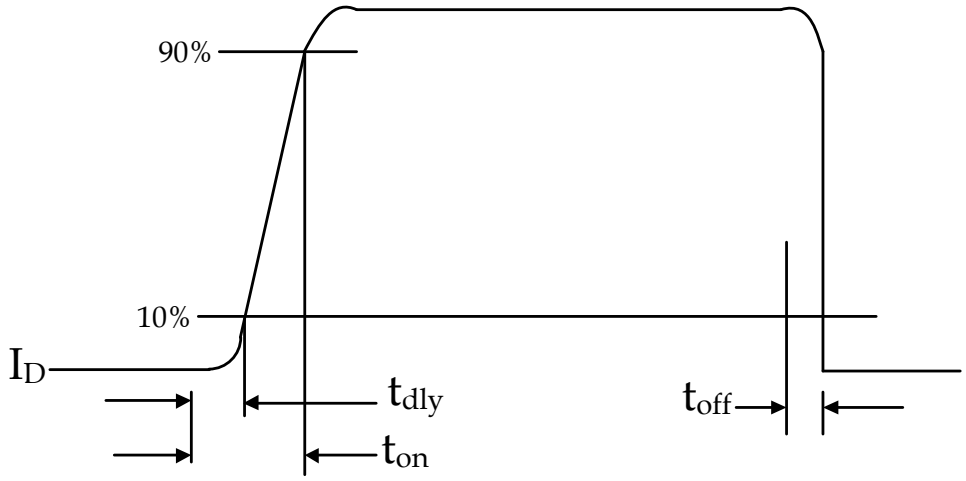


Figure 7.3: Delay characteristics of PVN012 switches

at a 4 MHz oscillation frequency. The result is then compared with reference point (digital value of the minimum LDO working voltage, $V_{\text{in}}^{\text{min}}$) and the switching between the supercapacitor charge and discharge phases was made accordingly. The microcontroller firmware was developed to drive the switches based on an algorithm shown in the flow chart in Fig. 7.4.

A switch-over period, t_{sw} was designed to accommodate any transition delays of the PVN012 switches. This creates a short time duration just before the circuit is transferred from the supercapacitor charge mode to the discharge mode. The time duration is set by the PIC micro-controller according to the switch delay. The time duration is determined according to the data sheet of the switch and typically is about 300 milliseconds. Figure 7.3 shows the delay characteristics of the PVN012 switch.

To keep the linear regulator powered during switch transitions, a buffer capacitor (C_B) of sufficient capacitance was connected in between the linear regulator input and the ground terminal. In t_{sw} time duration, the buffer capacitor is expected to discharge into the LDO input. The value of the buffer capacitor can be determined as shown in Eqn.(7.1) using the maximum load current capability of the LDO (I_L^{max}), switching time delays of a PVN012 switch (t_{sw}) and the minimum possible input voltage at the LDO input ($V_{\text{in}}^{\text{min}}$). A 1000-$\mu$F electrolytic capacitor was chosen as the buffer capacitor for the 5V-to-2V SCALDO design.

$$C_B = \frac{I_L^{\text{max}} t_{\text{sw}}}{V_{\text{in}}^{\text{min}}} \tag{7.1}$$

Figures 7.2 and 7.5 show two prototype versions of the 5V-to-2V SCALDO regulator. The schematics and the PCB layouts of these prototypes, designed using Altium Designer, are available in Appendix B. Appendix C shows the data sheet of the PVN012 solid

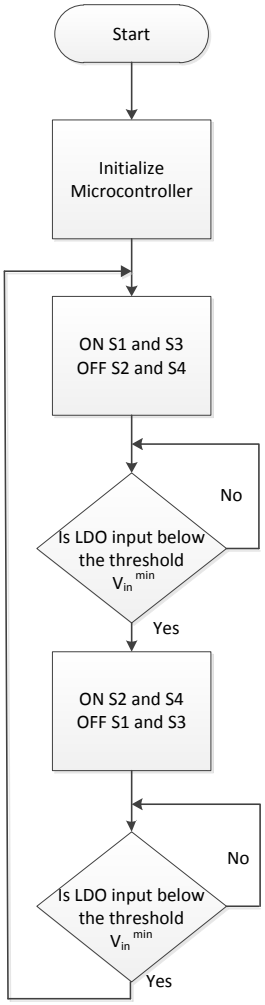


Figure 7.4: The flowchart of the PIC algorithm

state relay. The microcontroller firmware developed to drive the PVN012 switches is in Appendix D.

7.1.1 Load Regulation

Figure 7.6 shows the oscilloscope waveforms during the circuit operation for four values of load current between 100 to 500 mA for a fixed input supply voltage of 5 V. When the current flowing through the supercapcitor increases, the supercapacitor charge-discharge time period (time taken to meet the threshold voltage level) decreases. Therefore both the charging and discharging cycles of the supercapacitor become shorter. As a result, the switch operating frequency increased from 0.08 to 1.35 Hz, as shown in Table 7.2. In the Fig. 7.6 oscillographs, the green (1), purple (2), blue (3) and orange (4) traces represent the LDO output voltage (V_{reg}), the voltage across the supercapacitor (V_{SC}), the input voltage of the LDO (V_{in}) and the input current of the system (I_{in}) respectively.

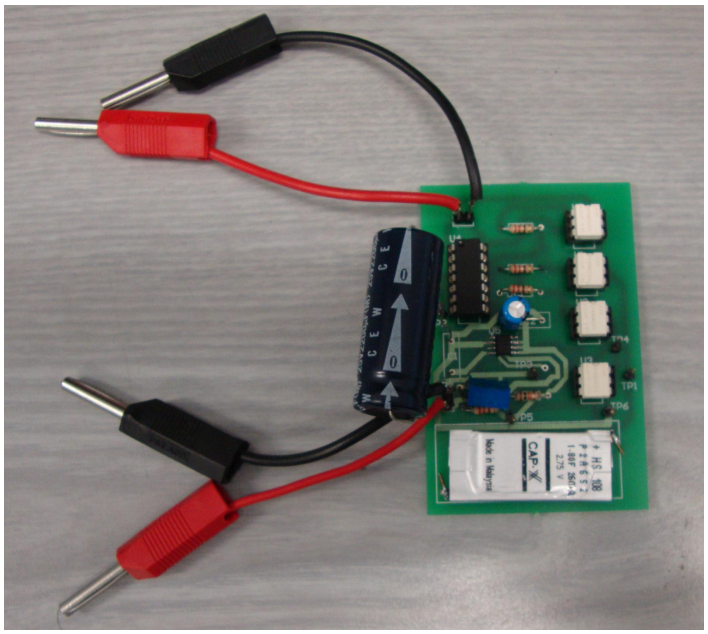


Figure 7.5: The prototype of the 5V-to-2V SCALDO regulator

The purple trace (2), V_{SC}, clearly shows the supercapacitor charge-discharge cycles during the circuit operation. The blue trace (3), illustrates how the LDO input voltage changes during the charge-discharge cycles. The waveform of I_{in} (4), shows the current drawn from the unregulated power supply during the charge-discharge cycles. This clearly shows that the circuit draws a considerable current only in the charging phase of the supercapcitor. In the discharging phase only a little current is drawn for the control circuits to function. This I_{in} was measured by connecting a resistor of 0.1 Ω in series with the unregulated power supply and the input terminal of the circuit.

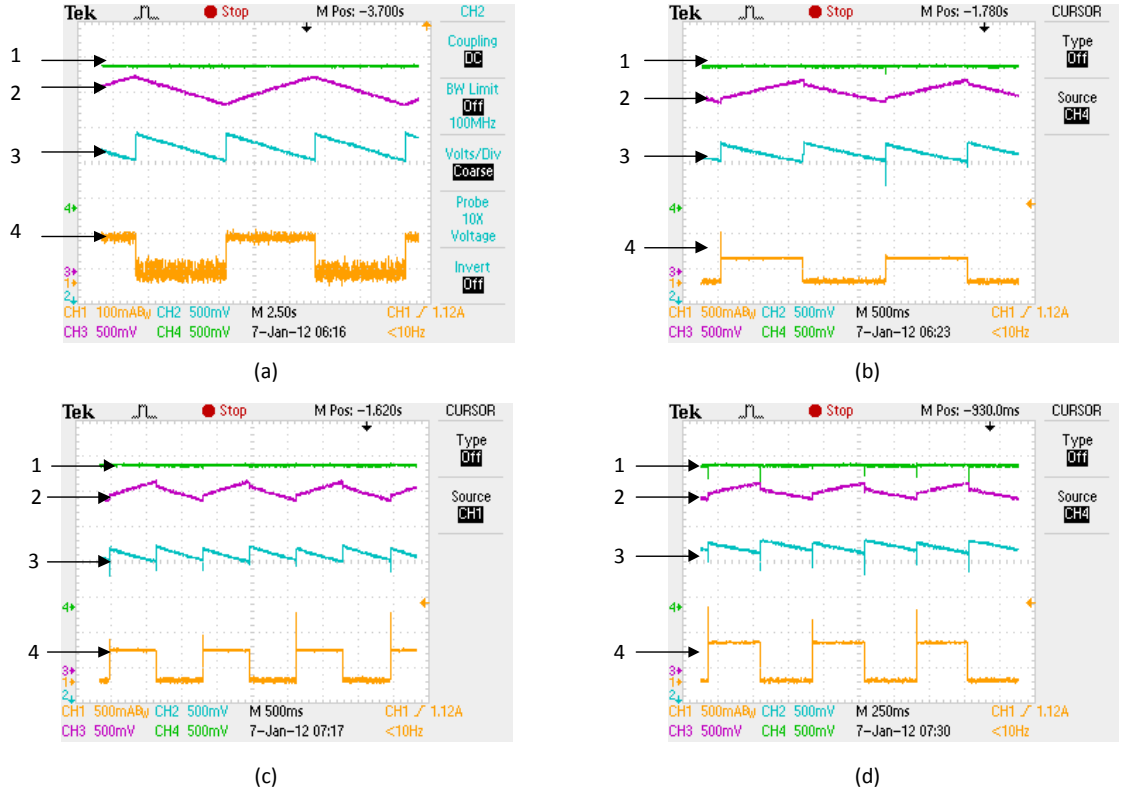
In these SCALDO prototypes, the control circuit current was not set at a minimum value due to the time constraints and the limited budget. Therefore, in the calculations the control circuit current is not considered. More details on further improvements to reduce the control circuit current will be discussed in the Chapter 10.

In the following calculations, assume that V_p, I_{in}, V_{reg}, I_L and I_c are the input voltage of the unregulated power supply, the current drawn from the unregulated power supply, the output voltage, the output current and the control circuit current of the SCALDO regulator respectively. Neglecting the control circuit current, the average current drawn from the unregulated power supply during a supercapacitor charge-discharge cycle is,

$$I_{\text{avg}} = \frac{[I_{\text{in}} - I_c]}{2} \tag{7.2}$$

The overall end-to-end efficiency of SCALDO cycle can be estimated as,

$$\eta = \frac{V_{\text{reg}} I_L}{V_p I_{\text{avg}}} 100\% \tag{7.3}$$



1 LDO output voltage
2 Voltage across the supercapacitor
3 Input voltage of the LDO
4 Input current drawn from the unregulated power supply

Figure 7.6: Oscilloscope waveforms of 5V-to-2V SCALDO regulator for load currents of (a) 200 mA (b) 300 mA (c) 400 mA (d) 500 mA

Table 7.2 represents the experimental results and the end-to-end efficiencies (ETEE) of the 5V-to-2V SCALDO regulator which were estimated using Eqns. (7.2) and (7.3). According to Table 7.2, this regulator has a maximum load regulation variation of about 0.02%/mA. Figure 7.7 shows the load regulation plot based on the above experimental results.

7.1.2 Line Regulation

When the input voltage increases, the operating frequency of the switches decreases. The reason is, when the difference between the unregulated input voltage and the threshold voltage level at the input of the LDO increases, the amount of energy stored in the supercapacitor also increases. Therefore, both the charge and the discharge cycles of the supercapacitor take longer and this results in a lower operating frequency of the switches

Table 7.2: The Load Regulation experimental results of 5V-to-2V SCALDO regulator

Load current (mA)	Output voltage (V)	Supercapacitor charging time (ms)	Supercapacitor discharging time (ms)	Input current (mA)	Control circuit current (mA)	Circulation frequency (Hz)	Efficiency with negligible control current%
100	2.02	6.4	6.4	138	36	0.08	79.2
200	2.0	2.20	2.2	245	40	0.23	78.0
300	2.0	1.18	1.18	350	40	0.42	77.4
400	2.0	0.68	0.68	455	40	0.74	77.1
500	2.0	0.37	0.37	560	40	1.35	76.9

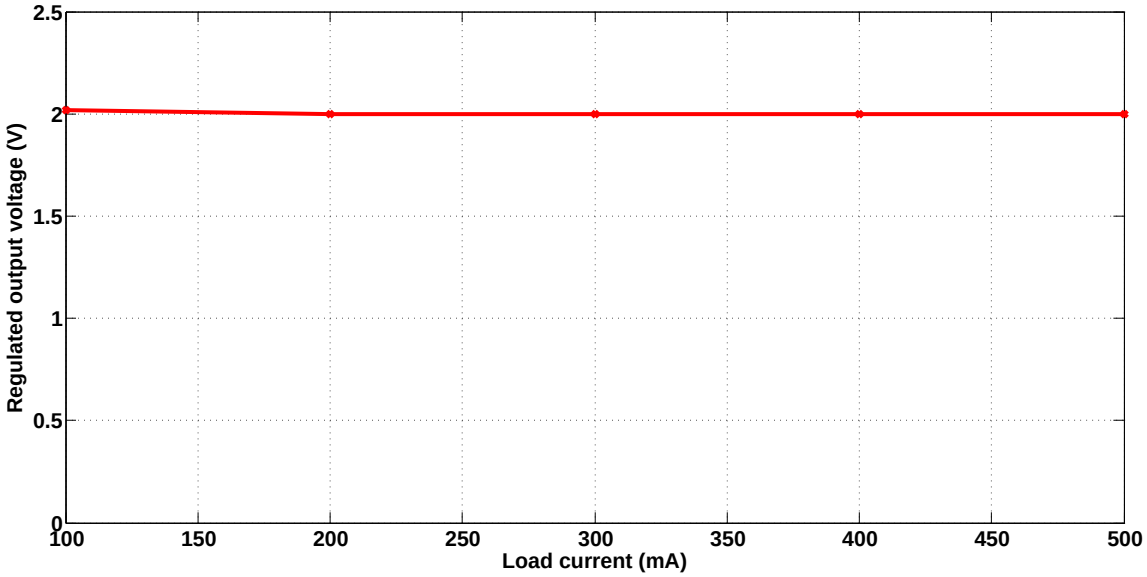


Figure 7.7: The load regulation plot of the 5V-to-2V SCALDO regulator at an input voltage of 5 V

as shown in Table 7.3. Figure 7.8 indicates the oscilloscope waveforms during the circuit operation, for input voltages ranging from 4.6 V to 5.6 V in steps of 0.2 V. The load current is maintained at 200 mA at these stages. In Fig. 7.20 the purple (1), blue (2), green (3) and orange (4) traces represent the voltage across the supercapacitor (V_{SC}), the input voltage of the LDO (V_{in}), the LDO output voltage (V_{reg}) and the input current of the system (I_{in}) respectively.

Table 7.3 represents the experimental values of the line regulation of the 5V-to-2V SCALDO regulator and Fig. 7.9 depicts the corresponding line regulation plot. According to the results in Table 7.3 there was not significantly visible variations in output voltage to the input voltage variations. As with load regulation calculations, the control circuit current was neglected in the efficiency calculations and efficiency estimations were carried out according to Eqn. (7.2) and (7.3).

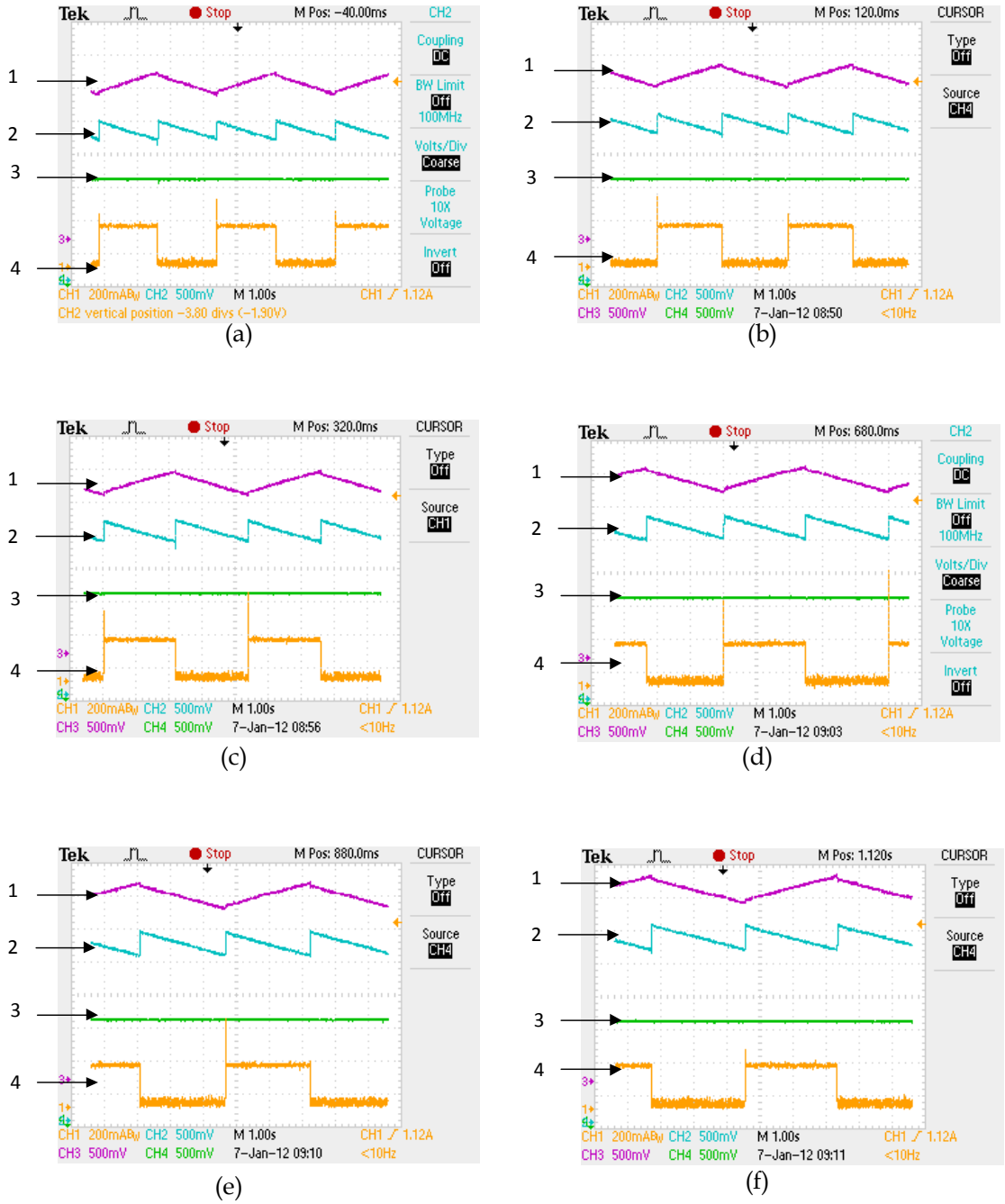
Table 7.3: The line regulation experimental results of 5V-to-2V SCALDO regulator at a load current of 200 mA

Input voltage (V)	Output voltage (V)	Supercapacitor charging time (ms)	Supercapacitor discharging time (ms)	Input current (mA)	Control circuit current (mA)	Circulation frequency (Hz)	Efficiency with negligible control current%
4.4	1.92	1760	1760	240	24	0.284	80.8
4.6	1.94	1800	1800	248	32	0.278	78.1
4.8	1.96	1960	1960	264	32	0.255	70.4
5.0	1.96	2200	2200	256	32	0.227	70.0
5.2	1.96	2480	2480	264	40	0.202	67.3
5.4	1.96	2560	2560	272	40	0.195	62.6
5.6	1.96	2760	2760	280	40	0.181	58.3

7.1.3 End-to-End Efficiency (ETEE)

According to the load regulation experimental results, the end-to-end efficiencies were calculated as shown in Table 7.2. The corresponding efficiency plotted against load current is shown in Fig. 7.10. The prototype achieves overall end-to-end efficiencies in the range of 77 to 79%, compared to the maximum theoretical efficiency 40% for a 5V-to-2V linear regulator. The results indicate a 1.6 to 3.8% difference between the theoretical and measured end-to-end efficiencies of the SCALDO design.

Using the line regulation data in Table 7.3, efficiency plotted against the input voltage was drawn as in Fig. 7.11. This figure shows a comparison of theoretical performance of



1 Voltage across the supercapacitor

2 Input voltage of the LDO

3 LDO output voltage

4 Input current drawn from the unregulated power supply

Figure 7.8: The oscilloscope waveforms of 5V-to-2V SCALDO regulator for an input voltage of (a) 4.6 V (b) 4.8 V (c) 5.0 V (d) 5.2 V (e) 5.4 V (f) 5.6 V at a load current of 200 mA

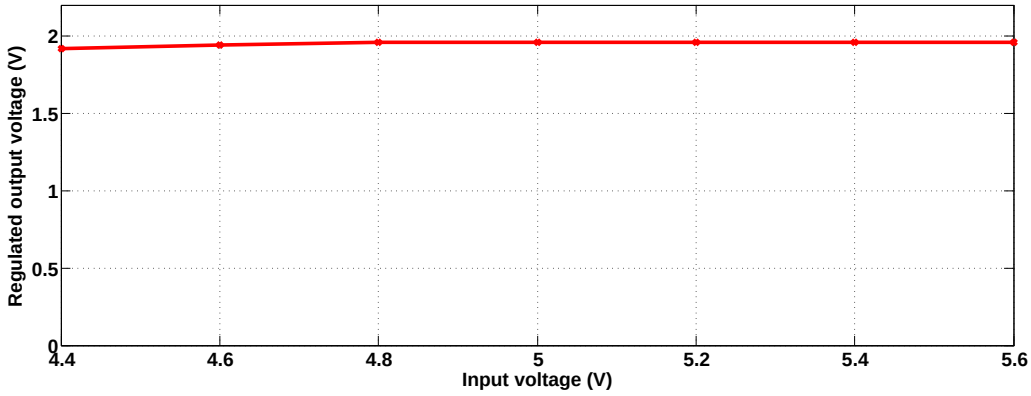


Figure 7.9: Line regulation experimental results of 5V-to-2V SCALDO regulator at a load current of 200 mA

SCALDO technique (upper trace), practical performance of SCALDO technique (middle trace) and performance of standard linear regulator (lower trace) for a 5V-to-2V regulator. The prototype achieves overall end-to-end efficiencies in the range of 58 to 81%, compared to the maximum theoretical efficiencies in the range 35 to 44% for a 5V-to-2V linear regulator.

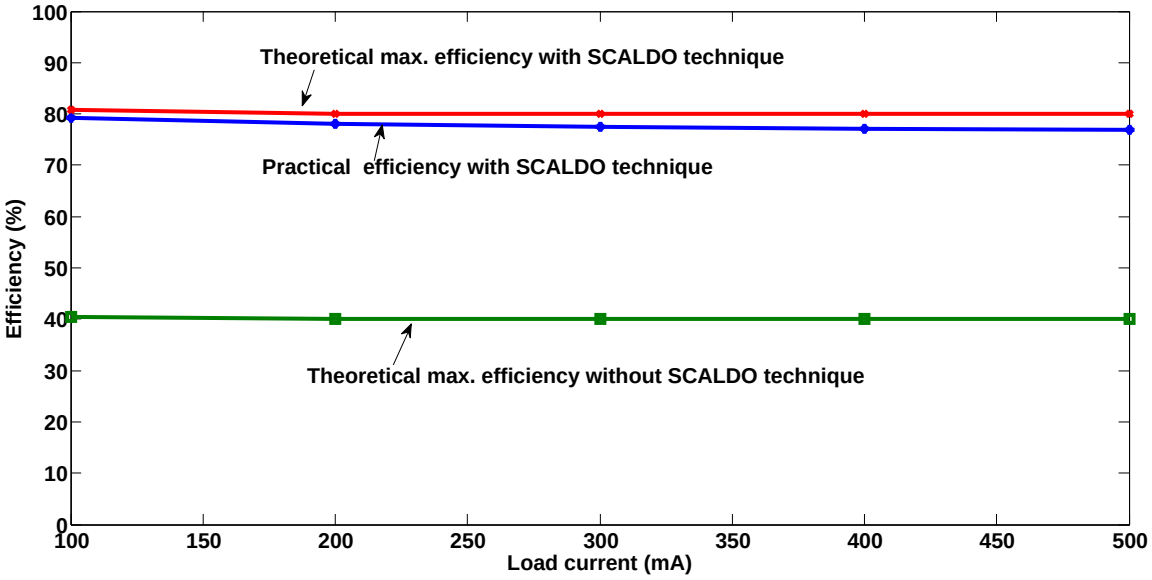


Figure 7.10: Efficiency vs Load current of the 5V-to-2V SCALDO regulator at an input voltage of 5 V: Theoretical results with SCALDO technique (upper trace), practical results with SCALDO technique (middle trace) and basic 5V-2V linear regulator theoretical performance (lower trace)

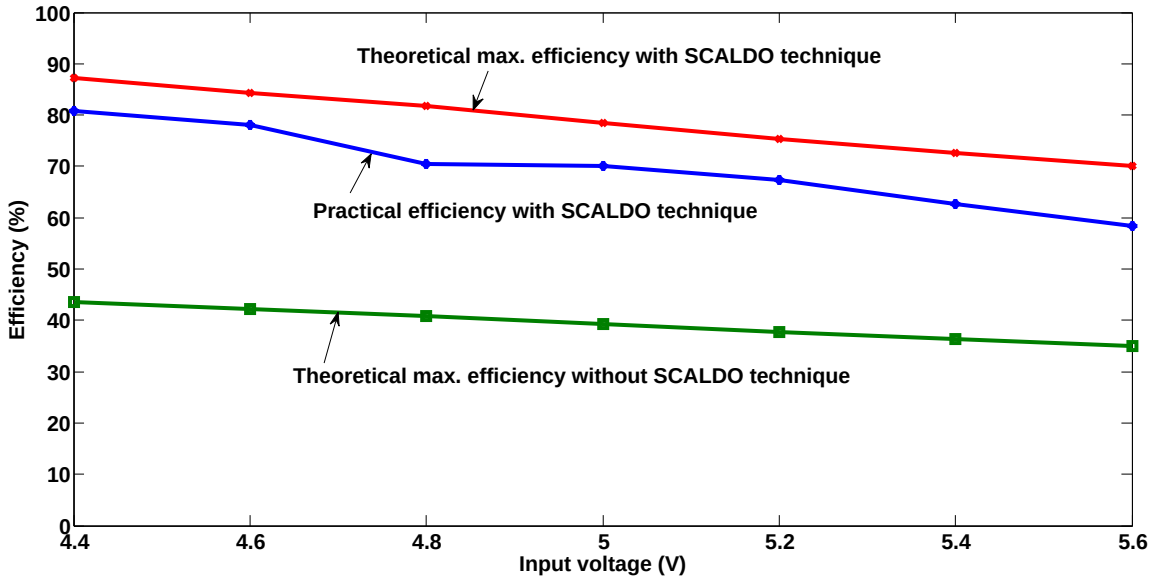


Figure 7.11: Efficiency vs Input voltage comparison for a 5V-to-2V regulator: Theoretical results with SCALDO technique (upper trace), practical results with SCALDO technique (middle trace) and basic 5V-2V linear regulator theoretical performance (lower trace) at a load current of 200 mA

7.1.4 Load Transient Response

Output Current Slew Rate of DC Power Supplies

A well-regulated power supply is critical for proper operation and reliability of modern high-speed microprocessors. They require fast delivery of large currents in a smaller time, tight supply-voltage tolerance, and intelligent voltage programming. This voltage regulation must be as tight as $\pm$ 5% and this tolerance is the resultant of DC set point accuracy, accuracy over temperature and input voltage variations, and transient response. Even if a processor voltage is being temporarily too high or too low can cause problems with the end operation of the processor. In achieving such rigorous voltage requirements the total performance of the power supply including the accuracy of the output voltage in a steady state condition and the transient response are vital [224]. The typical CPU voltage-regulator specifications from Intel and AMD call for load-current slew rates of 50 to 200 A/μs and peak currents of 60 A to more than 120 A [225].

There is an increasing demand for point-of-load (POL) converters that maintain good regulation in the presence of fast varying load transients (di/dt). A POL converter that is capable of handling transients up to 300 A/μs has recently been introduced. This level of performance presents new challenges to engineers during the converter design, and also

during the test and verification stages of product development. The combination of high-frequency converter operation and fast load transients demands stringent design practices and a thorough understanding of every element of the design and test setup [226].

In modern microprocessor-based systems, the operation at low voltages, GHz clock frequencies, high power, and the ability to survive fast current transients requires a new generation of voltage regulator modules (VRMs). Transient response is one of the most important specifications for a VRM and this requires special test gear to measure. A VRM must maintain regulation under high transition rate loading, so it is crucial to generate a fast load pulse or single transition to verify the voltage transient levels and transient response time under specified loading. As with traditional power supplies, different loading patterns can cause significant differences in transient response time and voltage level. Therefore, an electronic load that simulates fast load changes is necessary to verify the transient response of a VRM. In order to verify the transient response, measurements of the rise and fall times upon a step change in the load are necessary. Generally, this type of test requires a load that is able to produce a rise and fall time approximately five times faster than the power supply [227].

TEXIO PXL - 151A DC Electronic Load

DC Electronic loads are one such instrument that can support testing power supplies for various settings, configurations and methodologies.

Figure 7.12: TEXIO PXL-151A Electronic load

The PXL-151A Electronic Load provides 150 A of static, DC load with 150 A of dynamic load, featuring up to 100 A/μs slew rate. This electronic load has two input

current ranges: 0 to 37.5 A and 0 to 150 A. It has equipped with several discharging modes,

1. constant current (CC)
2. constant resistance (CR)
3. constant power (CP)
4. constant voltage (CV)

Table 7.4 illustrates some important specifications of TEXIO PXL-151A electronic load.

Table 7.4: Important specifications of TEXIO PXL-151A electronic load

Input Rating

Input Power	150 A range 37.5 A range	0 to 300 W 0 to 75 W
Input Voltage Range	CC, CP CR CV	0.3 to 30 V 0 to 30 V 0.8 to 30 V
Input Current Range	150 Range 37.5 A range	0 to 150 A 0 to 37.5 A

Short Mode

CC discharging mode	150 A range 37.5 A range	150 A 37.5 A
CR discharging mode	150 A range 37.5 A range	2 mΩ 8 mΩ

Switching Mode

Operating Mode		CC, CR, CP, CV
Frequency	Range Accuracy Resolution	1 to 50 kHz ± 1.5% of setting 0.1 Hz, 1 Hz, 10 Hz, 100 Hz

Slew Rate

Selectable discharging mode		CC, CR, CP
150 Range	Range Resolution	1 to 100 A/μs 0.5 A/μs
37.5 A Range	Range Resolution	0.25 to 25 A/μs 0.25 A/μs
Setting Accuracy		Typical value at 4 V input
Min. response time		500 ns

Load Transient Response of 5V-to-2V SCALDO Regulator

When the switching operation mode is enabled, the TEXIO electronic load is capable of generating current steps. A well-defined current waveform generated by the DC electronic load is shown in Fig. 7.13 and has 100 A/μs of maximum slew rate capability. Before

activating the switch operation, the values of PRESET A and B and the slew rates of the signal in both the rising and the falling edges can be set separately. There are two ways of setting the switch operation of the load as either switching frequency (1 Hz to 250 kHz) or duty ratio (1% to 99%).

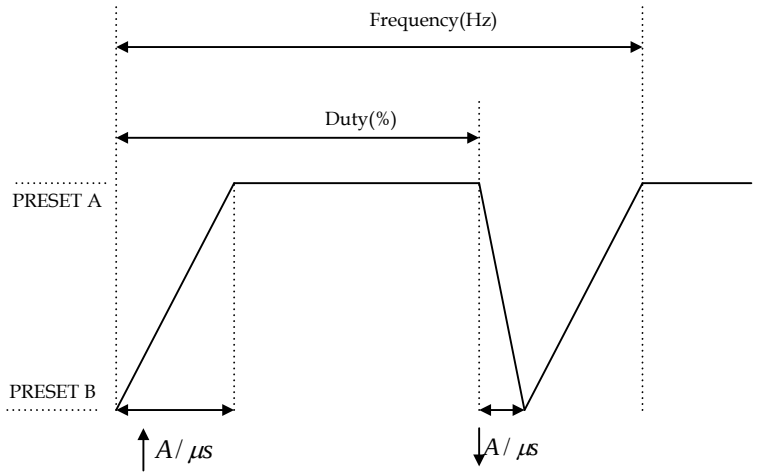


Figure 7.13: Typical current step of the TEXIO PXL-151A DC electronic load

Once the switch load current was set at the TEXIO DC load, it was connected to the SCALDO prototype and corresponding changes in the output voltage were observed from the Tektronix digital oscilloscope. For better observation of the variations, the AC coupling mode of the oscilloscope was enabled. For a given slew rate in the rising and falling edges of the load, corresponding output voltage variations were recorded in terms of transient voltage ripple and transient time. The experimental set-up used for the transient measurement is shown in Fig. 7.14 and the oscilloscope figures of these measurements are shown in Fig. 7.15. In these scope outputs the green (1) trace represents the current step and the blue (2) trace represents the corresponding voltage variation at the transitions. For a given slew rate, in the rising and falling edges of the load, the subsequent output voltage variations shown in Table 7.5 were recorded in terms of transient voltage ripple and transient time.

Table 7.5: Transient response measurements of 5V-to-2V SCALDO regulator

Slew rate (A/μs)	Ripple voltage (rising edge) (mV)	Transient time (rising edge) (ms)	Ripple voltage (falling edge) (mV)	Transient time (falling edge)(ms)
1	14.4	14.0	11.2	16.0
5	16.8	12.0	12.8	15.0
10	15.2	12.8	12.8	11.6
25	14.4	14.0	15.2	13.0

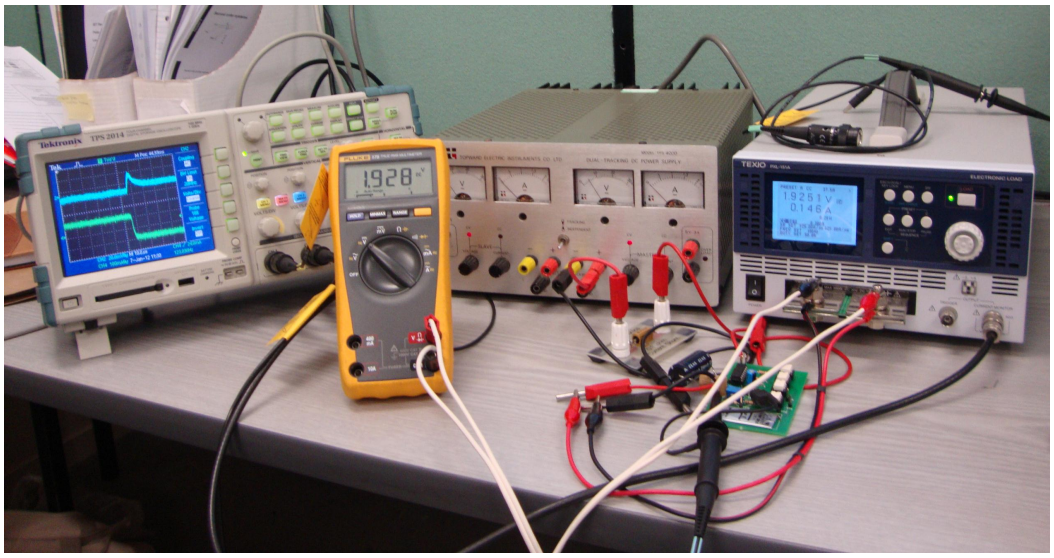


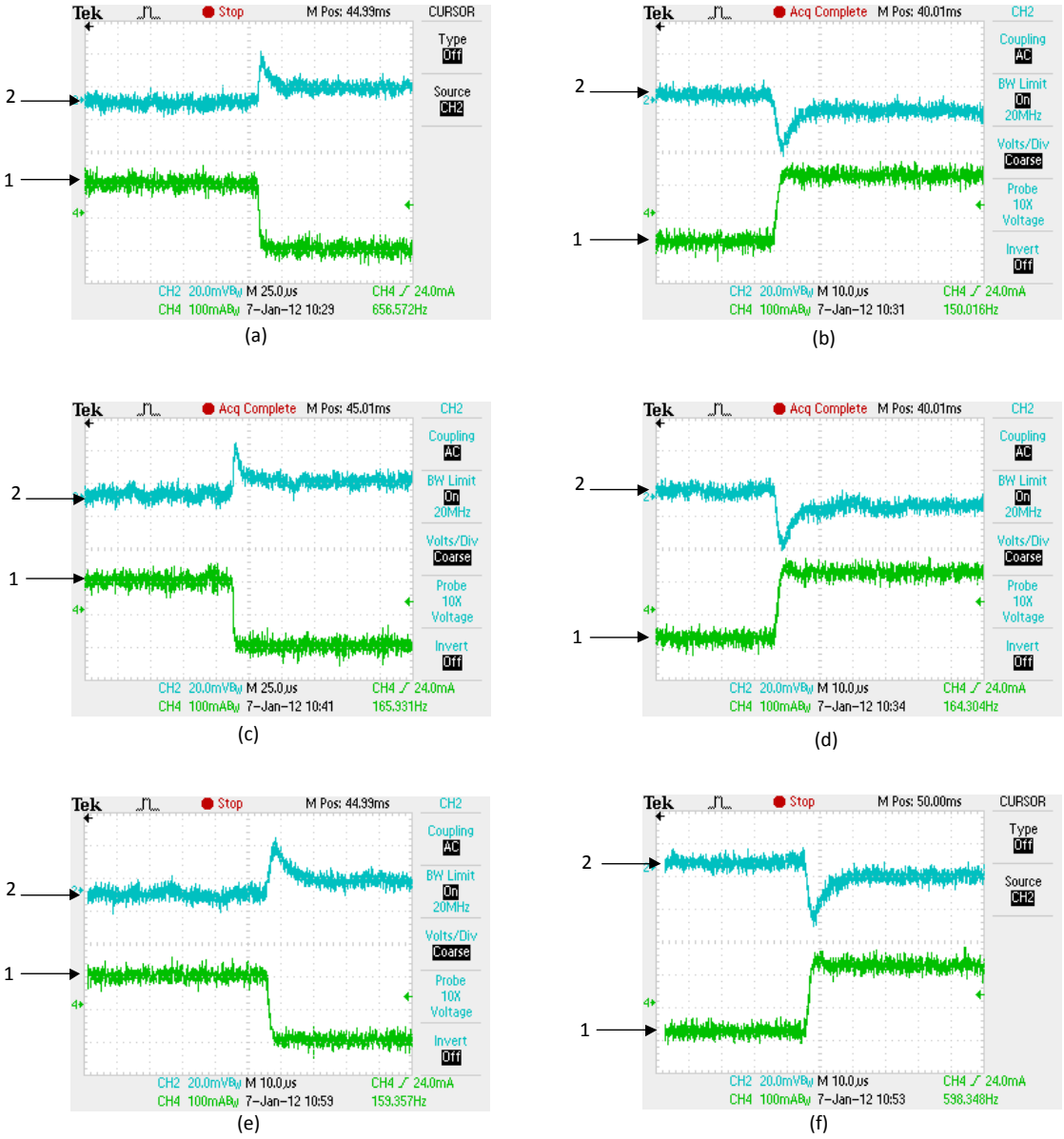
Figure 7.14: Transient measurement set up of the 5V-to-2V SCALDO regulator using TEXIO DC electronic load

7.2 12V-to-5V SCALDO Regulator

Fig. 7.16 shows the schematic implementation of the 12V-to-5V SCALDO regulator. This configuration is another applicable version of $V_p > 2V_{\text{in}}^{\text{min}}$ criteria. An LDO of the type MCP1827 from Microchip Technology (important specifications are shown in Table 7.1) was used as the main LDO and $V_{\text{in}}^{\text{min}}$ was maintained at 5.4 V. As the power supply input voltage was around 12 V and the regulated output is 5 V, three supercapacitors of 4 F/2.5 V of the type PC-series from Maxwell Technologies, were connected in series to maintain the required voltage level of the series dropper element. This resulted in 1.33 F/7.5 V capacitor as the series capacitor.

To keep the linear regulator powered during the transitions, a 4700 μF electrolytic capacitor was connected between the LDO input terminal and the ground terminal. The same type of PVN012 photovoltaic relay was used as S_1, S_2, S_3 and S_4 switches. PIC16F684 microcontroller based on the same algorithm was utilised as the controller to drive the photovoltaic switches and an independent 5 V regulator (LM7805) was connected to power the microcontroller.

Fig. 7.17 shows a prototype 12V-to-5V SCALDO regulator. The schematic and the PCB layout of the prototype, designed using Altium Designer, are shown in Appendix B. The microcontroller firmware was developed to drive the switches based on similar algorithm shown in the flow chart in Fig. 7.4.



1 Transient load current

2 Change of output volatge

Figure 7.15: Transients measurements of 5V-to-2V SCALDO (a) 1 A/μs falling edge (b) 1 A/μs rising edge (c) 10 A/μs falling edge (d) 10 A/μs rising edge (e) 25 A/μs falling edge (f) 25 A/μs rising edge

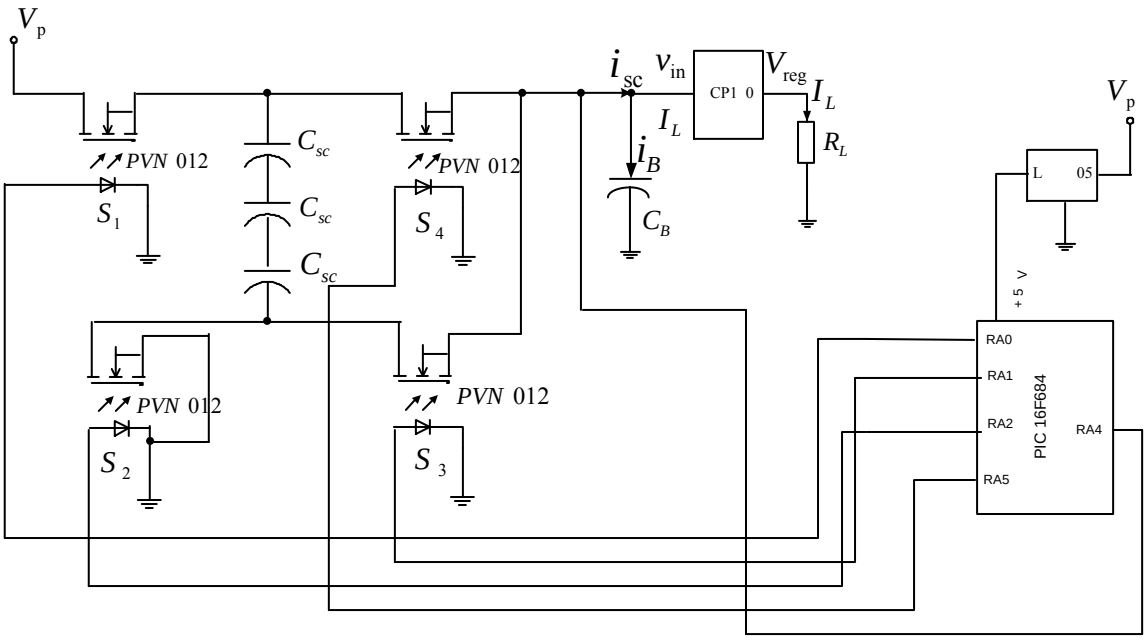


Figure 7.16: The schematic of the 12V-to-5V SCALDO regulator designed using MCP1827 LDO, 4F/2.5 V Maxwell supercapacitors, optically coupled switches (PVN012 photovoltaic switches), PIC 16F684 microcontroller and LM7805 regulator

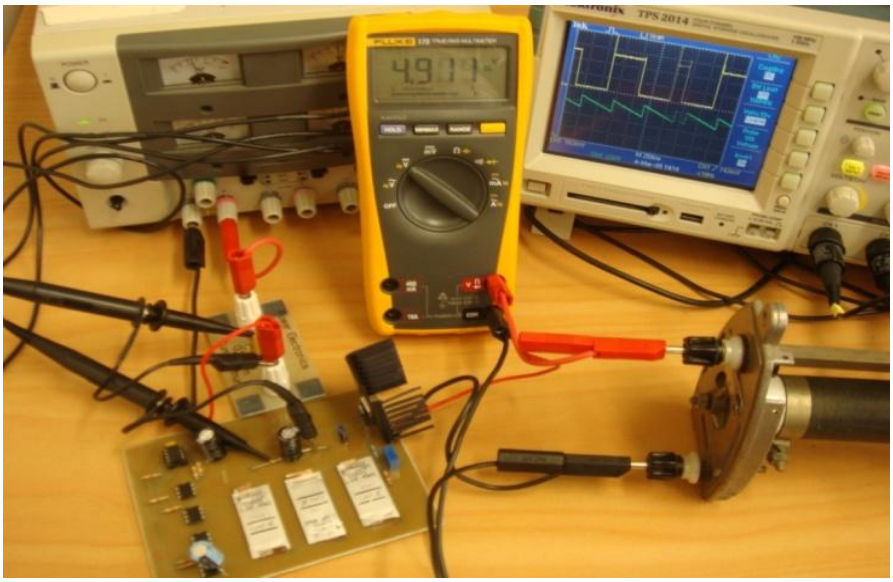
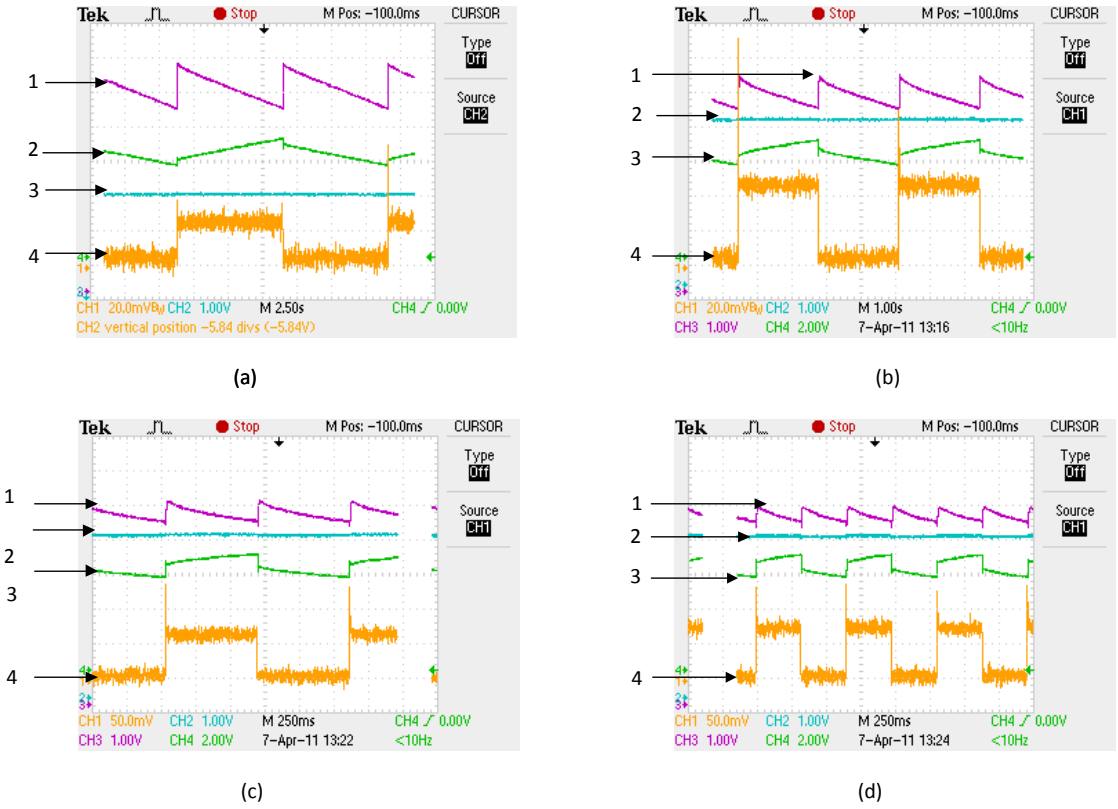


Figure 7.17: Prototype 12V-to-5V SCALDO regulator

7.2.1 Load Regulation

Fig. 7.18 (a) to (d) indicate the oscilloscope waveforms during circuit operation for load currents of 200, 400, 600 and 800 mA respectively. In Fig. 7.18 purple (1), green (2), blue (3) and orange (4) traces represent the input voltage of the LDO (V_{in}), the voltage across one of the three supercapacitors (V_{SC}), the LDO output voltage (V_{reg}) and the input current drawn from the unregulated power supply (I_{in}) respectively. As with 5V-to-2V prototype, the ETEE efficiencies of the 12V-to-5V prototype were calculated using Eqn. (7.2) and (7.3).



1 Input voltage of the LDO

2 Voltage across one of the three supercapacitors

3 LDO output voltage

4 Input current drawn from the unregulated power supply

Figure 7.18: Oscilloscope waveforms of 12V-to-5V SCALDO regulator for load currents of (a) 200 mA (b) 500 mA (c) 800 mA (d) 600 mA at an input voltage of 12 V

Table 7.6 represents the experimental results and the end-to-end efficiency (ETEE) results of the 12V-to-5V SCALDO regulator. As shown in this table, the circulation frequency increases 0.05 to 4 Hz with increase of the load current to 100 to 800 mA

respectively. Fig. 7.19 shows the load regulation plot based on the above experimental results and load regulation is about 0.04%/mA.

Table 7.6: The load regulation experimental results of 12V-to-5V SCALDO regulator at an input voltage of 12 V

Load current (mA)	Output voltage (V)	Supercapacitor charging time (ms)	Supercapacitor discharging time (ms)	Input current (mA)	Control circuit current (mA)	Circulation frequency (Hz)	Efficiency with negligible control current%
100	4.96	10.45	10.45	160	60	0.05	82.7
200	4.88	5.5	5.5	266	64	0.09	80.5
300	4.84	3.15	3.15	370	64	0.16	79.1
400	4.80	1.85	1.85	472	64	0.27	78.8
500	4.76	0.95	0.95	568	64	0.53	78.7
600	4.72	0.46	0.46	660	60	1.09	78.1
700	4.68	0.25	0.25	760	60	2.00	77.4
800	4.64	0.12	0.12	860	60	4.17	76.3

7.2.2 Line Regulation

Fig. 7.20 (a) to (d) indicate the oscilloscope waveforms during circuit operation for input voltages of 13.5, 13, 12 and 11.5 V respectively. The load current is maintained at 250 mA. In Fig. 7.20, the purple (1), green (2), blue (3) and orange (4) traces represent the input voltage of the LDO (V_{in}), the voltage across one of the three supercapacitors (V_{SC}), the LDO output voltage (V_{reg}) and the input current of the system (I_{in}) respectively. Table 7.7 represents the experimental values of the line regulation of the 12V-to-5V SCALDO regulator. Furthermore, as the input voltage increases the circulation frequency decreased from 2.17 to 0.014 Hz as shown in table. Figure 7.21 depicts the corresponding line regulation plot. There were not significant variations in the output voltage in the line regulation experimental results.

7.2.3 End-to-End Efficiency (ETEE)

According to the load regulation experiment results, the end-to-end efficiencies were calculated as shown in Table 7.6. The corresponding efficiency plotted against load current is shown in Fig. 7.22. The middle trace shows the improved efficiency in the new SCALDO implementation. These results shows an experimental efficiencies in the range of 77 to

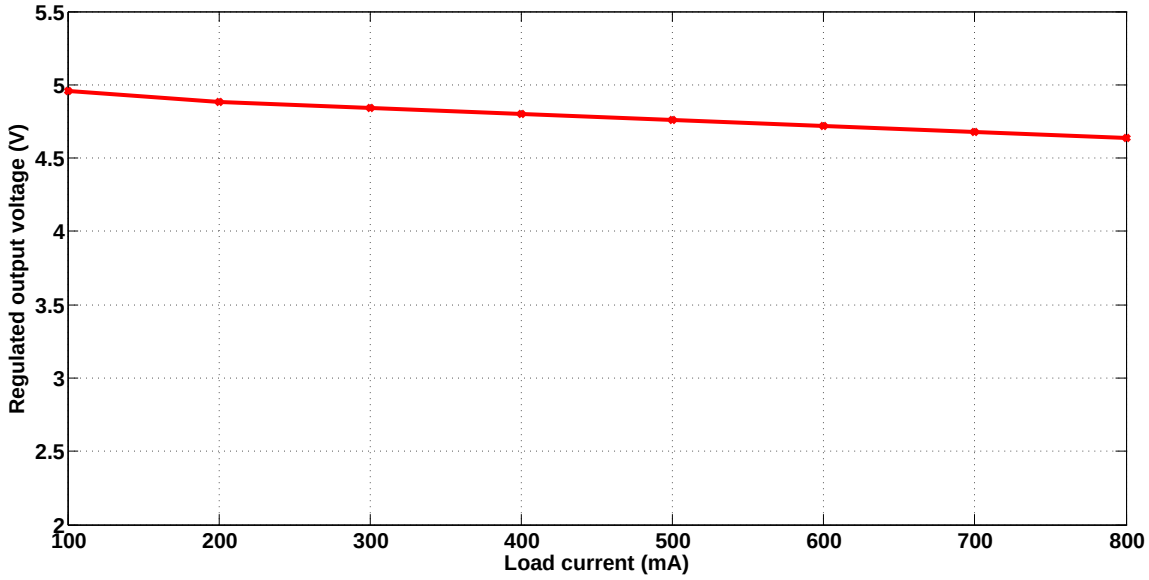
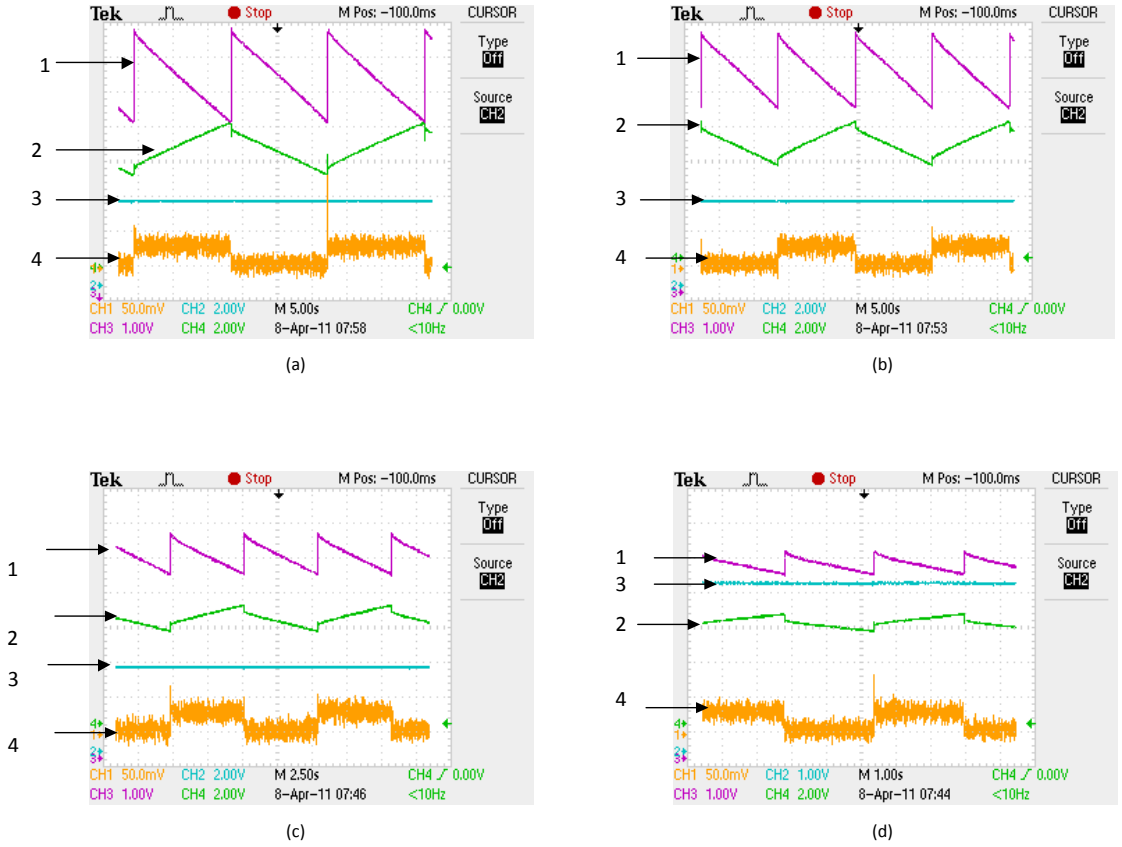


Figure 7.19: The load regulation plot of the 12V-to-5V SCALDO regulator at an input voltage of 12 V

Table 7.7: The line regulation experimental results of 12V-to-5V SCALDO regulator at a load current of 250 mA

Input voltage (V)	Output voltage (V)	Supercapacitor charging time (ms)	Supercapacitor discharging time (ms)	Input current (mA)	Control circuit current (mA)	Circulation frequency (Hz)	Efficiency with negligible control current%
11	4.84	0.72	0.72	320	60	2.78	84.6
11.5	4.88	2.6	2.6	320	60	0.77	81.6
12	4.88	5.3	5.3	320	60	0.38	78.2
12.5	4.88	8.3	8.3	320	60	0.24	75.1
13	4.88	11.2	11.2	320	60	0.18	72.2
13.5	4.88	14	14	320	60	0.14	69.5



1	Input voltage of the LDO
2	Voltage across one of the three supercapacitors
3	LDO output voltage
4	Input current drawn from the unregulated power supply

Figure 7.20: Oscilloscope waveforms of the 12V-to-5V SCALDO regulator for input voltages of (a) 13.5 V (b) 13 V (c) 12 V (d) 11.5 V at a load current of 250 mA

83%. The discrepancy between the maximum theoretical efficiency and the experimental efficiency is less than 1.6%.

Using the line regulation data in Table 7.7, efficiency plotted against the input voltage was drawn as in Fig. 7.23. The 12V-to-5V SCALDO prototype achieves overall end-to-end efficiencies in the range of 70 to 85%, compared to the maximum theoretical efficiency of 44% for a conventional linear regulator used for the same input-output combination. The middle trace of Fig. 7.23 shows the improved efficiency in the new SCALDO implementation. The graphs indicate a 2.8 to 3.5% difference between the theoretical and measured power efficiencies for the lossless-dropper supercapacitor technique. These comparisons demonstrates the clear efficiency advantage of the supercapacitor-based lossless-dropper approach of the SCALDO regulator.

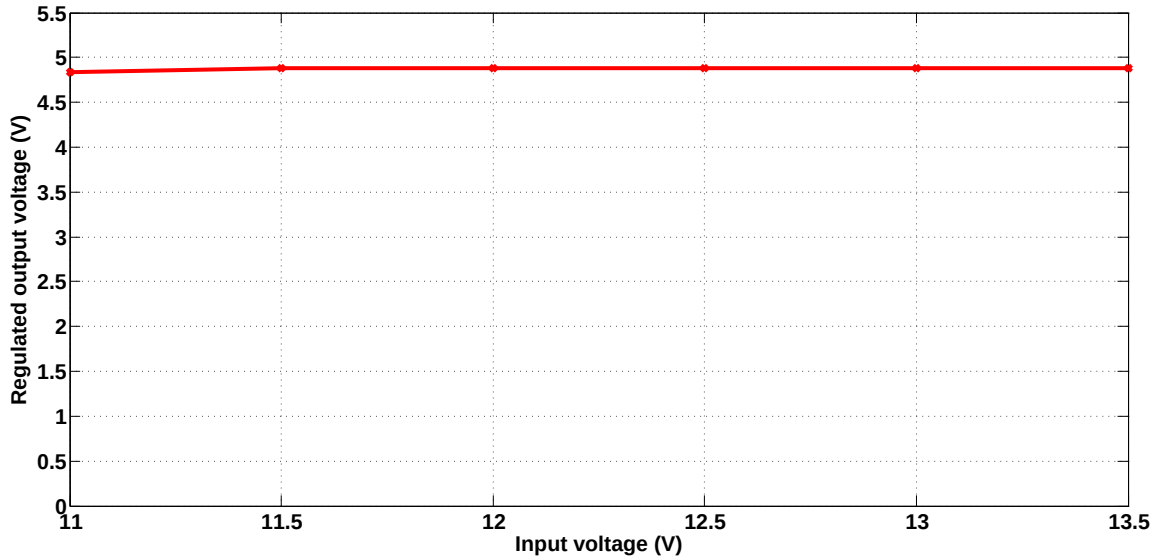


Figure 7.21: The line regulation experimental results of 12V-to-5V SCALDO regulator at a load current of 250 mA

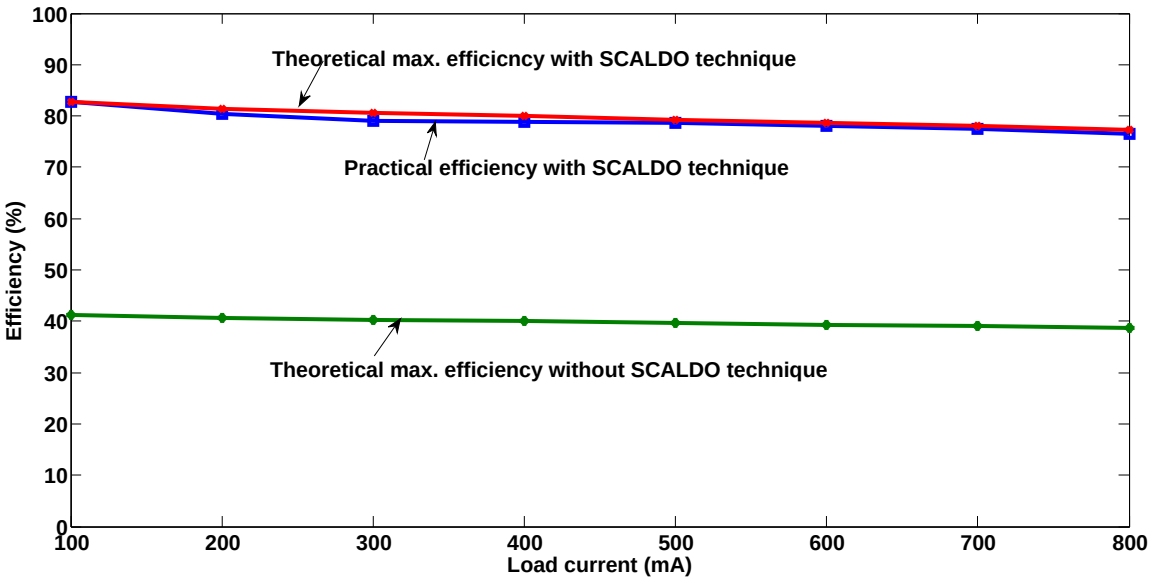


Figure 7.22: Efficiency vs load current of the 12V-to-5V SCALDO regulator at an input voltage of 12 V

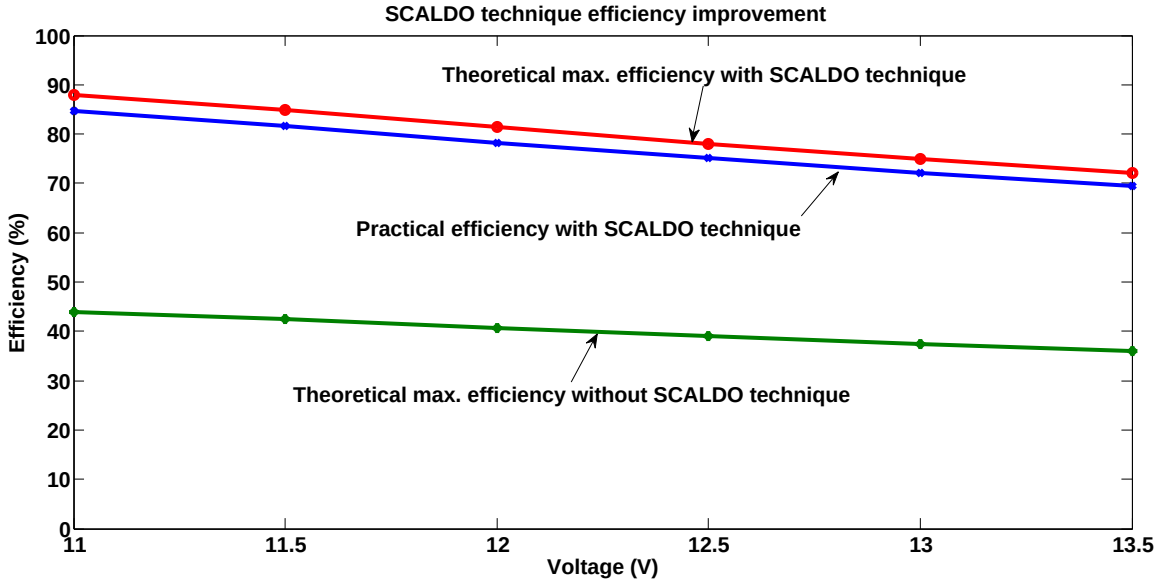


Figure 7.23: Efficiency comparison for a 12V-to-5V regulator: Theoretical results with SCALDO technique (upper trace), practical results with SCALDO technique (middle trace) and basic 12V-5V linear regulator theoretical performance (lower trace) at a load current of 250 mA

Load Transient Response of 12V-to-5V SCALDO Regulator

Transient measurements of the 12V-to-5V SCALDO prototype were carried out using a similar approach to the 5V-to-2V SCALDO regulator using the TEXIO PXL-151A DC electronic load. Figure 7.24 shows the transient voltage changes for 12V-to-5V SCALDO regulator where the green (1) trace shows the current step and the blue (2) trace shows the corresponding transient voltage change.

7.3 5.5V-to-3.3V SCALDO Regulator

The block diagram of Fig. 7.25 shows the 5.5V-to-3.3V SCALDO regulator which is an implementation of the $V_p < 2V_{\text{in}}^{\text{min}}$ criterion, $n = 3$ case. Fig. 7.26 shows the schematic. An LDO LT1963-3.3 from Linear Technology, which has the following specifications, was used as the main low dropout regulator in this prototype.

- Output current of 1.5 A
- Fixed output voltage at 3.3 V
- Dropout voltage of 340 mV
- Quiescent current of 1 mA
- Optimized for fast transient response

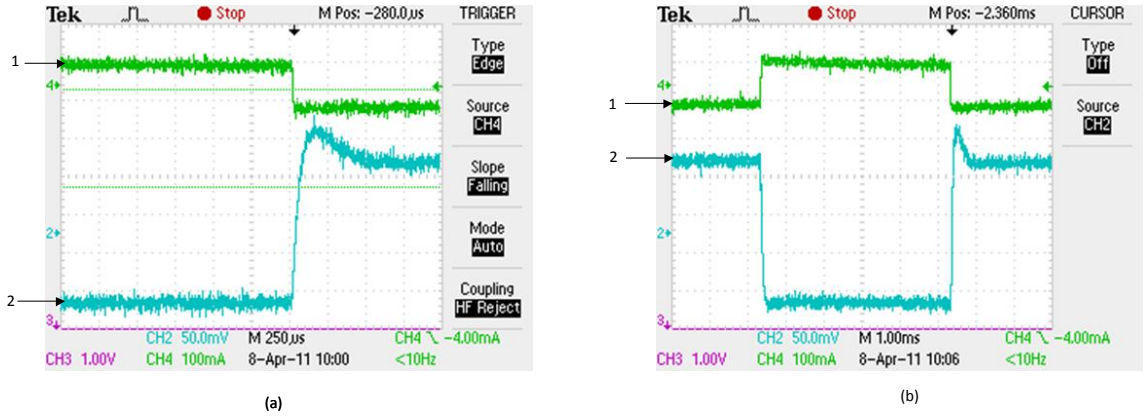


Figure 7.24: Transient measurements of 12V-to-5V SCALDO for (a) falling edge (b) rising/-falling edge

In order to optimise LDO operation, the LDO input voltage was kept at least 0.3 V above the required output voltage, thus, $V_{\text{in}}^{\text{min}}$ was maintained at 3.6 V. Originally, it was planned to design a 5V-to-3.3V regulator but due to switch resistance losses and supercapacitor ESR losses, the input voltage was increased to 5.5 V to overcome the issue of $V_{\text{in}}^{\text{min}}$ reaching an unacceptable level. Three supercapacitors of 1.2 F/5.5 V, of the type Cap-XX, were used as the group of identical supercapacitors (C_{SC}). A PIC microcontroller of the type PIC16F684 was used as the controller and the same algorithm was used to drive the solid state switches. The LDO input voltage was monitored through the RA4 port pin of the PIC microcontroller. The switch set (6 nos) S_{p1}, S_{p2}, S_{p3}, S'_{p1}, S'_{p2}, S'_{p3} and the switch set (4 nos) S_{s0}, S_{s1}, S_{s2}, S_{s3} were controlled through the RC1 and RC2 port pins respectively. In order to control several switches using a single control signal, three current amplifiers of the BC547A were used for the parallel and series set of switches as shown in Fig. 7.26. The three supercapacitors were kept in parallel using the switch set S_{p1}, S_{p2}, S_{p3}, S'_{p1}, S'_{p2},S'_{p3}. This capacitor group was connected in series with the LDO input to keep the supercapacitors charging from the unregulated power supply, while maintaining the requirement for the LDO operation. During the charge process, when 3.6 V for the LDO was reached, the controller switched on switch group S_{s0}, S_{s1}, S_{s2}, S_{s3} and switched off the other group of switches to keep the three supercapacitors in series to release their stored energy. The stored energy was released until the 3.6 V condition for the LDO was met and then switched back to the charging configuration again. To keep the linear regulator powered during this transition, a buffer capacitor (C_B) with sufficient capacity was connected between the linear regulator input and the ground terminal. Ten PVN012 photovoltaic relays were used as switches to keep the set of supercapacitors in charge and discharge configurations. The microcontroller firmware developed for this technique was

based on the same algorithm as the $V_p > 2V_{\text{in}}^{\text{min}}$ configuration in the flow chart of Fig. 7.4. Fig. 7.27 shows the final prototype developed for a 5.5V-to-3.3V regulator. The schematic and the PCB layout drawn in Altium Designer are available in Appendix B.

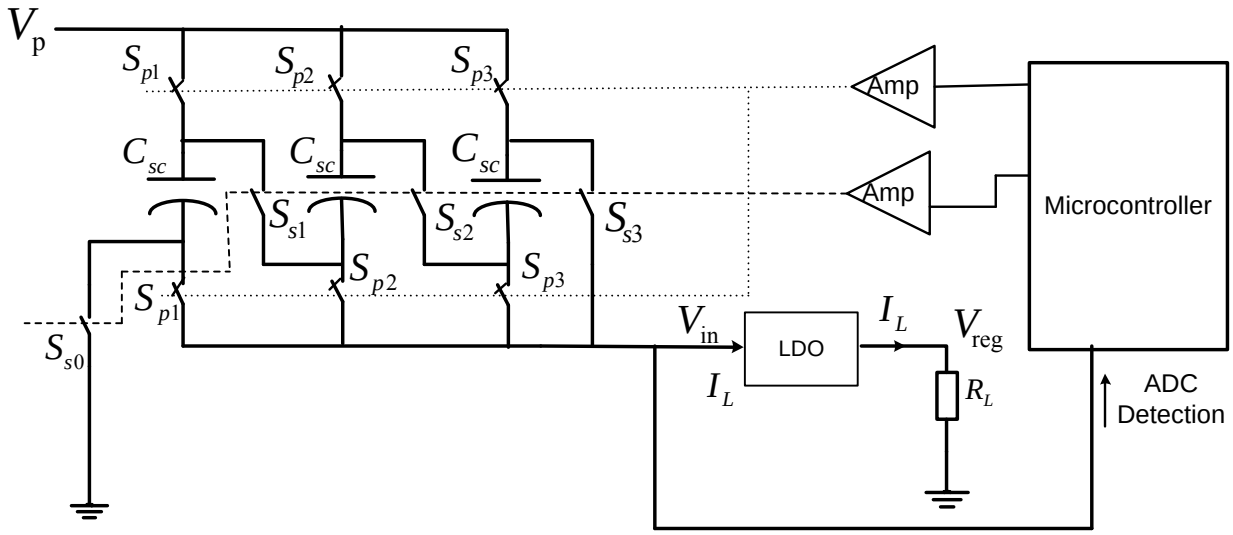


Figure 7.25: Block diagram of the 5.5V-to-3.3V SCALDO regulator

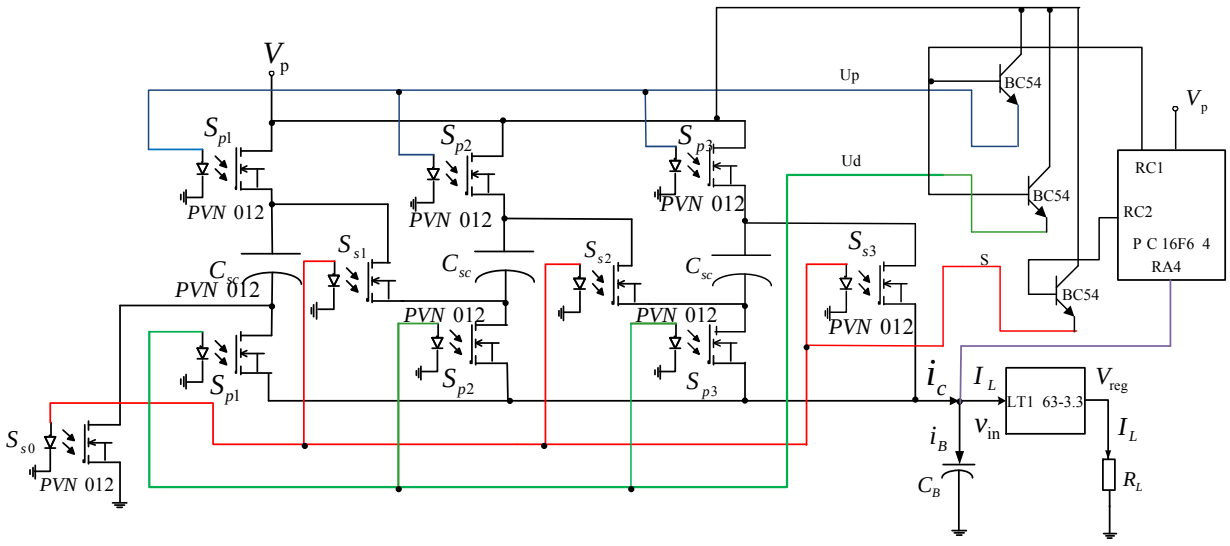


Figure 7.26: Schematic of the 5.5V-to-3.3V SCALDO regulator designed using an LDO LT1963-3.3, three 1.2 F/5.5 V Cap-XX Supercapacitors, ten optically coupled switches (PVN012 Photovoltaic switches), a PIC 16F684 microcontroller, BC547A amplifiers and a LM7805 regulator

7.3.1 Load Regulation

Figure 7.29 indicates the oscilloscope waveforms during the circuit operation for load currents of 200, 400, 600, 800, 1000 and 1300 mA respectively. Input voltage was maintained

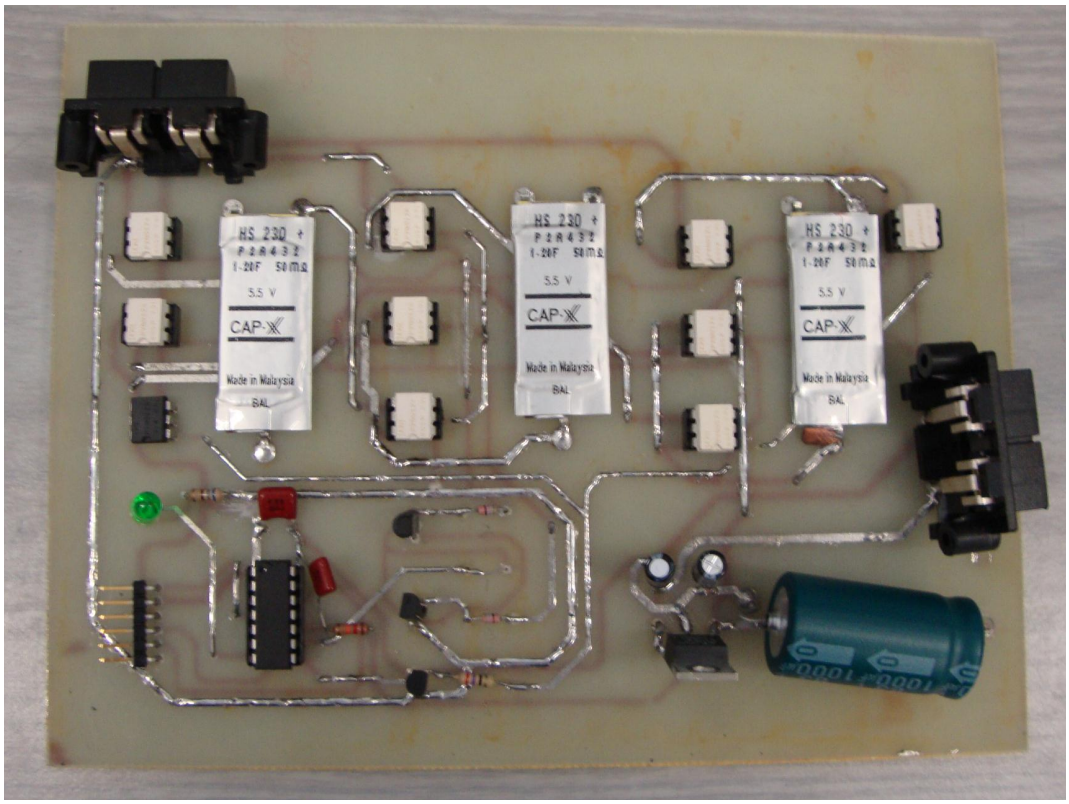


Figure 7.27: Prototype of the 5.5V-to-3.3V SCALDO regulator

at 5.5 V. As the load current increased, both the charge and the discharge phases cycled more quickly resulted in circulation frequency increase from 0.02 to 1.79 Hz. In Fig. 7.29, the blue (1), purple (2), green (3) and orange (4) traces represent voltage across one of the three supercapacitors (V_{SC}), LDO output voltage (V_{reg}), the input current of the system (I_{in}) and input voltage of the LDO (V_{in}) respectively. Table 7.8 and Fig. 7.28 show the corresponding experimental results and the load regulation graph respectively. Maximum deviation in load regulation is about 0.04%/mA. With the increasing load currents, due to the increasing losses across the many PVN012 switches and ESR of the supercapacitors, V_{in} can be pushed to a value below the minimum value. This increases the error in load regulation.

7.3.2 Line Regulation

Table 7.9 represents the experimental values of the line regulation of the 5.5V-to-3.3V SCALDO regulator and there were not significantly visible output voltage variations to the changes to the input voltage variations. Figure 7.30 depicts the corresponding line regulation plot where load current was fixed at 300 mA during these measurements. As shown in Table 7.9, the circulation frequency decreases from 53 to 28 mHz with the increase of the input voltages from 5.3 to 5.9 V.

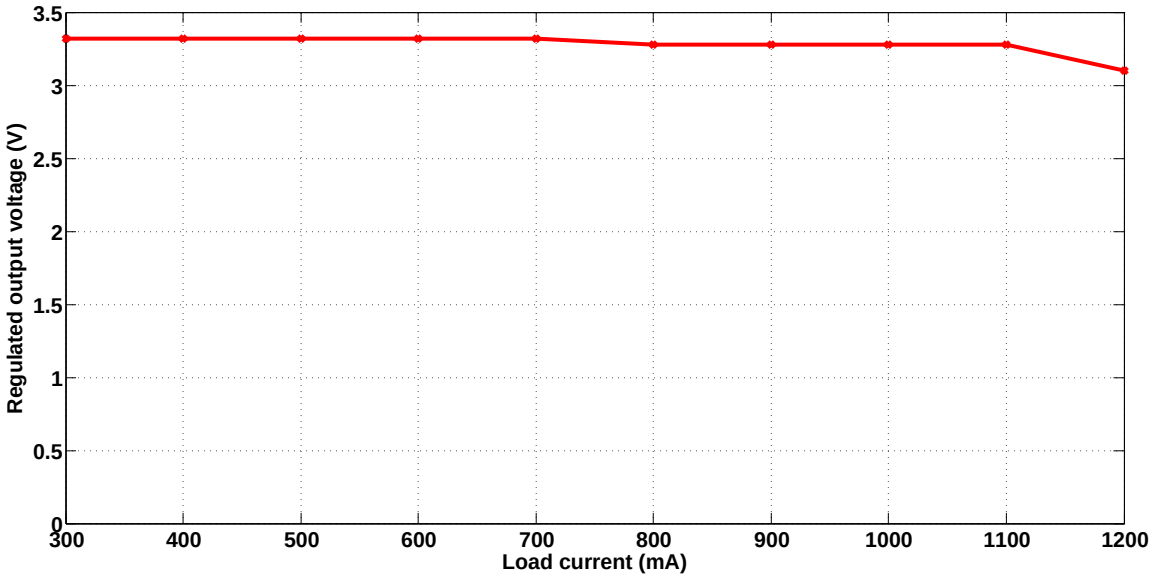
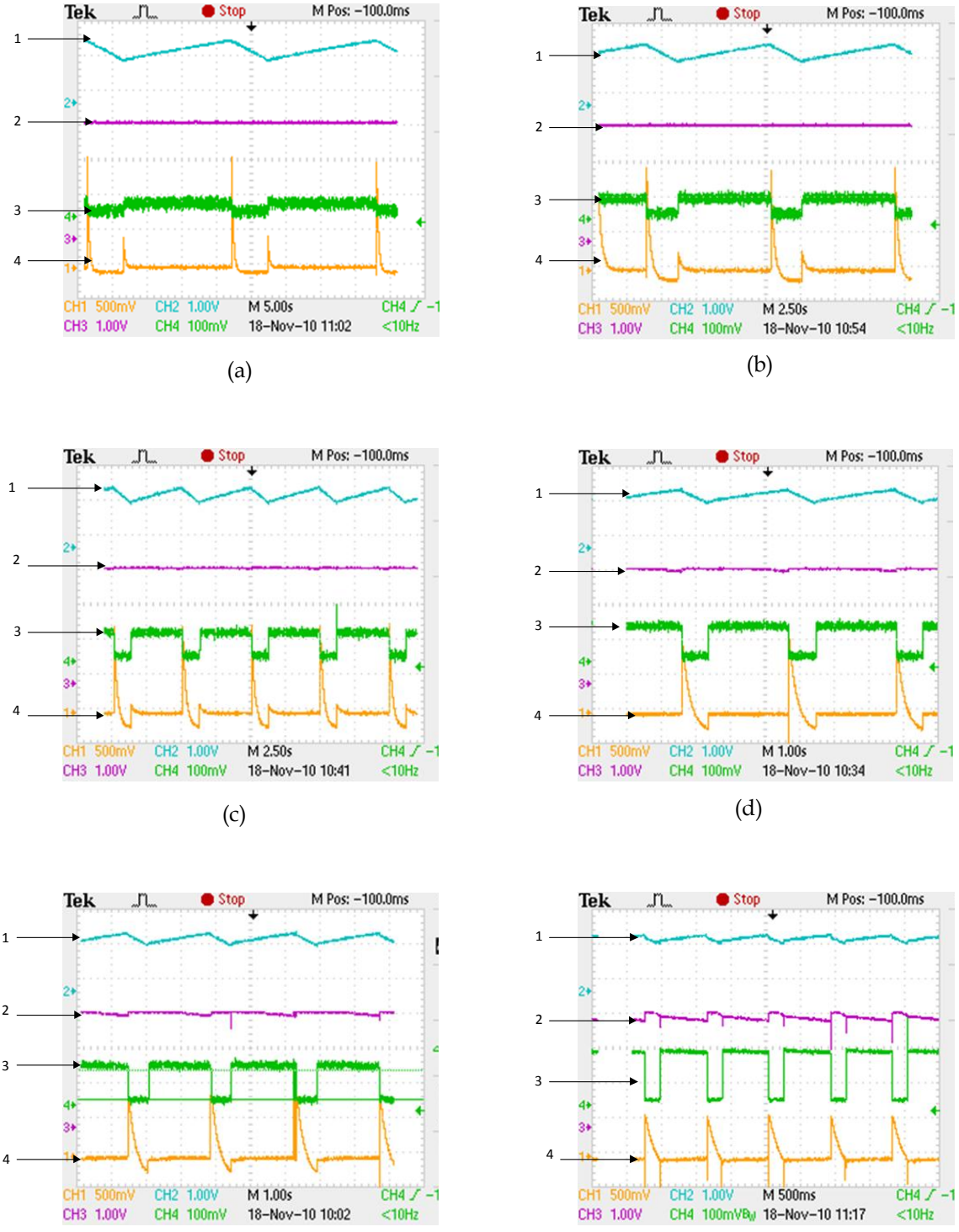


Figure 7.28: Load Regulation results of 5.5V-to-3.3V SCALDO regulator at input voltage of 5.5 V

Table 7.8: Load Regulation experimental results of 5.5V-to-3.3V SCALDO regulator at input voltage of 5.5 V

Load current (mA)	Output voltage (V)	Supercapacitor charging time (ms)	Supercapacitor discharging time (ms)	Input current (mA)	Control circuit current (mA)	Circulation frequency (Hz)	Efficiency with negligible control current%
300	3.32	9700	3200	480	160	0.08	75.3
400	3.32	6700	2200	560	160	0.11	80.2
500	3.32	5000	1700	680	160	0.15	77.8
600	3.32	3700	1200	840	160	0.20	70.5
700	3.32	2880	960	960	160	0.26	70.4
800	3.28	2320	800	1080	160	0.32	69.7
900	3.28	1280	560	1160	160	0.54	77.2
1000	3.28	1560	480	1280	160	0.49	69.6
1100	3.28	1160	380	1320	160	0.65	75.1
1200	3.10	920	300	1440	160	0.82	70.1
1300	3.04	660	220	1560	160	1.14	68.4
1400	3.04	440	120	1680	160	1.79	64.8



1 Voltage across the supercapacitor

2 LDO output voltage

3 Input current drawn from the unregulated power supply

4 Input voltage of the LDO

Figure 7.29: Oscilloscope waveforms of the 5.5V-to-3.3V SCALDO regulator for load currents of (a) 200 mA (b) 400 mA (c) 600 mA (d) 800 mA (e) 1000 mA (f) 1300 mA at input voltage of 5.5 V

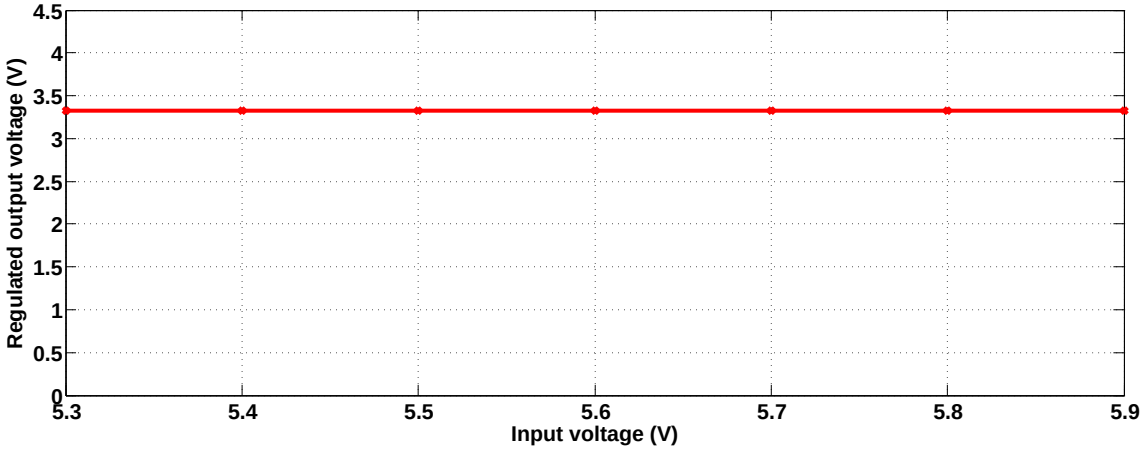


Figure 7.30: Line Regulation results of 5.5V-to-3.3V SCALDO regulator at a load current of 300 mA

Table 7.9: Line Regulation experimental results of 5.5V-to-3.3V SCALDO Regulator at a load current of 300 mA

Input Voltage (V)	Output voltage (V)	Supercapacitor charging time (ms)	Supercapacitor discharging time (ms)	Input current (mA)	Control circuit current (mA)	Circulation frequency (Hz)	Efficiency with negligible control current%
5.3	3.32	14200	4600	440	140	0.053	82.93
5.4	3.32	16000	5200	480	140	0.047	81.46
5.5	3.32	18400	6000	440	140	0.041	80.05
5.6	3.32	20400	6400	440	140	0.037	77.89
5.7	3.32	22400	7200	440	140	0.034	76.97
5.8	3.32	24400	8000	440	140	0.031	76.01
5.9	3.32	26800	8800	440	140	0.028	74.75

7.3.3 End-to-End Efficiency (ETEE)

In the following calculations, V_p, I_{in}, V_{reg}, I_L and I_c are used as before. Neglecting the control circuit current, the average current drawn from the unregulated power supply during a supercapacitor charge-discharge cycle is,

$$I_{\text{avg}} = \frac{[I_{\text{in}} - I_c]\, t_{\text{ch}}}{t_{\text{ch}} + t_{\text{dch}}} \tag{7.4}$$

where t_{ch} and t_{dch} are charge and discharge times respectively.

The overall end-to-end efficiency of during a SCALDO cycle can be estimated as,

$$\eta = \frac{V_{\text{reg}} I_L}{V_p I_{\text{avg}}} 100\% \tag{7.5}$$

As shown in Table 7.9 using the line regulation data, the end-to-end efficiencies were estimated according to Eqns (7.4) and (7.5). These values were plotted against the input voltage as shown in Fig. 7.31. This figure shows a comparison of the theoretical performance of SCALDO technique (upper trace), the practical performance of SCALDO technique (middle trace) and the performance of a standard linear regulator (lower trace) for a 5.5V-to-3.3V regulator. The prototype achieves overall end-to-end efficiencies in the range of 75 to 83%, compared to the maximum theoretical efficiency of 56-63% for a conventional linear regulator used for the same inputoutput combination. The middle trace of Fig. 7.31 shows the improved efficiency in the new SCALDO implementation. The graphs indicate around 1% difference between the theoretical and measured power efficiencies for the SCALDO technique due to the losses in switch resistances and the capacitor ESR.

7.3.4 Load Transient Response

Fig. 7.32 shows the oscilloscope figures of the transient measurements for 5.5V-to-3.3V SCALDO regulator. For a given slew rate, in the rising and falling edges of the load, following output voltage variations shown in Table 7.10 were recorded in terms of transient voltage ripple and transient time.

Transient response is a complicated situation based on the output capacitor and the behaviour of the LDO itself. In this SCLADO analysis, further detailed analysis on finer details were not carried out due to the time constraints of the project.

7.4 Chapter Summary

The design and experimental details of practically useful step-down, SCALDO DC-DC converter combinations: 5V-to-2V, 12V-to-5V and 5.5V-to-3.3V are given in this chapter.

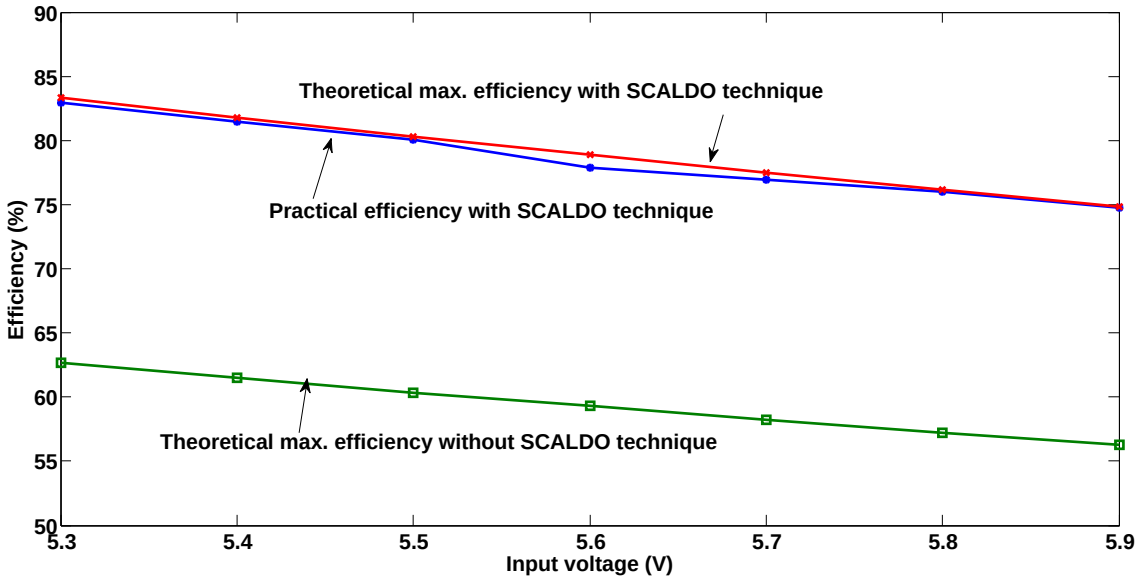
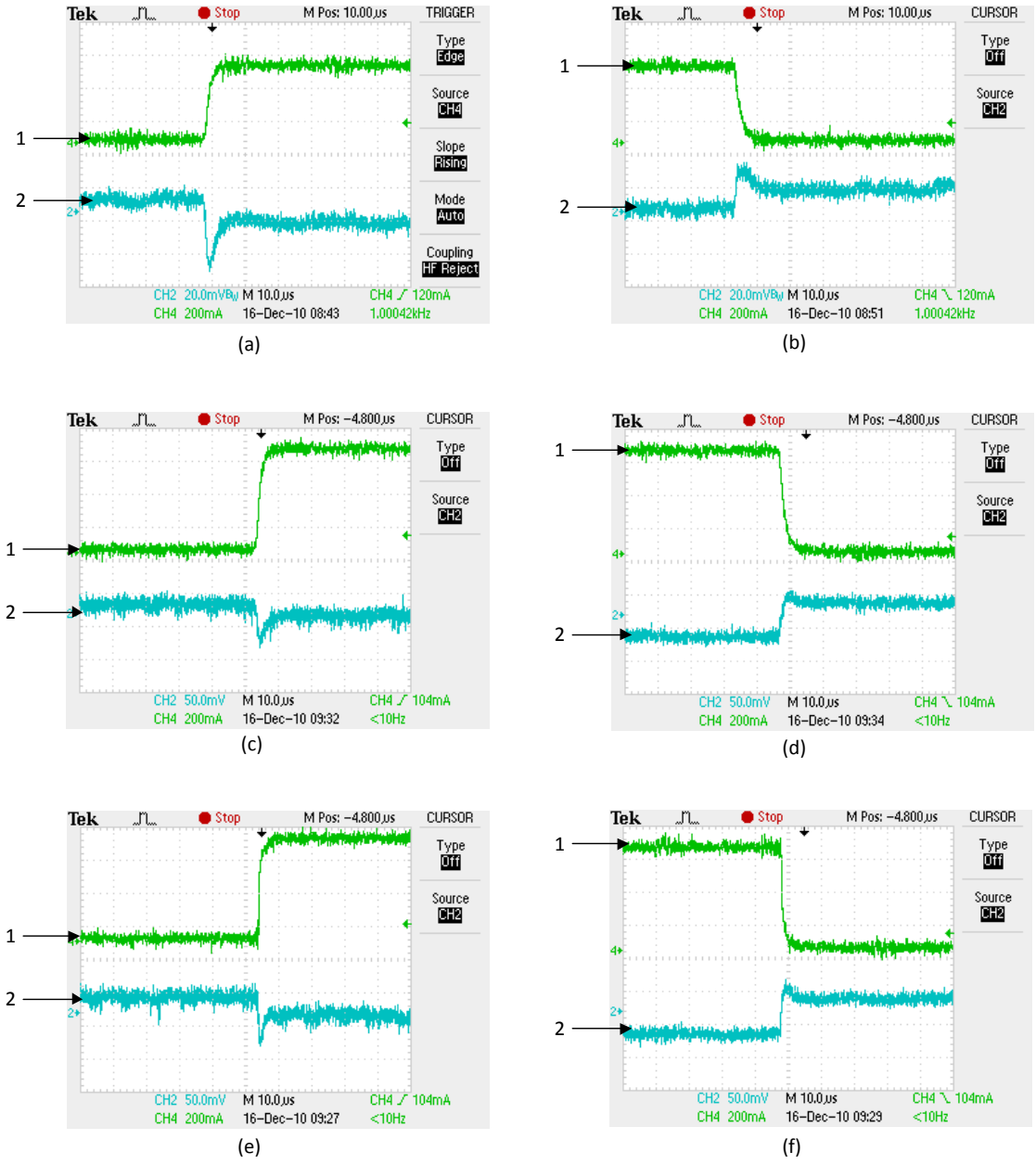


Figure 7.31: Efficiency comparison for a 5.5V-to-3.3V SCALDO regulator: Theoretical results with SCALDO technique (upper trace), practical results with SCALDO technique (middle trace) and basic 5.5V-to-3.3V linear regulator theoretical performance (lower trace)

Table 7.10: Transient measurements of 5.5V-to-3.3V SCALDO regulator

Slew rate (A/μs)	Load current(mA)	Transient time (ms) Rising edge	Transient time (ms) Falling edge	Ripple voltage (mV) Rising edge	Ripple voltage (mV) Falling edge
1	300	8.4	8.4	20.0	14.4
1	600	8.0	9.2	42.0	28.8
1	800	7.6	8.0	64.0	66.0
20	300	4.4	5.6	28.0	24.4
20	600	5.5	5.6	50.4	44.8
20	800	4.4	6.4	74.0	76.0



1 Transient load current

2 Change of output volatge

Figure 7.32: Transients of 5.5V-to-3.3V regulator using SCALDO technique (a) 1A/μs 50 mA to 600 mA rising edge (b) 1 A/μs 50 mA to 600 mA falling edge (c) 1 A/μs rising edge 50 mA to 800 mA (d) 1 A/μs falling edge 50 mA to 800 mA (e) 20 A/μs rising edge 50 mA to 800 mA (f) 20 A/μs falling edge 50 mA to 800 mA

The steady-state load and line regulation parameters and transient response of these prototypes illustrates performances similar to commercial linear regulators. According to the efficiency plots drawn from the experimental data taken from these prototypes, the SCALDO technique is capable of achieving significantly high end-to-end efficiency in the range of 70 to 85% which is significantly higher than the corresponding efficiencies in linear regulators used for the same input-output voltage combinations.

The next chapter presents the essential theory of supercapacitor circulation, with analytical results and comparisons with experimental measurements from a 12V-to-5V prototype.

Chapter 8

Theoretical Foundations and Preliminary Experimental Validation

8.1 Laplace Transform Theory

The Laplace transform is an integral transform method which is particularly useful in solving linear ordinary differential equations and it is a powerful tool which is very commonly used in electrical engineering. This transform allows equations in the "time domain" to be transformed into an equivalent equation in the complex s domain. In this way the Laplace transformation reduces the problem of solving a differential equation to solving an algebraic equation.

The Laplace transform is defined as shown follows. If $f(t)$ a function defined for $t > 0$, and the Laplace transform of $f(t)$, denoted by $\mathcal{L}[f(t)]$, is defined as,

$$\mathcal{L}[f(t)] = \int_0^\infty e^{-st} f(t)\,\mathrm{d}t \tag{8.1}$$

where s is the complex frequency, composed of real and imaginary parts:

$$s = \sigma + j\omega \tag{8.2}$$

The function $f(t)$ and $F(s)$ form a Laplace transform pair, denoted by,

$$f(t) \Longleftrightarrow F(s) \tag{8.3}$$

The inverse transform from $F(s)$back to $f(t)$ is achieved.

The Laplace Transform can be applied to different circuit elements, and then the circuit can be solved entirely in the s domain. For example, the time-domain relationship between voltage and current for a capacitor is given by,

$$i(t) = C\frac{\mathrm{d}v(t)}{\mathrm{d}t} \tag{8.4}$$

Solving for voltage, gives,

$$v(t) = \frac{1}{C}\int_0^t i(t')\,\mathrm{d}t' \tag{8.5}$$

Transforming into the Laplace domain,

$$V(s) = \frac{1}{C}\frac{1}{s}I(s) \tag{8.6}$$

$$\frac{V(s)}{I(s)} = \frac{1}{sC} = Z_{cap} \tag{8.7}$$

Corresponding relationships for a resistor and inductor are listed in Table 8.1.

Table 8.1: Laplace transform relationships for resistor, capacitor and inductor

Time domain	Frequency domain	Impedance
$v(t) = Ri(t)$	$\frac{V(s)}{I(s)} = R$	R
$v(t) = \frac{1}{C}\int i(t)\,\mathrm{d}t$	$\frac{V(s)}{I(s)} = \frac{1}{sC}$	$\frac{1}{sC}$
$v(t) = L\frac{\mathrm{d}i(t)}{\mathrm{d}t}$	$\frac{V(s)}{I(s)} = sL$	sL

The Laplace transform method for solving ordinary differential equations proceeds as follows:

1. The differential equation is transformed into an algebraic equation using Laplace transform identities
2. Solve the algebraic equation for the variable of interest
3. Transform back to the time domain to obtain the solution using the inverse Laplace transform.

The following example illustrates how the solution of a electrical circuit can be obtained using the Laplace transformation. It considers a simple RC circuit which consists of a resistor and a capacitor in series. The capacitor initially has a charge of V_0 and it will discharge the stored energy through the resistor when the switch is closed at time $t = 0$. Fig. 8.1(a) illustrates the time domain circuit and Fig. 8.1(b) shows the corresponding the Laplace-domain circuit.

Considering Fig. 8.1(b), according to Kirchoff's voltage law following the relationship can be obtained.

$$\frac{V_0}{s} = \frac{1}{sC}I(s) + RI(s) \tag{8.8}$$

Solving for I(s),

$$I(s) = \frac{CV_0}{1 + sRC} \tag{8.9}$$

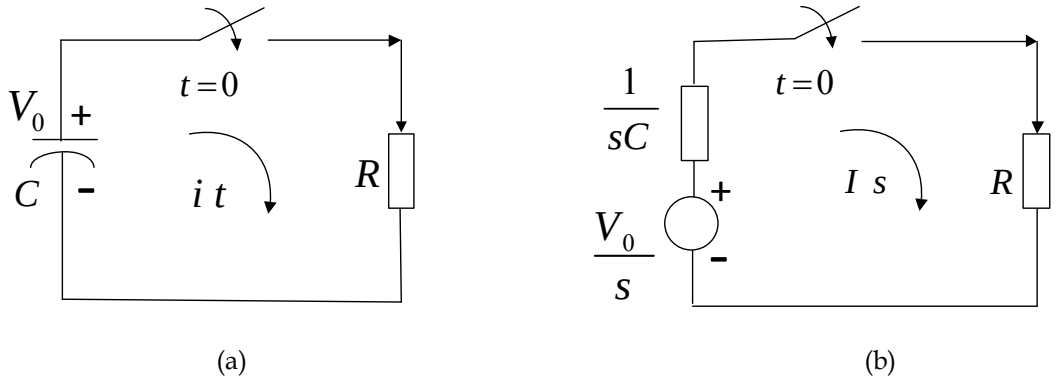


Figure 8.1: Simple *RC* circuit(a) time-domain and (b) Laplace-domain representation. (The capacitor carries an initial charge with voltage V_0 at time $t = 0$)

Taking the Inverse Laplace Transform, the current flowing through the loop can be found as,

$$\mathcal{L}^{-1}[I(s)] = i(t) = \frac{V_0}{R} e^{(-t/RC)} u(t) \tag{8.10}$$

where u(t) is the unit function.

8.2 Initial Start-up Charging

The SCALDO concept was developed utilising a pre-charged supercapacitor as a voltage dropper in the series path. One clear advantage of the SCALDO technique is that the same circuitry shown in Fig. 8.2(a) can be utilised in charging an uncharged supercapacitor.

The start-up charging process can be initiated by closing the switches s_1 and s_3 and placing the uncharged supercapacitor and the buffer capacitor in series with the unregulated power supply as shown in Fig. 8.2(b). In this case, until the LDO input voltage reaches the required $V_{\text{in}}^{\text{min}}$ value, LDO draws only a negligible amount of current due to the fact that the pass transistor does not enter its active region during that time period. During the initial start-up of the circuit, the power supply acts as a current source because of its current limited nature and works in its maximum possible current (I_P) capability. This time period is fairly small and is in the range of a few milliseconds. For a 2 A capable power supply and a 4700 μF buffer capacitor it takes 12 ms to reach 5.4 V, $V_{\text{in}}^{\text{min}}$ threshold.

Once the buffer capacitor exceeds $V_{\text{in}}^{\text{min}}$, the LDO begins powering the load but the power supply still remains as a current source as shown in Fig. 8.2(c). As soon as the series pass-element is activated, the load current starts flowing into the LDO, so that the current flowing through the buffer capacitor decreases to $I_p - I_L$. This process continues until the power supply voltage equals the sum of supercapacitor and buffer capacitor

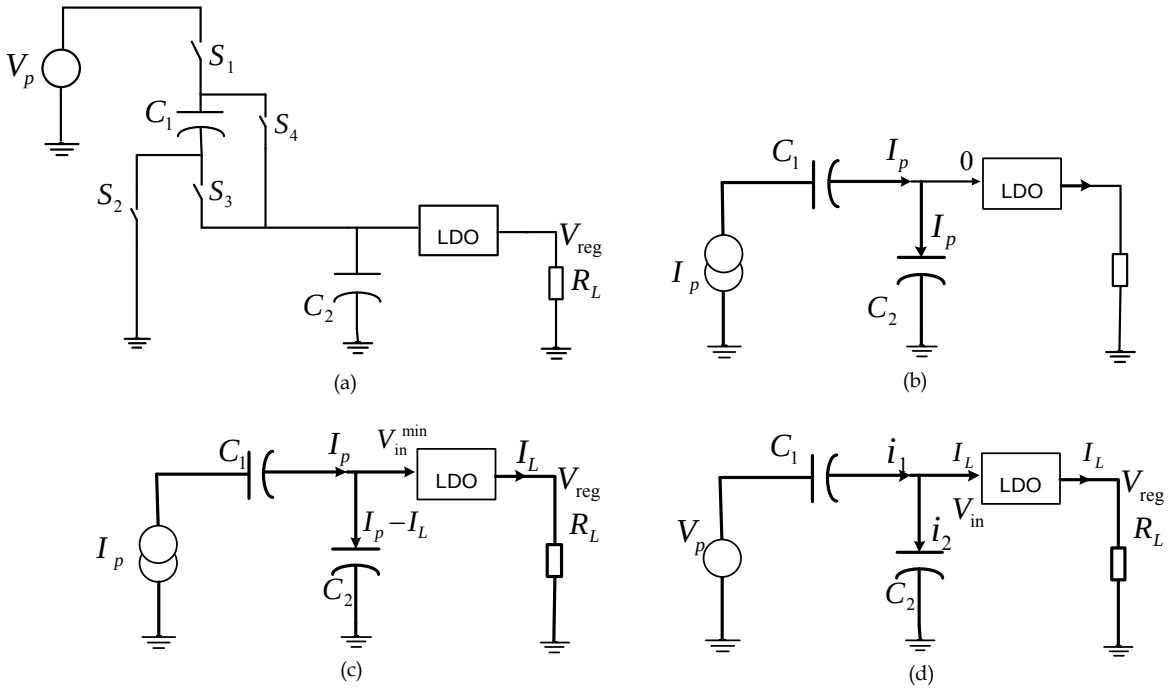


Figure 8.2: Initialisation phase of a uncharged supercapacitor

voltages. Then the circuit translates to configurations as shown in Fig. 8.2(d) where the power supply acts as a voltage source. The supercapaitor charging process continues until the changeover value of the LDO input voltage is met. This sequence only occurs once during the start-up and the LDO shows a lower efficiency in that time period.

8.3 Circuit Theory for the Supercapacitor Circulation

In analysing the circuit theory for the supercapcitor circulation, the $V_p > 2V_{\text{in}}^{\min}$, $n = 1$ (i.e., single capacitor) configuration was chosen for simplicity. As shown in Fig. 8.3, for a full charge-discharge cycle, the circuit operation was moved through four different phases. At first the time domain analysis was used, but it came up with a set of complex equations which were somewhat difficult to solve. So the Laplace transform theory was chosen as a better way for analysing the circuit operation.

After the initialisation, the circuit works with a net zero accumulation of charge in the capacitors across a complete cycle. Therefore, the present analysis was based on the assumption that the capacitor maintains a constant average DC voltage, and during different phases of the cycle the instantaneous voltage varies. In the following analysis, the circuit operation is considered as four working phases, as shown in Fig. 8.3: charging and discharging of the supercapacitor interrupted by brief transitions as the circuit is switched between these energy storage and delivery modes. Table 8.2 lists the parameters and definitions used for the analysis in time and frequency domains. In this table, when

choosing symbols, uppercase and lowercase letters are used to denote the fixed values and the variables respectively. In order to distinguish Laplace domain variables and time domain variables, tilde symbol is used to denote Laplace variables. But, the standard format of denoting Laplace variables is using upper-case s notations as discussed in section 8.1. Fig. 8.4 illustrates an example of various different symbols used for the supercapacitor in Table 8.2.

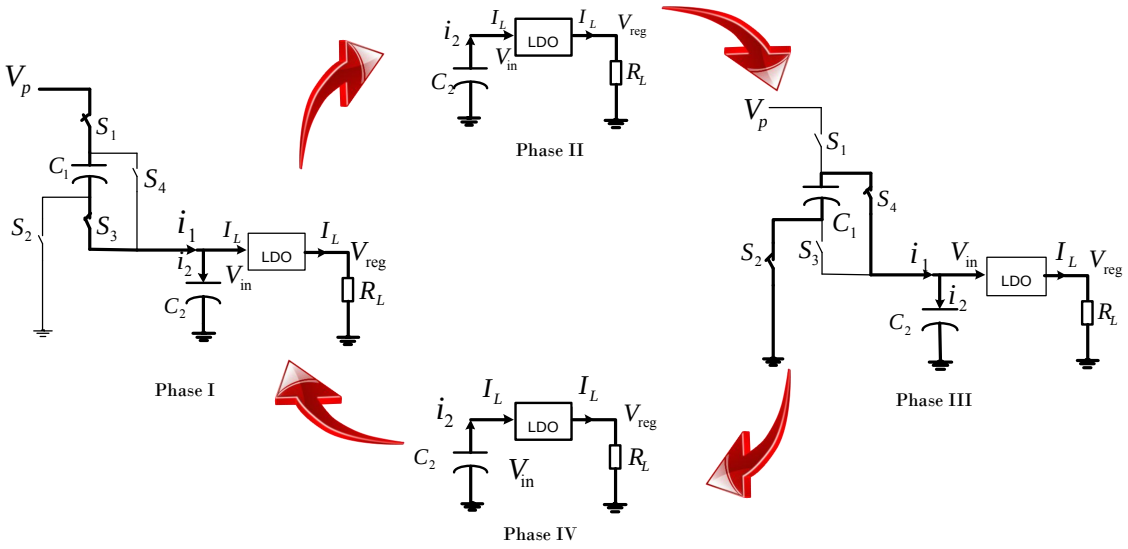


Figure 8.3: The four phases of circuit operation

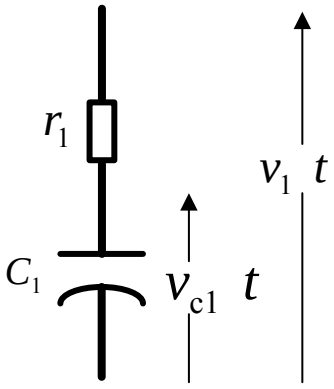


Figure 8.4: An example of various symbols used for the supercapacitor in Table 8.2: Supercapacitor (C_1) has an equivalent series resistance of r_1 and external and internal voltage of $v_1(t)$ and $v_{c1}(t)$ respectively

8.3.1 Phase I: Charging

This is the charging phase of the supercapacitor. The following initial conditions are indicated for this charging phase, assuming that the final conditions of the discharging phase

Table 8.2: Symbols and definitions used for analysis using Laplace technique

Time domain	Laplace domain	Description
$i_1(t)$	$\widetilde{i_1}(s)$	Supercapacitor current
$i_2(t)$	$\widetilde{i_2}(s)$	Buffer capacitor current
I_L	$\frac{I_L}{s}$	Constant load current
$v_1(t)$	$\widetilde{v_1}(s)$	External voltage across supercapacitor
$v_2(t)$	$\widetilde{v_2}(s)$	External voltage across buffer-capacitor
$v_{c1}(t)$	$\widetilde{v_{c1}}(s)$	Internal voltage across supercapacitor
$v_{c2}(t)$	$\widetilde{v_{c2}}(s)$	Internal voltage across buffer-capacitor
$V_2^{\min}$	$\frac{V_2^{\min}}{s}$	Threshold voltage for the LDO input
V_1^{IV}	$\frac{V_1^{\mathrm{IV}}}{s}$	External voltage across supercapacitor at the end of phase IV for the assumed initial condition
V_2^{IV}	$\frac{V_2^{\mathrm{IV}}}{s}$	External voltage across buffer capacitor at the end of phase IV for the assumed initial condition
$V_{c1}^{\mathrm{I...IV}}$	$\frac{V_{c1}^{\mathrm{I...IV}}}{s}$	Final values of the internal voltages of the supercapacitor at the end of phase I, II, III, IV respectively
$V_{c2}^{\mathrm{I...IV}}$	$\frac{V_{c2}^{\mathrm{I...IV}}}{s}$	Final values of the internal voltages of the buffer-capacitor at the end of phase I, II, III, IV respectively
V_p	$\frac{V_p}{s}$	Unregulated power supply voltage
C_1	$\frac{1}{sC_1}$	Supercapacitor capacitance
C_2	$\frac{1}{sC_2}$	Buffer capacitor capacitance
	r_1	Equivalent series resistance for C_1
	r_2	Equivalent series resistance for C_2
	r	On-resistance of the solid state relay (SSR) used to perform the switching function
	t_{sw}	Transition time between series/parallel due to switch delays

(phase IV) are such that the current flowing through the buffer capacitor is negligibly small and the total load current was drawn from the supercapacitor. The initial external (i.e., measurable) voltages across buffer and super capacitors at the end of phase IV are given by,

$$V_2^{\mathrm{IV}} = V_2^{\min} \tag{8.11}$$

$$V_1^{\mathrm{IV}} = V_2^{\mathrm{IV}} + 2rI_L \tag{8.12}$$

where the factor 2 in Eqn. (8.12) arises from the on-resistance of the two switches S_1 and S_3 (assumed identical).

Equations (8.11) and (8.12) imply the following initial values for the internal (i.e., unobservable) voltages,

$$V_{c1}^{\mathrm{IV}} = V_1^{\mathrm{IV}} + r_1 I_L \tag{8.13}$$

$$V_{c2}^{\mathrm{IV}} = V_2^{\mathrm{IV}} - \frac{I_L t_{\mathrm{sw}}}{C_2} + r_2 I_L \tag{8.14}$$

where t_{sw} is the transition time in switching from charging to discharging and vice versa, and the buffer and super capacitors have ESR values r_2 and r_1 respectively.

Figure 8.5(b) represents the Laplace transformation of the Phase I circuit shown in Fig 8.5(a). From the Laplace equivalent circuit, the following relationships can be derived,

$$\widetilde{i_1}(s) = \widetilde{i_2}(s) + \frac{I_L}{s} \tag{8.15}$$

$$\frac{V_p}{s} = \frac{V_{c1}^{\mathrm{IV}}}{s} + \left[\frac{1}{sC_1} + r_1 + 2r\right]\widetilde{i_1}(s) + \frac{V_{c2}^{\mathrm{IV}}}{s} + \left[\frac{1}{sC_2} + r_2\right]\widetilde{i_2}(s) \tag{8.16}$$

Here, the tilde symbol denotes a Laplace transformed quantity, e.g. $i_1(t) \leftrightarrow \widetilde{i_1}(s)$

Resolving Eqns. (8.15) and (8.16),

$$\widetilde{i_2}(s) = \frac{V_p - V_{c1}^{\mathrm{IV}} - V_{c2}^{\mathrm{IV}} - [r_1 + 2r]\, I_L - \dfrac{I_L}{C_1 s}}{\left[\dfrac{1}{C_1} + \dfrac{1}{C_2}\right] + [r_1 + r_2 + 2r]\, s} \tag{8.17}$$

$$\widetilde{i_2}(s) = \frac{a_1}{a_2 + s} - a_3 \frac{1}{(a_2 + s)} \tag{8.18}$$

where,

$$a_1 = \frac{V_p - V_{c1}^{\mathrm{IV}} - V_{c2}^{\mathrm{IV}} - [r_1 + 2r]\, I_L}{[r_1 + r_2 + 2r]\, s}$$

and $a_2 = \dfrac{C_1 + C_2}{C_1 C_2} \dfrac{1}{r_1 + r_2 + 2r}$ defines an effective rate constant

and $a_3 = \dfrac{I_L}{C_1 [r_1 + r_2 + 2r]}$

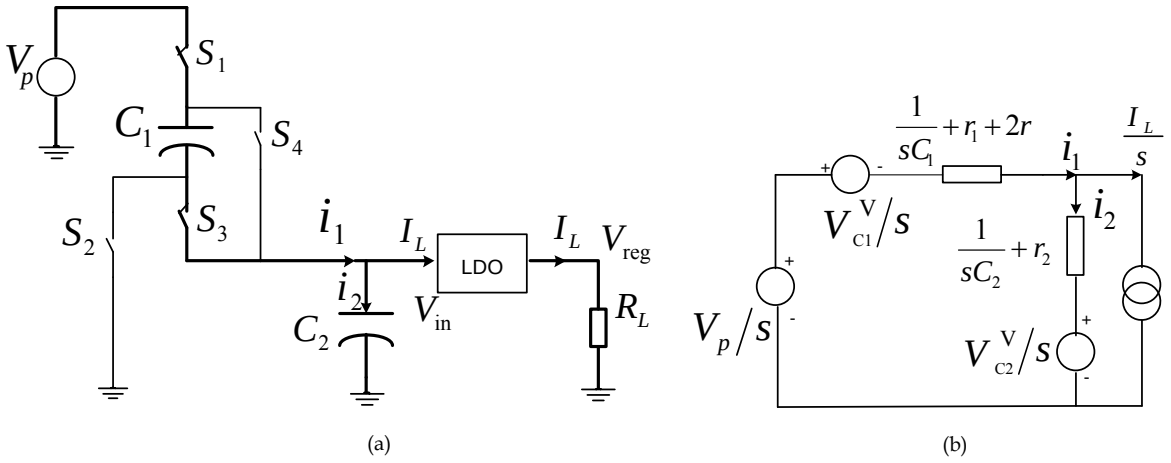


Figure 8.5: Supercapacitor charging configuration and its Laplace transformation (a) Switching configuration for the charging phase (b) Laplace transformation of the charging phase where supply voltage and initial capacitor voltages= fixed voltage sources, load= constant current sink, impedances=series combination of capacitive impedance plus ESR (plus switch resistance)

For convenience, we define a_4 as the a_3/a_2 ratio, $\quad a_4 = \dfrac{a_3}{a_2} = \dfrac{C_2 I_L}{C_1 + C_2}$

Taking the inverse Laplace transform of Eqn. (8.18), the instantaneous current flowing through the buffer capacitor is,

$$i_2(t) = [a_1 + a_4] \exp(-a_2 t) - a_4 \tag{8.19}$$

so that the instantaneous current through the supercapacitor is,

$$i_1(t) = I_L + i_2(t) \tag{8.20}$$

Internal voltages across the buffer and super capacitors are given by,

$$v_{c2}(t) = V_{c2}^{\mathrm{IV}} + \frac{1}{C_2} \int_0^t i_2(t') \, \mathrm{d}t' \tag{8.21}$$

and

$$v_{c1}(t) = V_{c1}^{\mathrm{IV}} + \frac{1}{C_1} \int_0^t i_1(t') \, \mathrm{d}t' \tag{8.22}$$

while the external voltages (i.e., the observable voltages including the ESR of r_2) and r_1 are given by,

$$v_2(t) = v_{c2}(t) + i_2 r_2 \tag{8.23}$$

and

$$v_1(t) = v_{c1}(t) + i_1 r_1 \tag{8.24}$$

Phase I continues until $v_2(t)$, the LDO input voltage meets the following condition

$$v_2\,(t) \leq V_2^{\min} \tag{8.25}$$

8.3.2 Phase II: Switchover to Discharging

This phase is in operation for a short duration just before the circuit is transferred to the supercapacitor discharge mode. This switchover period, t_{sw} is designed to accommodate any transition delays of switches used. In t_{sw} time duration, as shown in Fig. 8.6, the buffer capacitor is expected to discharge into the LDO input. According to the switch delay, the corresponding time duration is set by the PIC micro-controller. In practice, t_{sw} is very short compared to the times in phase I and III. The time duration is determined according to the data sheet of the switch and typically it is in the order of few milliseconds while time duration of other phases can be in the order of a few seconds. Switches used for SCALDO prototypes have delay characteristics as shown in Fig. 7.3 in Chapter 7.

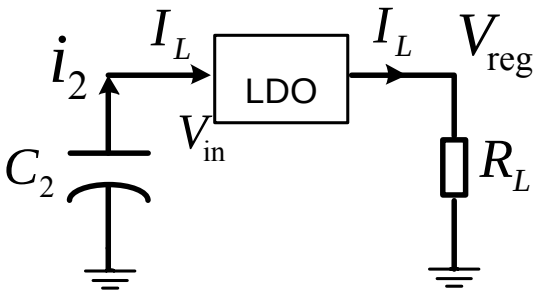


Figure 8.6: Switching transition from phase I to phase III

Based on Fig 8.6, the internal voltage across the buffer capacitor is given by,

$$v_{c2}\,(t) = V_{c2}^{\text{I}} - \frac{1}{C_2}\int_0^{t_{\text{sw}}} I_L \mathrm{d}t' \tag{8.26}$$

while the internal voltage across the supercapacitor remains fixed at ,

$$v_{c1}(t) = V_{c1}^{\text{I}} \tag{8.27}$$

since it is effectively disconnected from the circuit during this phase.

The external voltage across the buffer capacitor and supercapacitor are respectively given by,

$$v_2(t) = v_{c2}(t) - r_2 I_L \tag{8.28}$$

and

$$v_1(t) = v_{c1}(t) - r_1 I_L \tag{8.29}$$

Phase II continues for a period of t_{sw} which is set by the micro-controller to take account of settling time of the solid-state switches.

8.3.3 Phase III: Discharging

In this phase, the supercapacitor is placed in parallel with the buffer capacitor so that energy accumulated by the supercapacitor during the phase I charging phase is discharged through the LDO.

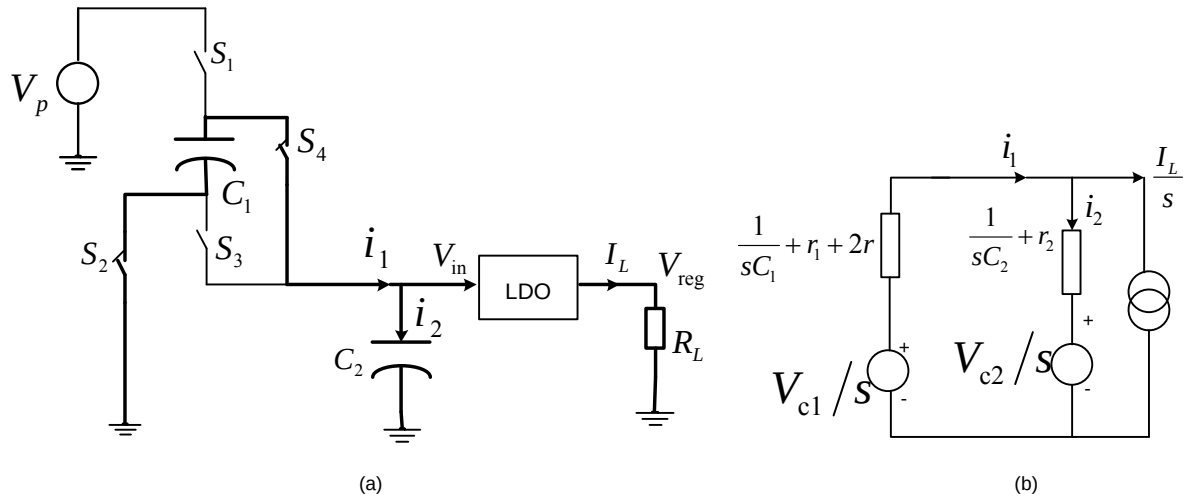


Figure 8.7: Discharge phase (a) Supercapacitor discharging (b) Laplace transformation of the discharging configuration

Fig. 8.7(b) represents the Laplace transformation of the Phase III circuit shown in Fig. 8.7(a). Based on Laplace transformations, the following relationships can be derived:

$$\widetilde{i_1}(s) = \widetilde{i_2}(s) + \frac{I_L}{s} \tag{8.30}$$

$$\frac{V_{c1}^{\text{II}}}{s} - \left[\frac{1}{sC_1} + r_1 + 2r\right]\widetilde{i_1}(s) = \frac{V_{c2}^{\text{II}}}{s} + \left[\frac{1}{sC_2} + r_2\right]\widetilde{i_2}(s) \tag{8.31}$$

Resolving Eqn.(8.30) and 8.31,

$$\widetilde{i_2}(s) = \frac{V_{c1}^{\text{II}} - V_{c2}^{\text{II}} - [r_1 + 2r]\, I_L - \dfrac{I_L}{C_1 s}}{\left[\dfrac{1}{C_1} + \dfrac{1}{C_2}\right] + [r_1 + r_2 + 2r]\, s} \tag{8.32}$$

$$\widetilde{i_2}(s) = \frac{a_1'}{a_2 + s} - a_3 \frac{1}{(a_2 + s)} \tag{8.33}$$

where a_2, a_3 and a_4 were defined following Eqn. (8.18) and $a_1^{'}$, is defined as,

$$a_1^{'} = \frac{V_{c1}^{\mathrm{II}} - V_{c2}^{\mathrm{II}} - [r_1 + 2r]\, I_L}{[r_1 + r_2 + 2r]\, s}$$

Taking the inverse Laplace transform of Eqn.(8.33), the instantaneous current flowing through the buffer capacitor is,

$$i_2(t) = \left[a_1^{'} + a_4\right] \exp\left(-a_2 t\right) - a_4 \tag{8.34}$$

so that the instantaneous current through the supercapacitor is,

$$i_1(t) = I_L + i_2(t) \tag{8.35}$$

Internal voltages across the buffer and supercapacitors are given by,

$$v_{c2}(t) = V_{c2}^{\mathrm{II}} + \frac{1}{C_2} \int_0^t i_2(t^{'})\, \mathrm{d}t^{'} \tag{8.36}$$

and

$$v_{c1}(t) = V_{c1}^{\mathrm{II}} + \frac{1}{C_1} \int_0^t i_1(t^{'})\, \mathrm{d}t^{'} \tag{8.37}$$

while the external capacitor voltages are,

$$v_2(t) = v_{c2}(t) + i_2 r_2 \tag{8.38}$$

and

$$v_1(t) = v_{c1}(t) - i_1 r_1 \tag{8.39}$$

Phase III continues until $v_2(t)$, the LDO input voltage, meets the following condition

$$v_2\,(t) \leq V_2^{\min} \tag{8.40}$$

8.3.4 Phase IV: Switchover to Charging

This is the final phase of the circuit in which the supercapacitor is returned to its initial configuration of being in series with the unregulated supply. During switchover, the buffer capacitor alone supplies the LDO. Figure 8.6 depicts the situation here, similar to the Phase II described above.

Based on Fig. 8.6, the internal voltage across the buffer capacitor is given by,

$$v_{c2}(t) = V_{c2}^{\mathrm{III}} - \frac{1}{C_2} \int_0^{t_{\mathrm{sw}}} I_L\, \mathrm{d}t^{'} \tag{8.41}$$

while the internal voltage across the supercapacitor remains fixed at,

$$v_{c1}(t) = V_{c1}^{\mathrm{III}} \tag{8.42}$$

since it is disconnected from the circuit during this phase.

The external voltage across the buffer capacitor and supercapacitor are respectively given by Eqns. (8.23) and (8.24) listed earlier for phase II. Phase IV continues for a period of t_{sw} set by the microcontroller. Phase I then resumes to continue the charge-discharge cycling.

8.4 Comparison with Experimental Results

Using the above theoretical derivations, MATLAB codes were written to evaluate the time-varying capacitor voltages and currents across the four phases of circuit operation. Appendix E shows the corresponding MATLAB codes. The following set of components used in the implementation of 12V-to-5V SCALDO regulator were assumed for these MATLAB derivations:

1. A total capacitance of 1.33 F based on the series combination of three 2.5 V supercapacitors from Maxwell Technologies. Each has capacitance of 4 F and ESR of 100 mΩ
2. Switches implemented using solid state relays (SSR), type PVN012 from International Rectifier, each with an on resistance of 100 mΩ
3. An LDO of type MCP 1827ADJ from Microchip Technologies
4. A simple microcontroller from the PIC family, PIC16F684

Table 8.3: Parameter values used for MATLAB calculations

$V_2^{\min}$	V_p	C_1	C_2	r_1	r_2	r	I_L	t_{sw}
5.4 V	12 V	1.33 F	4700 μF	300 mΩ	400 mΩ	100 mΩ	0.2 A	3 ms

Fig. 8.8 represents the external voltages of buffer capacitor and supercapacitor based on the evaluations in MATLAB for the actual practical values of 12V-to-5V SCALDO configuration shown in Table 8.3. These MATLAB evaluations were based on the equation sets (8.24) and (8.23) for Phase I; (8.29) and (8.28) for Phase II; (8.39) and (8.38) for Phase III and (8.29) and (8.28) for Phase IV shown in the above derivations. In this evaluation and analysis, the supercapacitor model used was the first-order approximation (see Chapter 5) with an ESR in series with an ideal capacitor. Hence, simulated results have only linear charge-discharge profiles. Fig 8.8 shows the actual scope waveforms of the buffer-capacitor and supercapacitor voltages during the four phases. A comparison between the theoretical predictions and the practical implementation based on Figs. 8.8(a),

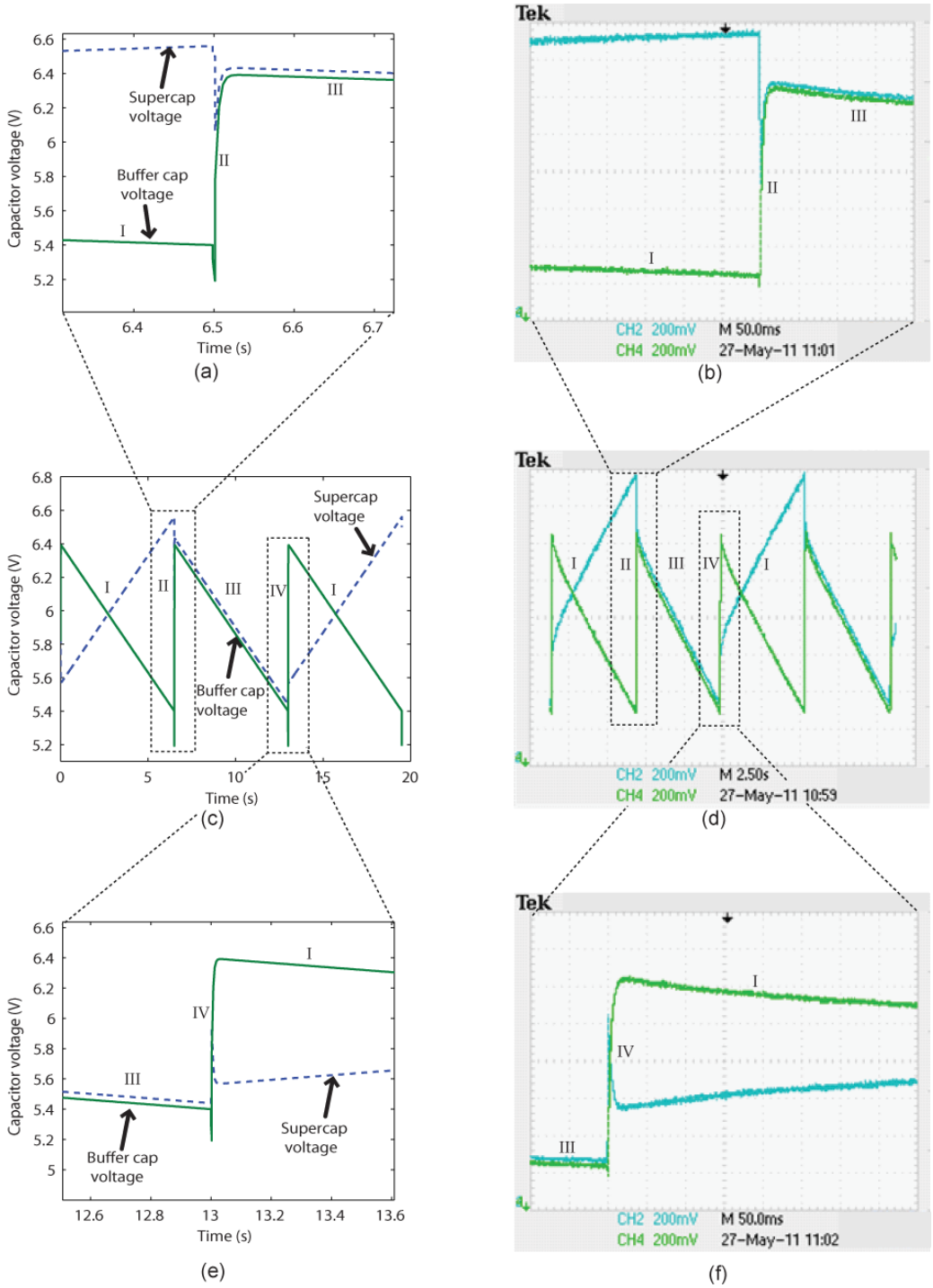


Figure 8.8: Supercapacitor voltage and buffer-capacitor voltage(LDO input voltage) variations during the circuit operation for 12V-to-5V supercapcitor assisted LDO model (a) Predicted charging-discharging transition (b) Oscillograph of the charging-discharging transition (c) Predicted waveforms for several cycles of operation (d) Oscillograph during circuit operation (e) Predicted discharging-charging transition (f) Oscillograph of the discharging to charging transition

(b), (e) and (f) is given in Table 8.4. A summary of this theoretical analysis on the SCALDO technique is presented in [7].

As shown in Fig. 8.8, the analytical results tally with the practical waveforms observed in a 12V-to-5V SCALDO regulator, thus confirming that the simplifying assumptions used to describe the circuit elements are reasonable. Furthermore, the theoretical model predicts that the buffer-capacitor waveform oscillates twice as fast as the supercapacitor, and this is verified in the actual circuit measurements. According to Table 8.4, the theoretical predictions of the supercapacitor and buffer capacitor voltages agree with the actual circuit measurements.

Table 8.4: Comparison between theoretical predictions and practical implementation of supercapacitor-assisted LDO recirculation model

		Theoretical values			Experimental values		
		Starting voltage (V)	Final voltage (V)	Period (s)	Starting voltage (V)	Final voltage (V)	Period (s)
Supercap voltage	During supercap charging	5.57	6.56	6.5	5.58	6.50	5.5
	During supercap discharging	6.42	5.44	6.5	6.26	5.4	5.5
Buffer cap voltage	During supercap charging	6.39	5.40	6.5	6.21	5.4	5.5
	During supercap discharging	6.39	5.40	6.5	6.21	5.4	5.5

As shown in Table 8.4, there is a discrepancy (around 1 s) in the time period of the the analytical results and practical waveforms. In our analytical solution, only the ESR terms of the capacitors and the switch on-resistances were taken into account, but in a practical situation, in a discrete PCB design, PCB copper traces and other conducting materials of the components have considerable resistances. For example, the 0.25 mm (10 mil) wide traces frequently used in PCB designs have a resistance/length of about 19 mΩ/cm (48 mΩ /inch), which is quite large [228]. Furthermore, due to the limitation of information available in the data sheet, the on-resistance of a PVN012 solid state relay was assumed as a fixed value of 100 mΩ (which is defined as the on-resistance for a 1 A pulsed load at 25 °C) for any load current. In low load currents the on-resistance of a PVN012 switch could be a much higher value than the assumption due to MOSFET based construction[236]. The effect of increasing temperature on the on-resistance [229] of a switch is negligible in this case, as there are no heat generating elements in the design. (The data sheet of the PVN012 is available in Appendix C.)

The factors that cause supercapacitor ageing that were discussed in Chapter 5 [230–234], the number of cycles, temperature and supercapacitor voltage are not significant in the SCALDO design. Specifically, in the SCALDO technique, the effect on supercapacitor ESR with increasing number of cycles can be negligible as the depth of discharge of the supercapaciotrs is very small during the circuit operation. The supercapacitor maintains a constant average DC voltage during different phases of the cycle and the instantaneous voltage varies around this average DC value. In 12V-to-5V SCALDO regulator, the average DC voltage of the supercapacitor was around 6 V and the instantaneous voltage was at slightly higher and lower value around 6 V. Furthermore, the effect of increasing temperature on the ESR is at a negligible value as the SCALDO design does not have any heat generating elements. The effect of unbalanced voltage on supercapacitor on ESR is also not an issue as the SCALDO designs use of identical supercapacitors and voltage was equally balanced among the supercapacitors.

In the analytical solution, in order to compensate for the errors that could be created by the PVN012 switch on-resistance and the parasitic resistances in the PCB traces of the circuit, an additional series resistance of 180 mΩ was added to the design parameters. As shown in Table 8.5, when an extra 180 mΩ resistance is added to the analytical solution, voltages and time periods of the analytical results tally with the practical waveforms observed in a 12V-to-5V SCALDO regulator.

Table 8.5: Comparison between theoretical predictions with additional 180 mΩ resistance and practical implementation of supercapacitor-assisted LDO recirculation model

		With additional 180 mΩ			Experimental values		
		Starting voltage (V)	Final voltage (V)	Period (s)	Starting voltage (V)	Final voltage (V)	Period (s)
Supercap voltage	During supercap charging	5.64	6.49	5.57	5.58	6.50	5.5
	During supercap discharging	6.35	5.51	5.57	6.26	5.40	5.5
Buffer cap voltage	During supercap charging	6.24	5.40	5.57	6.21	5.4	5.5
	During supercap discharging	6.24	5.40	5.57	6.21	5.40	5.5

Unlike switched-capacitor converters, in this SCALDO technique, the supercapacitor is used as a lossless-dropper, so there are no large inrush currents during the steady-state operation. Furthermore, the possibility of generating inrush currents during in the initial start-up is controlled by the current-limited nature of the power supply. During the major

portion of the overall switching cycle, all switches carry the average load current. Only during the early part of the parallel connection phase does some voltage equalization across the buffer capacitor and supercapacitor occur, with the possibility of a transient high current flowing between the two capacitors.

8.5 Chapter Summary

The performance and associated waveforms of the individual phases (charge, discharge and transition) of SCALDO regulators is accurately predicted by an analytical solution developed using Laplace transforms. Analytical results obtained using Laplace transform-based Matlab simulations, tally well with actual waveforms observed in a 12V-to-5V SCALDO regulator, indicating that the analytical technique can be generalized to other useful configurations, and confirming that the simplifying assumptions are reasonable and justifiable.

This analytical solution can be extended to include energy losses during SCALDO operation. More details on loss estimation are provided in the next chapter.

Chapter 9

Loss Estimation and Validation of the SCALDO Implementation

9.1 SCALDO Losses and Loss Minimization

As discussed in Chapter 3, the overall energy loss in switched-mode power supplies can be in the range of 8 to 30%, despite the fact that ideal versions of switched-mode converters have theoretical efficiencies of 100%. There are six factors that can contribute to energy loss:

1. Static losses in transistor switches
2. Diode DC losses
3. Dynamic losses in switches due to transition from off-to-on and on-to-off states
4. Losses in capacitors
5. Losses in inductive components
6. Losses in control circuits

In switch-mode converters, when the switching frequency is increased, minimising these losses requires significant design and construction efforts. The SMPS design engineers have to carefully optimize the designs for best possible end-to end efficiency and to minimize RFI/EMI radiation.

Due to the design complexity created by these loss terms in switch-mode converters, low dropout regulators (LDOs) have been introduced to address the requirements of noise-sensitive and fast transient loads in portable devices. For LDO designs, the major losses are due to transistor voltage drop and the energy consumption of the control circuits. In typical cases, the dropout voltage is in the order of 0.1 to 2 V with the control circuits using extremely low power, providing efficiencies around 65% at the lower end, and much higher for lower dropout voltages. For example for an LDO with 3.5-to-3.3 V conversion, the efficiency will be about 94%, significantly better than for a switched-mode converter. By using supercapacitors as lossless voltage-droppers in the series path and reusing energy stored in the supercapacitors, combined with a commercial low dropout linear regulator, SCALDO-based DC-DC converters can be designed with high end-to-end efficiencies.

The use of supercapacitors combined with LDOs in the SCALDO technique, though simple enough to appreciate, has several implementation issues. Some of the important loss contributors and implementation issues are:

- ESR losses and leakage current losses in the supercapacitors
- Losses due to switch resistances and switch transitions
- Losses of the parasitics in the circuit
- Losses associated with paralleling of buffer capacitors and supercapacitors
- Control circuit energy consumption

It is important to note that, losses require significant design efforts are of no avail without significant construction efforts. A poor circuit layout can undo an excellent design-and vice versa.

9.1.1 ESR Losses and Leakage Current Losses in the Supercapacitors

In the SCALDO technique, supercapacitor is charged and discharged at the same DC current equal to the load current. This makes the DC ESR of the devices creating a significant ohmic loss. However, DC ESR supercapacitor are in the range of fractional milliohm to less than 100 milliohms allows the losses to be minimised. Particularly for large supercapacitors, this could be very much lower than typical MOSFET $R_{DS(on)}$ related losses.

At higher load currents, the voltage drop across a supercapacitor ESR ($I_L R_{\mathrm{ESR}}$) can create a voltage drop to push the LDO to an input voltage below its $V_{\mathrm{in}}^{\mathrm{min}}$ which is an unacceptable level for the proper operation of the LDO. Therefore, selecting supercapacitors with very low ESR is an important. Energy losses associated with the ESR, similar to the case of switching power supplies, contributes to reduce the overall efficiency. Very small ESR, in the range of fractional milliohm to less than 100 mΩ in modern supercapacitors allows capacitor losses to be minimised, making a near-ideal lossless voltage dropper in the series path.

Given the low leakage currents in new families of supercapacitors, typically within a range of 5 to about 50 μA, compared to their high charge/discharge current capabilities in the range of tens to several hundred amperes, leakage current related losses are negligible [175,223]. As shown in Fig. 9.1, when a supercapacitor charges, the leakage current decays over time. The equilibrium value of the leakage current is determined by capacitance, voltage, and time. At room temperature, a rule of thumb for equilibrium-leakage-current in supercapacitors is 1 μA/F [223].

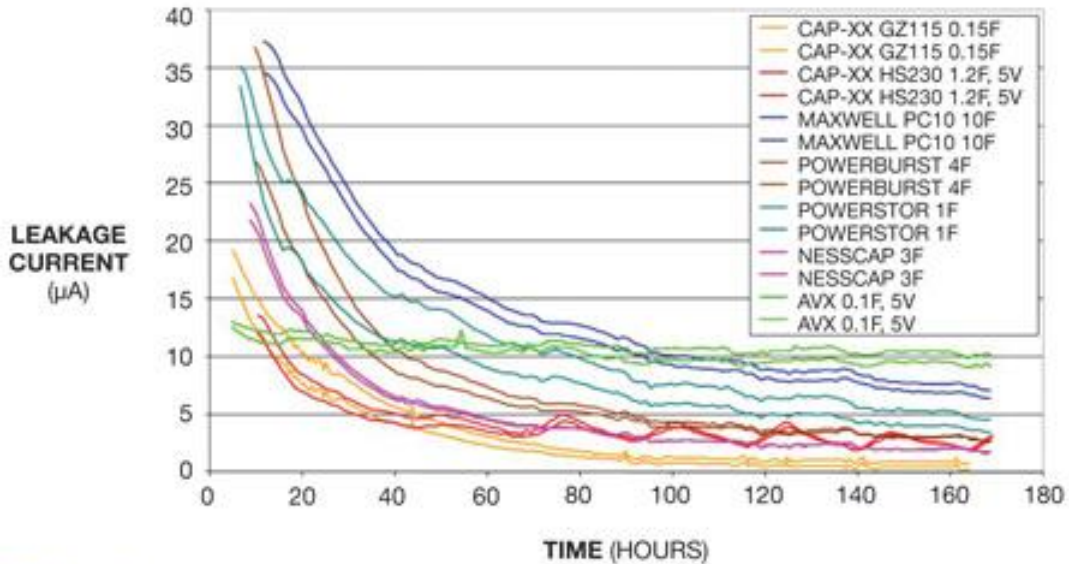


Figure 9.1: Leakage current of commercial supercapacitors [223]

9.1.2 Losses due to Switches

In different phases of the SCALDO operation, the arrangement of switches is reversed. If commercial discrete MOSFETs are used, the body diode may create unwanted discharge paths and jeopardize the SCALDO implementation. This is the reason that solid state relays were chosen instead of standard MOSFET switches in proof-of-concept circuits. In discrete implementations, selected RF power MOSFETs without body diodes can be used as switches . In future IC versions of implementation, where switches can be developed without the body diode, this will not be an issue.

Similar to supercapacitor ESR, the dissipation across the switch resistances also contributes to make the LDO input voltage lower. PVN012 solid state relays with 100 mΩ on-resistances were used as the switches in the proof-of-concept prototypes. Originally, a 5V-to-3.3V regulator was planned but due to switch resistance losses (6 switches in the charging phase and 4 switches in the discharging phase) and supercapacitor ESR losses, the input voltage was maintained at 5.5 V to prevent $V_{\text{in}}^{\min}$ dropping to an unacceptable level.

For high current capable LDO circuits, efforts should be taken to reduce the number of switches. One such improvement, applicable to the present SCALDO design has been identified. Using two identical LDOs, the number of switches can be reduced from $3n+1$ to $2n$. This reduced-switch SCALDO (RS-SCALDO) topology has been suggested as a solution for modern VRM requirements. Further research is currently being carried out by another researcher. More theoretical and experimental details on this new modification can be found in [235]. As shown in Fig. 9.3, for the $V_p > 2V_{\text{in}}^{\min}$ basic SCALDO design,

using two identical LDOs, the number of switches can be reduced to 2 instead of the 4 switches used in the present design.

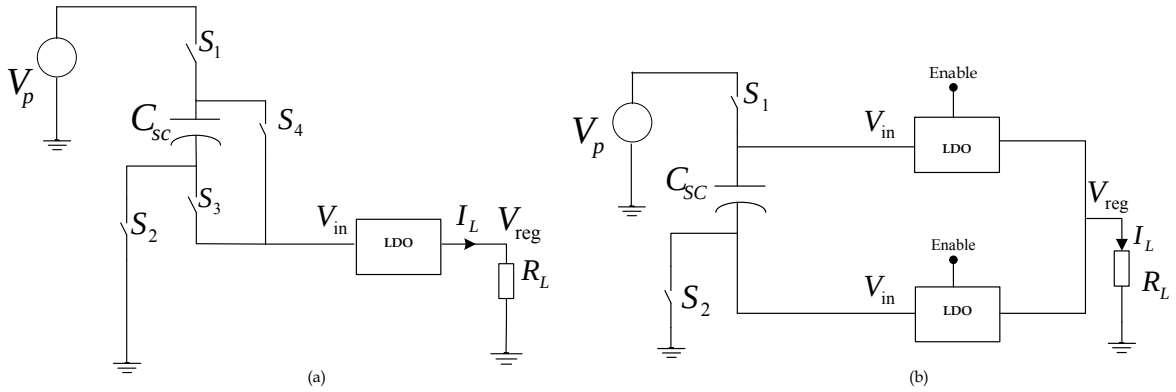


Figure 9.2: (a) Basic SCALDO configuration with single LDO and 4 switches (b) Modified RS-SCALDO (Reduced switches) configuration with 2 identical LDOs and 2 switches

Given that the SCALDO technique works in the range of fractional hertz to a few 10 Hz order frequencies, dynamic losses are significantly lower than SMPS, while creating no RFI/EMI issues, which creates significant impact in powering portable appliances with analogue circuit blocks.

9.1.3 Losses of the Parasitics in the Circuit

In a discrete PCB design, the copper traces and the conducting materials of the components can have considerable resistances. A 0.25 mm (10 mil) wide copper trace has resistance/length of about 19 mΩ/cm (48 mΩ /inch) [228]. Similar to supercapacitor ESRs and switch on-resistances, dissipation across these resistances creates additional loss terms. In designing more compact PCBs with shorter PCB traces, the effect of these parasitics can be minimised.

9.1.4 Paralleling of Capacitors with Unequal Voltages

There is a small delay between the switching transition from the charging phase to discharge phase and vice versa. A buffer capacitor is required to supply the LDO during the transitions to maintain the continuity of the regulation. The value of the buffer capacitor was determined as shown in Chapter 7, Eqn 7.1. However, the size of the buffer capacitor can be very small compared to the supercapacitor and may also have a different terminal voltage than the supercapacitor at the time of transfer into the discharge mode.

In practice, if two capacitors of different voltages are placed in parallel, by discharging some energy within their ESRs and the path resistances, the two parallel capacitors reach a common voltage. As illustrated in Eqn. (5.16), if two capacitors C_{sc} and C_B have terminal voltages of V_{sc} and V_B respectively, loss of energy due to paralleling is given by,

$$E_L = \frac{1}{2}\frac{C_{\text{sc}}C_B}{C_{\text{sc}}+C_B}\left[V_{\text{sc}}-V_B\right]^2 \tag{9.1}$$

Equation (9.1) indicates that when there is a large difference between capacitor voltages, the dissipation in the ESRs will be increased. However, if the buffer capacitor, C_B is very much smaller than the supercapacitor, C_{sc} the loss is:

$$E_L \approx \frac{1}{2}C_B\left[V_{\text{sc}}-V_B\right]^2 \tag{9.2}$$

This indicates that as in the case of SCALDO design, if the C_B is very much smaller than the C_{sc}, the energy loss can be relatively small and negligible.

In the SCALDO technique, the two capacitors (supercapacitor and the buffer capacitor) of different voltages came in parallel at the beginning of the discharging phase of the switching cycle a similar situation of paralleling of capacitors was observed. For the 12V-to-5V SCALDO prototype, according to Eqn. (9.2), the energy loss due to paralleling of capacitors can be estimated as:

$$E_L^p = \frac{1}{2}C_B((V_p - V_{\text{in}}^{\min}) - V_{\text{in}}^{\min})^2 \tag{9.3}$$

Substituting the values of 12 V input supply, 4700 μF supercapacitor and 5.4 V $V_{\text{in}}^{\min}$ voltage, gives,

$$E_L^p = \frac{1}{2}0.0047((12-5.4)-5.4)^2 = 3\text{ mJ} \tag{9.4}$$

If the buffer capacitor is very much smaller than the supercapacitor, the energy loss is negligible. However, in the SCALDO implementation, the LDO input terminal is also connected to the two parallel capacitors. Therefore, the above situation shown in Eqn. (9.2) gives only a worst-case estimation.

To minimise the loss of paralleling capacitors, an improvement was suggested by the University of Waikato research group led by Nihal Kularatna [3]. In the solution, when the two capacitors are at different voltages, the voltages of the two capacitors are measured, and the transfer is made at a time when the two capacitors are at nearly the same voltage.

Fig. 9.3 depicts a circuit that monitors the voltage across the two capacitors using the comparator of the PIC microcontroller. When a common voltage was identified, the capacitor configuration is switched from series to parallel. This modification minimizes the energy loss and improves overall efficiency. Fig. 9.4 indicates a comparison of the efficiency improvement of this modification with the original 12V-to-5V SCALDO design. The result is an approximate 5% increase in efficiency compared to the original circuit, but with an increased circulation frequency. With a lower discharge voltage achieved by

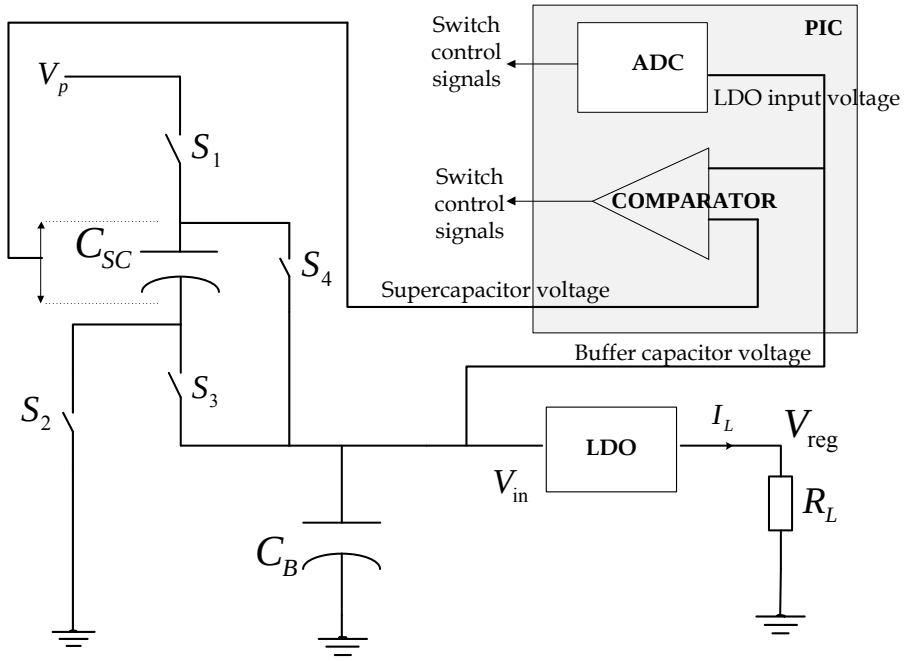


Figure 9.3: Modified SCALDO configuration with a comparator to make voltage across the two capacitors equal to minimise energy losses resulting from paralleling of capacitors [3]

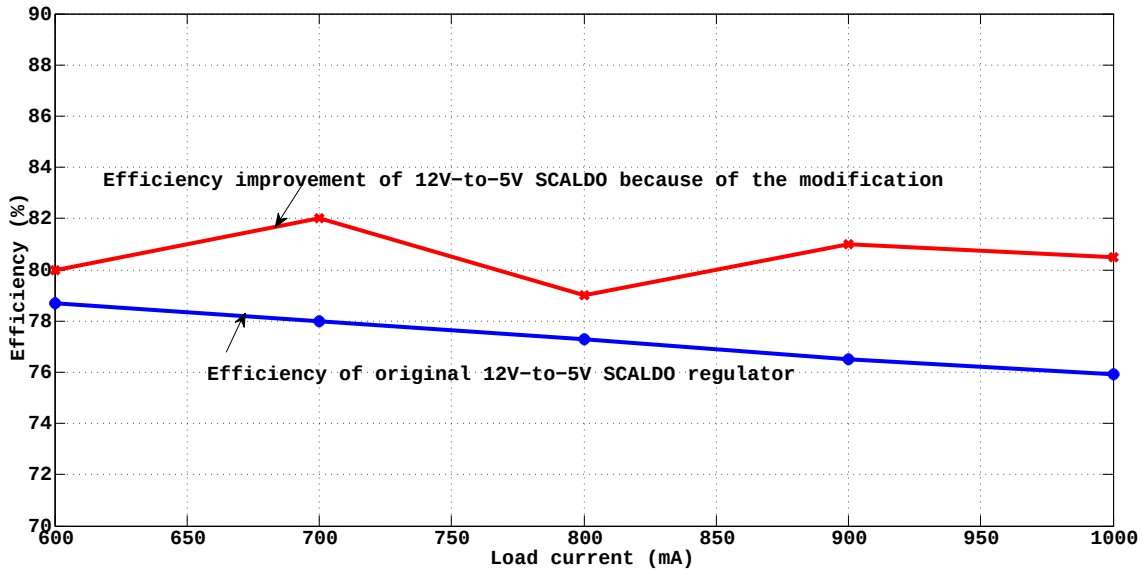


Figure 9.4: Comparison of efficiency improvement of modified SCALDO design (to minimise the losses caused by paralleling of capacitors) with the original SCALDO design [3]

this condition, the operation frequency of the new configuration increased to around 59 Hz [3].

9.1.5 Control Circuit Power Consumption

In SCALDO designs, a PIC microcontroller was used to drive the solid state switches. Typically, a current around 60 mA, was taken into the microcontroller during the 12V-to-5V SCALDO operation and a 5 V supply voltage was used to power it. The power loss of the PIC controller was around 0.3 W, which is fairly significant, but, with the limited budget and the time-frame of the research, a PIC microcontroller was the most economic solution available. However, in future SCALDO designs such as monolithic SCALDO implementations, measures can be taken to maintain the controller circuit power consumption at a bare minimum. Therefore, in our present analysis, the power consumption of the PIC microcontroller was not taken into account.

9.2 Loss Estimation

The Laplace transform-based theoretical solution discussed in Chapter 8 can be extended to analyse and estimate the SCALDO energy losses due to switch resistances, supercapacitor ESR and PCB parasitics during the four phases of the SCALDO operation. The terminology used in the Chapter 8 analysis is used for these derivations as well.

The power loss at a given instance in Phase I, can be estimated using the supercapacitor current, i_1, which was derived from the previous analysis.

$$P_{\mathrm{I}} = i_1^2(r_1 + 2r + r_e) \tag{9.5}$$

where r_e is the resistance added to compensate for the parasitics in the circuit.

The corresponding energy loss during Phase I can be found as,

$$E_{\mathrm{I}} = \int_0^{t_1} P_{\mathrm{I}}(t)\,\mathrm{d}t \tag{9.6}$$

In Phase II, using the buffer capacitor current, i_2 which was derived from the previous analysis, the power loss can be estimated as,

$$P_{\mathrm{II}} = i_2^2 r_2 \tag{9.7}$$

The corresponding energy loss during Phase II can be estimated as,

$$E_{\mathrm{II}} = \int_{t_1}^{t_2} P_{\mathrm{II}}(t)\,\mathrm{d}t \tag{9.8}$$

Similarly, utilising i_1, power loss in Phase III is,

$$P_{\text{III}} = i_1^2(r_1 + 2r + r_e) \tag{9.9}$$

and the energy loss can be found as,

$$E_{\text{III}} = \int_{t_2}^{t_3} P_{\text{III}}(t)\,\mathrm{d}t \tag{9.10}$$

The same Eqn.(9.8) can be used to estimate the energy loss in Phase IV.

As shown in Appendix E, the above equations were added to the MATLAB-based analytical solution developed in Chapter 8 to compute the energy losses for the four phases of the 12V-to-5V SCALDO cycle. The numerical integration was handled by `trapz(X,Y)` function in MATLAB which computes the integral of Y with respect to X using the trapezoidal method. As shown in Table 9.1, the energy losses of the four phases for a load current ranging from 200 to 600 mA in steps of 50 mA were obtained using this analytical solution.

The corresponding power losses can be calculated using the following equation.

$$\text{Power loss} = \frac{\text{Energy loss}}{\text{Phase time period}} \tag{9.11}$$

Table 9.1 shows the energy losses and the power losses of the 12V-to-5V SCALDO regulator for the four phases of the charge-discharge cycle. Note that Phase I and II are identical to Phase III and IV respectively.

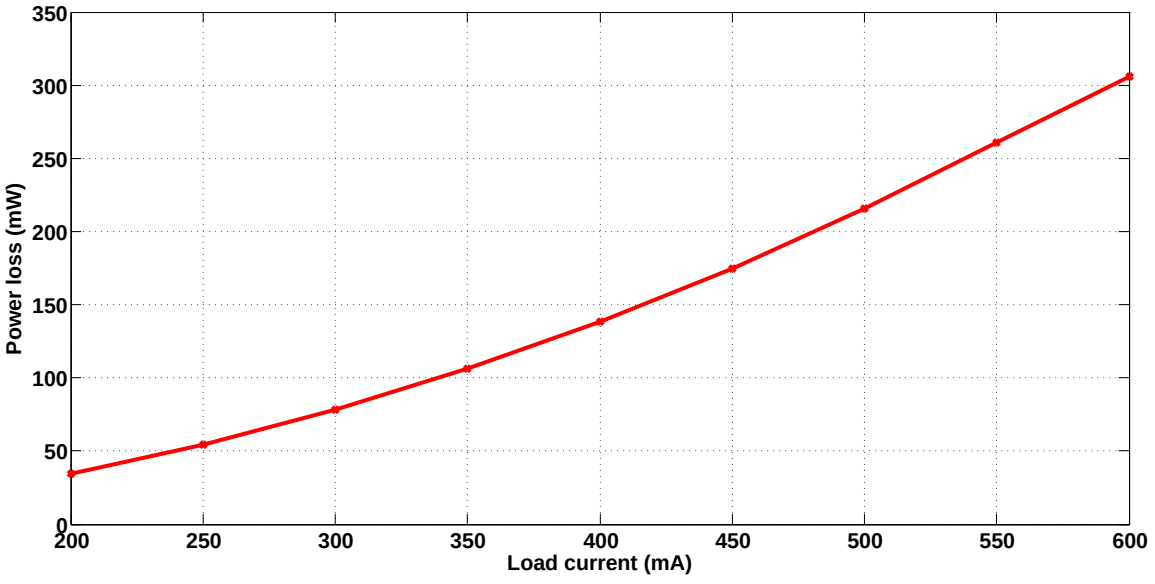


Figure 9.5: Power losses of Phase I of 12V-to-5V SCALDO regulator due to capacitor ESRs and switch on-resistances

Table 9.1: Theoretical estimations of the power/energy losses for the four phases of 12V-to-5V SCALDO regulator

Load current (mA)	200	250	300	350	400	450	500	550	600
Charge time (s)	5.57	4.00	2.97	2.22	1.67	1.24	0.89	0.61	0.37
Energy loss (mJ) Phases I & III	193	217	232	236	231	216	192	158	113
Power loss (mW) Phases I & III	34.7	54.1	78.1	106.0	138.4	174.8	216.0	261.0	306.1
Energy loss (μJ) Phases II & IV	48	75	108	147	192	243	300	363	432
Power loss (μW) Phases II & IV	160	250	360	490	640	810	1000	1210	1440

In Phase I (the charging phase of the supercapacitor), the power loss increases as shown in Fig. 9.5 with the gradually increasing load current. The similar situation occurs during Phase III (the discharging phase). The relationship between the load current and the power loss is assumed to be in the form of;

$$P_L^I = kI_L^m \tag{9.12}$$

In order to find the values k and m, the logarithmic values of normalised load current and normalised power of Phase I were fitted to a polynomial, as X and Y respectively using the `polyfit(X,Y,N)` function in MATLAB. This command finds the coefficients of a polynomial $P(X)$ of degree N that fits the data Y best in a least-squares sense. Using the first order polynomial approximation, the unknowns m and k were found to be 1.9891 and 0.0015 respectively. MATLAB code developed for this analysis is available in Appendix F. The value of m is close to 2 so it reveals that the power losses are proportional to I^2

during the supercapacitor charging. The same scenario applies to the discharge phase as well. This shows that the resistive losses (I^2R losses) are the dominant loss components in the supercapacitor charge and discharge phases of the SCALDO design. Furthermore, it is evident from the theoretical and experimental results of the time periods that I^2 power losses make the charge-discharge time decreases proportionally.

Table 9.1 estimations show the resistive power dissipation of the individual phases of the SCALDO design due to the supercapacitor ESR, switch on-resistances and parasitics of the PCB traces. The total resistive losses of the four phases can be estimated using the power losses of the individual phases. Figure 9.6 shows the total power losses and the losses of the individual phases of the 12V-to-5V SCALDO regulator. The power losses of Phase III and IV are identical to the losses of Phase I and II respectively.

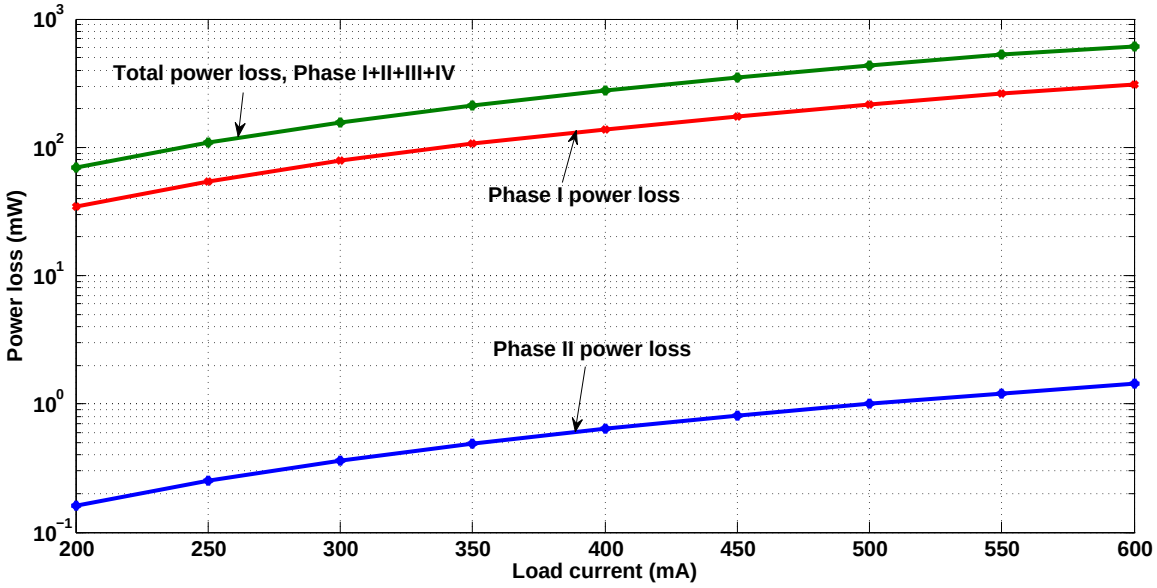


Figure 9.6: Total resistive power losses of the SCALDO 12V-to-5V SCALDO regulator and the power losses of the individual phases

The basic reasons for power losses in the SCALDO technique are associated with the paralleling of capacitors and resistive dissipation. The control circuit power loss was neglected in these analysis. Considering these two factors, the total power losses of the 12V-to-5V SCALDO design were estimated as shown in the Table 9.2.

As shown in the pie chart in Fig. 9.7, power loss due to capacitor paralleling is typically about 1% compared to the total resistive power losses in the design. As shown in this figure, for higher load currents, the effect on paralleling capacitors becomes a smaller percentage of the total power losses and is negligible. The resistive losses have considerable

Table 9.2: Total power loss estimation of the 12V-to-5V SCALDO regulator

Load current (mA)	Total resistive power loss of the four phases (mW)	Approximate capacitor paralleling power loss (mW)	Total power loss (mW)
200	69.6	3	72.6
300	157.0	3	160.0
400	278.1	3	281.1
500	433. 9	3	436.9
600	615.2	3	618.2

impact on the overall design. Therefore, careful selection of low ESR supercapacitors and switches, and compact PCB design is important.

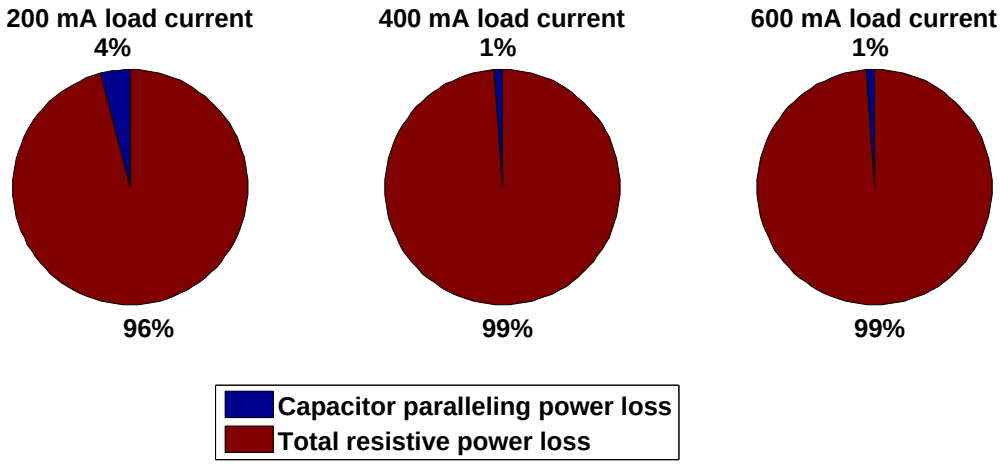


Figure 9.7: Percentage power loss estimation of the 12V-to-5V SCALDO regulator due to capacitor paralleling and resistive terms in the circuit

9.3 SCALDO Loss Measurements

In the following calculations, assume that V_p, I_{in}, V_{reg}, I_L and I_c are the input voltage of the unregulated power supply, the current drawn from the unregulated power supply, the output voltage, the output current and the control circuit current of the SCALDO regulator respectively.

Neglecting the power consumption of the control circuit, the average current drawn from the unregulated power supply during a supercapacitor charge-discharge cycle is,

$$I_{avg} = \frac{[I_{\text{in}} - I_c]}{2} \tag{9.13}$$

The overall power loss of during a SCALDO cycle can be estimated as,

$$P_L = V_p \frac{[I_{\text{in}} - I_c]}{2} - V_{\text{reg}} I_L \tag{9.14}$$

For the 12V-to-5V SCALDO regulator, according to the experimental results shown in Table. 7.6, the total power losses can be calculated using Eqn. 9.14 as shown in Table 9.3.

Table 9.3: Total power loss measurements of 12V-to-5V SCALDO regulator

V_p-Input voltage (V)	I_{in}-Input current (mA)	I_c-Control circuit current (mA)	I_L-Load current (mA)	V_{reg}-Output voltage (V)	P_L-Power loss (mW)
12	160	60	100	4.96	104
12	266	64	200	4.88	236
12	370	64	300	4.84	384
12	470	64	400	4.8	516
12	568	64	500	4.76	644
12	668	64	600	4.72	792

Figure 9.8 shows a comparison of the measured and estimated power losses of the 12V-to-5V SCALDO prototype. The power loss measurement represents the overall losses created by the supercapcitor and its circulation circuit and the LDO. In our estimations, the power loss of the supercapcitor and its circulation circuit was only taken into account. Therefore, the discrepancy between the two traces in Fig. 9.8 is mainly accounted for the power loss of the LDO. Furthermore, as discussed in Chapter 8, because of the limitation of information available in the data sheet, in our estimations, the on-resistance of a PVN012 solid state relay was assumed as a fixed value of 100 mΩ for any load current. But, in low load currents the on-resistance of a PVN012 switch could be a much higher due to MOSFET based construction [236]. As a result, the corresponding power losses due to switch on-resistances could be much larger than the estimated.

9.4 Chapter Summary

Though the SCALDO technique is versatile and simple to appreciate, the prototypes showed several implementation issues. Specifically, the supercapacitor ESRs, the switch on-resistances and parasitics in the PCB traces are the source of quantifiable energy losses. The Laplace transform-based analytical solution discussed in Chapter 8 is extended to estimate the losses during the four phases of SCALDO operation.

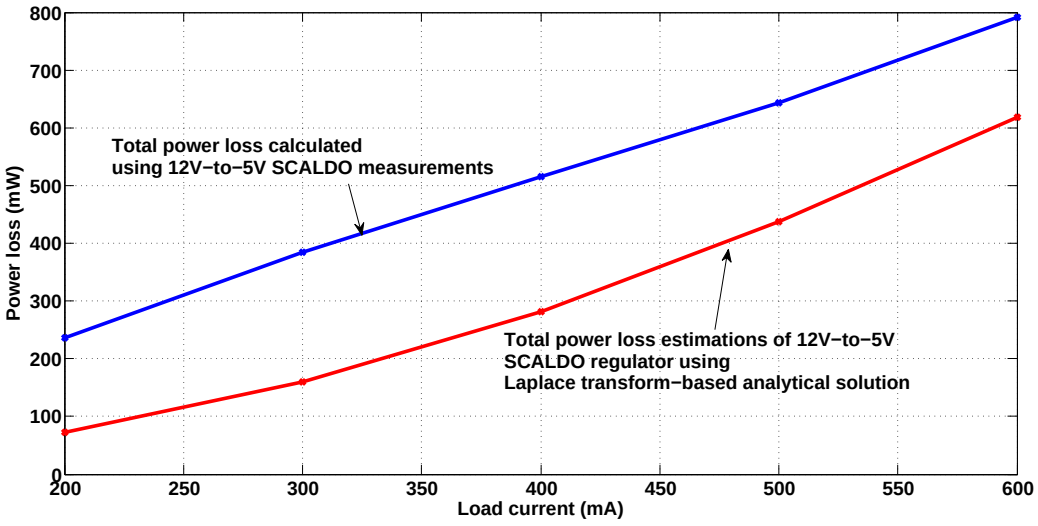


Figure 9.8: Comparison of the measured and estimated power losses of the 12V-to-5V SCALDO prototype

Chapter 10

Conclusions and Recommendations

10.1 Conclusions

This research investigated the theoretical basis and implementation of the patented Supercapacitor Assisted Low Dropout (SCALDO) regulator technique for 12V-to-5V, 5.5V-to-3.3V and 5V-to-2V configurations. The main conclusion of the research is that the SCALDO approach is a viable solution that demonstrates a new approach to the design of DC-DC converters suitable for processor power supplies requiring high end-to-end efficiency (ETEE).

It is the versatile properties of supercapacitors such as extraordinary power density and energy density, larger charge-discharge time, higher cycle time and longer life span that have made them a good choice for the SCALDO technique as a voltage dropper element in the series path. Because of the larger capacitance, the supercapacitor shows an interesting phenomenon in that when it is connected in series to a circuit for a finite time, the capacitor does not act as a blocking element to that circuit due to charging during that time. This property is used to advantage in the SCALDO technique as the series dropper element.

In the SCALDO approach, a single supercapacitor, or an array of supercapacitors, is utilised in the series path to store energy while acting as a voltage dropper element. The stored energy is then released using a very low frequency supercapacitor circulation technique. A commercially available LDO is combined with the supaercapaciotr circulation circuit to maintain the regulation. This technique provides a way of achieving significantly higher efficiencies which are closer to the efficiencies of practical switching regulators. In such SCALDO prototypes the overall end-to-end efficiencies were improved significantly than the conventional linear regulators, while maintaining the useful hallmarks of a linear regulator.

The SCALDO technique allows the development of medium-current linear regulators with the availability of commercial LDOs with output current ratings of up to about 10 A, and thin-profile supercapacitors with DC voltage ratings from 2.3 V to 5.5 V. The SCALDO approach is applicable to standard step-down, DC-DC converter combinations such as 12V-to-5V and 5V-to-3.3V and 5V-to-2V. Although the steady-state parameters,

load regulation and line regulation of these prototypes have performances similar to commercial linear regulators, SCALDO end-to-end efficiencies are significantly higher than the efficiencies achieved in linear regulators used for the same input-output voltage combinations. The SCALDO design has efficiency multiplication factors in the range of 1.33 to 3. For the conventional 5V-to-2V, 12V-to-5V and 5.5V-to-3.3V linear regulators the maximum theoretical efficiency is 40, 42, and 60% whereas in SCALDO proof of concept prototypes had a measured ETEE is of 78, 83 and 80% respectively. The efficiency graphs in Chapter 7 indicate the useful nature of the new SCALDO "lossless-dropper" approach.

Supercapacitors with thin profiles and smaller sizes make the overall SCALDO design compact and simple as shown in the proof-of-concept prototypes. Furthermore, the supercapacitor is the best candidate for the SCALDO technique, as the ESR values (in the range of fractional milliohm to less than 100 milliohm) are less than or comparable to the $R_{DS(on)}$ values of low voltage MOSFETs. Given the low leakage currents in new families of supercapacitors (usually within a range of 5 to about 50 μA, compared to their high charge /discharge current capabilities in the range of tens to several hundred amperes) leakage current related losses of SCALDO technique are negligible. When selecting supercapacitors, all commercially available supercapacitors from different manufacturers thoroughly investigated to select the right components with a higher voltage rating, larger capacitance, low ESR and smaller physical dimensions.

In practical applications such as portable devices, there are switched-mode front ends followed by LDO circuits to provide optimum power management solutions. In this case, switched-mode front ends carry bulky inductors, and additional components to mitigate RFI/EMI artifacts. In SCALDO approach, since the circulation frequency is rather low (in the order of less than ten hertz) no RFI/EMI filters or bulky inductors are required. Elimination of inductors in the SCALDO design, make the final prototype more compact, saving a significant area on the PCB. Supercapacitors that were used in this approach utilise only a smaller area, compared to inductors used in similar capacity switched-mode power supplies.

There were concerns raised from some reviewers of the publications that this SCALDO approach is a merely a variation of the well-known switched capacitor converter. It is important to note that the operation of this topology is quite different from that of standard switched-capacitor DC-DC converters where capacitors are charged from the input supply and later discharged using a different configuration to the load side. In this new technique, after initial start-up, the supercapacitor simply acts as a series (theoretically lossless) voltage dropper maintaining an average DC voltage throughout the cycle, and is not connected in parallel to the input supply cycle at any stage. The differences between the SCALDO and charge pump approaches are detailed in the thesis.

In general, the SCALDO technique is applicable to a wide range of input-output combinations in step down converters, provided that a low dropout regulator is available

for the specified output voltage. Furthermore, this technique can be modified to use larger supercapacitors, in the order of tens of farads to hundreds of farads, to build higher current capability, from 5 to 10 A. With the availability of commercial LDOs, with output current ratings of up to about 10 A, such higher load current implementations of the SCALDO technique are feasible.

As per the experimental analysis carried out using SCALDO prototypes and TEXIO electronic load, SCALDO implementations show excellent transient characteristics for fast varying loads. As with other linear regulator topologies, the SCALDO technique shows good transient characteristics compared with switched-mode counterparts. Furthermore, since this solution is a step-down configuration where the unregulated power supply (or the supercapacitor alone) is supplying the LDO input, high switching current transients do not occur at the input.

Using Laplace transforms, a methodology to accurately predict the performance and associated waveforms of the charge, discharge and transition phases of SCALDO technique was developed. Applying standard data sheet parameters to this analysis permits the prediction of the essential theory of supercapacitor circulation. The Laplase transform-based analytical results and experimental measurements tally well with the practical waveforms observed in a 12V-to-5V converter. These results confirm that the simplifying assumptions used to describe the circuit elements are reasonable and justifiable. The steady-state charge/discharge behaviour was a key contribution of the analysis, but the analytical work was also used to predict the behaviour of the circuit at transition times. This is evident from the MATLAB calculation based figures which showed the transitions from one state to the other, which exactly tally with the experimental results shown in the corresponding oscillographs. The choice of Laplace transform-based MATLAB simulations allows generalization of the SCALDO technique to a wider variety of input-output voltage combinations in future work. Furthermore, the analysis indicates that time discrepancy between the analytical results and the experimental data is due to the effect of switch on-resistances and the resistances of PCB traces in a practical discrete design.

The same Laplase transform-based analysis was further developed to quantify secondary losses of the SCALDO technique. The Laplace transform-based loss calculations of the SCALDO design were revealed that the resistive loss components are the dominant loss contributors in the SCALDO design.

After designing and analysing the performance of 12V-to-5V, 5V-to-2V and 5.5V-to-3.3V SCALDO prototypes, some implementation issues were identified. At higher currents, there are significant losses in the dissipation across capacitor ESRs and switches. These losses are device dependant and can be minimised by careful selection of components. Furthermore, significantly high control circuit current is a remarkable issue in the present design. Measures should be taken to maintain the control circuit current at a bare minimum in future implementations. Losses due to switch transitions are minimal

in this case as the capacitor switching frequency is very low. Power loss due to paralleling capacitors with different voltages is specific to particular implementation. To minimize this effect, the two capacitor voltages can be monitored and when the two capacitors are nearly at the same voltage the transfer from charge to discharge can be implemented.

At the beginning of the research, the control loop designs of DC-DC converters shown in Chapter 4, were studied to analyse behaviour of the control loop of the SCALDO technique. But, with the development of the project, more theoretically and experimentally useful areas were identified as priorities to work on before the control loop analysis. With the revised objectives of the research and the limited time frame, the control loop analysis was kept aside to be continued by another researcher.

In summary, the SCALDO technique of using linear regulators with a lossless voltage-dropper concept with supercapacitors at the input side, achieves highly efficient DC-DC conversion, with a low noise and high current slew rate-capable output. This technique could lead to the development of new DC power supply designs featuring high end-to-end energy efficiencies that are comparable to switch-mode power supplies, but without the significant design efforts needed to minimize static and dynamic losses at high frequencies with associated RFI/EMI artefacts.

10.2 Recommendations

Based on the results of experimental and theoretical analysis of the SCALDO approach, the following recommendations are suggested for future implementations. Minimising the losses associated with the design and making the design more compact, will give the SCALDO technique more opportunity to be a successful candidate for modern battery-operated portable products.

(a) Integrated implementation of SCALDO design

Monolithic integration of switches, LDO and the control circuitry should permit a more compact version suitable for load currents less than 1 A. In such a monolithic integration, discharge through the body diode of the switches can be completely eliminated. Furthermore, measures can be implemented to minimise the control circuit power consumption in a monolithic version. Implementing the body diode-free MOSFET switches with low on-resistance, suitably configured LDO and the low power control circuitry in an integrated circuit, will minimise the losses associated with the discrete implementation of the SCALDO technique.

Further investigations on new SCALDO topologies to minimise the losses should be carried out for a monolithic implementation. As discussed in Chapter 9, implementing the reduced switch SCALDO (RS-SCALDO) design, the switch resistance losses can be

reduced significantly. Using two identical LDOs, the number of switches used in a basic $V_p > 2V_{\text{in}}^{\text{min}}$ SCALDO design can be reduced from four to two, which is a significant achievement. Such a topology is more suitable in implementing the SCALDO in an integrated circuit design. More theoretical and experimental details on this new modification is currently under analysis. Further experimental and theoretical analysis need to be carried out designing RS-SCALDO prototypes with respect to $V_p > 2V_{\text{in}}^{\text{min}}$ and $V_p < 2V_{\text{in}}^{\text{min}}$ topologies.

(b) SCALDO-based VRM implementation

With the increasing demand of modern microprocessors, there is a potential opportunity for an transient response-enhanced, efficiency-improved VRM design in modern processor power supplies. A VRM based on the SCALDO technique would resolve present limitations on output voltage regulation range, transient response and working efficiency of the modern VRMs. The RS-SCALDO design is directly applicable to VRM implementation to minimise losses due to switch resistances.

For higher load currents, monolithic integration would not be feasible. High current LDOs with 10 A capability are commercially available. For higher load currents, a discrete component LDO needs to be developed. Careful selection of supercapacitors with low ESR, and appropriate switches with low on-resistance, is essential. In such implementations, selected RF power MOSFETs without body diodes which have high current capability can be used.

(c) Further improvements to the Laplace transform-based theoretical analysis

Laplace transform-based theoretical analysis has to be done on other developed SCALDO prototypes with respect to higher-order $V_p > 2V_{\text{in}}^{\text{min}}$ and $V_p < 2V_{\text{in}}^{\text{min}}$ topologies and it should be further extended to develop a generalised model for supercapacitor circulation. Furthermore, suitable measures should be taken to minimise the effect of parasitic resistances in discrete SCALDO designs. In the present analysis of Laplace transform based theory of supercapacitor circulation, the first-order model of the supercapacitor is considered. In a future analysis, the higher-order supercapacitor models discussed in Chapter 5 can be considered to get more accurate predictions.

(d) Inrush current limiting at the initial start-up

In the present SCALDO designs, a typical DC power supply was utilised as the unregulated power supply. Therefore, due to the current-limited nature of the power supply, in the initial start-up phase of the circuit of uncharged capacitors, higher inrush currents did not occur at the initial switch-on. However, measures should be taken to limit inrush current in future SCALDO designs because of possible occurrences of high initial inrush current due to various type of unregulated power supplies.

(e) Control loop analysis of the SCALDO technique

With inclusion of a very large capacitor (single supercapacitor or an array of supercapacitors) in series with a commercial LDO, the effect on the control loop of the overall SCALDO design should be analysed. Using this analysis, any essential deviations from the ideal control loop of the typical linear regulator should be identified. This detailed analysis on control loop design aspects of the SCALDO technique is more useful in a monolithic integration of the SCALDO technique. Bode plot-based frequency response analysis can be used in analysing the feedback loop and stability of linear regulators and SMPS. The background and literature available in Chapter 4, can be utilised as a basis to start SCALDO control loop analysis.

(f) Development of a SCALDO based AC input based desktop computer power supply

The SCALDO technique can be utilised in developing an AC input based desktop computer power supply, where overall end-to-end efficiency can be significantly high, while having no RFI/EMI suppression circuits. In designing such a power supply, the bulk DC obtained from the AC mains can be stepped down to a voltage around 12 V using a fast supercapacitor charger. Then 12 V DC can be further stepped down to other useful DC rails such as 5.5 V, 3.3 V, 2.3 V etc using SCALDO-based DC-DC converters. Development of such computer power supply SCALDO converters would assure excellent transient performance and a robust design. Such implementation requires the design of discrete high current capable LDOs.

Appendix A

SCALDO Patent Document

US007907430B2

(12) **United States Patent**
Kularatna et al.

(10) **Patent No.: US 7,907,430 B2**
(45) **Date of Patent: Mar. 15, 2011**

(54) **HIGH CURRENT VOLTAGE REGULATOR**

(75) Inventors: **Nihal Kularatna**, Auckland (NZ); **Lewis Jayathu Fernando**, Kalutara (LK)

(73) Assignee: **WaikotoLink Limited**, Hamilton (NZ)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 174 days.

(21) Appl. No.: **12/338,723**

(22) Filed: **Dec. 18, 2008**

(65) **Prior Publication Data**

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(51) **Int. Cl.**
H02M 3/18 (2006.01)
G05F 1/00 (2006.01)
H02J 7/00 (2006.01)

(52) **U.S. Cl.** **363/59**; 323/266; 320/167

(58) **Field of Classification Search** 363/59; 323/266; 327/536; 320/167, 142
See application file for complete search history.

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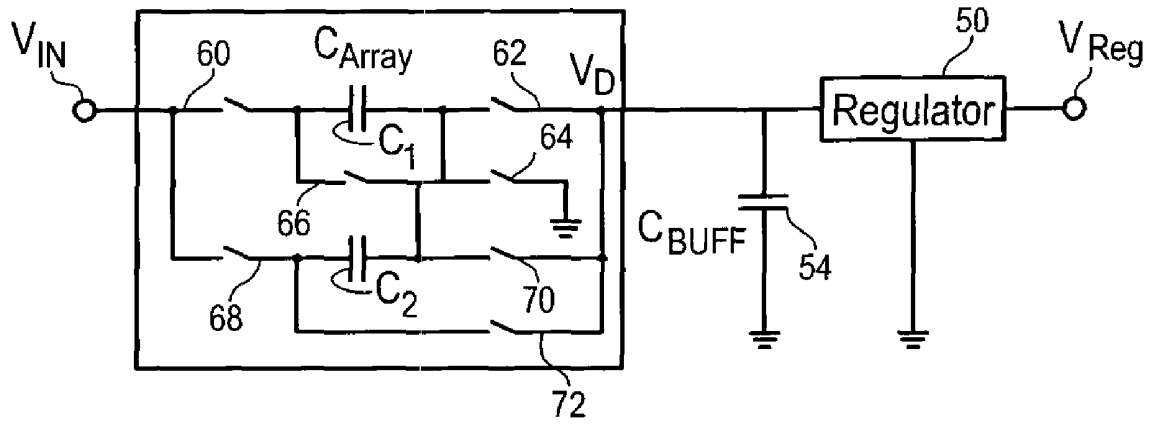
Primary Examiner — Shawn Riley
(74) *Attorney, Agent, or Firm* — Morrison & Foerster LLP

(57) **ABSTRACT**

A linear voltage regulator which includes on its input side an array of switched super capacitors coupled between the power source and the load. This apparatus is capable of delivering currents typically from milliamperes to greater than several amperes at very low switching frequencies. In addition by using capacitors rather than resistors or transistor devices to drop voltage on the input side, power consumption is reduced. The array of capacitors is switched by simple analog circuitry or a switching logic with or without a processor subsystem and the capacitors themselves are of the super capacitor type, thus providing very high capacitance, and are effectively series connected during certain phases of operation with the input terminal of the conventional linear voltage regulator portion of the apparatus. Energy stored in the super capacitors during the various phases of operation is reused.

15 Claims, 6 Drawing Sheets



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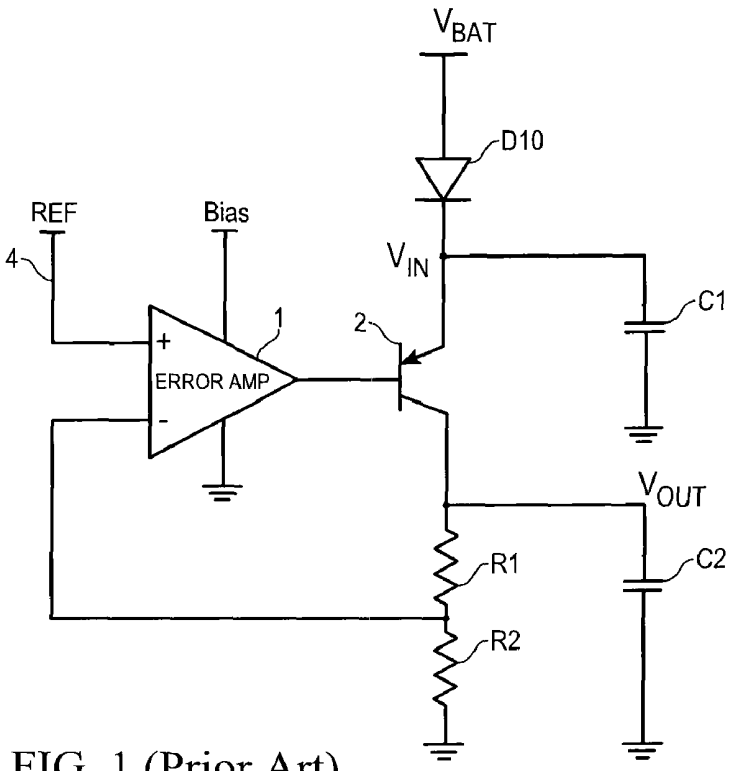


FIG. 1 (Prior Art)

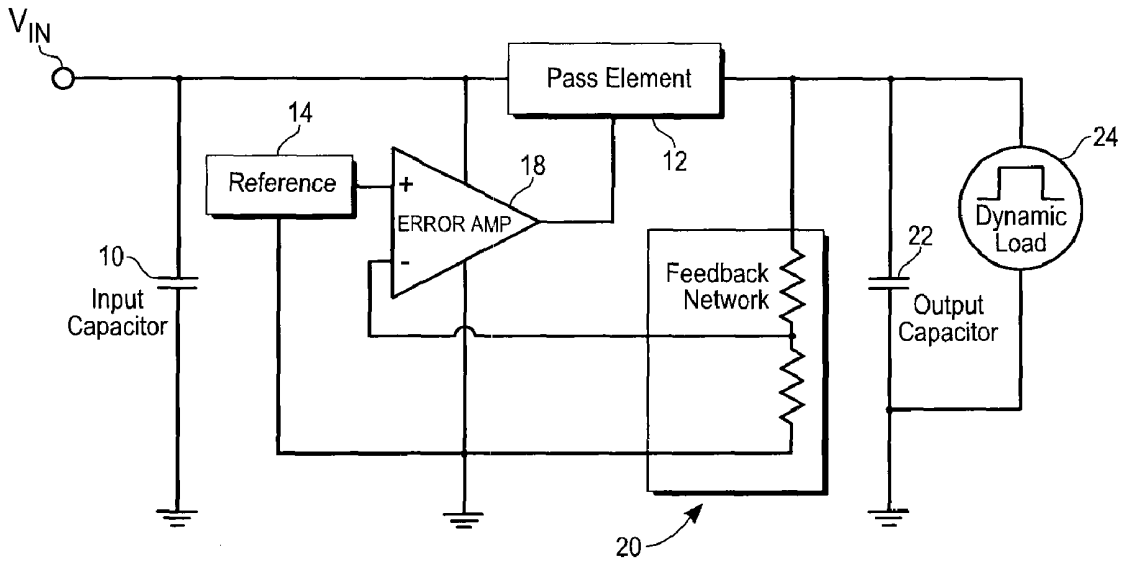


FIG. 2A

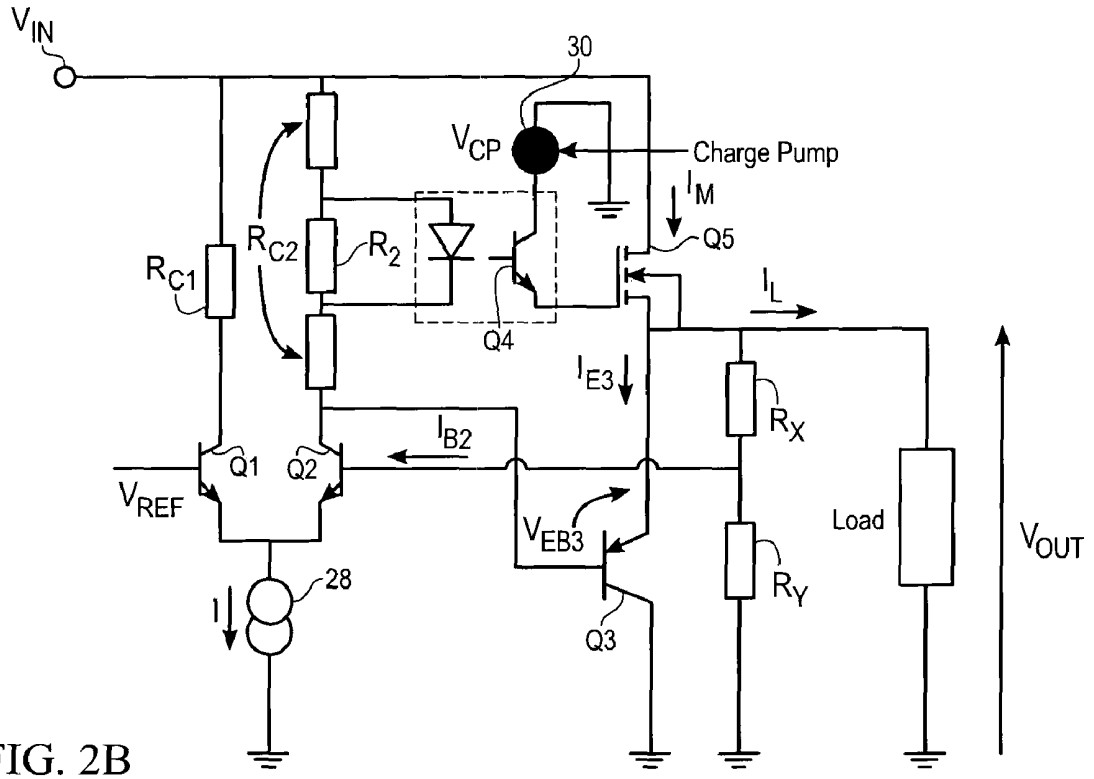

V_{IN}
30
V_{CP}
Charge Pump
I_M
Q5
R_{C2}
R_2
R_{C1}
Q4
I_L
I_{E3}
R_X
I_{B2}
Q1
Q2
V_{REF}
V_{EB3}
Load
V_{OUT}
28
I
R_Y
Q3

FIG. 2B

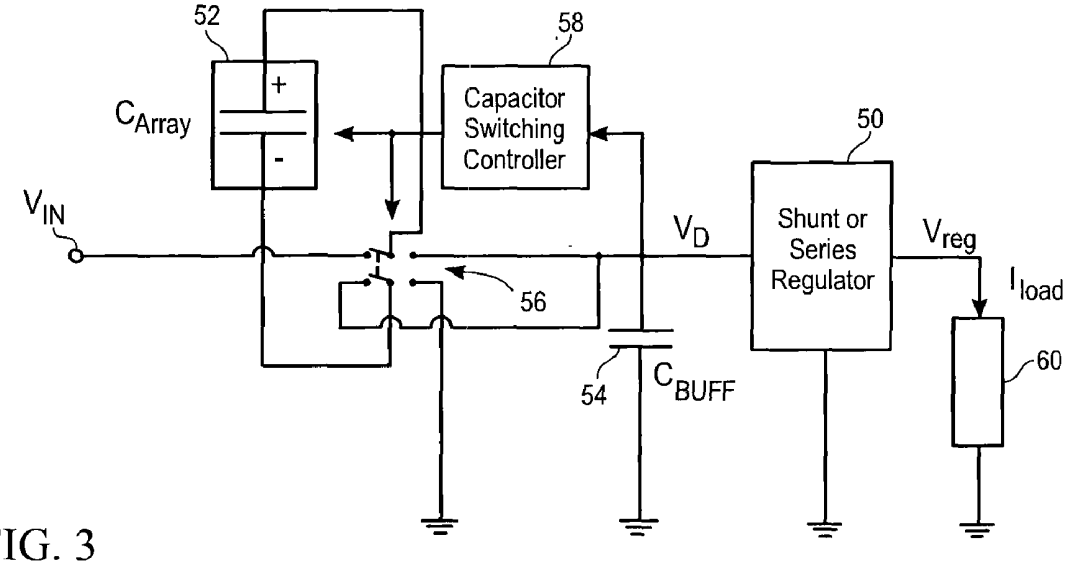

52
58
C_{Array}
+
-
Capacitor Switching Controller
50
V_{IN}
V_D
Shunt or Series Regulator
V_{reg}
I_{load}
56
60
54
C_{BUFF}

FIG. 3

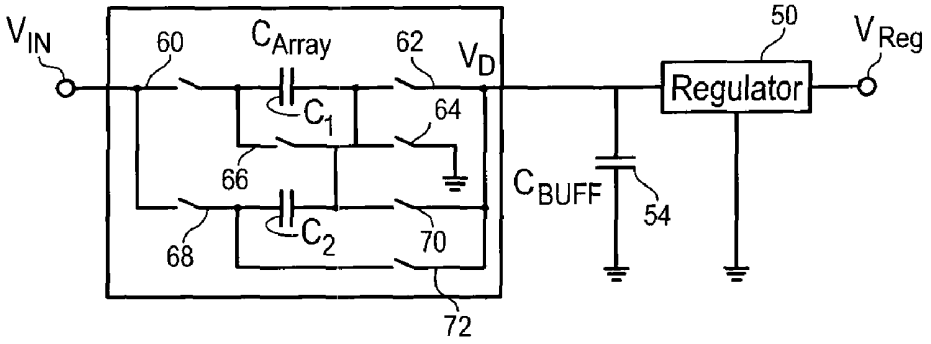


FIG. 4A

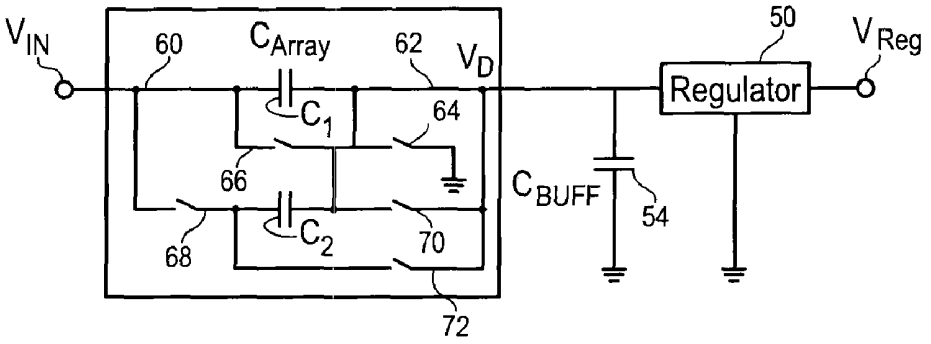


FIG. 4B

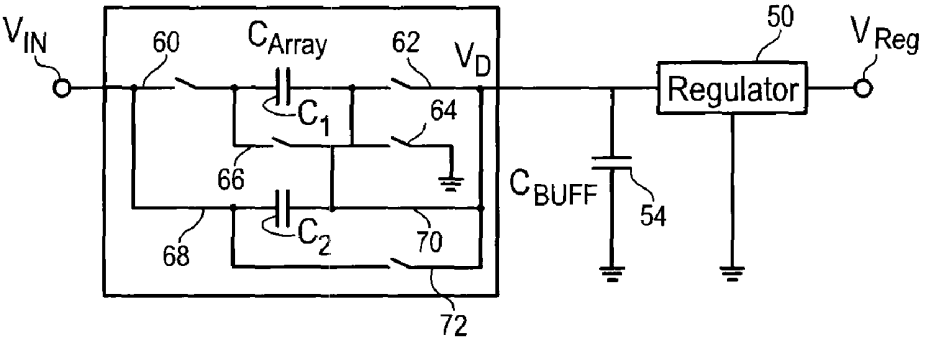


FIG. 4C

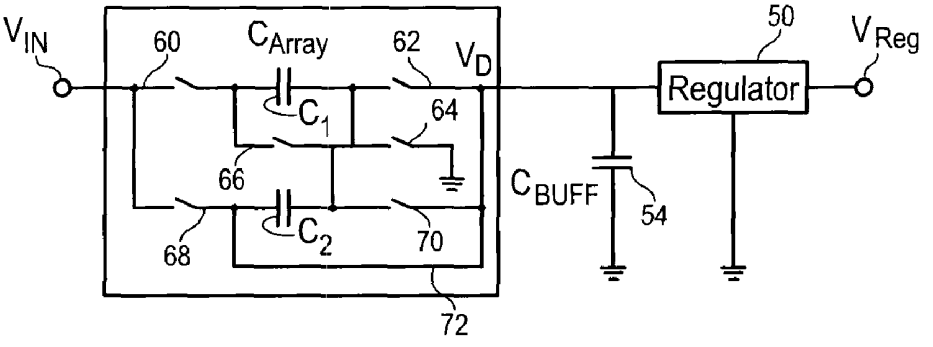


FIG. 4D

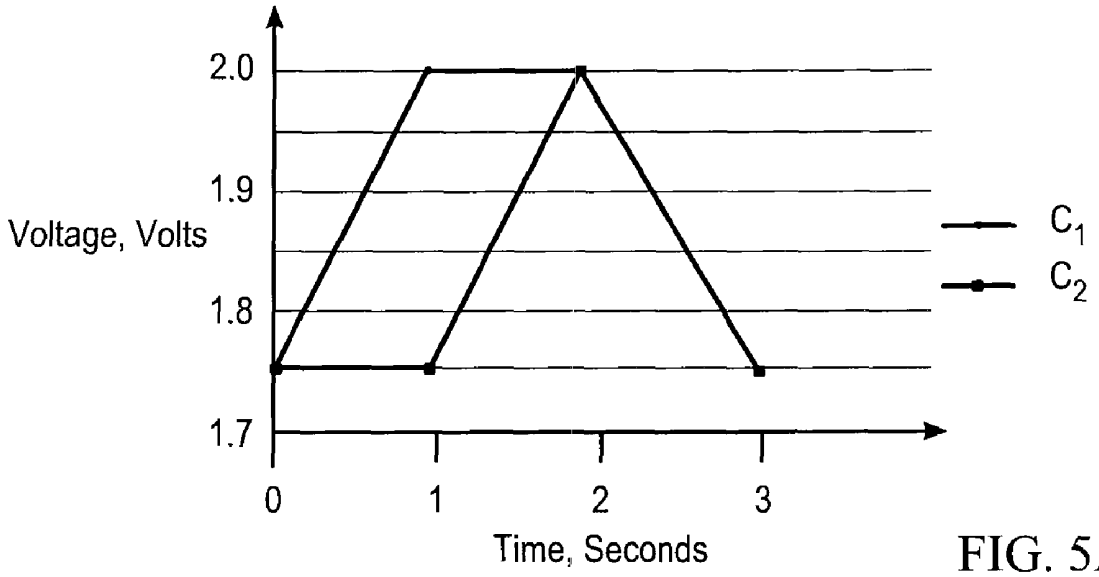

2.0
1.9
1.8
1.7
Voltage, Volts
0
1
2
3
Time, Seconds
C1
C2

FIG. 5A

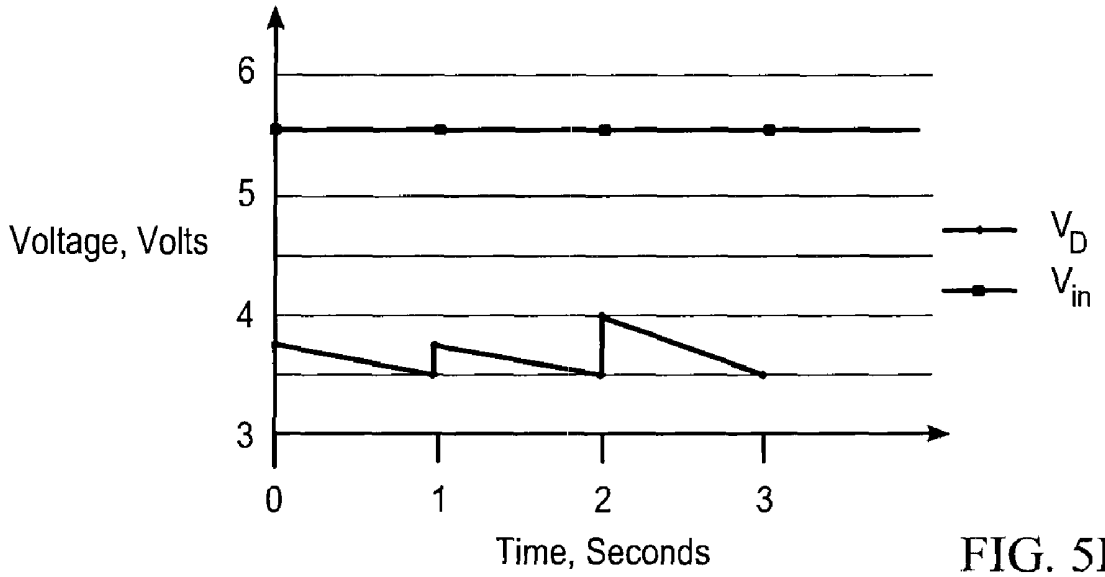

6
5
4
3
Voltage, Volts
0
1
2
3
Time, Seconds
VD
Vin

FIG. 5B

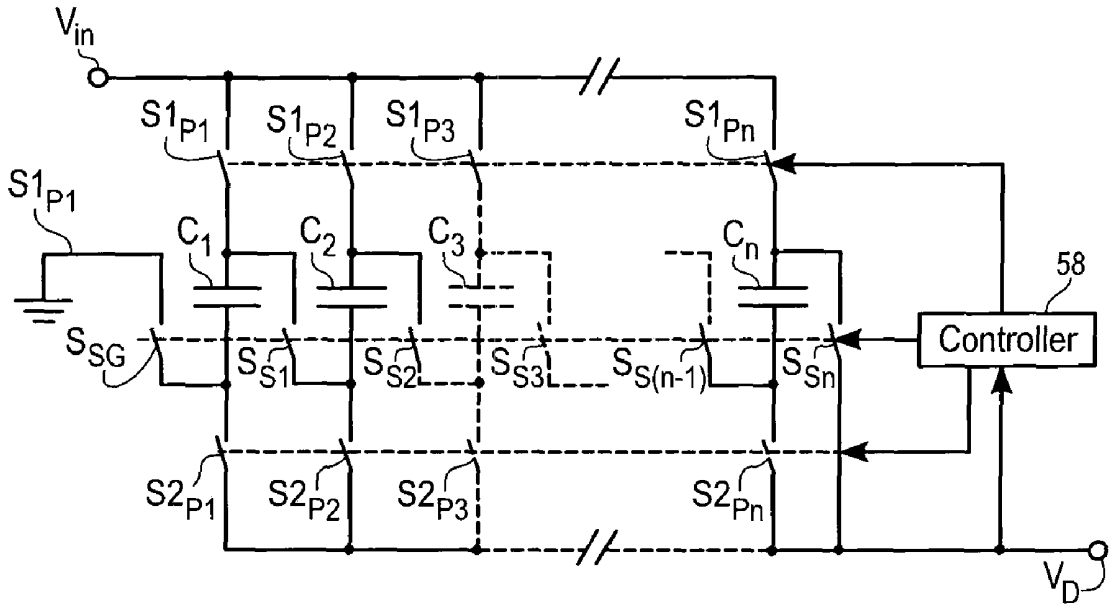

Vin
S1P1
S1P2
S1P3
S1Pn
S1P1
C1
C2
C3
Cn
58
SSG
SS1
SS2
SS3
SS(n-1)
SSn
Controller
S2P1
S2P2
S2P3
S2Pn
VD

FIG. 6A

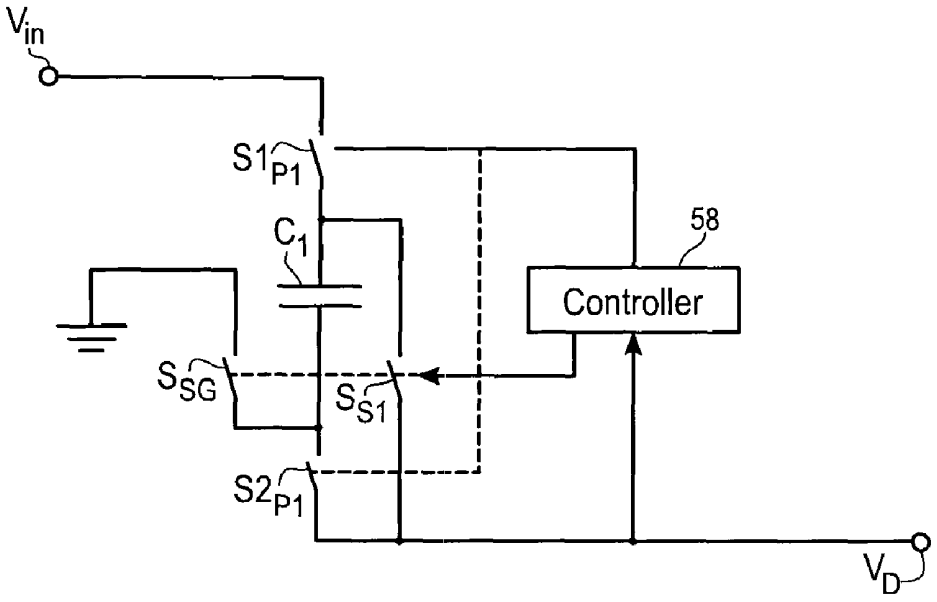

Vin
S1P1
C1
58
Controller
SSG
SS1
S2P1
VD

FIG. 6B

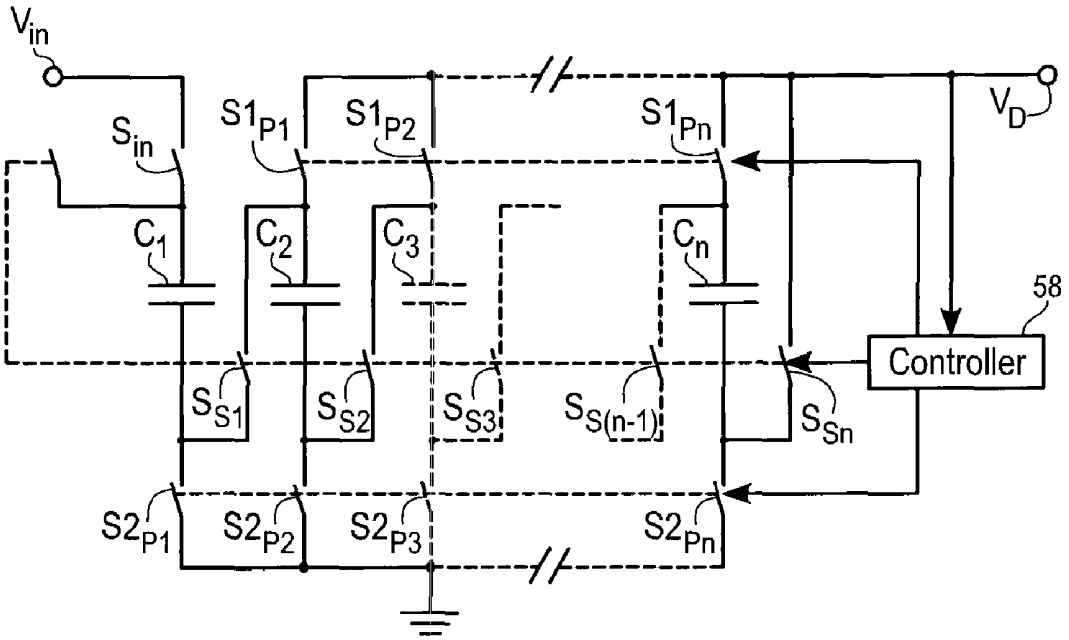

V_{in}
S_{in}
$S1_{P1}$
$S1_{P2}$
$S1_{Pn}$
V_D
C_1
C_2
C_3
C_n
58
Controller
S_{S1}
S_{S2}
S_{S3}
$S_{S(n-1)}$
S_{Sn}
$S2_{P1}$
$S2_{P2}$
$S2_{P3}$
$S2_{Pn}$

FIG. 6C

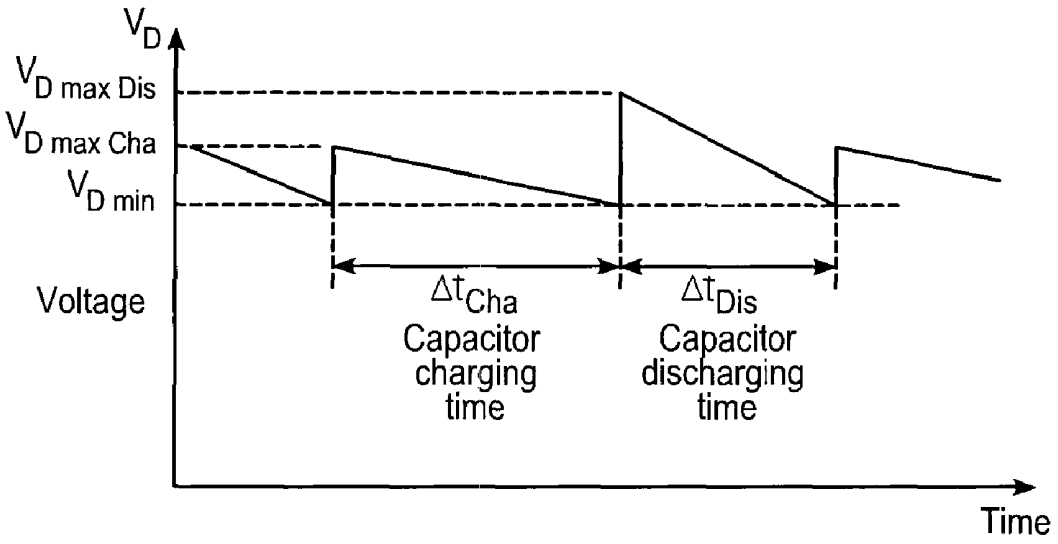

V_D
$V_{D\ max\ Dis}$
$V_{D\ max\ Cha}$
$V_{D\ min}$
Voltage
Δt_{Cha}
Capacitor charging time
Δt_{Dis}
Capacitor discharging time
Time

FIG. 7

HIGH CURRENT VOLTAGE REGULATOR

FIELD OF THE INVENTION

This disclosure relates to voltage regulators (power supplies) used for supplying electric current.

BACKGROUND

Voltage regulators are well-known in the electrical engineering field. They are also referred to as "power supplies" and are electronic or electrical circuits which output electric current at a particular DC (direct current) voltage level. They are widely used in electrical and electronic devices. Typically the actual electricity source is mains current or a battery and these voltage regulators convert and condition the battery output or mains current to a particular voltage level.

All electronic circuits, analog or digital, require such a well-regulated and stabilized DC power supply. An ideal DC power supply provides a constant output voltage irrespective of the value of the load current and the nature of the load while the output is free of noise, ripple and transient dips or surges. In modern electronic systems, DC power requirements vary widely. In small portable electronic devices, DC power supplies carry multiple "rail" voltages and values may vary from ±15 V to sub 1 V levels. Common values of voltage rails (supply) are 48V, 24V, 12V, 9V, 6V, 5 V, 3.3 V, and 1.8 to 3 V. Typical current output capability varies from tens of milliamperes to several amperes.

For larger non-portable devices with processor subsystems, a DC power supply typically has an output voltage from +5 volts to less than 3.3 volts with current requirements of several to 150 amperes. Efficiency of a power supply, particularly in high current systems, is of primary concern to avoid power wastage. A requirement for a portable device of course is also to achieve compactness of the power supply along with efficiency so as to minimize battery drain. Typical DC power supplies are linear, switch mode, and switched capacitor type, although these all have various deficiencies.

FIG. **1** shows a prior art "low drop out" (LDO) linear voltage regulator of FIG. **1** of LoCascio U.S. Pat. No. 4,779,037, incorporated herein by reference in its entirety. This is a low drop out voltage regulator with a switched redundant input. "Low drop out" refers to having a low dropout voltage. Such low dropout voltage regulators are of the type generally referred to as linear voltage regulators. The FIG. **1** device includes error amplifier **1** to compare an input reference voltage applied at terminal **4** to a signal proportional to the output voltage. Error amplifier **1** controls transistor **2** through which output current flows by adjusting transistor **2** so the output voltage at terminal V_{out} equals a fixed multiple of the reference voltage. The source or input voltage, which is typically unregulated, is supplied here from a battery connected at terminal VBAT via a diode D_{10} to the emitter of transistor **2**.

In FIG. **1**, a redundant source voltage V_{in} is also supplied, although this is not always the case with such devices. In this case, the redundant voltage is supplied from capacitor C_1. Capacitor C_2 is provided for filtering at the output terminal V_{out}. Also in this case coupled at the collector of transistor **2** are two series connected resistors R_1 and R_2. Such a voltage regulator is characterized by its "drop out" voltage, which is the lowest source voltage which allows the regulator output voltage to remain substantially constant at some proportion of the reference voltage.

Voltage regulators have several performance parameters. One is noise created by circuit elements in the regulator circuit. High noise levels are undesirable since they may be

RF (radio frequency) signals which interfere with operation of other portions of an electronic device of which the voltage regulator is a part. Most switch mode regulators generate noise at a frequency of 100 kHz to 3 MHz, which is undesirable. Another parameter is the output current capability since it is important for certain applications that the voltage regulator output relatively high levels of current. Typically however, high levels of current require switching regulators rather than low noise linear regulators of the type shown in FIG. **1**. It is a drawback that typically linear regulators are not capable of high amperage (current) output due to excessive heating effects in the series or the shunt transistor elements in the regulator.

Efficiency is also important and refers to the proportion of input power dissipated in the voltage regulator. The approximate efficiency of a typical linear voltage regulator (of the type shown in FIG. **1**) is proportional to V_{out}/V_D, where in FIG. **1** V_D is the supply voltage of the battery VBAT. Often a minimum amount of voltage drop is needed between the supply voltage and output voltage to achieve regulation, hence there is a limit to the highest efficiency possible in a given design. However, use of a series resistor or allowing a larger voltage drop across the transistor to drop the voltage is inefficient since these are inherently power dissipation devices and inefficient. The present inventors have identified that it would be useful to be able to drop part of the difference between the supplied voltage and the regulated output in a non-resistive fashion to improve efficiency. Clearly the lower this effective input voltage to the voltage regulator, the higher its efficiency.

SUMMARY

In accordance with the invention, a linear voltage regulator circuit has its power input terminal series connected to one or more super capacitors. The super capacitors are coupled thereto by an array of switches. The super capacitor array functions as an input voltage dropper in lieu of a resistor or transistor with a large voltage drop as described above. A capacitor in series takes up part of the voltage drop which directly contributes to heat dissipation and it allows the circuit to reuse the energy stored in the capacitor. Once a capacitor is fully charged, it blocks DC current, so series capacitors have not been a practical means of reducing power dissipation of a linear regulator. However, very large capacity capacitors (so-called "super capacitors") are now commercially available which take a longer time to charge and hence allow for a low switching frequency of the capacitors. This has the advantage of charging the super capacitors for a relatively longer time without blocking the DC current path and indirectly reducing high frequency noise generation, due to the low frequency switching of capacitors.

Since even a super capacitor alone and in series when subject to DC voltage charges up eventually and stops conducting, the capacitor alone is not suitable. However by using a switched capacitor array, the capacitors are cyclically charged and discharged to provide a suitable voltage drop with minimal loss. This provides a voltage regulator of the linear type that has high efficiency, low noise generation and outputs high current if needed. In embodiments of the present voltage regulator, the capacitor changeover frequency, which relates to the switching frequency, is only in the range of typically fractional Hz to 300 Hz, about 1/1000 of that of switched mode regulators and which advantageously is not RF. The present regulator in various embodiments delivers currents in excess of 1 ampere, up to 10 amperes or more. Typically such high current draw requirements in the past

required switching voltage regulators, which are inherently noisy, rather than a low noise linear voltage regulator as used here. Furthermore efficiency of the present regulator is about 60-85% and especially high under no-load conditions.

Super capacitors are well-known devices also referred to as electric double-layer capacitors or ultracapacitors. The term "super capacitor" here is intended to include these. Such devices are electrochemical capacitors having an unusually high energy storage density compared to ordinary, for instance, electrolytic capacitors. They store charges thousands of times greater than a physically similar sized electrolytic capacitor. For instance, a typical D-cell sized electrolytic capacitor has a capacitance of only hundreds of microfarads, while the same size super capacitor has a capacitance range of 0.1 farads to several farads, or even up to a few hundreds of farads which is an improvement of about 10,000 times. Commercial double-layer capacitors are available having capacities as high as 5,000 farads.

Unlike traditional capacitors, electric double-layer or super capacitors do not have a conventional dielectric, but instead include a structure that contains an electrical double layer. Hence, the effective thickness of the dielectric is exceedingly thin, which combined with a very large surface area, is responsible for the high capacitances. Each of the two layers by itself is quite conductive, but at the interface where the layers are effectively in contact, no significant current can flow between the layers. However the double layer can typically only withstand a relatively low voltage, so such super capacitors typically have relatively low voltage ratings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows schematically a prior art linear voltage regulator of the low drop out type.

FIGS. **2**A and **2**B show variations of the FIG. **1** device, also in the prior art.

FIG. **3** shows in a combined schematic and block diagram a linear voltage regulator in accordance with the present invention.

FIGS. **4**A-**4**D show operation of the FIG. **3** circuit.

FIGS. **5**A and **5**B show graphically operation of the FIG. **3** circuit.

FIGS. **6**A, **6**B and **6**C show variations of the FIG. **3** regulator.

FIG. **7** shows graphically capacitor switching in accordance with FIG. **6**B.

DETAILED DESCRIPTION

FIGS. **2**A and **2**B show schematically in the prior art variations of the FIG. **1** LDO linear voltage regulator. The FIG. **2**A type is referred to as a series type and is typically found in commercial-type integrated circuit voltage regulators, while FIG. **2**B shows a shunt or parallel type voltage regulator. The FIG. **2**A circuit includes input capacitor **10** coupled to a pass element **12**. The reference voltage terminal **14** and the feedback network **20** are coupled to the error amplifier **18**. On the output side, there is a second (output) capacitor **22** and dynamic load **24** (not shown in FIG. **1**). The FIG. **2**B device includes an error amplifier based on transistors Q**1** and Q**2** and the current source **28**. Resistors RC**1** and RC**2** are part of this error amplifier. A charge pump **30** is connected to a third transistor Q**4** which may be inside an opto-isolator in this shunt regulator configuration. Power transistors Q**3** and Q**5** are connected between the unregulated input, regulated output terminal and ground, with the resistors R_X and R_Y as shown functioning as the feedback network to have closed loop regulation.

FIG. **3** shows schematically in accordance with the invention a low dropout type linear voltage regulator. The main portion of this is the conventional shunt or series LDO linear voltage regulator **50**, which corresponds for instance to the prior art devices of FIGS. **1**, **2**A or **2**B. In this case capacitance C_{Array} **52** is a super capacitor array with associated switches **56** arranged according to the level of the unregulated input voltage applied at terminal Vin as explained below. Capacitor C_{BUFF} **54** may be a super capacitor or any other suitable capacitor which is used to power the LDO for capacitor charging and discharging change-over points. Operation of switches **56** is controlled by conventional capacitor switching controller **58** which is, e.g., logic circuitry, mixed signal circuitry or a suitable microcontroller. The regulated output voltage is at terminal V_{reg}, corresponding to V_{out} in FIG. **1**. The load is shown generally at **60**. The capacitors in the array C_{Array} are switchably connected by switches **56** to the V_D input terminal of regulator **50** so as to take up the larger part of the voltage drop between terminals V_{in} and V_D so that efficiency is improved.

While charging such a series connected super capacitor array, it takes up most of the dropout voltage energy, related to $(V_{in}\text{-}V_D)*I_{load}$, which is stored in the capacitors of the array C_{Array} and the voltage drop is taken over by the capacitors in the array C_{Array}. This is in contrast to a conventional linear regulator where this drop is across a resistive element, such as a transistor or resistor and is responsible for the bulk of the efficiency loss. Thereby efficiency of the present regulator is high and comparable to that of a switching regulator. Using an array of super capacitors C_{Array} and switches **56** to charge up to approximately the voltage level of V_{in}-V_D, the FIG. **3** circuit can operate with ideally no loss, except for whatever internal resistance is present in the super capacitor array C_{Array} and/or the switches **56**, and, any transient related energy losses.

During periods of charging and discharging, the voltage variation across the capacitor array, C_{Array}, is

$$\Delta V_C = \frac{I_L \Delta t}{C},$$

where I_L is the load current and Δt is the charge or discharge time. If the value C is high, which is of course the case with the super capacitors in C_{Array}, then ΔV_C is small during the time of charging and discharging while passing a current through the capacitors to keep the regulator and load working. That is, there are no dropouts. The goal is to keep the effective ΔV_C within the value of V_{Dmax}-V_{Dmin}, where these refer respectively to the maximum and minimum voltages at terminal V_D during the charging or discharging modes.

In this case the super capacitors in the array C_{Array} are switched by switches **56** at relatively low frequencies to minimize noise. The goal is to switch array C_{Array} to obtain the best effective ΔV_C over a full switching cycle, as explained below.

FIGS. **4**A-**4**D illustrates an exemplary capacitor switching cycle for the FIG. **3** apparatus. FIG. **4**A shows key elements of the FIG. **3** circuit with like elements similarly labeled, except that here instead of showing C_{Array} **52** and the switches **56** generally, a more detailed network is shown with two super capacitors C_1 and C_2 and associated switches **60**, **62**, **64**, **66**, **68**, **70** and **72**. In one embodiment these switches are each a

transistor or a solid state relay with sufficient capacity to carry the expected currents at the required voltages. Such transistors are generally referred to as "power transistors" and may be integrated or discrete devices. Possible switch devices are bipolar power transistors, power mosfets, insulated gate bipolar transistors, thyristors, or solid state relays. Any type of semiconductor switch with adequate capacity or even a mechanical relay is usable. In FIG. **4**D, load **60** is not shown, merely for simplicity. FIG. **4**A shows the circuit itself, but not in any operating mode, and is only for purposes of circuit illustration.

FIGS. **4**B-**4**D show the three consecutive operating phases, labeled Phase 1, Phase 2 and Phase 3, through which the circuit cycles on a continuous basis. It is to be understood that each switch in FIG. **4** is conventionally controlled by the capacitor switching controller **58** of FIG. **3**, also omitted here for simplicity. Such control of switches is routine in the power supply field and so no further detail is provided.

In Phase 1 in FIG. **4**B, assume the input voltage V_{in} is 5.5 V, the capacitor array has no internal resistance and the resistance across each switch in its ON state is zero. In Phase 1, capacitor C_1, which is connected by switch **60** to terminal V_{in}, charges from 1.75 V to 2 V. Capacitor C_2 remains at its previous state (since it is disconnected by switches **68** and **70**) at 1.75 V. The voltage at terminal V_D, which is connected by switch **62** to capacitor C_1, increases to 5.5−1.75 volts=3.75 V, then decreases linearly to 5.5−2 V=3.5 V.

In FIG. **4**C which is Phase 2, capacitor C_1 is disconnected at all three of its terminals and capacitor C_2 as shown is series connected between terminals V_{in} and V_D. At this point capacitor C_1 remains at 2 V since it is disconnected, while capacitor C_2 charges from 1.75 V to 2 V. Then V_D increases to 5.5−1.75 V=3.75 V, then decreases linearly to 5.5−2 V=3.5 V. Typically the voltage is cycling only between 3.75 and 3.5 volts in these two phases. In the last Phase 3 shown in FIG. **4**D, both capacitors C_1 and C_2 are disconnected from input terminal V_{in}, but are connected to discharge via switch **72** to terminal V_D. Capacitor C_1 discharges from 2 to 1.75 V and similarly capacitor C_2 discharges from 2 to 1.75 V. Hence the voltage at V_D increases to 4 V and then decreases linearly to 3.5 V. The total voltage swing here is only 3.5-4 V, which is a relatively modest, thereby providing relatively linear voltage. As pointed out above, the typical switching frequency is a fraction of a Hz to 300 Hz, so each phase is approximately a few seconds to 3 milliseconds in duration.

FIGS. **5**A and **5**B show this operation graphically. In FIG. **5**A, the horizontal scale is time (in seconds) and the vertical scale is voltage (in volts). There are two plots, for capacitors C_1 and C_2.

FIG. **5**B shows operation of the regulator at terminals V_D and V_{in} where again the horizontal scale is seconds and the vertical scale volts. The supply voltage at terminal V_{in} is constant, while the voltage at terminal V_D fluctuates within the relatively narrow range of 3.5-4 V.

FIGS. **6**A, **6**B and **6**C show schematically variations of the capacitor array and switches portion of the FIG. **3** circuit, all being embodiments in accordance with this disclosure. For the FIG. **6**A embodiment, the capacitor array $C_1, C_2, \ldots, C_n$ and switches are arranged for an input voltage V_{in} which is expected to be less than twice the capacitor array output voltage at terminal V_D. The switches here are designated $S1_{p1}, \ldots, S1_{pn}$ (first row); $S_{s1}, \ldots, S_{sn}$ (second row) and $S2_{p1}, \ldots, S2_{pn}$ (third row), and switch S_{SG}. The number of capacitors used here, illustrated as being "n" in number, is a design choice dependent on the value of $V_D/(V_{in}-V_D)$ as explained in more detail below. Hence all the capacitors here are connected in parallel relative to the input terminal V_{in} when charging. All the parallel connected capacitors charge at once, not one by one as in the FIG. **4** embodiment. However for discharge purposes, the switches are set so all the capacitors are coupled in series to terminal V_D.

FIG. **6**B shows a simpler embodiment with only a single capacitor C_1 in the switched capacitor array which is used when the supply voltage at V_{in} is approximately twice the value of the voltage at V_D. The four switches here are designated $S1_{p1}$, $S2_{p1}$, S_{s1} and S_{SG}.

FIG. **6**C shows in another embodiment an arrangement of capacitors and switches for the case where the supply voltage at V_{in} is greater than twice that at V_D. Here capacitors C_1, $C_2, \ldots, C_n$ are in series when connected to terminal V_{in}. The switches here are arranged somewhat similar, but not the same, as in FIG. **6**A, again being arranged in three rows (banks). All the capacitors are connected in parallel to discharge to terminal V_D. The number of capacitors n here again depends on the ratio of the voltage at terminal V_{in} to V_D.

In the FIG. **6**C embodiment for high voltage drop$\{(V_{in}-V_D)>V_D\}$ recovery, all the capacitors in the array are connected in series and then that series connected capacitor array is connected between the power source and the input terminal, and then the capacitors are connected in parallel and discharged to the input terminal. For low voltage drop$\{(V_{in}-V_D)<V_D\}$ recovery, all the capacitors in the array are connected in parallel and then that parallel connected capacitor array is connected between the power source and the input terminal, and then the capacitors are connected in series and discharged to the input terminal.

Table 1 indicates relationships for calculating the capacitor values, numbers, and other important technical parameters for design purposes:

TABLE 1

Parameter	$V_{in} < {}_2V_{Dmin}$	$V_{in} > 2V_{Dmin}$
n	$n \geq \frac{V_{Dmin} + \Delta V_D + I(3R_{ON} + r_S)}{V_{in} - V_{Dmin} - I(R_{ON} + r_S)}$	$n \leq \frac{V_{in} - V_{Dmin} - I(3R_{ON} + r_S)}{V_{Dmin}\lvert\Delta V_D \rvert I(R_{ON}\lvert r_S)}$
V_{Cmax}	$V_{in} - V_{Dmin} - \frac{I}{n}(2R_{ON})$	$\frac{I}{n}\{V_{in} - V_{Dmin} - I(n+1)R_{ON}\}$
$V_{Dmax,Dis}$	$n(V_{in} - V_{Dmin}) - I((n+3)R_{ON} + (n+1)r_S)$	$\frac{1}{n}[(V_{in} - V_{Dmin}) - I\{(n+3)R_{ON} + (n+1)r_S\}]$
$V_{Dmax,Cha}$	$\frac{1}{n}[nV_{in} - V_{Dmin} - I\{(n+3)R_{ON} + (n+1)r_S\}]$	$[V_{in} - nV_{Dmin} - I\{(n+3)R_{ON} + (n+1)r_S\}]$

TABLE 1-continued

Parameter	$V_{in} < {}_2V_{Dmin}$	$V_{in} > 2V_{Dmin}$
Δt_{Dis}	$\frac{C}{n}\left[\frac{nV_{in} - (n+1)V_{Dmin}}{I} - \{(n+3)R_{ON} + (n+1)r_S\}\right]$	$C\left[\frac{V_{in} - (n+1)V_{Dmin}}{I} - \{(n+3)R_{ON} + (n+1)r_S\}\right]$
Δt_{Cha}	$C\left[\frac{nV_{in} - (n+1)V_{Dmin}}{I} - \{(n+3)R_{ON} + (n+1)r_S\}\right]$	$\frac{C}{n}\left[\frac{V_{in} - (n+1)V_{Dmin}}{I} - \{(n+3)R_{ON} + (n+1)r_S\}\right]$
η_r	$1 + \frac{1}{n}$	$1 + n$

In Table 1:
V_{in} Input voltage to the circuit
ΔV_D Expected minimum voltage fluctuation of V_D
R_{ON} On resistance of the switch
r_S Internal resistance of the capacitors
n Number of capacitors.
V_{Cmax} Maximum voltage across each capacitor
$V_{Dmax,\,Dis}$ Maximum voltage at V_D when discharging
$V_{Dmax,\,Cha}$ Maximum voltage at V_D when charging
Δt_{Dis} Time taken to discharge the capacitors to minimum V_D (V_{Dmin}) from $V_{Dmax,\,Cha}$
Δt_{Cha} Time taken to charge the capacitors from its discharged voltage until V_D reached to V_{Dmin}. When the discharged capacitors start charging V_D goes to $V_{Dmax,\,Cha}$ and gradually decrease till V_{Dmin}
η_r Supercapacitor based efficiency improvement factor, which is the overall efficiency increasing factor of the present technique.

$$\eta_r = \frac{\text{Input power when directly connect the regulator to } V_{in}}{\text{Input power when connect the regulator to } V_{in} \text{ through this technique}}$$

Table 1 thereby shows (for the two indicated voltage regimes) equations to select the number of capacitors (n) in the capacitor array, the voltage rating of each capacitor (V_h Cmax) the parameters for finding the switching frequency (Δt_{Dis}, Δt_{Cha}), the voltage variation limits of the regulator input ($V_{Dmax.Dis}$, $V_{Dmax.Cha}$) and the relative efficiency increase (η_r) due to the present method. The two columns of Table 1 $V_{in}<2V_{Dmin}$ and $V_{in}>2V_{Dmin}$ show the relationship for the switching schemes of FIGS. **6**A and **6**C respectively.

These equations are derived based on these assumptions: the power consumed by the controller circuit is negligible compared with the output power; all the capacitors are identical and have equivalent series resistance of r_s; all the switches are identical and have ON resistance R_{ON}.

FIG. **7** shows (similarly to FIG. **5**B) graphically a waveform of the voltage V_D (for the embodiment of FIG. **6**B) when a capacitor in the present apparatus is charging and discharging. When the output draws current through the capacitor, the voltage across the capacitor increases from its initial voltage until V_D reaches V_{Dmin}. So voltage V_D starts decreasing from $V_{Dmax\,Cha}$ to V_{Dmin}. When voltage V_D reaches voltage V_{Dmin} the capacitor starts powering the regulator. At this instance the voltage V_D goes to value $V_{Dmax\,dis}$ and with the discharging of the capacitor, V_D gradually decreases up to voltage V_{Dmin}.

It has been determined that with the exemplary FIG. **6**B apparatus overall efficiency is about 80%. In the prior art, efficiency is approximately 5/12, less than 42%.

A parallel combination (or a diode connection) of the present voltage regulator can be used for very high current operations, or redundancy of a power supply. Thereby, for very high current applications, multiple instances of the present apparatus are coupled in parallel. This arrangement may include single or multiple banks of super capacitors and controllers, for high current or high voltage output requirements.

This disclosure is illustrative and not limiting; further modifications and improvements will be apparent to those skilled in the art in light of this disclosure and are intended to fall within the scope of the appended claims.

The invention claimed is:

1. A voltage regulation apparatus comprising:

a power supply terminal adapted to be coupled to a power source;

a linear voltage regulator circuit having an input terminal;

a switched capacitor element functioning as a voltage dropper and serially coupled between the power supply terminal and the input terminal of the linear voltage regulator, the switched capacitor element including at least one super capacitor having a capacitance of at least 0.1 farad and at least one transistor or solid state relay; and

an output terminal coupled to an output terminal of the linear voltage regulator.

2. The apparatus of claim **1**, wherein the switched capacitor element includes at least two super capacitors each series coupled to at least one switch, the two super capacitors being capable of being serial or parallel coupled by the at least one transistor or solid state relay relative to one another and to the input terminal of the linear voltage regulator.

3. The apparatus of claim **1**, further comprising control logic coupled to operate the switched capacitor element.

4. The apparatus of claim **1**, wherein the linear voltage regulator circuit is of the series or shunt type.

5. The apparatus of claim **1**, wherein the linear voltage regulator circuit is of the low drop out type.

6. The apparatus of claim **1**, wherein in operation the apparatus provides a current of at least one ampere at the output terminal.

7. The apparatus of claim **3**, wherein the control logic operates the apparatus in at least three phases, including:

a first phase where only a first super capacitor in the switched capacitor element is connected;

a second phase where only a second super capacitor in the switched capacitor element is connected; and

a third phase where neither of the first and second super capacitors are connected to the power supply terminal but both are connected to the input terminal of the linear voltage regulator.

8. A method of providing a regulated voltage from a power source using a capacitance coupled to an input terminal of a linear voltage regulator, comprising the acts of:

series coupling a first super capacitor functioning as a voltage dropper and having a capacitance of at least 0.1 farad in the capacitance between the power source and the input terminal;

disconnecting the first super capacitor and series coupling by a transistor or solid state relay a second super capacitor between the power source and the input terminal of the linear voltage regulator; and

disconnecting the second super capacitor from the power source and discharging both super capacitors to the input terminal.

9. The method of claim 8, further comprising the acts of:

series coupling the super capacitors between the power source and the input terminal; and

disconnecting the super capacitors from the power source, connecting the super capacitors in series and discharging the super capacitors from the input terminal.

10. The method of claim 8, further comprising the acts of:

series coupling the super capacitors between the power source and the input terminal; and

disconnecting the super capacitors from the power source, connecting the super capacitors in parallel and discharging the super capacitors to the input terminal.

11. The method of claim 8, wherein the connecting and disconnecting are performed by switches coupled to a control element.

12. The method of claim 8, wherein the linear voltage regulator is of the series or shunt type.

13. The method of claim 8, wherein the linear voltage regulator is of the low drop out type.

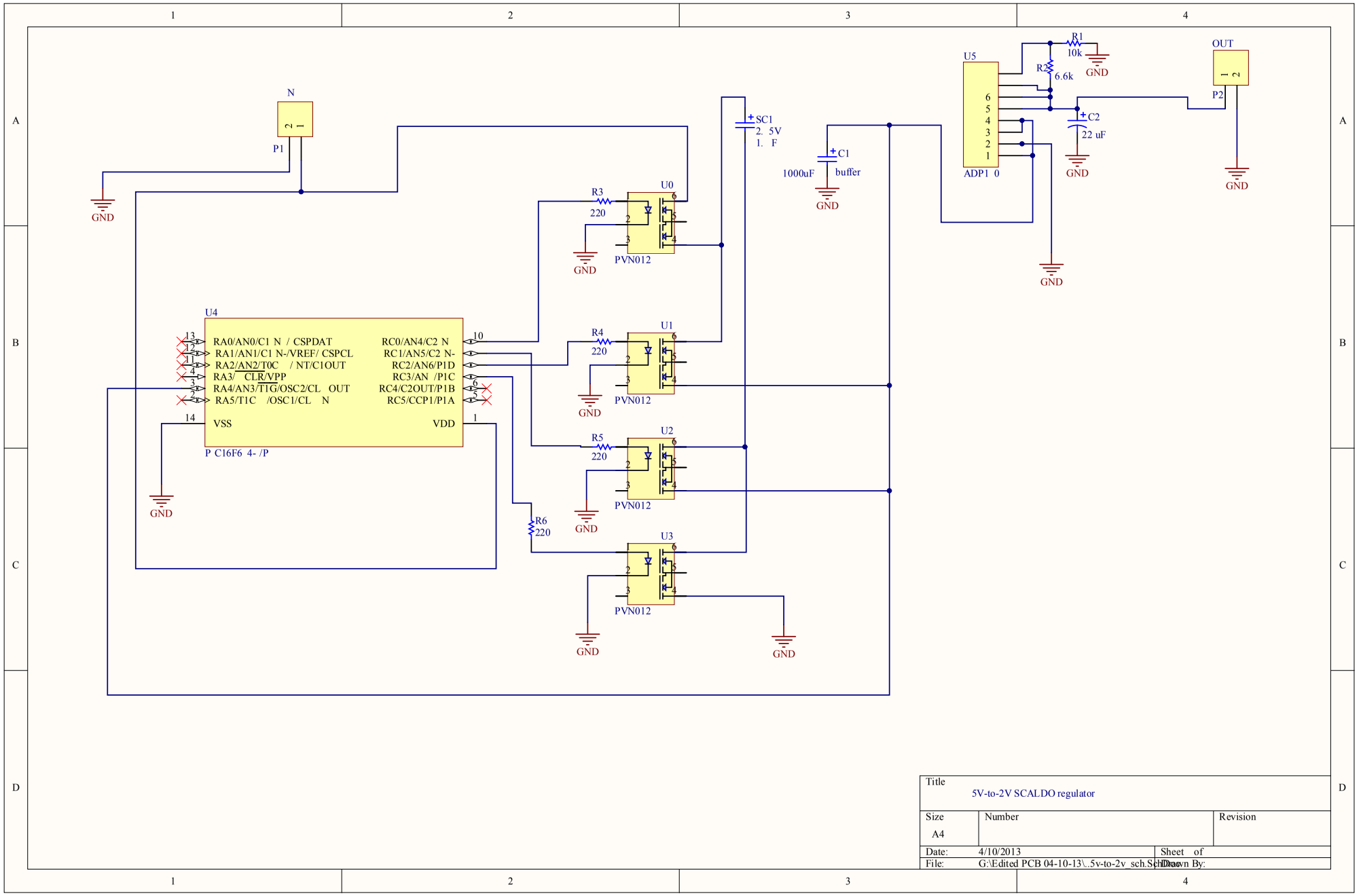
14. The method of claim 8, further comprising outputting a current of at least one ampere from the linear voltage regulator.

15. The method of claim 8, wherein a switching rate of the method is less than about 300 Hz.

* * * * *

Appendix B

Schematics and PCB layouts of the SCALDO Prototypes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SC1
2. 5V
1. F
C1
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buffer
U5
ADP1 0
R1
10k
R2
6.6k
C2
22 uF
OUT
P2
U4
RA0/AN0/C1 N / CSPDAT
RA1/AN1/C1 N-/VREF/ CSPCL
RA2/AN2/T0C / NT/C1OUT
RA3/ CLR/VPP
RA4/AN3/T1G/OSC2/CL OUT
RA5/T1C /OSC1/CL N
VSS
RC0/AN4/C2 N
RC1/AN5/C2 N-
RC2/AN6/P1D
RC3/AN /P1C
RC4/C2OUT/P1B
RC5/CCP1/P1A
VDD
P C16F6 4- /P
R3
R4
R5
R6
220
U0
U1
U2
U3
PVN012
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Size
A4
Number
Revision
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4/10/2013
Sheet of
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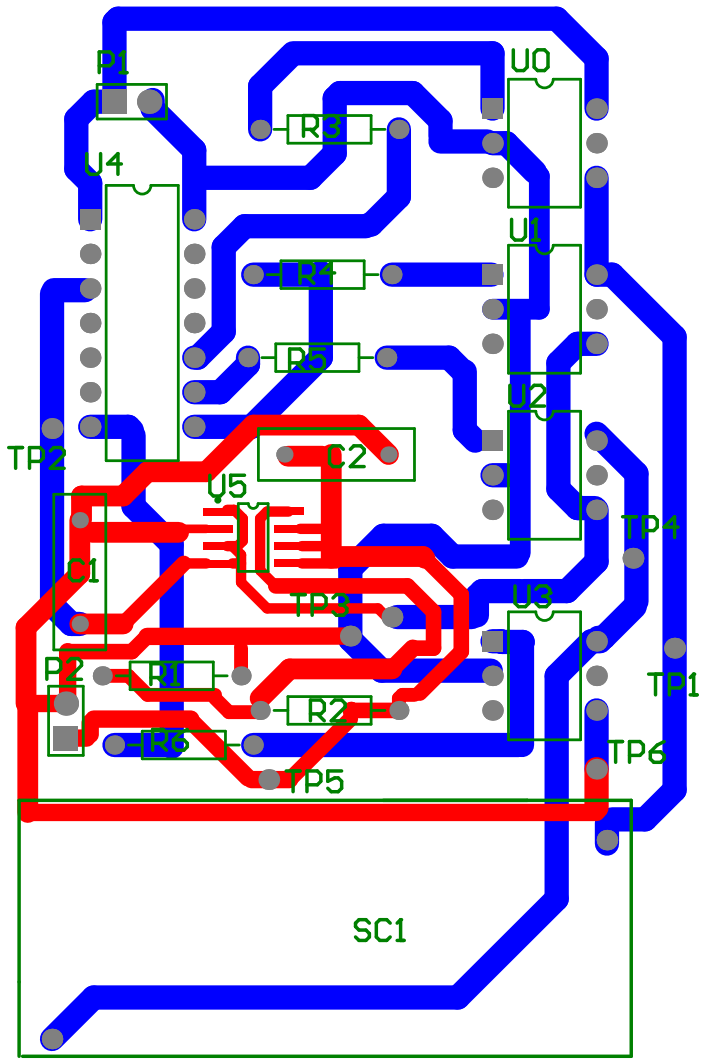
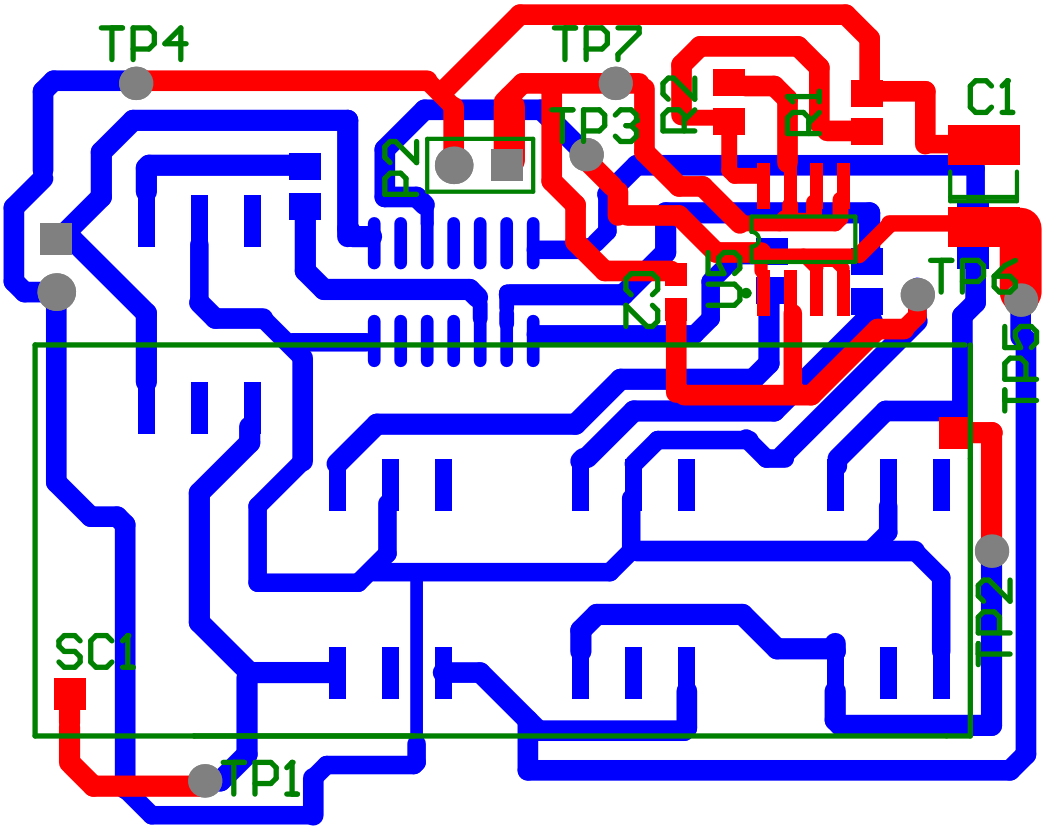
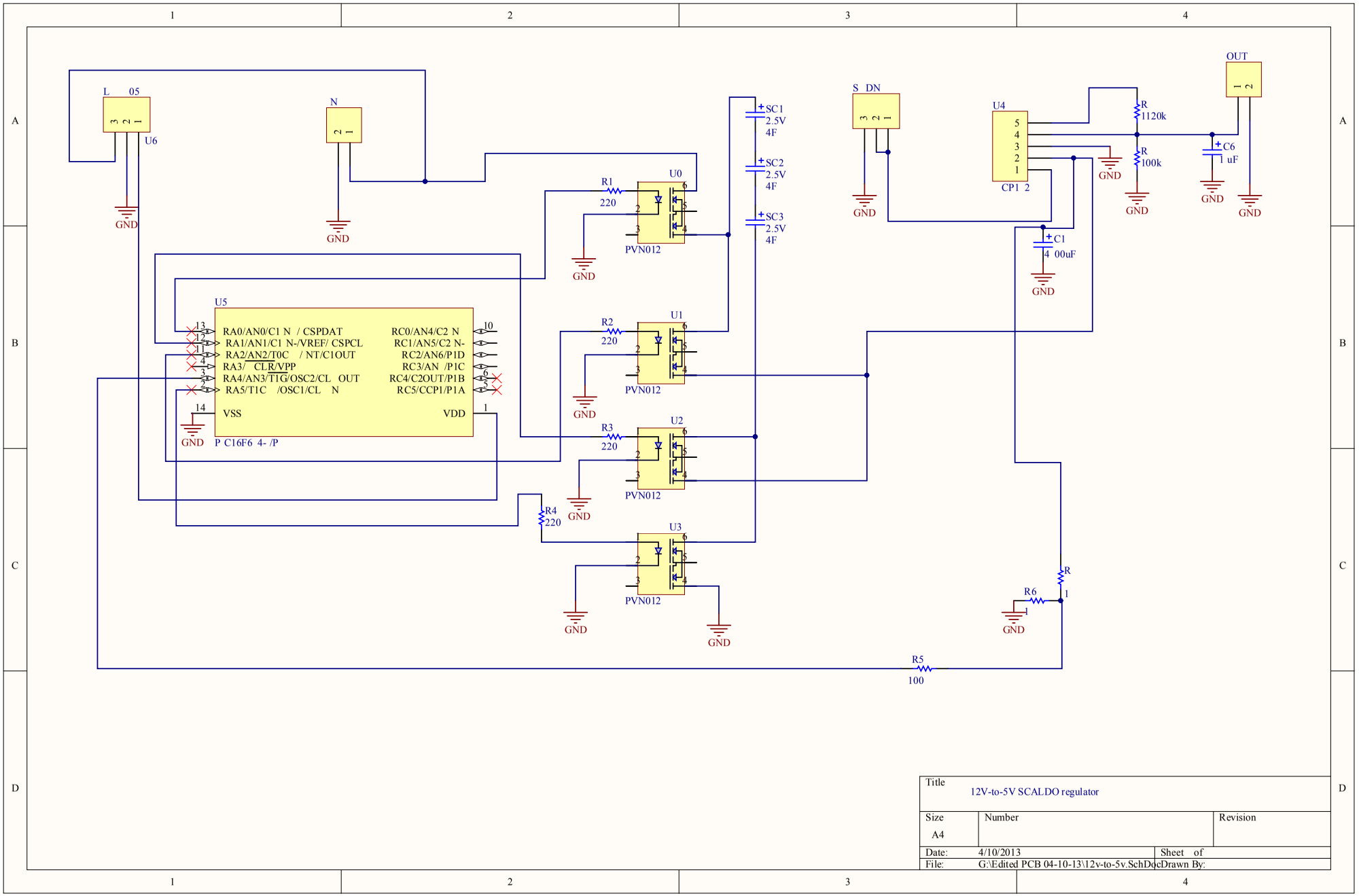


5V-to-2V SCALDO regulator- Version1



5V-to-2V SCALDO regulator- Version2


L 05
U6
N
GND
SC1
2.5V
4F
SC2
2.5V
4F
SC3
2.5V
4F
S DN
U4
CP1 2
R
1120k
R
100k
C6
1 uF
OUT
C1
4 00uF
U0
R1
220
PVN012
U1
R2
220
PVN012
U2
R3
220
PVN012
U3
R4
220
PVN012
U5
RA0/AN0/C1 N / CSPDAT
RA1/AN1/C1 N-/VREF/ CSPCL
RA2/AN2/T0C / NT/C1OUT
RA3/ CLR/VPP
RA4/AN3/T1G/OSC2/CL OUT
RA5/T1C /OSC1/CL N
VSS
RC0/AN4/C2 N
RC1/AN5/C2 N-
RC2/AN6/P1D
RC3/AN /P1C
RC4/C2OUT/P1B
RC5/CCP1/P1A
VDD
P C16F6 4- /P
R6
R5
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Size
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Number
Revision
Date: 4/10/2013
Sheet of
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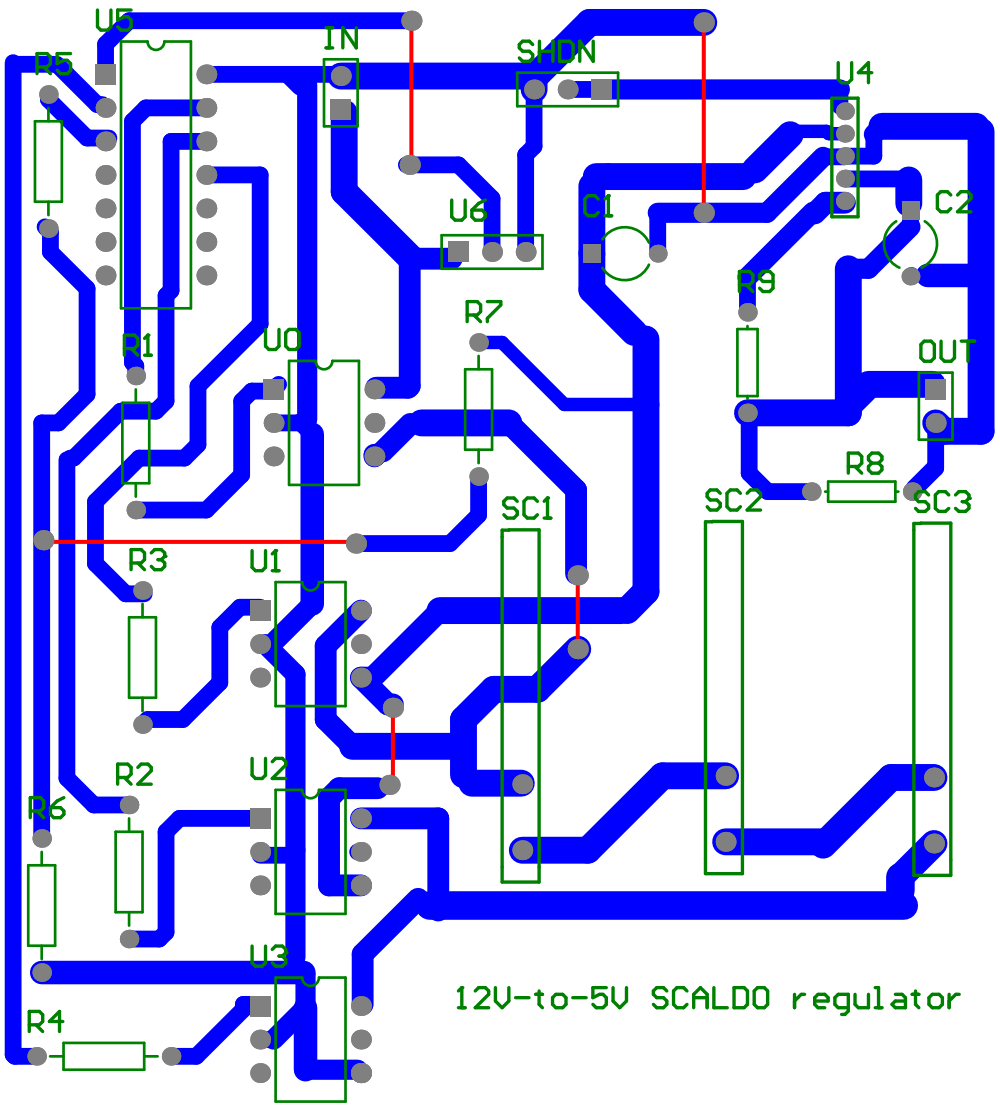
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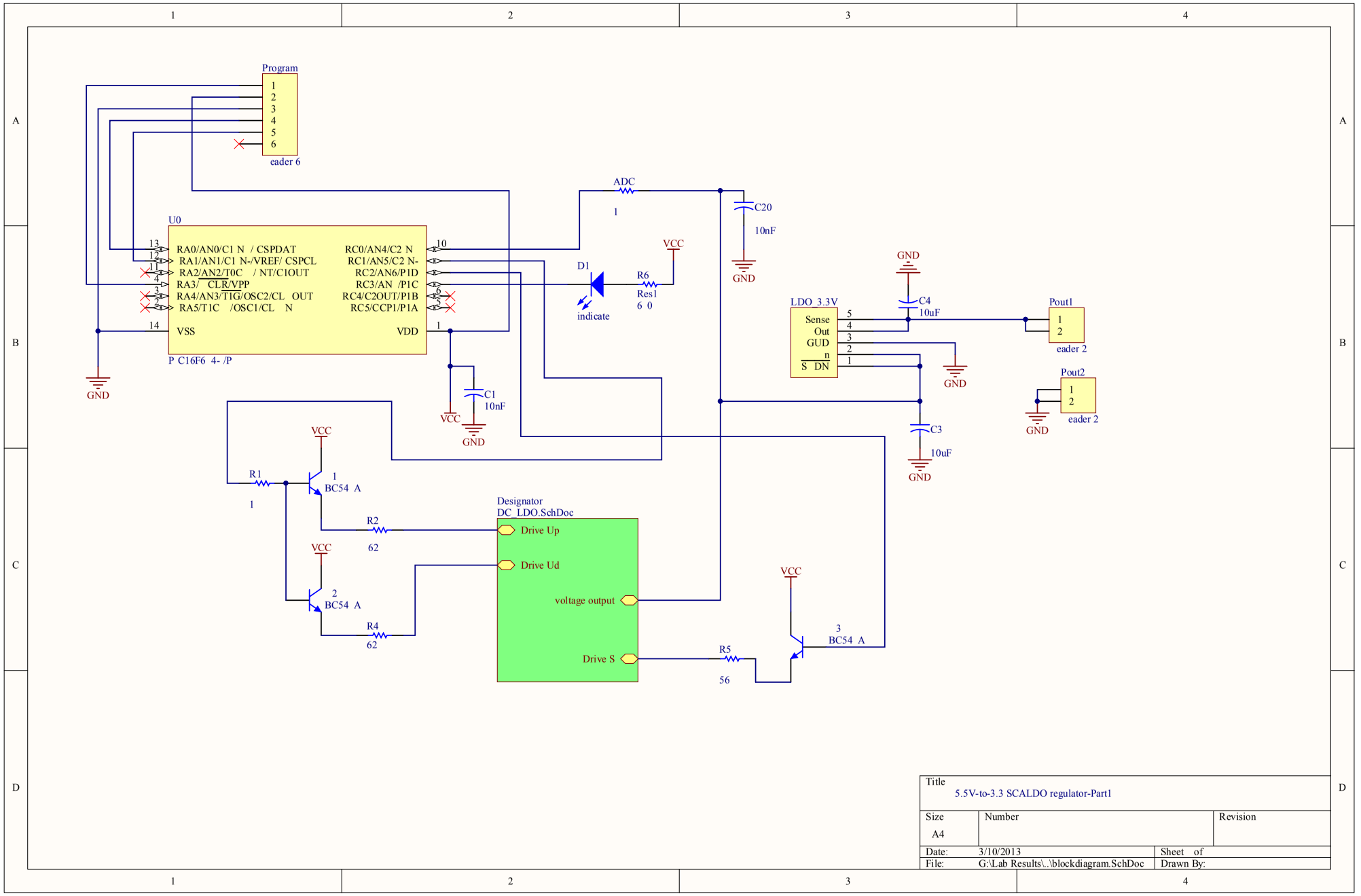
IN
SHDN
U4
R5
U6
C1
C2
R9
R7
R1
U0
OUT
R8
SC1
SC2
SC3
R3
U1
R2
U2
R6
U3
R4
12V-to-5V SCALDO regulator


Program
1
2
3
4
5
6
eader 6
U0
RA0/AN0/C1 N / CSPDAT
RA1/AN1/C1 N-/VREF/ CSPCL
RA2/AN2/T0C / NT/C1OUT
RA3/ CLR/VPP
RA4/AN3/TIG/OSC2/CL OUT
RA5/T1C /OSC1/CL N
VSS
RC0/AN4/C2 N
RC1/AN5/C2 N-
RC2/AN6/P1D
RC3/AN /P1C
RC4/C2OUT/P1B
RC5/CCP1/P1A
VDD
P C16F6 4- /P
GND
ADC
1
C20
10nF
VCC
D1
R6
Res1
6 0
indicate
C1
10nF
LDO_3.3V
Sense
Out
GUD
n
S DN
C4
10uF
C3
10uF
Pout1
Pout2
eader 2
R1
1
BC54 A
R2
62
R4
62
R5
56
Designator
DC_LDO.SchDoc
Drive Up
Drive Ud
voltage output
Drive S
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Size
A4
Number
Revision
Date: 3/10/2013
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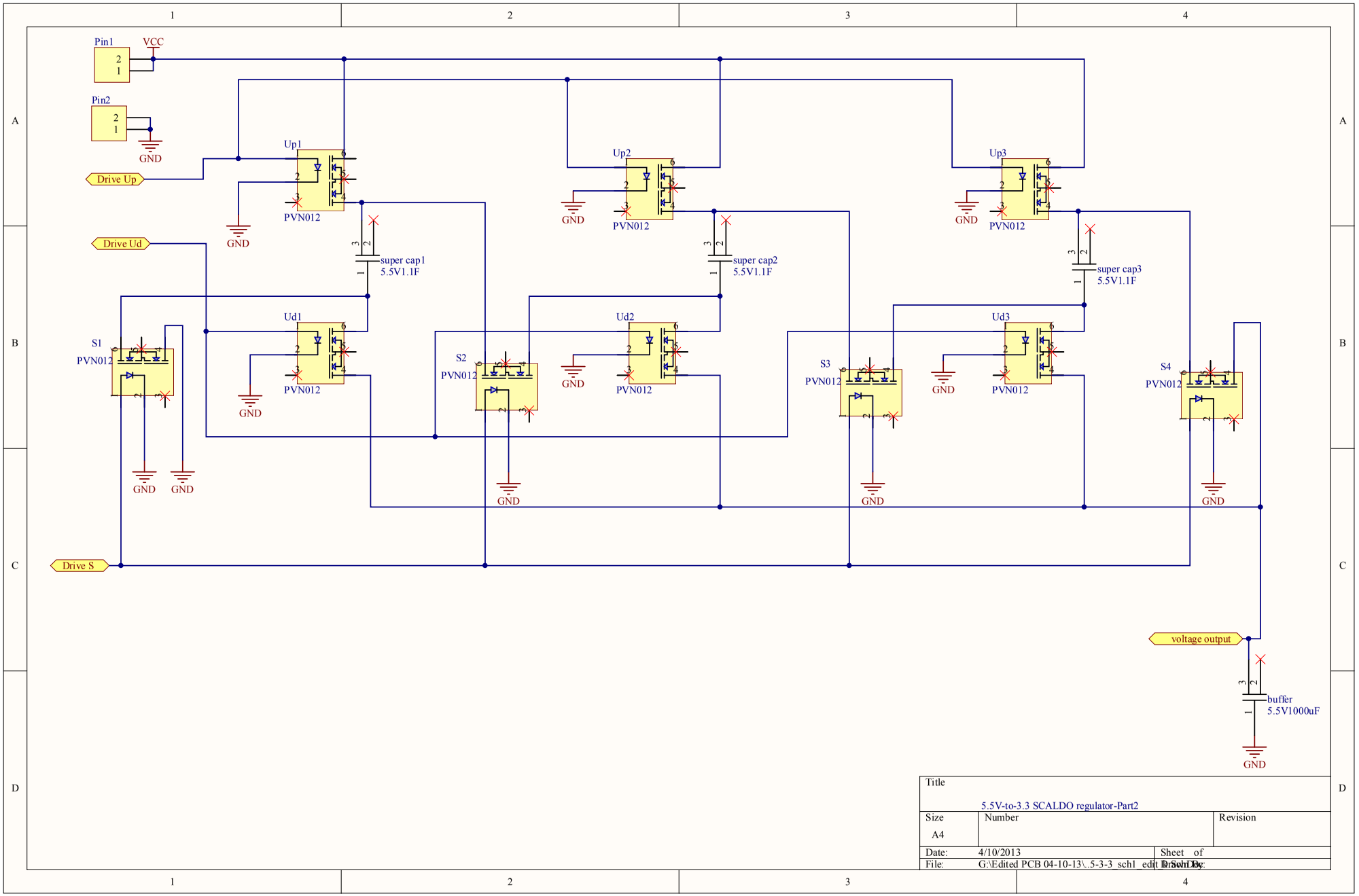
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VCC
Pin2
GND
Drive Up
Drive Ud
Drive S
Up1
Up2
Up3
Ud1
Ud2
Ud3
S1
S2
S3
S4
PVN012
super cap1
5.5V1.1F
super cap2
5.5V1.1F
super cap3
5.5V1.1F
voltage output
buffer
5.5V1000uF
Title
5.5V-to-3.3 SCALDO regulator-Part2
Size
A4
Number
Revision
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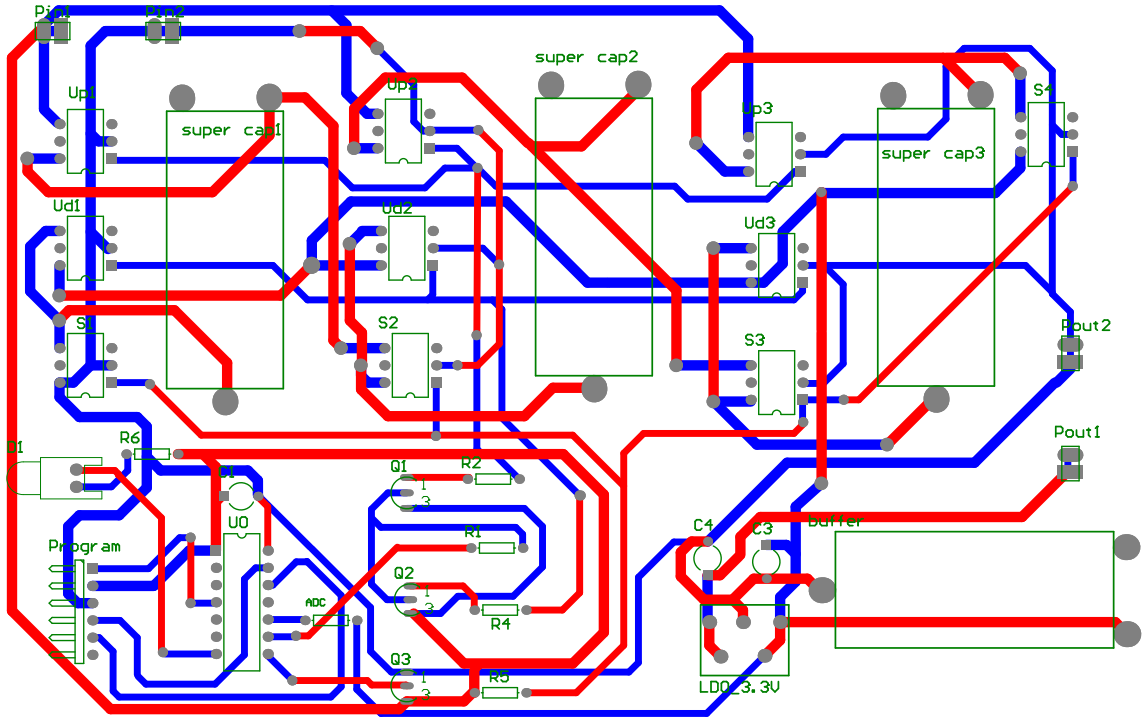


5.5V-to-3.3V SCALDO regulator

Altium Limited 12a Rodborough Rd Frenchs Forest NSW 2086	PCB DESIGNER:	5.5V-to-3.3V SCALDO regulator
	DATE:	PART NO.: / REV:
	FILE NAME:	DWG NO: / SCALE:

Appendix C

Data Sheet of PVN012 Solid State Relay

International
IOR Rectifier

Data Sheet No. PD 10034 revK

Series PVN012PbF

Microelectronic Power IC

HEXFET® Power MOSFET Photovoltaic Relay

Single Pole, Normally Open, 0-20V, 2.5A AC/ 4.5A DC

General Description

The PVN012 Series Photovoltaic Relay at 100 milliohms features the lowest possible on-state resistance in a miniature package — lower than a comparable reed relay.

The PVN012 is a single-pole, normally open solid-state relay. It utilizes a GenerationV HEXFET output switch, driven by an integrated circuit photovoltaic generator of novel construction. The output switch is controlled by radiation from a GaAlAs light emitting diode (LED) which is optically isolated from the photovoltaic generator.

These units exceed the performance capabilities of electromechanical relays in life, sensitivity, stable on-resistance, miniaturization, magnetic insensitivity and ruggedness. They are ideally suited for switching high currents or low level signals without distortion or injection of electrical noise.

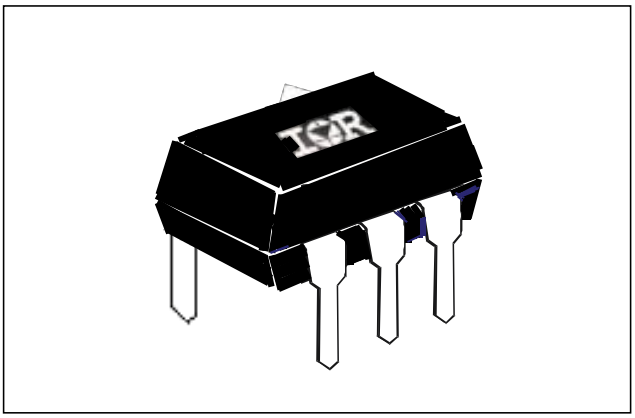
Series PVN012 Relays are packaged in a 6-lead molded DIP package with either thru-hole or surface mount (gull-wing) terminals. They are available in standard plastic shipping tubes or on tape-and-reel. Please refer to part identification information opposite.

Applications

- Portable Electronics
- Programmable Logic Controllers
- Computers and Peripheral Devices
- Audio Equipment
- Power Supplies and Power Distribution
- Instrumentation

Features

- 100mΩ On-Resistance
- GenV HEXFET output
- Bounce-free operation
- 2.5 - 4.5 Amp capacity
- Linear AC/DC operation
- 4,000 V_{RMS} I/O isolation
- Solid-State reliability
- UL recognized
- ESD Tolerance:
  - 4000V Human Body Model
  - 500V Machine Model



Part Identification

PVN012PbF	thru-hole
PVN012SPbF	surface-mount
PVN012S-TPbF	surface-mount, tape and reel

(HEXFET is the registered trademark for International Rectifier Power MOSFETs)

Electrical Specifications (-40°C ≤ T_A ≤ +85°C unless otherwise specified)

INPUT CHARACTERISTICS	Limits	Units
Minimum Control Current (see figure 1)	3.0	mA
Maximum Control Current for Off-State Resistance @ T_A = +25°C	0.4	mA
Control Current Range (Caution: current limit input LED, see figure 6)	3.0 to 25	mA
Maximum Reverse Voltage	6.0	V

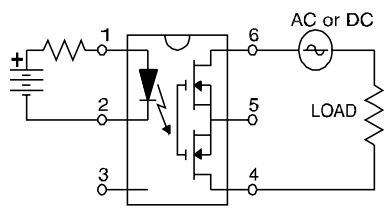
OUTPUT CHARACTERISTICS		Limits	Units
Operating Voltage Range		0 to ±20	$V_{(DC\ or\ AC\ peak)}$
Maximum Continuous Load Current @ T_A=+40°C, 5mA Control (see figure 1)			
	A Connection	2.5	A (DC or AC)
	B Connection	3.0	A (DC)
	C Connection	4.5	A (DC)
Maximum Pulsed Load Current @T_A=+25°C, (100 ms @ 10% duty cycle)			
	A Connection	6.0	A (DC or AC)
Maximum On-State Resistance @T_A=+25°C, for 1A pulsed load, 5mA Control (see figure 4)			
	A Connection	100	mΩ
	B Connection	65	
	C Connection	40	
Minimum Off-State Resistance @ T_A=+25°C, ±16V_{DC}		0.16 x 10^8	Ω
Maximum Turn-On Time @T_A=+25°C (see figure 7), for 1A, 20 V_{DC} load, 5mA Control		5.0	ms
Maximum Turn-Off Time @T_A=+25°C (see figure 7), for 1A, 20 V_{DC} load, 5mA Control		0.5	ms
Maximum Output Capacitance @ 20V_{DC} (see figure 2)		300	pF

GENERAL CHARACTERISTICS		Limits	Units
Minimum Dielectric Strength, Input-Output		4000	V_{RMS}
Minimum Insulation Resistance, Input-Output, @T_A=+25°C, 50%RH, 100V_{DC}		10^{12}	Ω
Maximum Capacitance, Input-Output		1.0	pF
Maximum Pin Soldering Temperature (10 seconds maximum)		+260	°C
Ambient Temperature Range:	Operating	-40 to +85	
	Storage	-40 to +100	

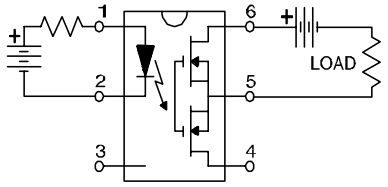
International Rectifier does not recommend the use of this product in aerospace, avionics, military or life support applications. Users of this International Rectifier product in such applications assume all risks of such use and indemnify International Rectifier against all damages resulting from such use.

Connection Diagrams

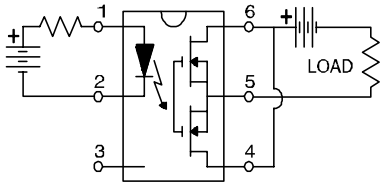
"A" Connection



"B" Connection



"C" Connection



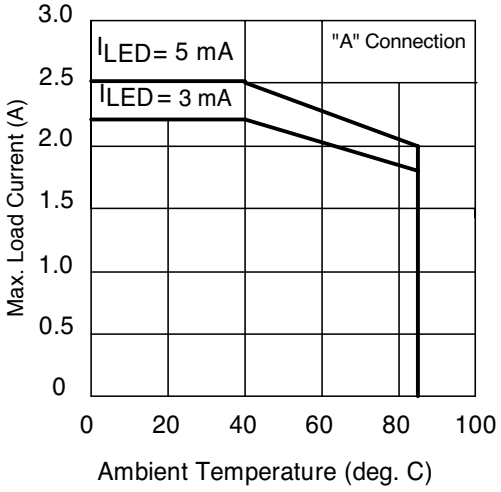


Figure 1. Current Derating Curves*

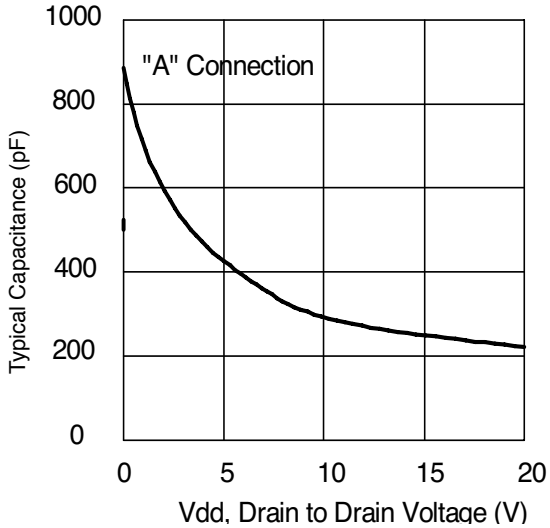


Figure 2. Typical Output Capacitance

* Derating of 'B' and 'C' connection at +85°C will be 70% of that specified at +40°C and is linear from +40°C to +85°C.

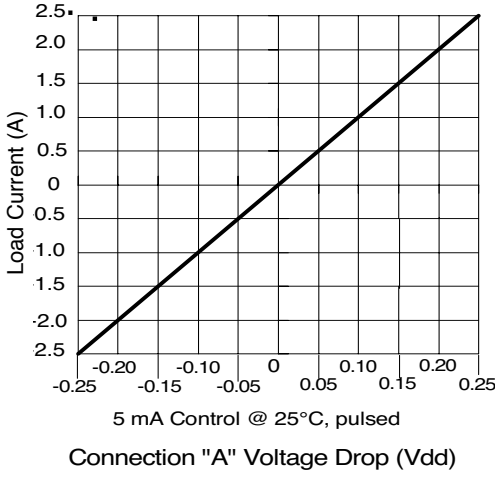


Figure 3. Linearity Characteristics

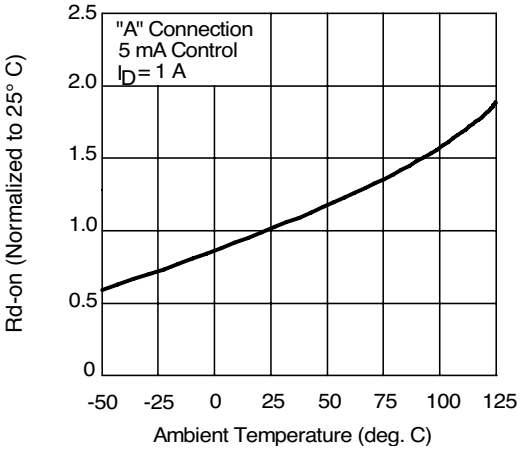


Figure 4. Typical Normalized On-Resistance

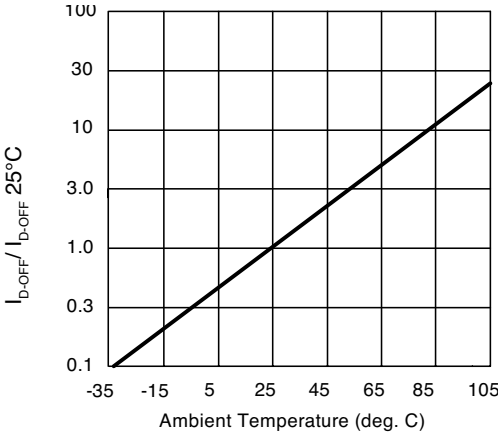


Figure 5. Typical Normalized Off-State Leakage

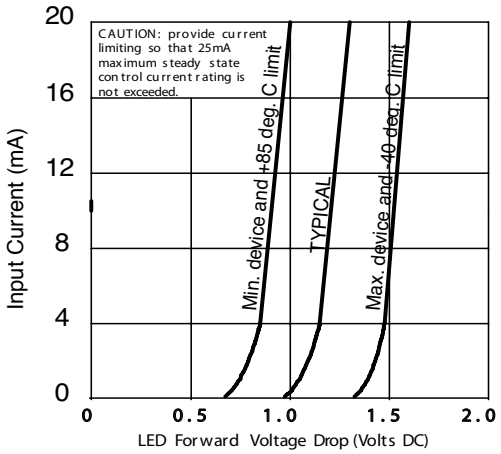


Figure 6. Input Characteristics (Current Controlled)

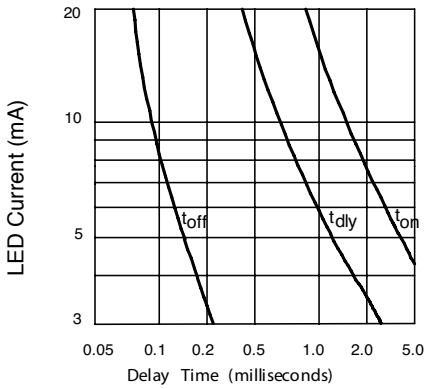


Figure 7. Typical Delay Times

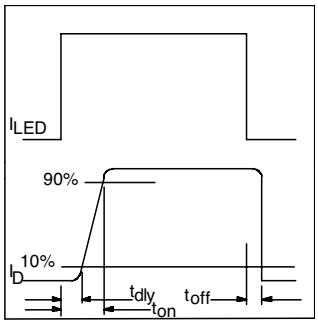
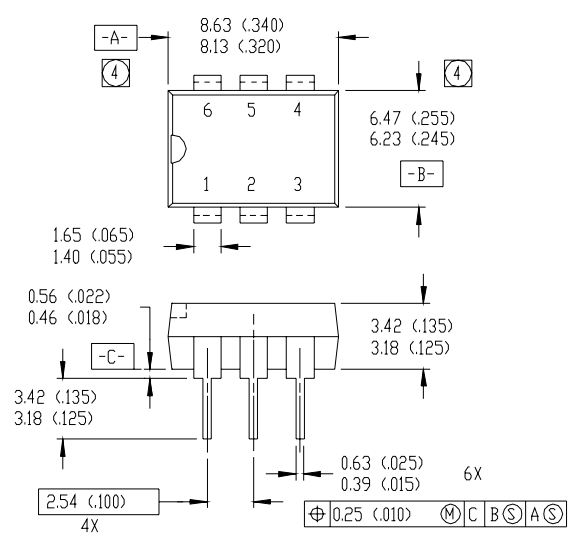
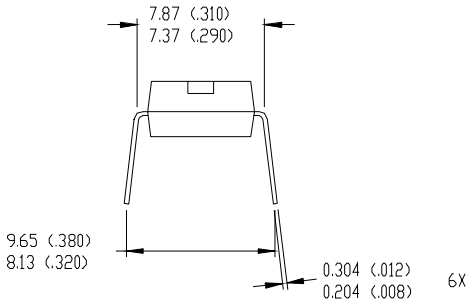


Figure 8. Delay Time Definitions

Case Outlines



NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2 CONTROLLING DIMENSION: INCH.
3 DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 (.010).



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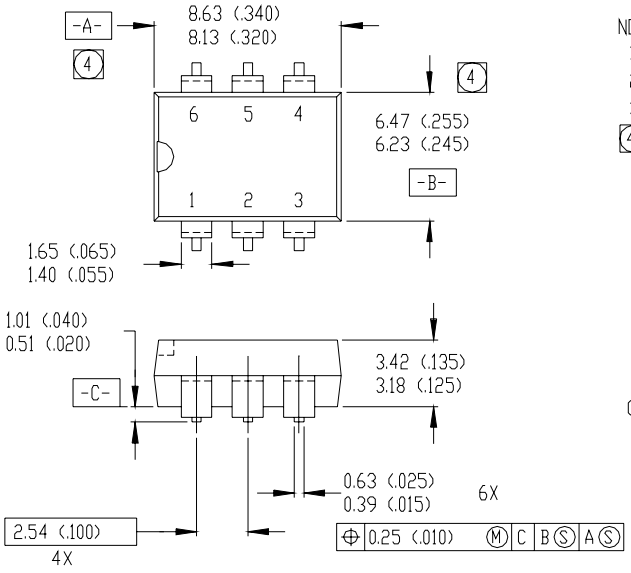

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2 CONTROLLING DIMENSION: INCH.
3 DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
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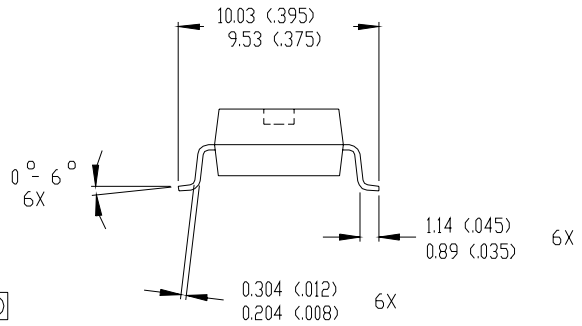

01-2009 01

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

Appendix D

PIC Program to Drive Solid State Relays

Note: This is the program developed for the 5V-to-2V SCALDO regulator. The same program was used for the other two SCALDO prototypes (12V-to-5V, 5.5V-to-3.3V) with minor changes.

```
// PIC16F684 using 4Mz internal oscillator

#include <pic.h>
#include <stdlib.h>
#include <stdio.h>

// Initial configuartions
__CONFIG(INTIO & WDTDIS & PWRTEN & MCLRDIS & UNPROTECT \
  & UNPROTECT & BORDIS & IESODIS & FCMDIS);

int state1;     //state variables to keep the track of charging
        // and discharging phases
int state2;

int ADC_value = 0;      //initial ADC detecting result
const int ref_LDO = 492;    // reference value of the LDO input voltage, 2.4 V
int i;
int j;              //local variable used in the delay loop

void supercap_discharging()
{
    PORTC = 0B00001100;     //turn on s2, s4 and
            //turn off s1, s3 begin supercap discharging
                // where RC2—s2 and RC3—s4

}

void supercap_charging()
```

```
{

    PORTC = 0B00000011; //turn on s1, s3 and
        //turn off s2, s4 switches begin supercap charging
                // where RC0—s1 and RC2—s3
}

//pick the point where ADC value below the referance
//during charging process and  change over to discharging

void ADC_dchg_sw()
{
    while (state1 == 0)
    {
        ADC_value = 0; //Initalise ADC variable
        GODONE = 1; //Enable ADC
        for (i=0; i<100; i++);  //delay to ready ADC
        ADC_value = (ADRESH << 8) + ADRESL; //read the inline ADC value
                        //and combin the higher and lower bits

        if (ADC_value<ref_LDO)  // check whether the LDO input voltage is
//below the reference value
        {

            state1 = 1;
            state2 = 0;
            GODONE = 0;
            supercap_discharging(); //change switches to supercapacitor discharging

            for (i=0; i<500; i++);      //switch—over delay
        }
    }
}

//pick the point where ADC value below the referance
//during the discharging process and change over to charging
void ADC_chg_sw()
{
    while(state2 == 0)
    {
        ADC_value = 0; //Initalise ADC variable
        GODONE = 1; //Enable ADC
        for (i=0; i<100; i++);
        ADC_value = (ADRESH << 8) + ADRESL; //read the inline ADC
                        //and combin the Higher and lower bits

        if(ADC_value<ref_LDO)
```

```
        {

            state1 = 0;
            state2 = 1;
            GODONE = 0;
            supercap_charging();    //change switches to supercapacitor charging
            for (i=0; i<500; i++); //switchover delay
        }
    }
}

void main()
{
    //Initailse the ADC
    PORTA=0;
    TRISA = 0b00010000;     //RA4 is analog input of the ADC

    ANSEL  = 0b00001000;        // Channel AN3 is selected since we are using RA4 as
                    //AN3 is the analog input from LDO input voltage


    TRISC = 0b00000000;     // RC0—RC4 are the output from the PIC to drive the switc
    ADCON1 = 0b00010000;        //bit 4—6 ADCS<2:0> = 001 which gives Fosc/8*/

    ADCON0 = 0b10001101;        //Bit 7 high — Digital data right justified
                    //Bit 6 low  — VDD as the voltage reference
                    //Bit 5 — Unimplemented
                    //Bit 4,3,2 = 011 — Channel 03 (AN3) is selected since we are usi
                    //Bit 1 low — Setting this bit will start ADC cycle
                    //Bit 0 high — A/D converter module is operating
    //Start the charing process
    state1 = 0;
    state2 = 1;
    supercap_charging();
    for (i=0; i<100; i++);      //delay

while(1)
    {
        supercap_charging();
        ADC_dchg_sw();                  // turn to discharing
        ADC_chg_sw();           // turn to charging
    }
}
```

Appendix E

Laplace-Transform Based Analytical Solution

```
function LDO_phases
% LDO_phases.m
% Calculate currents and voltages for each of the four phases of LDO
% regulator.
% v1: 12-May-2011 Initial design
% v2: 13-May-2011 Generalized for multiple cycles
% v3: 16-May-2011 Generalized for multiple cycles/ check for the exact
% initial conditions
% v4: 20-May-2011 Generalized for multiple cycles/ check for the exact
% initial conditions, single function for switch transition time
% v5: 05-Aug-2013 Enrgy loss calculations of the SCALDO regulator



IL = 0.20;      % Load current (amps)
C1 = 1.3;       % Supercapacitor capacitance (F)
C2 = 0.0047;        % Buffer capacitor capacitance (F)
Vp = 12;        % Input voltage (volts)
r = 0.100+0.18;         % Switch on-resistance (ohms)
            % + compensation (PCB parasitics and on-resistance)
r1 = 0.300;     % Supercapacitor ESR (ohms)
r2 = 0.400;     % Buffer capacitor ESR (ohms)
V2_MIN = 5.4;       % threshold voltage for C2 voltage(volts)

a2 = (C2 + C1) / ((C1*C2) * (r1 + r2 + 2*r));   % time-constant
a4 = IL*C2 / (C2 + C1);

% define our time-bases
t_max = 10.0;       % assumed max time per phase
t_sw = 0.003;       % switch settling time (3 ms)

%Both time-bases have similar time spacing
```

```
t1 = linspace(0, t_max, 1000000)';  % charging time
tsw = linspace(0,t_sw, 300)';       % time between switch transitions and
                                        % delay set by the microprocessor

% initial voltages on capacitors at start of charging

v2_0 = V2_MIN;           % buffer capcitor
v1_0 = v2_0+ 2*IL*r;     % supercapcitor initial voltage
                         %compensating switch voltages


vc2_0 = v2_0 - IL*t_sw/C2 + IL*r2;  % internal voltage of buffer cap


vc1_0 = v1_0 + IL*r1;            % internal voltage of supercap
                                        % considering the ESR drop


%%% phase I
[t, I1, I2, Vc1, Vc2, V1, V2] = phaseI(t1, vc1_0, vc2_0);
time = t;
[i1 i2 vc1 vc2 v1 v2] = deal(I1, I2, Vc1, Vc2, V1, V2);

%%%phase II
 [t, I1, I2, Vc1, Vc2, V1, V2] = phaseII_or_IV(tsw, vc1(end), vc2(end));
 time = [time; t + time(end)];
 [i1 i2 vc1 vc2 v1 v2] = deal([i1; I1], [i2; I2], [vc1; Vc1], [vc2; Vc2], ...
                                        [v1; V1], [v2; V2]);


%plot the figure for the initial charging phase
figure(1); clf;

subplot(211);

plot(time, [i1 i2], '-', 'linewidth', 2); zoom on; grid on;
xlabel('Time (s)');
ylabel('Capacitor current (A)');
subplot(212);
plot(time, [v1 v2 ], 'linewidth', 2); zoom on; grid on;
xlabel('Time (s)');
ylabel('Capacitor voltage (V)');

for i = 1:1


    %%% phase III
```

```
        [t, I1, I2, Vc1, Vc2, V1, V2] = phaseIII(t1, vc1(end), vc2(end));
    time = [time; t + time(end)];
    [i1 i2 vc1 vc2 v1 v2] = deal([i1; I1], [i2; I2], [vc1; Vc1], [vc2; Vc2], ...
                                        [v1; V1], [v2; V2]);


    %%% phase IV
    [t, I1, I2, Vc1, Vc2, V1, V2] = phaseII_or_IV(tsw, vc1(end), vc2(end));
    time = [time; t + time(end)];
    [i1 i2 vc1 vc2 v1 v2] = deal([i1; I1], [i2; I2], [vc1; Vc1], [vc2; Vc2], ...
                                        [v1; V1], [v2; V2]);

    %%% phase I
    [t, I1, I2, Vc1, Vc2, V1, V2] = phaseI(t1, vc1(end), vc2(end));
    time = [time; t + time(end)];
    [i1 i2 vc1 vc2 v1 v2] = deal([i1; I1], [i2; I2], [vc1; Vc1], [vc2; Vc2], ...
                                        [v1; V1], [v2; V2]);

    %%% phase II
    [t, I1, I2, Vc1, Vc2, V1, V2] = phaseII_or_IV(tsw, vc1(end), vc2(end));
    time = [time; t + time(end)];
    [i1 i2 vc1 vc2 v1 v2] = deal([i1; I1], [i2; I2], [vc1; Vc1], [vc2; Vc2], ...
                                        [v1; V1], [v2; V2]);

end

%plot a figure for multiple cycles
figure(2); clf;
plot(time, [v1 v2], 'linewidth', 2); zoom on; grid on;
xlabel('Time (s)');
ylabel('Capacitor voltage (V)');



%-------------------------------------------------------------------------
function [tout, i1, i2, vc1, vc2, v1, v2] = phaseI(time, Vc1_0, Vc2_0)

    a1 = (Vp - Vc1_0 - Vc2_0 - IL*(r1 + 2*r)) / (r2 + r1 + 2*r);
    E = exp(-a2*time);

    i2 = (a1 + a4)*E - a4;          % Buffer capacitor current
    i1 = IL + i2;                   % Supercapacitor current

    dv2 = 1/C2*(((a4 + a1)/a2*(1 - E)) - a4*time);  % buffer capacitor voltage change
    vc2 = Vc2_0 + dv2;      % internal buffer capacitor voltage
    v2  = vc2 + i2*r2;      % external capacitor voltage
```

```
    dv1 = 1/C1*(((a4 + a1)/a2*(1 - E)) + (IL-a4)*time); % supercapacitor voltage change
    vc1 = Vc1_0 + dv1;      % internal supercapacitor voltage
    v1 = vc1 + i1*r1;       % external supercapacitor voltage

    tout = time;

    % has v2 dropped below V2_MIN? If so, truncate the calculation!
    mask = find(v2 < V2_MIN);
    if ~isempty(mask)
        tout(mask) = [];
        i1(mask) = []; i2(mask) = [];
        vc1(mask) = []; vc2(mask) = []; v1(mask) = []; v2(mask) = [];
        T_1 = tout(end)
        f1 = (i1.^2).*(r1+2*r) % Phase I power loss
        z1 = trapz(tout,f1)     % Phase I energy loss

       end
   end
%-------------------------------------------------------------------------------
function [tout, i1, i2, vc1, vc2, v1, v2] = phaseIII(time, Vc1_0, Vc2_0)

    a1 = (Vc1_0 - Vc2_0 - IL*(r1 + 2*r)) / (r2 + r1 + 2*r);
    E = exp(-a2*time);

    i2 = (a1 + a4)*E - a4;          % Buffer capacitor current
    i1 = IL + i2;                   % Supercapacitor current

    dv2 = 1/C2*(((a4 + a1)/a2*(1 - E)) - a4*time);  % buffer capacitor voltage change
    vc2 = Vc2_0 + dv2;      % internal buffer capacitor voltage
    v2  = vc2 + i2*r2;      % external capacitor voltage

    dv1 = 1/C1*(((a4 + a1)/a2*(1 - E)) + (IL-a4)*time); % supercapacitor voltage change
    vc1 = Vc1_0 - dv1;      % internal supercapacitor voltage
    v1 = vc1 - i1*r1;       % external supercapacitor voltage

    tout = time;

    % has v2 dropped below V2_MIN? If so, truncate the calculation!
    mask = find(v2 < V2_MIN);
    if ~isempty(mask)
        tout(mask) = [];
        i1(mask) = []; i2(mask) = [];
        vc1(mask) = []; vc2(mask) = []; v1(mask) = []; v2(mask) = [];

       f3 = (i1.^2).*(r1+2*r) % Phase III power loss
       z3 = trapz(tout,f3)  % Phase III energy loss
    end
```

```
    end
%-------------------------------------------------------------------------
 function [tout, i1, i2, vc1, vc2, v1, v2] = phaseII_or_IV(time, Vc1_0, Vc2_0)


    i2 = -IL*ones(size(time));          % Buffer capacitor current
    i1 = IL + i2;                        % Supercapacitor current

    vc2 = Vc2_0-IL*time/C2 ;            % internal voltage of buffer cap

    v2  = vc2-IL*r2;                    % external capacitor voltage

    vc1 = Vc1_0*ones(size(time)) ;      % internal supercapacitor voltage
                                       % convert a scalar to a vector

    v1 = vc1;                         % external supercapacitor voltage

    tout = time;

   f2 = (i2.^2).*r2  % Phase II and IV power loss
   z2 = trapz(tout,f2) % Phase II and IV energy loss

end
%-------------------------------------------------------------------------

%-------------------------------------------------------------------------
end
```

Appendix F

SCALDO Power Loss Estimations

```
% Calculatation of power losses of 12V-to-5V SCALDO regulator
%  v1: 07-Sept-2013%

% Phase I energy(mJ) derived from the MATLAB analytical solution
E_I = [193 217 232 236 231 216 192 158 113];

% Phase II energy(microJ) derived from the MATLAB analytical solution
E_II= [48 75 108 147 192 243 300 363 432];

% Phase I timing
t_d =[5.569 4.009 2.969 2.2262 1.669 1.2357 0.889 0.6054 0.3691];

t_sw =0.3; %  Phase II timing (switch-over time period)

I_L= [200 250 300 350 400 450 500 550 600]; % load current


%calculation of power losses
P_I = E_I./t_d % Phase I power loss (mW)
P_II = E_II./(1000*t_sw);  % Phase II power loss (converted into mW)
P_III =P_I; % Phase II power loss (mW)
P_IV = P_II; % Phase IV power loss (mW)
P= P_I+P_II+P_III+P_IV % Power loss of the four phases due to resistive losses

%Fit phase I for a polynomial
pf= polyfit(log10(I_L/I_L(1)), log10(P_I /P_I(1)),1)

% Plot power losses of Phase I
figure(1); clf;
plot(I_L, P_I,'-r');
grid on;
xlabel('Load current (mA)');
ylabel('Power loss (mW)');

% Plot total power losses and power losses of individual phase
```

```
% This power losses account for all the resistive losses
figure(2); clf;
semilogy(I_L, P_I,'-r',I_L, P_II,'-b',  I_L, P,'-g');
grid on;
xlabel('Load current (mA)');
ylabel('Power loss (mW)');
```

Appendix G

Commercial Supercapacitors

Table G.1: Commercially available supercapacitors

Company name	Device name	Capacitance (F)	Cell/module voltage (V)	Type
Asahi Glass	EDLC	500–2000	3, 14/42	Carbon/non-aqueous
AVX	Bestcap	0.022–0.56	3.5–12	Carbon/polymer aqueous
Cap-XX	Supercapacitor	0.09–2.8	2.25–4.5	Carbon/non-aqueous
Cooper	PowerStor	0.47–50	2.3–5	Aerogel/non-aqueous
Epcos	Ultracapacitor	5–5000	2.3, 2.5	Carbon/non-aqueous
Maxwell	Boostcap PowerCache	1.8–3000	2.5	Carbon/non-aqueous
NEC	Supercapacitor	0.01–6.5	3.5–12	Carbon/aqueous Carbon/organic
Nippon	Chemi-Con DLCAP	300–3000	2.3, 2.5	Carbon/non-aqueous
Ness	NessCap	35000	2.3, 2.7	Carbon/organic
Matsushita Panasonic	Gold capacitor	0.1–2500	2.3–5.5	Carbon/organic
ELNA	Dynacap	0.333–100	2.5–6.3	Carbon/non-aqueous
LS Mtron	LS Ultracapacitor	100–5400	2.5–2.8	Carbon/non-aqueous
Cellergy	Supercapacitor	0.015–0.7	1.4–12	Carbon/non-aqueous

Table G.2: Comparison of typical electrolytic capacitors and supercapacitors for their useful specifications

			Parameters			
	Capacitor type	Manufacturer	Capacitance (F)	Terminal voltage (V)	Short circuit current(A)	ESR (mΩ)
Less than 1 J	Electrolytic	RSS	0.0022	16	104	153
1-5 J	Supercaps	Maxwell	1	2.7	3.85	700
1-5 J	Supercaps	Cap-xx	2.4	2.3	115	14
1-5 J	Electrolytic	Cornell Dubilier	0.0022	50	704	71
5-50 J	Supercaps	Maxwell	10	2.5	14	180
5-50 J	Supercaps	Cap-xx	1.2	4.5	112.5	40
5-50 J	Supercaps	Nesscap	10	2.3	33	70
5-50 J	Electrolytic	Cornell Dubilier	0.082	16	1441	11.1
5-50 J	Electrolytic	VICOR	0.00027	200	325	614
Above 50 J	Supercaps	Maxwell	350	2.7	840	3.2
Above 50 J	Supercaps	Nesscap	120	2.3	144	16
Above 50 J	Supercaps	Maxwell	1500	2.7	5700	0.47
Above 50 J	Supercaps	Maxwell	3000	2.7	9300	0.29

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