Supercapacitor Assisted Inverter for the purposes of Input Ripple Control

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Abstract

This thesis describes the use of a series/parallel supercapacitor to actively control the input ripple of a DC-AC power inverter through the use of a new inverter topology. The topology is made up of two 'sub-inverters' placed in series, with a supercapacitor which is in parallel with one and series with the other. By varying the current draw of each sub-inverter both the current flow into the inverter and the current flow in and out of the supercapacitor can actively be manipulated by adjusting the ratio of the current drawn by each sub-inverter. When the sub-inverter in series with the supercapacitor draws more current than the one in parallel the supercapacitor bank begins charging and more power is drawn by the inverter than is output, conversely when the parallel sub-inverter draws more current than the series one then the supercapacitor bank discharges and the inverter outputs more power than its input. By manipulating the ratio of the current draws the inverter can draw more power than it outputs during low periods of the output cycle and store it, and then release this energy during high periods of the output cycle. This technique overcomes the inefficiencies of using a conventional parallel input capacitor arrangement as the capacitor is charged in series with a load, resulting in only a negligible amount of energy lost in the path resistance.

Acknowledgements

I would like to thank my family for the immense support they have provided for me over the course of my university journey, this has afforded me the opportunity of postgraduate study that I otherwise would not have had.

I also thank my supervisor Dr Nihal Kularatna for giving me the guidance and inspiration to complete this work, your random ideas of new circuits are more useful to others than you likely realize.

Finally, I would like to show my appreciation for the influential thinkers of old, who through their ideas I have discovered over the last few years have shaped the view of the world I hold today. “Reason obeys itself; and ignorance submits to whatever is dictated to it” - Thomas Paine, 1737-1809.

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Chapter 1

1.1 Introduction

In order for the output by solar cells to be distributed via a mains supply grid it must first be converted from direct current (DC) electricity to alternating current (AC), this function is performed by a device known as an Inverter.

As solar energy becomes more common and the world begins to move away from environmentally unfriendly means of electricity generation such as coal and gas the demand for higher performance inverters has increased significantly. Unlike other forms of electricity generation which typically rely on mechanical force to generate electricity and can be setup to produce an alternating current output, solar cells by themselves can only output direct current. This poses an issue when the energy is intended to be transmitted over a mains supply grid for consumption at a remote location.

1.2 Objectives

In this project, a new topology of power inverter was developed with the aim of addressing the performance aspect of input ripple for the conversion of solar cell output to alternating current.

The topology developed utilizes two inverters, a master and a slave, and a

supercapacitor bank as a bulk energy storage medium where during cycle periods of low power output excess energy can be temporarily stored for later use by the slave inverter. The two inverters are arranged in such a way that the slave is in parallel with the supercapacitor bank and the primary is in series, by adjusting the output of the two inverters the input power can be manipulated on the fly over the different parts of the output cycle to maximize utilization of the solar cell regardless of the instantaneous power output.

Unlike other inverters which rely on a network of bulky capacitors and inductors to passively filter the input this can be considered to have an active filter, which aside from offering superior performance at the cost of additional development time allows for a potentially smaller physical device size as well as reliability and noise improvements.

The main objectives of this project were to develop a new topology to address the input ripple performance of existing power inverters while allowing for a small form factor, this was done as part of a potential submission by the power electronics research group at the University of Waikato for the Little Box Challenge. The Little Box Challenge was a competition sponsored by Google and numerous electronics components manufacturers to develop a small form factor high performance power inverter for use with solar cells.

1.3 Outline

This thesis is divided into 7 chapters:

Chapter 1 provides an summary of the entire content of this thesis, covering the purpose of the project and giving a brief summary of each chapter.

Chapter 2 deals with the fundamental aspects of the project and aims to provide a general understanding to those who are unfamiliar to this area of power electronics. Included are overviews of solar cells, the fundamentals of mains grid power distribution, power inverters, and supercapacitors.

Chapter 3 is an examination and evaluation of three commercially available inverters for use in cars to power domestic appliances.

Chapter 4 is the groundwork for the proposed new inverter topology, covering everything from the development of the initial 'switched supercapacitor' idea to the evaluation of the first proof of concept device.

Chapter 5 covers further development of the concept, converting it into an AC inverter. Issues with the basic 'switched' topology are discussed.

Chapter 6 follows from the issues with the 'switched' topology mentioned in the previous chapter with the conceptualization and development of the

final 'switchless' topology.

Chapter 7 discusses the 'switchless' topology and addresses potential future developments which are outside the scope of this research.

Chapter 2

2.1 Solar Cells

In their most basic description solar cells, also known as photovoltaic cells, are devices which capture light energy typically in the infra-red and visible spectrum and convert it into electrical energy. Aside from niche applications such as powering satellites their main use is in solar installations for generating power for the mains electricity system as a perceived environmentally friendly alternative to fossil fuel power generation such as coal and oil.

As the push for cleaner forms of power production has intensified the demand for higher performance from devices such as solar cells has increased due to the need for these systems to be able to provide economic benefit, known as grid parity the price of a unit of electricity produced by a solar panel compared to existing local means affects the rate of adoption of solar as the unit must be able to produce electricity at a lower cost than what it is being sold to the mains grid for. While the cost of panels is constantly falling due to increased production according to Swanson's law [1] (which states that solar cell cost falls by 20% for every doubling of production) the demand for better performance from these units is increasing in order to maximize the economic benefit and minimize return on investment time.

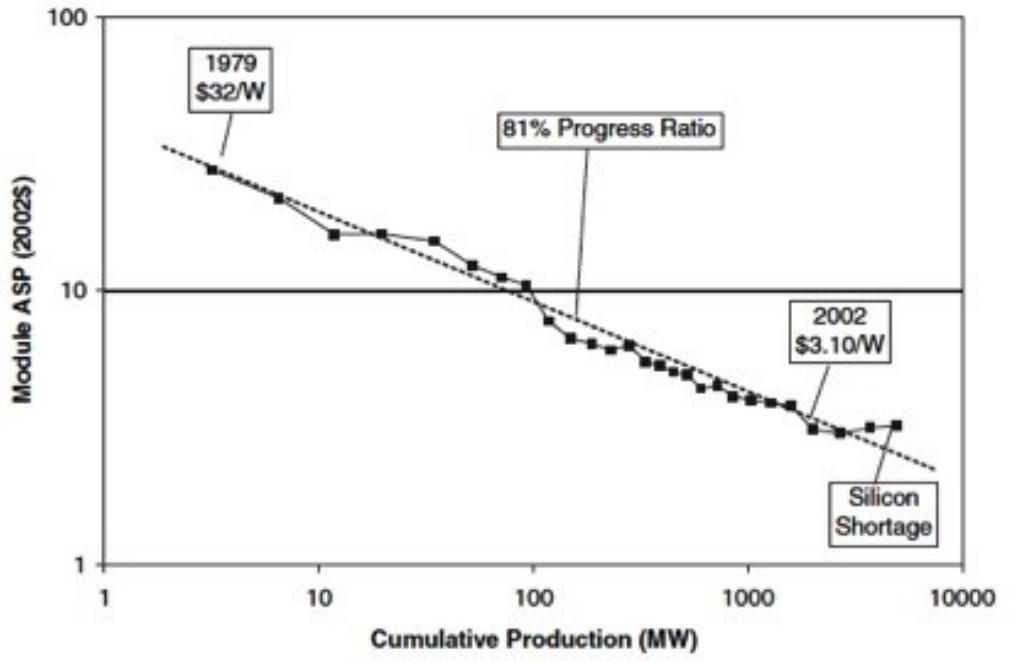

Figure 2.1: Swanson's Law, the cost of solar cells per watt falls by approximately 20% for every doubling of production, Module ASP is the cost per Watt and Cumulative Production is the total power output of solar panels manufactured per year [2].

2.1.1 Solar cell theory and equivalent circuit

The method by which solar cells convert captured light into electrical energy is found in the common electronic component the diode. Here the PN junction is exposed to light in order to move electrons to higher energy bands which generates a potential voltage between the two metal contacts, when a load is connected between the two metal contacts a current will flow and the cell will output power. The maximum output voltage is defined as the open circuit voltage (where the current is zero) and the maximum current is defined as the short circuit current (where the voltage is zero, both of these are dependent on the solar irradiance falling onto the cell.

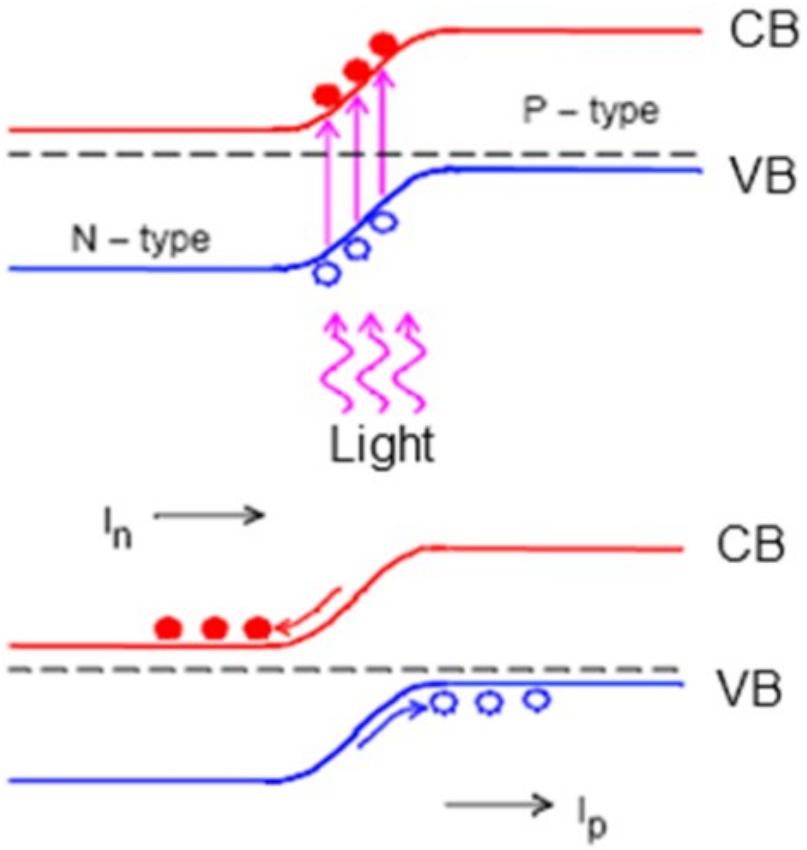

Figure 2.2: Band diagram of a silicon solar cell showing electron movement when exposed to light [3].

The voltage-current curve of the solar cell is non-linear, with the voltage dropping initially slowly with current before coming to a 'knee' where it begins to rapidly fall to zero, as noted earlier this curve is dependent on the amount of usable light falling onto the solar cell. As the power output of the cell is dependent on the voltage and current this V-I curve produces its own power output curve, with a clearly defined peak power.

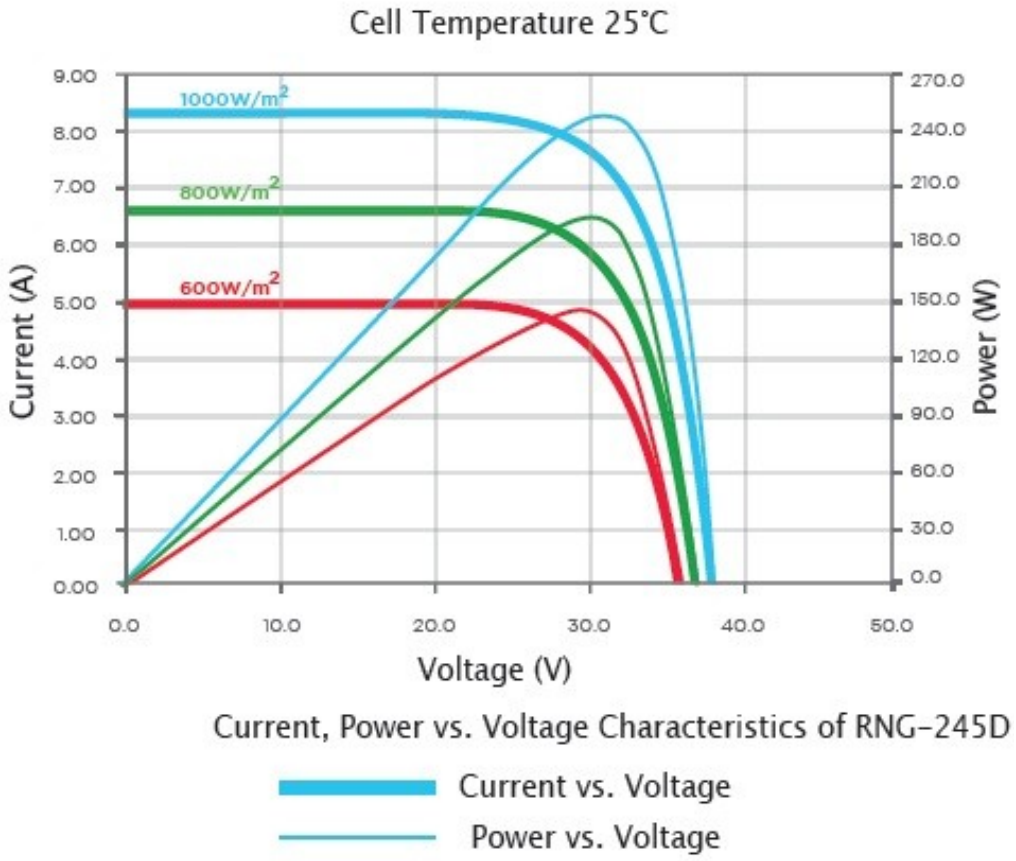

Figure 2.3: V-I and power output curves for a 245W commercial solar panel under various irradiance levels [4].

The cause of this characteristic curve is evident from the equivalent circuit diagram of the cell, the current source is dependent on the irradiance falling onto the cell. During open circuit conditions the current can only flow through the diode, limiting the output voltage to the diode voltage, under short circuit conditions the output current is limited to the output of the current source. Under other operating conditions the difference between the current draw of the load and that which is output by the current source is passed through the diode which gives rise to the V-I

curve of the cell looking like an inverted diode curve.

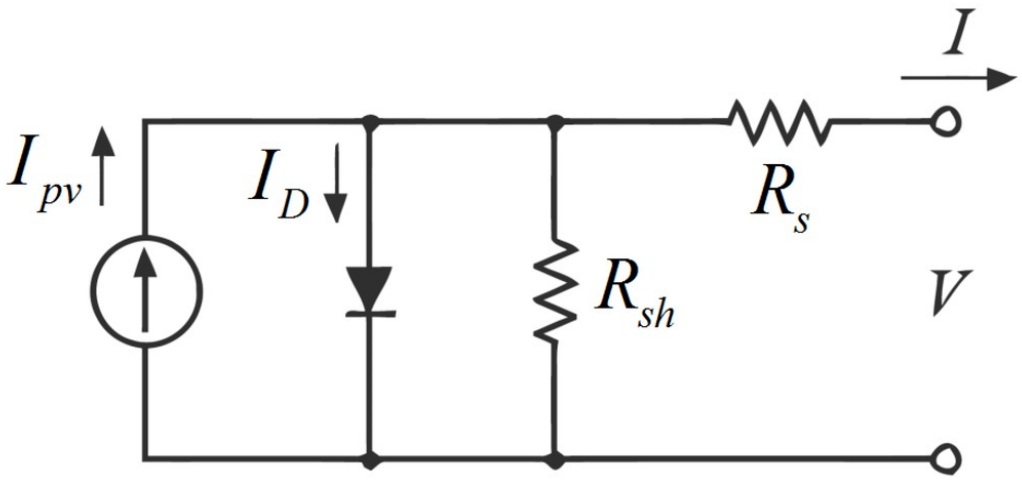

Figure 2.4: Solar cell equivalent circuit, the current source is dependent on the irradiance falling onto the cell [5].

There are two important aspects to note about solar cells which is clear from the equivalent circuit, the first is that the solar cell has no means of energy storage by itself, if light is being captured by the panel but the load is not available to use all the converted energy then it is wasted. The second being that the cell by itself can only output direct current (DC) electricity. These two aspects of solar cell are the main reason for this research, the reasons why will be discussed in section 2.3.

2.2 Mains power grid

The mains power grid is the infrastructure by which electricity produced at various locations ranging from large centralized power plants to small decentralized sources such as solar installations is distributed to

consumers ranging from industrial to domestic through several steps at different voltage levels. An overview of a typical mains grid is given in figure 2.5.

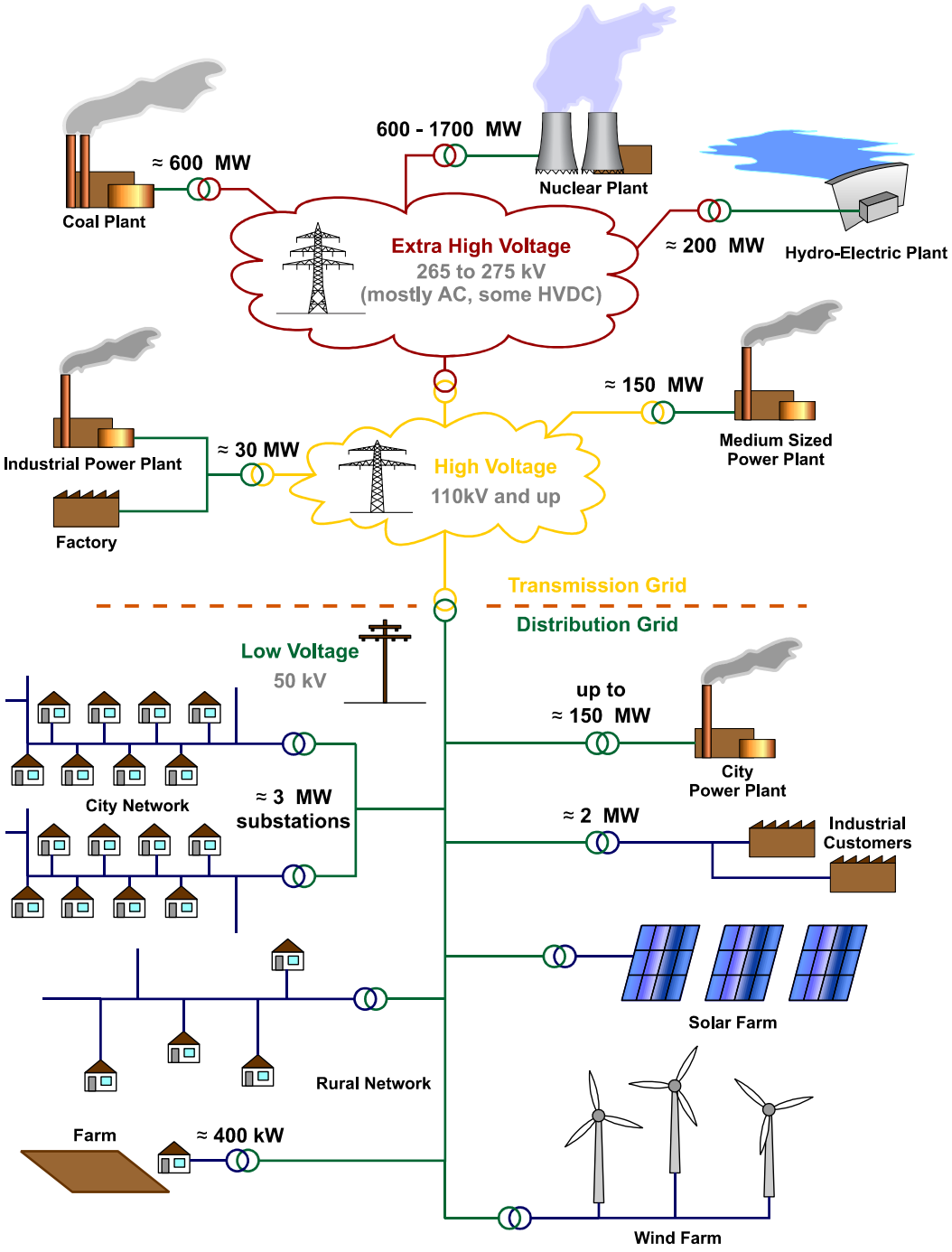

Figure 2.5: Typical mains power distribution grid.

On a distribution level the system relies on the electricity to be in the form of alternating current, or AC, at a transmission level direct current is sometimes used to minimize losses due to large line capacitance or where transmission is occurring between systems with different frequency AC systems.

The reason for the distribution level system being AC is due to its reliance on the use of transformers to step up and step down voltages in order to minimize resistive losses due to excessive currents, large power generation plants can output extremely large amounts of power without the need for excessively large conductors and as the power filters down through the system it is subsequently reduced as the currents become less and less. If the system was entirely DC then as they were being first constructed in the late 19th century either large numbers of power plants would need to be built due to the shorter maximum transmission length or far thicker conductors would be required to minimize losses, the high transmission and distribution voltages of the AC system require better insulation but this is far smaller in cost to thicker conductors.

Because of this, any power source which outputs a DC voltage such as a solar cell that wishes to provide energy to the grid must first convert it to AC, devices which convert DC to AC are known as inverters.

2.3 Power inverters

Power inverters are devices which convert DC electricity to AC electricity for use by home appliances or supplying energy to the mains grid. Inverter topology can take many forms depending on the desired input and output conditions, with each offering its own advantages and disadvantages. In each though there is at least some form of switching circuit to convert the uni-directional DC input to the bi-directional AC output.

Inverters are important devices for solar cells when the output is to be supplied to a load requiring and AC source such as the mains grid and their performance has a large impact on the effectiveness of the overall system.

Power inverter topologies vary depending on the application, however there are three main types [6] which can be divided into two basic groups. These are shown in figure 2.6, with the application determining which one will be used, note that the 'output filter' can include a transformer but this is typically reserved for the case where a DC/DC converter is not used.

2.3.1 Input filter

The input filter serves to block the input supply from inverter noise, the two main ones being the inverter switching frequency and the second order harmonic of the output frequency. Input filtering is typically done through the use of an LC low pass filter but can be done through other types [7].

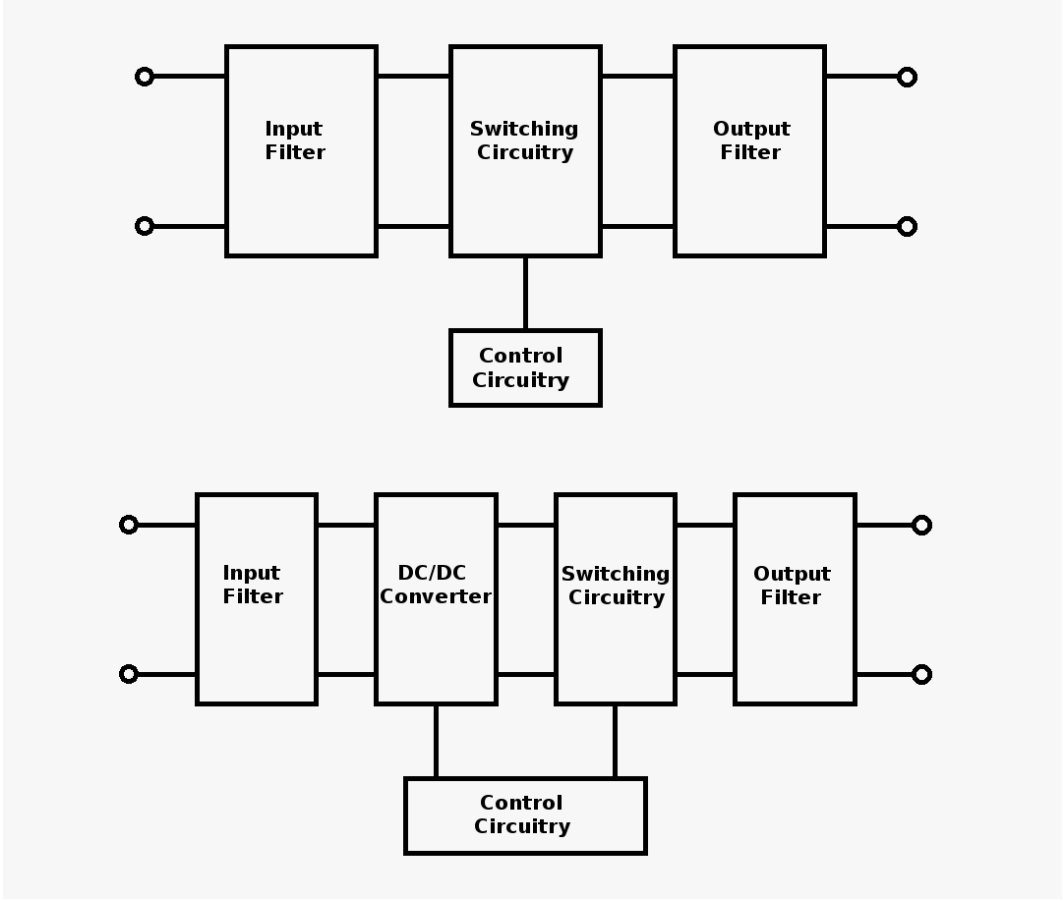

Figure 2.6: Two basic power inverter categories.

The filter works by acting as a temporary energy storage device with a much lower impedance than the source, during periods of high power draw energy is taken from the filter to reduce the load seen by the input supply and during periods of low power draw the filter draws excess energy and replenishes itself. In this sense the filter acts to smooth out the power input waveform of the inverter, reducing the peak and increasing the minimum.

The importance of input filtering varies by application, in the case of a battery or other source with a fixed energy supply filtering isn't crucial

outside of removing the switching noise and excessive peak currents in order to not disrupt other devices being powered by the same source. In the case of a solar cell or other power source input filtering is crucial as the source will output a fixed power and any time the inverter is incapable of using all of it the rest will be wasted. With solar installations it is important to utilize as much energy harvested by the solar cells as possible, converting it to AC and supplying it to the mains grid, if the inverter has input ripple then it is only drawing the maximum power available for a small amount of its operating cycle.

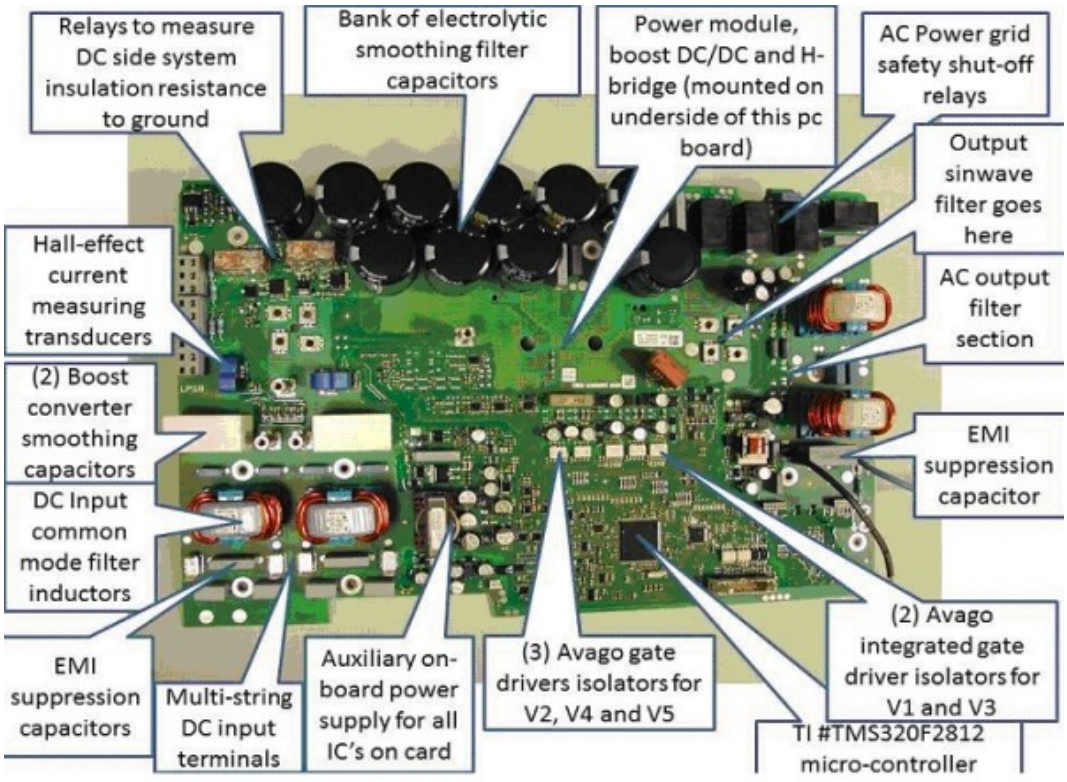

Figure 2.7: A commercial solar inverter showing the various components including the large electrolytic capacitor bank used to filter input ripple [8]

Inverter designers attempt to minimize input ripple by utilizing large capacitor banks in their designs, a commercial solar inverter with its large capacitor bank demonstrating this is shown in figure 2.7. These capacitor banks allow the inverter to store large amounts of energy during periods of the operating cycle with low power draw and release it during periods where the inverter is drawing large amounts of power. While this is effective at reducing the inverter input ripple it adds significantly to device size and cost, another thing which may not be evident is it also negatively contributes to the overall efficiency of the inverter due to resistive losses associated with charging a capacitor.

When a capacitor is charged to a voltage the total energy stored by that capacitor is given by equation 2.1, what is not obvious from this equation is that there is an equal amount of energy which is dissipated during charging of the capacitor due to the path resistance shown by equations 2.2-2.4. When large capacitor banks are used to store large amounts of energy during periods of the operating cycle of low power draw and then release it during periods where the power draw is high there is an equally large amount of energy which is lost. While this reduces overall efficiency of the inverter there is overall an increase in system efficiency as the inverter can utilize more of the solar cells output.

$$E_C = \frac{1}{2} C V^2 \qquad (2.1)$$

$$E_R = \int I^2 \cdot R \, dt \tag{2.2}$$

$$I = \frac{V}{R} \mathrm{e}^{\frac{-t}{RC}} \tag{2.3}$$

$$E_R = \int \frac{V^2}{R} \mathrm{e}^{\frac{-2t}{RC}} \cdot R \, dt = \frac{1}{2} C V^2 \tag{2.4}$$

The energy loss in equation 2.4 is the total energy loss which occurs when a capacitor is charged from 0V to a voltage V, a more general equation representing energy lost over the series resistance during charging is given by equations 2.5-2.6.

$$E_R = \frac{1}{2} C V_{Final}{}^2 - \frac{1}{2} C V_{Initial}{}^2 \tag{2.5}$$

$$E_R = \frac{1}{2} C \left(V_{Final}{}^2 - V_{Initial}{}^2 \right) \tag{2.6}$$

This indicates that the total energy lost by only partial charging is significantly less than what occurs from full charging, however this is still represents a non-trivial amount of energy for the inverter which reduces overall efficiency.

2.3.2 DC/DC converter

In the case of the input voltage being lower than the desired maximum output voltage a DC/DC converter is used to boost the input voltage to the required level, however this isn't always needed as the output circuitry could include a transformer for isolation which can perform the step-up

conversion. The DC/DC converter can include isolation if desired by the designer or required due to safety regulations [5].

2.3.3 Switching circuitry

In order to convert the DC to AC a switching circuit is needed, this can either be in the form of a push-pull arrangement using two transistors and a transformer [9] or a full-bridge design [6] which uses four transistors and does not require a transformer but may use one. These basic configurations are shown in figure 2.8.

Compared to the push-pull arrangement the full-bridge is far more common, having superior efficiency (both in the transformer and transformer-less configuration, although the latter is the more efficient of the two) and higher power handling capability.

2.3.4 Output filter

After the DC has been converted to an AC waveform another filter is required to remove the switching noise from the output waveform, like the input this is done with an LC filter, however if the switching circuity has a transformer only a capacitor is required due to the natural inductance of the transformer contributing to the filter, figure 2.9 shows a typical filter in the transformer and transformer-less case. With large mains-frequency transformers an output filter may not be needed.

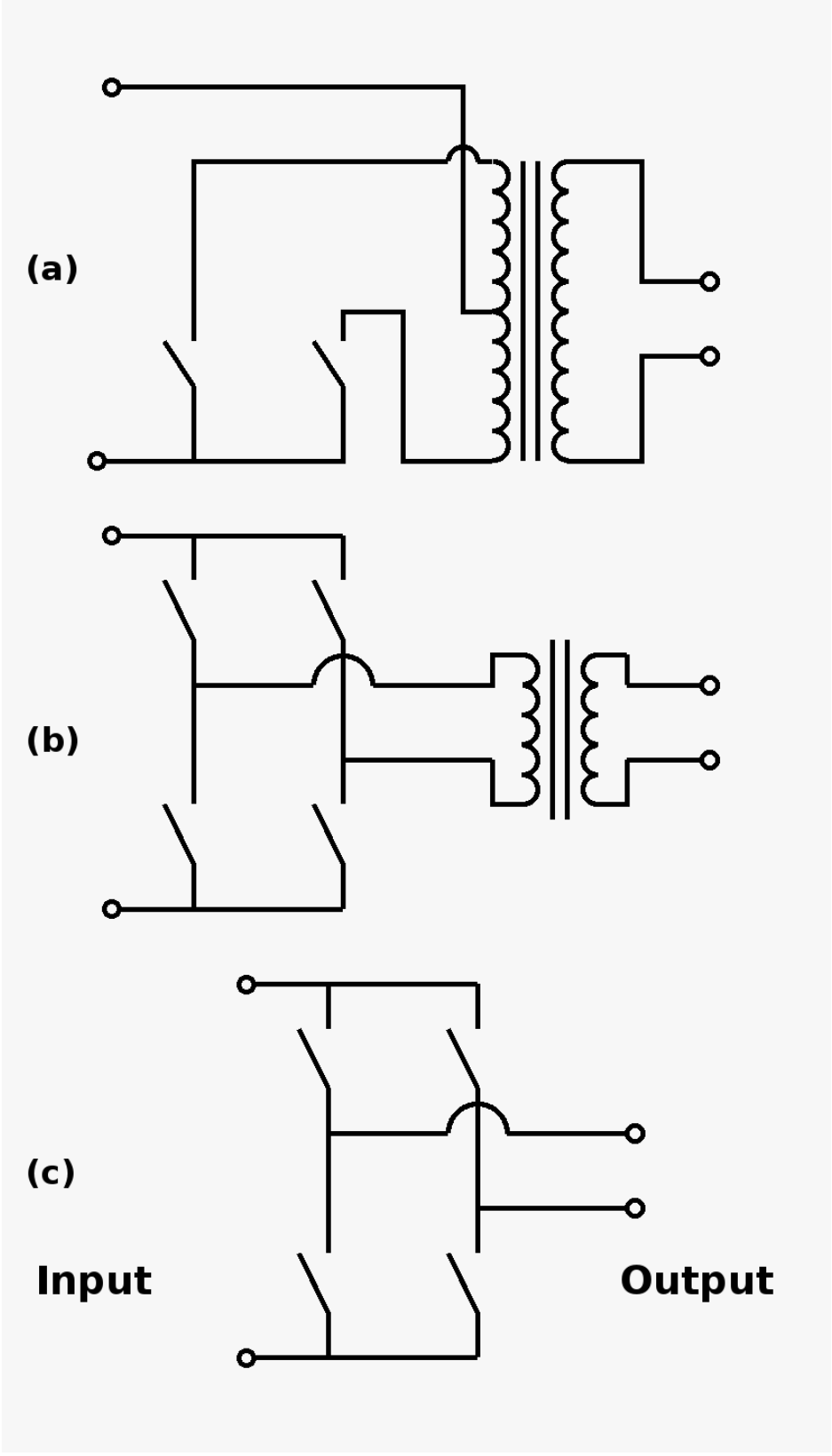

Figure 2.8: Push-pull (a), transformer isolated full-bridge (b), and non-isolated full-bridge (c) switching topologies.

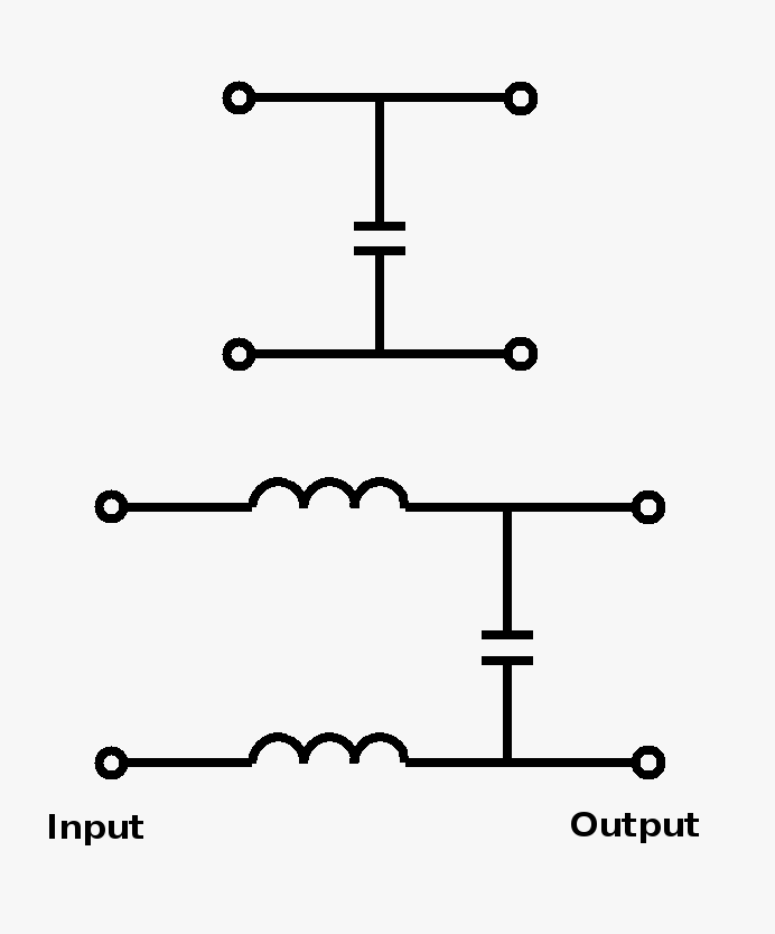

Figure 2.9: Possible inverter output filter for the transformer isolated (top) and non-isolated (bottom) cases.

2.3.5 Control circuitry

To drive the inverter a control circuit is required, this is commonly made up of a microcontroller and associated hardware such as voltage sensing circuitry although many low cost inverters which output a square waveform (known as 'modified-sine' inverters) have a simple oscillator circuit. In the case of a power inverter supplying energy to a mains grid the control circuitry does more than drive the switches at the appropriate frequency, safety standards require inverters supplying power to the mains grid to prevent conditions such as islanding where the mains utility has stopped

because of various reasons but inverters continue to supply power to the grid [10]. In this case if the inverter continues to supply power to the grid it would create an island of powered grid which may pose a danger to people working on grid infrastructure which they believe is unpowered.

Another important function the power inverter control circuitry performs when being powered by a solar panel is known as maximum power point tracking [11], as solar panels have a point on their V-I curve where they are producing maximum power it is crucial to maintain the inverter draw as close to this as possible in order to maximize the utilization of the solar panel.

2.3.6 The solar micro-inverter and nano-inverter

Current trends in solar inverter development are towards the development of micro and nano inverters, solar inverters which operate a single panel or small array of panels rather than a conventional inverter which runs a large array. By running the panels individually or in a small array they can individually be tracked for their maximum power point [12] which changes with solar irradiance, if a large array of cells is partially shaded then the V-I and maximum power curves of the array is negatively effected, figure 2.10 shows the characteristics of a solar panel under partially shaded conditions.

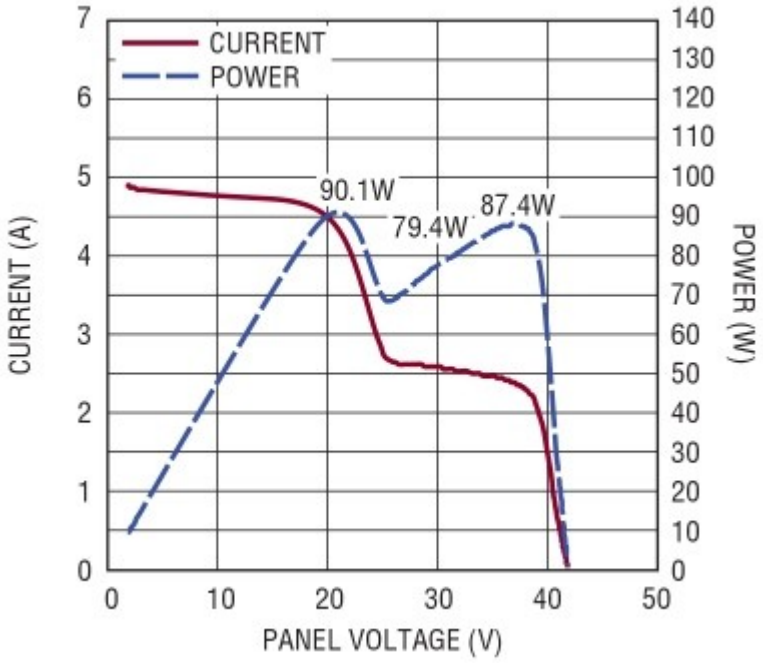

Figure 2.10: Example solar panel V-I curve under partially shaded conditions [13]

By dividing the panels into smaller arrays or single cells they can be individually tracked, if one array is partially shaded it does not negatively impact the performance of the overall system. Of course, such a system requires more inverter units than a conventional setup, putting an emphasis on low unit cost and small physical size. Because of this the conventional means of input ripple filtering utilizing large and expensive capacitor banks is unsuitable and alternate means of ripple control must be investigated.

2.4 Supercapacitors

Supercapacitors are a type of capacitor which utilize an effect known as double layer capacitance to store energy, double layer capacitance is an effect where an ion in a solution will move to the surface of a conductive

electrode and 'stick' without giving up its electrons if the electric field is below a certain voltage. This results in an extremely small charge separation distance on the order of less than a single nanometer which produces very large capacitances on the order of 1F in small packages to several thousand in larger ones.

Despite their large energy storage compared to conventional capacitors such as electrolytics, supercapacitors are also capable of high power outputs compared to devices such as batteries, this is shown by the Ragone plot of various energy storage devices in figure 2.11.

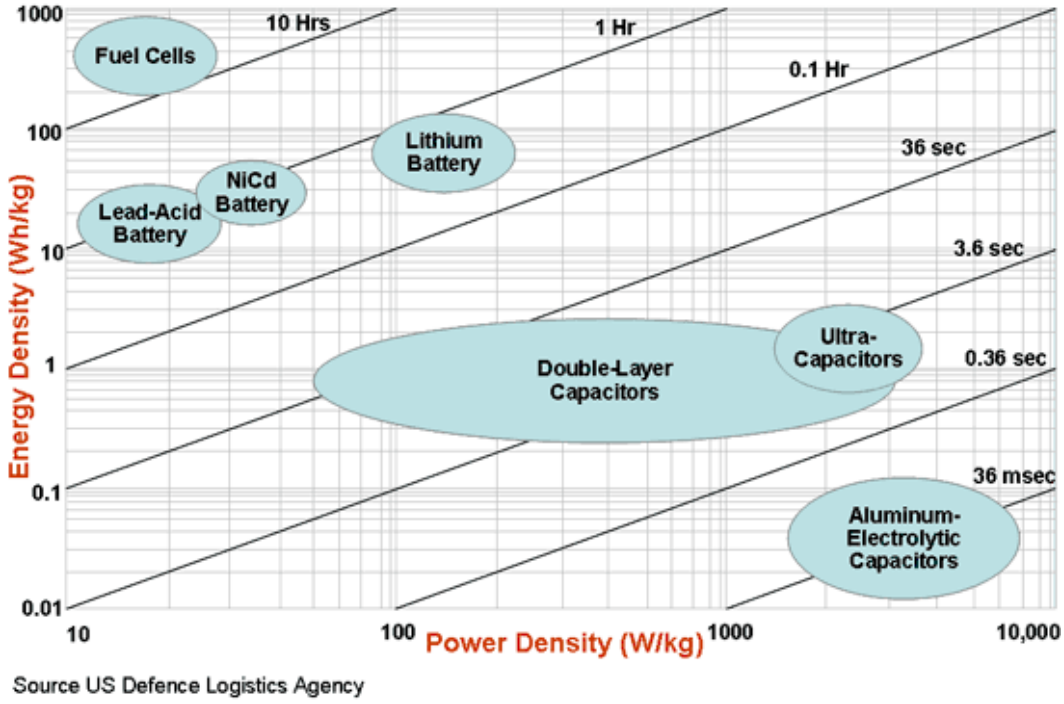

Figure 2.11: Ragone plot of various energy storage devices [14].

Chapter 3

3.1 Commercially available power inverters

In order to examine the issue of inverter input ripple several commercial inverters were tested, these units are automotive inverters used to take the 12V DC nominal car battery voltage available from common car cigarette lighter sockets and output a 230Vrms AC waveform for powering household appliances. While they aren't solar inverters their operation is similar, particularly with regards to input ripple filtering, the main differences between these and solar inverters is the lack of maximum power point tracking. Maximum power point tracking isn't relevant to automotive applications as the car electrical system is a voltage source capable of outputting large currents with only small drops in voltage rather than the solar cell which as discussed in chapter 2 is a current source with a non-linear V-I curve.

The inverters investigated were two modified sine wave units, one circa early 2000s and one current production (however their initial release date is unknown and the designs are likely far older), and one pure sine wave inverter. As they are designed to operate on 12V DC and output 230V AC all feature a step-up converter which also provides isolation.

All inverters were tested with an input voltage of 12V and with resistive incandescent bulb loads of 40W and 100W and a capacitive load of

2.75uF which at 50Hz gives approximately 45VA. Note that the capacitive load represents the worse case scenario in terms of power factor and most reactive load devices have additional capacitors or inductors to correct the power factor.

For quantification purposes, the input ripple is the ratio between the mean and peak to peak input currents expressed as a percentage.

3.2 Old model modified sine wave inverter

This device represents the lowest cost inverter, there is no complex control circuitry on this inverter as everything from the step-up conversion to output switching is done through oscillator circuits. The maximum power output of this inverter is 150W which is also the lowest of the three tested. Figure 3.1 show the internals of the square wave inverter, the small input capacitor and step-up converter circuitry is on the right hand side while the output switching circuitry is on the left.

As noted there is no microcontroller in this circuit, each section of the inverter has an oscillator made from a 555 timer with a CMOS logic chip to produce the required control signals to drive the transistors. The switching elements on both the step-up converter and output switching circuitry are BJTs, this is likely done to reduce the cost of the unit by not requiring complex bootstrap drivers.

The transistors on the output side have what appears to be some kind of temperature sensor, this is likely to perform the overload checking by monitoring the transistor temperature and shutting the inverter down when it exceeds its design limit which would occur after a period of excessive power draw.

Figure 3.1: Old model modified sine wave inverter, input is on the right and output on the left.

Figures 3.2 and 3.3 show the input current and output waveform with a 40W and 100W resistive load respectively. As they show the inverter has significant input ripple even with small resistive loads. This is likely due to its small input capacitor not being able to effectively supply the inverter

with energy during periods of the output cycle where the power output is non-zero. The input ripple with the 40W load is 69% and with the 100W load is 61%.

The input current and output voltage waveforms for the capacitive load is shown in figures 3.4, the input ripple with this load is 65%.

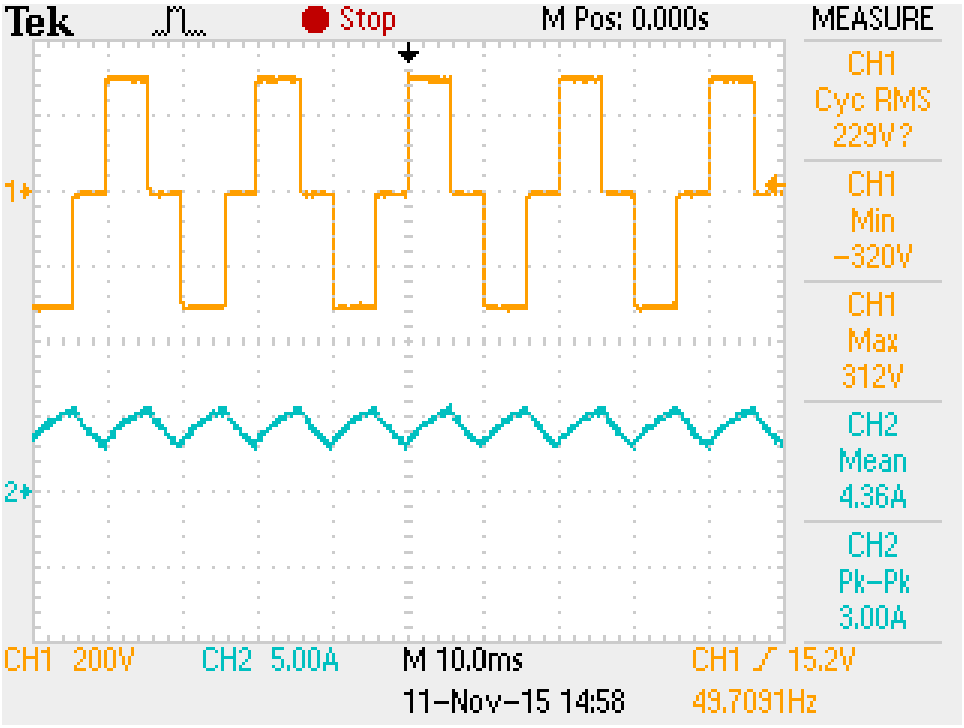

Figure 3.2: Input current (bottom trace) and output voltage (top trace) for the old model modified sine wave inverter with 40W resistive load.

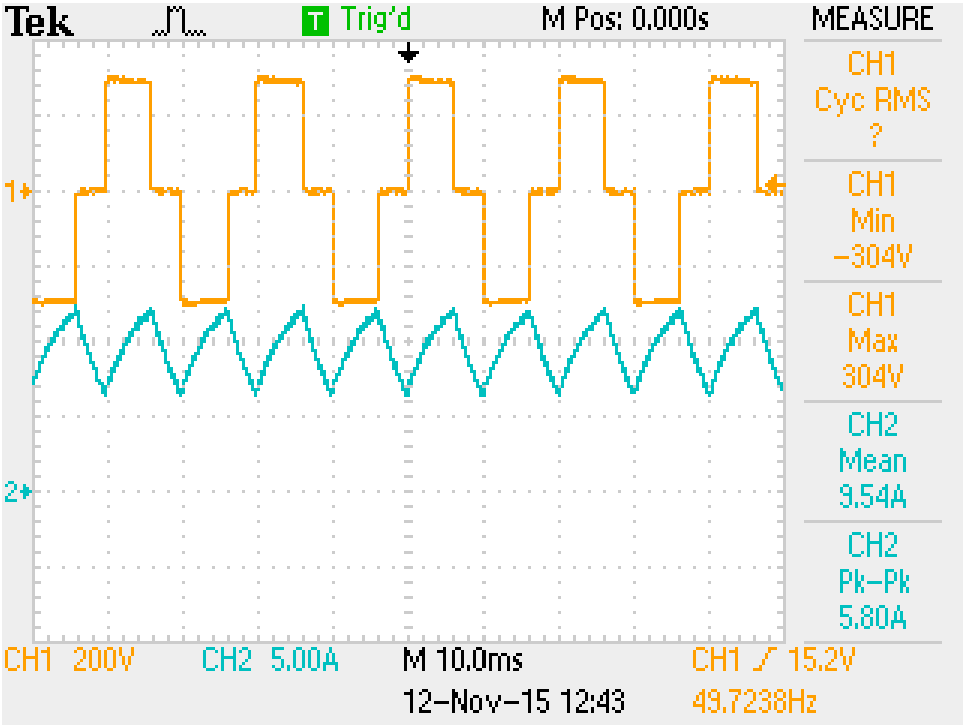

Figure 3.3: Input current (bottom trace) and output voltage (top trace) for the old model modified sine wave inverter with 100W resistive load.

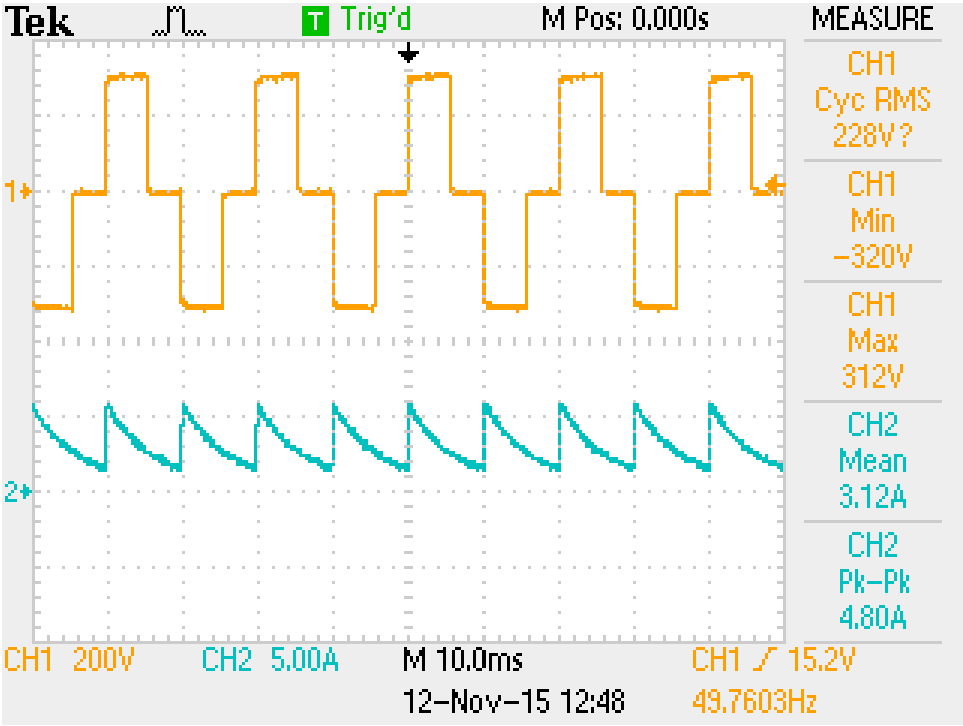

Figure 3.4: Input current (bottom trace) and output voltage (top trace) for the old model modified sine wave inverter with 45VA capacitive load.

3.3 Current model modified sine wave inverter

The modified sine wave inverter is shown in figure 3.4, compared to the previous inverter this has several improvements to the circuitry, namely the replacement of BJTs with MOSFETs and the overload protection now done via a current sense rather than monitoring the temperature of the switches. As with the previous inverter this one also only has a small filter capacitor as filtering of input ripple is not a significant issue.

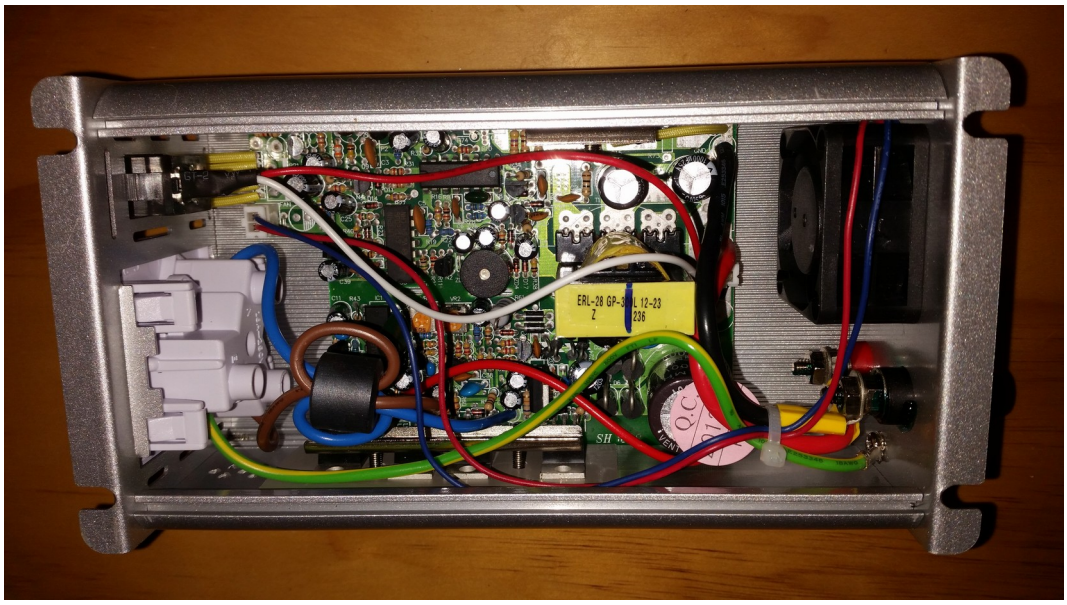

Figure 3.5: Current model modified sine wave inverter.

Like before the inverter was tested with the three loads, the waveforms are shown in figures 3.6-3.8, however unlike the previous inverter which used transistor temperature to detect overload this inverter would not drive the capacitive load. This is likely due to the current sense overload detecting what it thinks is a short circuit and cutting the output, when the capacitive load was connected the inverter would output the waveform shown in figure 3.7 once a second, presumably to test for the short circuit condition.

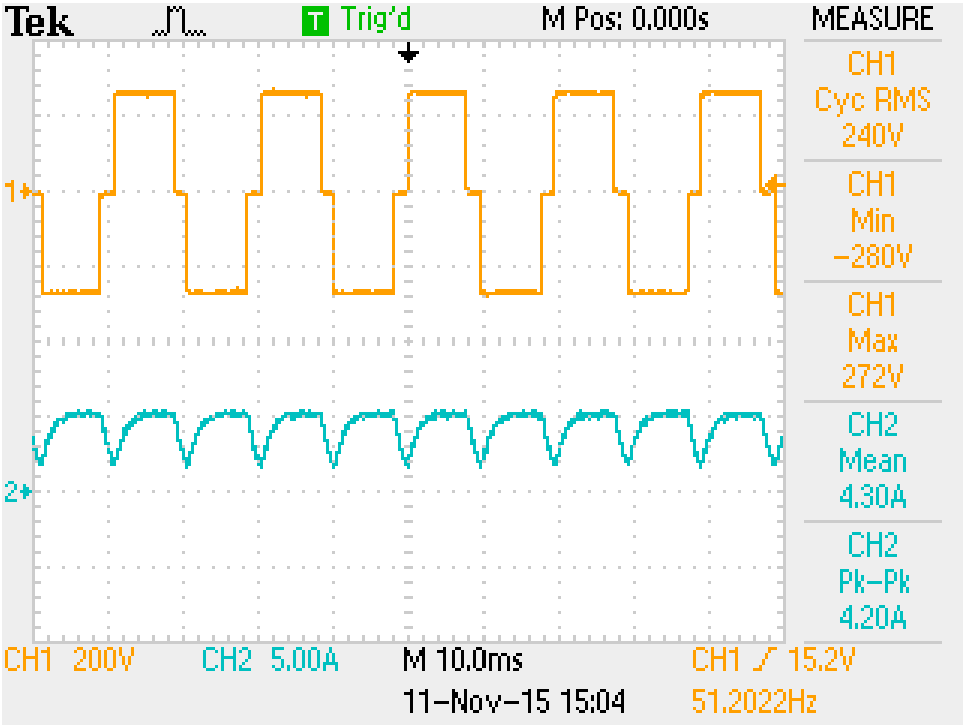

Figure 3.6: Input current (bottom trace) and output voltage (top trace) for the current model modified sine wave inverter with 40W resistive load.

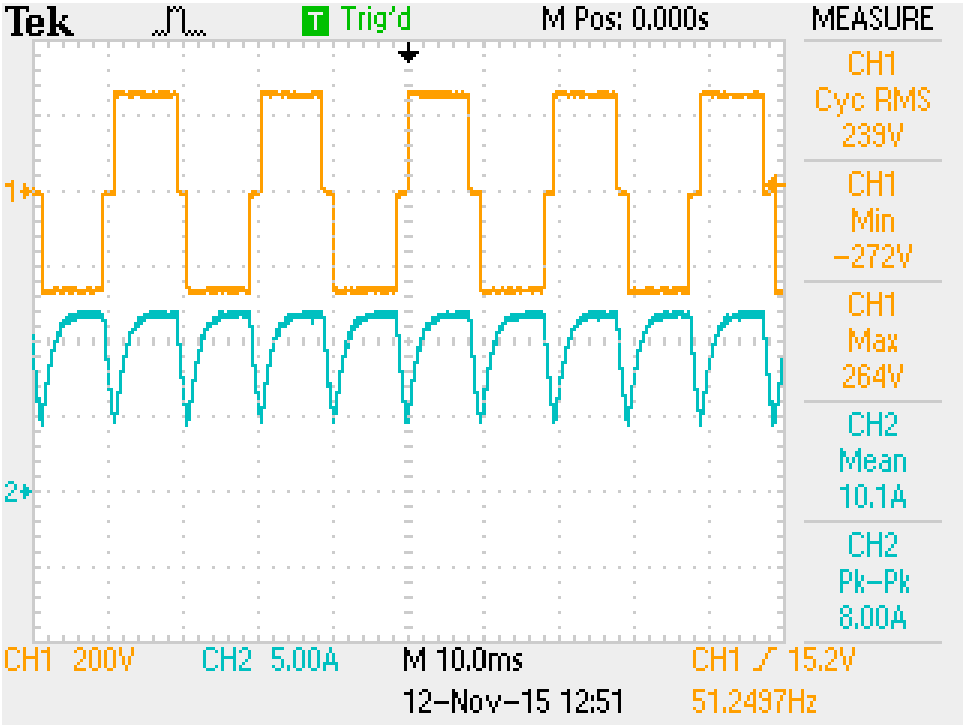

Figure 3.7: Input current (bottom trace) and output voltage (top trace) for the current model modified sine wave inverter with 100W restive load.

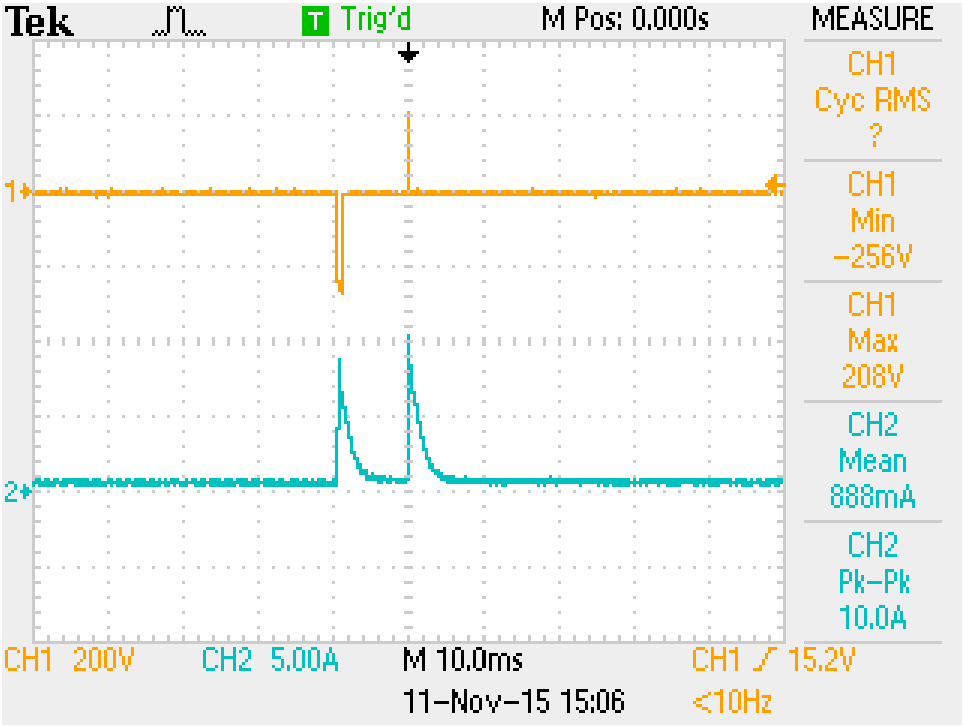

Figure 3.8: Input current (bottom trace) and output voltage (top trace) for the current model modified sine wave inverter with 45VA capacitive load. This waveform repeated approximately once a second.

The input ripple for this inverter with the 40W load is 98%, with the 100W load it is 79%, however, this isn't as bad as it first appears. The input current waveform for this inverter can be described as 'flatter' than the previous inverter which was more like a triangle wave, while the very large compared to the mean the dips in input current are far shorter, presumably because of the smaller 'off time' between the two halves of the output cycle where the inverter output is zero.

3.4 Pure sine wave inverter

The last inverter examined is the pure sine wave inverter, this unit quite

different to the previous two inverters in many aspects, from its circuit topology to the output waveform. The pure sine wave inverters are shown in figures 3.8 and 3.9, this inverter actually uses microcontrollers on both the step-up converter and the output switching, with the former being located on the main PCB while the latter being part of what appears to be an off the shelf controller which plugs into the main PCB and has the required bootstrap drivers for the MOSFET switches. Unlike the previous two inverters this unit has a large output filter, made up of a large toroidal inductor and several small capacitors, this is likely because the controller cant accurately output a pure 50hz sine wave under all conditions so the filter removes these unwanted higher order harmonics as well as the switching frequency from the output.

Figure 3.9: Pure sine wave inverter, input is on right and output is on left. Note the large toroidal inductor which forms part of the output filter.

What is also interesting about this inverter is the presence of a second transformer, this is likely a dedicated transformer for producing the low voltage for the microcontroller and is separate because of noise issues potentially disrupting voltage sensing or other functions if it was produced by the same transformer which does the step-up conversion.

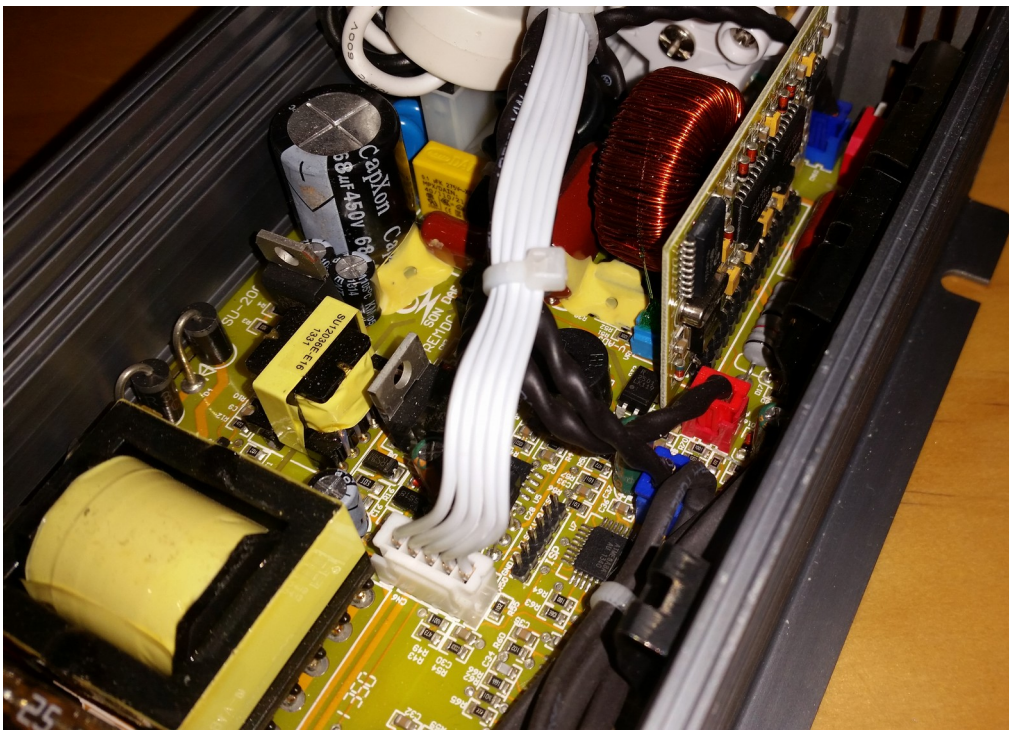

Figure 3.10: Close up of the circuitry of the pure sine wave inverter, note the vertical PCB which contains the microcontroller and associated MOSFET drivers for the output and large toroidal inductor behind it for the output filter.

Like with the other two inverters the pure sine wave unit only was tested with 40W and 100W resistive bulb load, the waveforms for these are shown in figures 3.10 and 3.11 respectively. As these show the input ripple for this inverter has a sine wave like shape with a frequency twice that of the output, there is also a slight phase delay between the two waveforms with the input current lagging behind the output by a small amount.

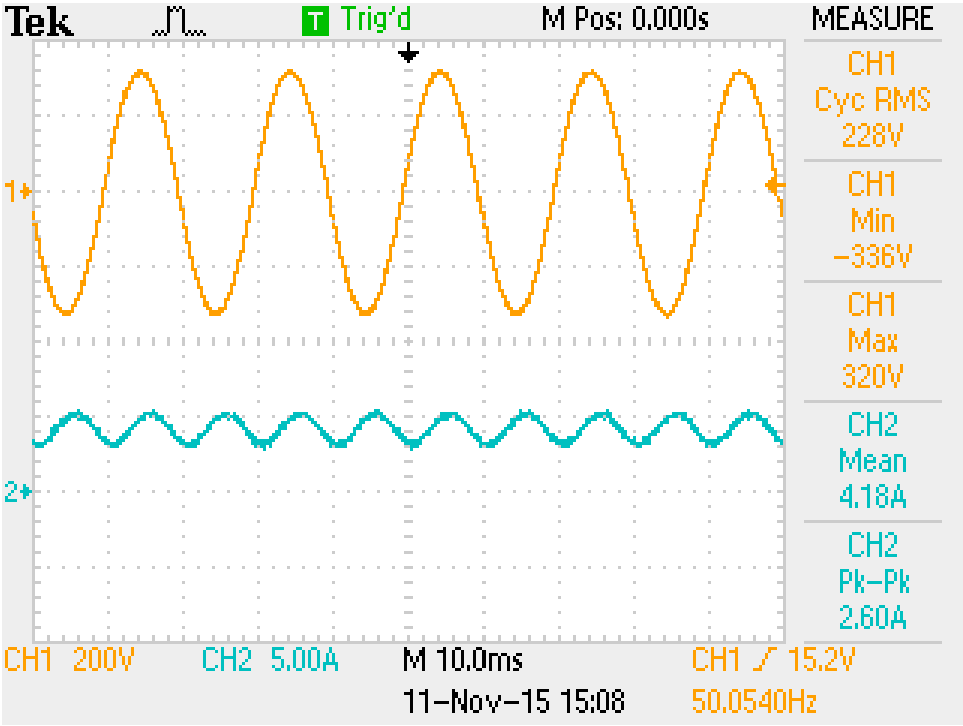

Figure 3.11: Input current (bottom trace) and output voltage (top trace) for the pure sine wave inverter with a 40W resistive load.

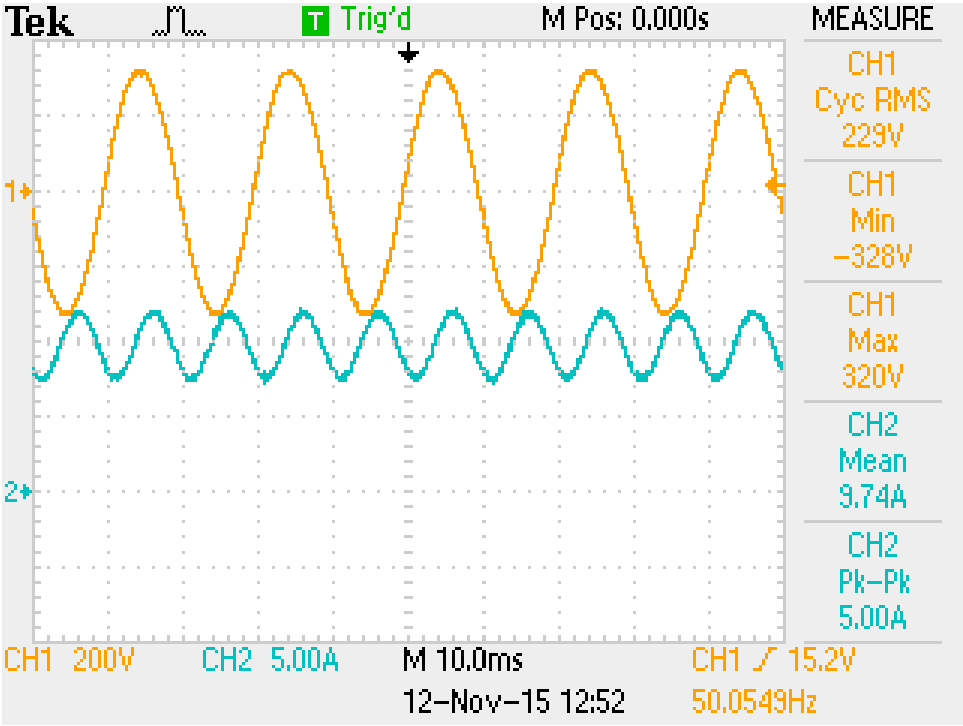

Figure 3.12: Input current (bottom trace) and output voltage (top trace) for the pure sine wave inverter with a 100W resistive load.

The ripple of the pure sine wave inverter with the 40W and 100W loads is 62% and 51% respectively. While the this is less than the current model modified sine wave inverter it is arguably worse as its more like the old model modified sine inverter in shape, with 'long' valleys and peaks while the current model modified sine inverter had large but short 'spikes' in current draw. In a sense the peak current isn't as close to the mean current as the modified sine inverter which had a peak current very close to the mean which is important as one of the main objectives of ripple filtering is to reduce the peak power requirements of the inverter so having the input current briefly drop to almost zero isn't as much of a concern as having half the input current cycle excessively higher than it needs to be. Figure 3.13 shows the three input current waveforms with the 100W load to demonstrate this concept.

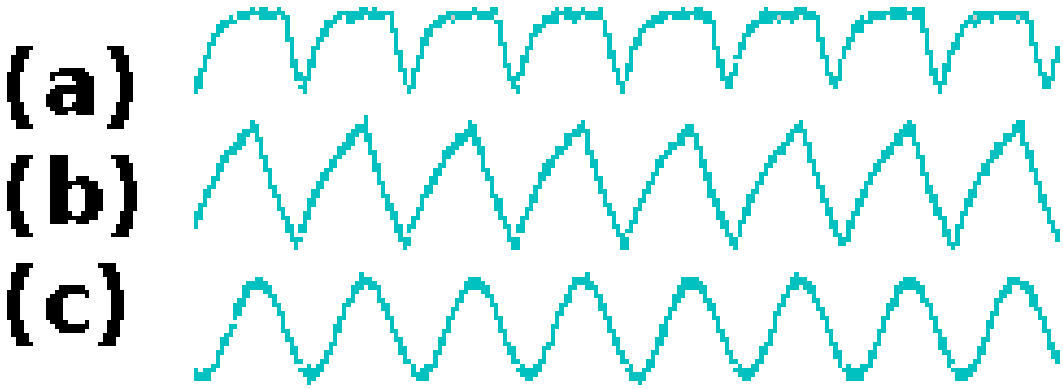

Figure 3.13: Input waveforms for the three inverters, the current model modified sine inverter (a) has a mean current close to the maximum than the minimum, compared to the old model modified sine (b) and pure sine (c) inverters which have a mean current half way between the minimum and maximum.

What this shows is that while ripple measurements which compare the mean and the peak to peak input values is useful in quantifying the input ripple performance of individual inverters it isn't the only metric to consider when evaluating overall inverter performance.

Chapter 4

4.1 Input ripple

As shown in the chapters 2 and 3, the input ripple of the inverter plays an important role in determining the performance of the inverter, especially when used with solar cells. In regards to solar systems if the inverter has poor input ripple performance then the solar cell not only must be over sized in order to meet the peak power requirements, but the inverter cant properly track the maximum power point of the solar cell which leads to lower efficiency. The causes for input ripple are simple, take the case shown in figure 4.1 of an inverter with no means of temporary energy storage outside and no losses, in this case the input power must equal the output power.

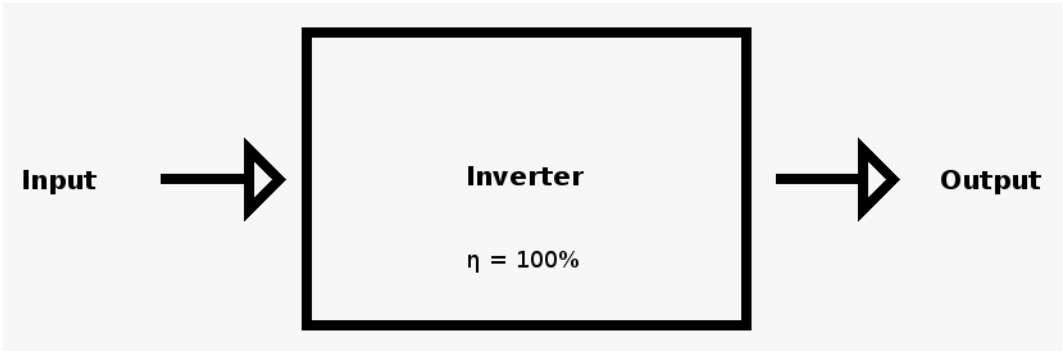

Figure 4.1: Ideal inverter.

What this means is that if the instantaneous output power is low then the instantaneous input power is low, if the instantaneous output power is high then the instantaneous input power is high. With an AC waveform the

output power being low can be due to either the output voltage being low (output phase is near 0 or 180 degrees) in the case of an ideal resistive load, or the output current being out of phase with the voltage due to the load being highly reactive. Figure 4.2 shows the voltage, current, and power waveforms for several cases of voltage and current phase angles. Note that in the case of the two waveforms not being in phase there is a period where the output power is negative, in the case of inverters this energy is wasted. Even if the inverter was capable of pushing energy back into the supply it would be wasted in the case of a solar panel because of its diode-like equivalent circuit, and may even cause damage if the current is high enough.

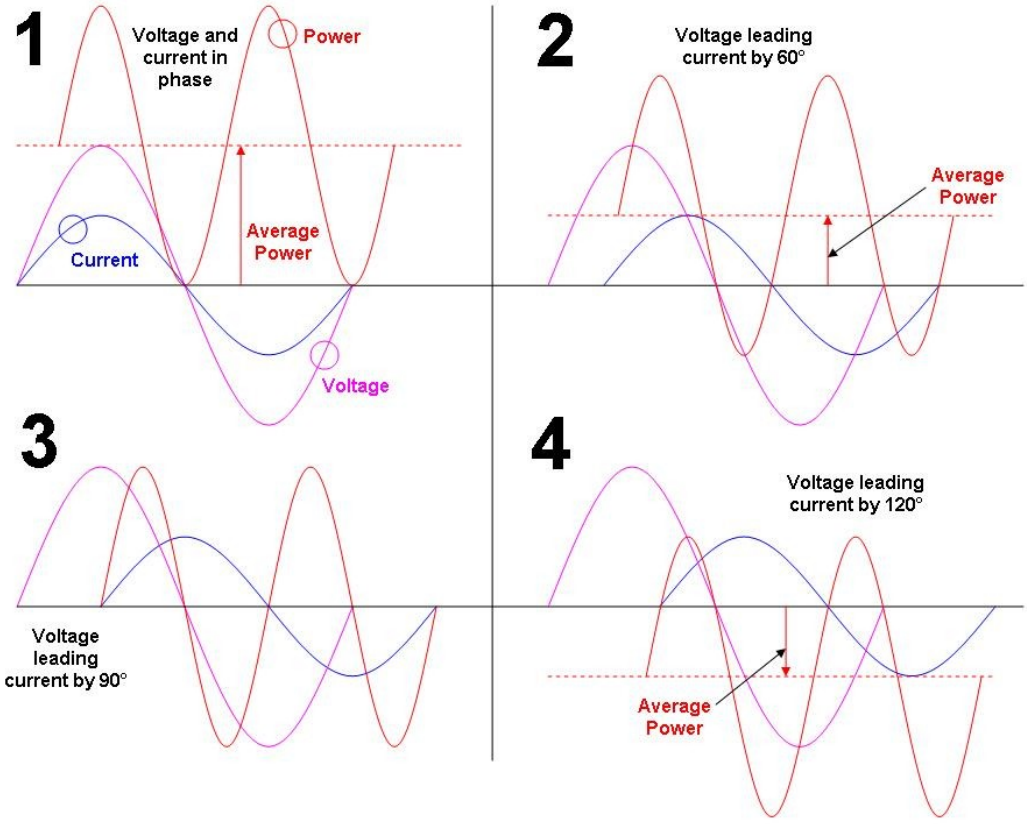

Figure 4.2: Voltage, current, and power waveforms for various phase angles.

It is evident that what is needed is a form of energy storage in the inverter, to not only store excess energy during periods of the output cycle with low output power for release during periods of high output power, but as a potential energy store for the case where power is flowing back into the inverter from a load due to a reactive component.

In the commercial inverters examined in chapter 3 this task was performed by an LC circuit. This circuit acts as a low pass filter to provide a long time constant from the perspective of the power supply by storing energy in the capacitor and using the inductor to prevent sudden changes in input current. While this circuit is simple to implement it suffers from several disadvantages if large amounts of ripple ripple reduction be desired. The primary concern is that the size of the components becomes excessive at high output powers, with the secondary concern is that charging of a capacitor in parallel with a load causes excessive energy loss. As shown in chapter 2 with equations 2.1-2.4 for any given amount of energy stored in a capacitor there is an equal amount of energy dissipated in the series resistance of the charging circuit, large amounts of energy stored in a parallel capacitor result in large energy loss which is counter-productive to efficiency.

4.1.1 Supercapacitors as bulk energy storage

The storing of energy in a capacitor causes a non-zero amount of energy to be dissipated through the path resistance, however if the load was

placed in series with the capacitor during charging then its equivalent resistance would become part of this path resistance. If the capacitor equivalent series resistance was small compared to the load resistance then amount of energy dissipated over it compared to the load would be negligible, causing most of the energy to not be lost.

This technique is applicable to inverters, however in its current form it is useless as (assuming a capacitor operating voltage of half the input) half the time the inverter draws twice the power required as its charging the capacitor and the other half it draws none as it discharges the capacitor. This is obviously not suitable for use in solar panels where drawing maximum energy at all times is a primary objective.

4.2 The switched supercapacitor assisted inverter

The idea of placing a large supercapacitor in series with the inverter to act as a losses voltage drop is useful to controlling input ripple as it causes the inverter to draw a larger amount of energy than it normally would which can then be used later to lower the amount of energy it draws from the power supply when the output power is high.

However, a single inverter by itself is incapable of using this as mentioned in section 4.1.1, in order to allow the inverter to draw current during discharge there must be a second inverter to discharge the capacitor while the main inverter runs directly from the full input. In other words the main

inverter is capable of running in series with the supercapacitor in order to increase the power draw during periods of low output and then when the capacitor is to be discharged it is switched to the secondary inverter which 'boosts' the output power while the primary inverter runs from the full input in order to increase the output power above the input power. Figure 4.3 demonstrates this concept. In order to avoid confusion these two inverters will be referred to as 'sub inverters'.

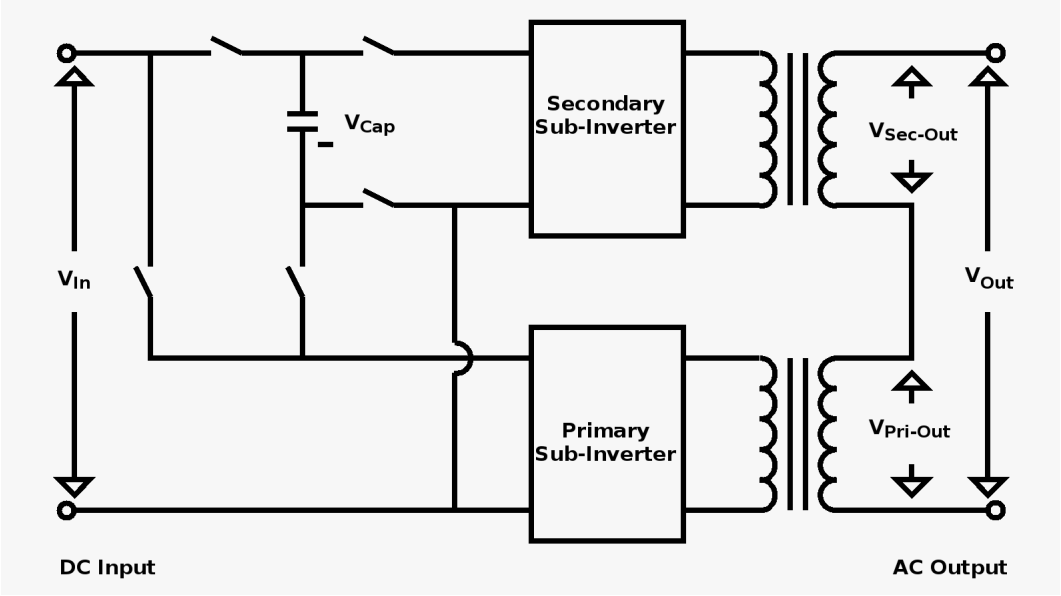

Figure 4.3: Switched supercapacitor assisted inverter.

Such a circuit would have three distinct operating modes.

4.2.1 Inverter operating mode 1

In this mode the main sub inverter in series with the capacitor, assuming

the capacitor is held at a voltage half that of the input then the main inverter needs to draw twice the current to achieve the same power output, figure 4.4 illustrates the parts of the output cycle where this mode is used.

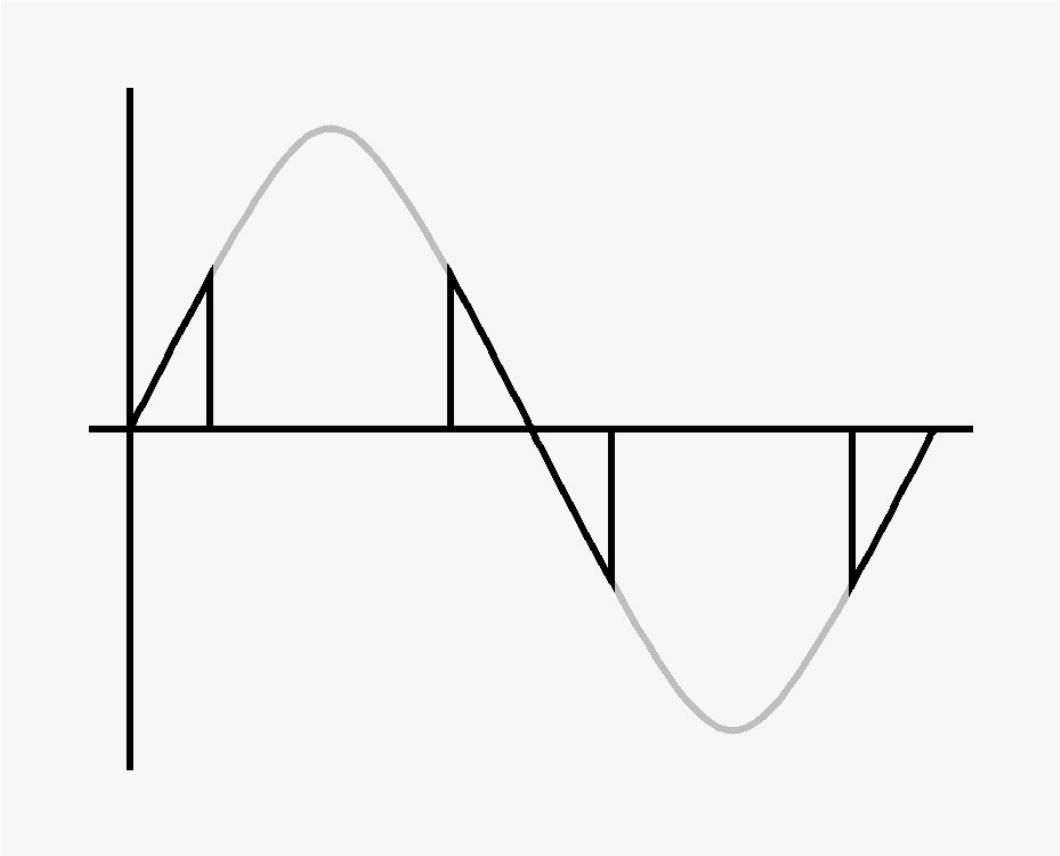

Figure 4.4: Periods of the output cycle where mode 1 is used.

In order to maintain capacitor charge balance, over any given half-cycle the energy stored in the capacitor when operating in this mode must be drawn by the secondary sub-inverter when running in mode 3 over that same half-cycle. Figure 4.5 shows the configuration of the inverter when running in this mode along with the input current flow, grayed-out areas indicate unused parts of the inverter. The relationship between the

instantaneous input and output power when operating in this mode is given by equations 4.1-4.3, the rate of change in capacitor voltage is given by equations 4.4-4.5.

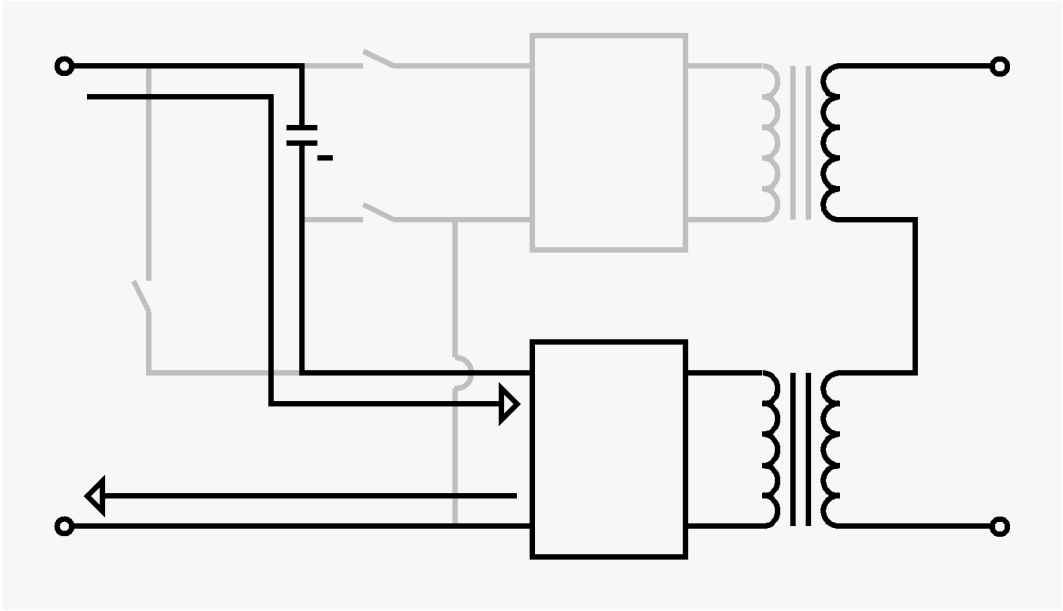

Figure 4.5: Switched supercapacitor assisted inverter during mode 1, arrows show input current flow through the inverter.

$$p_{Input} = i_{Primary} \cdot V_{Input} \tag{4.1}$$

$$p_{Output} = (V_{Input} - v_{Cap}) \cdot i_{Primary} \tag{4.2}$$

$$p_{Input} = p_{Output} \cdot \frac{V_{Input}}{(V_{Input} - v_{Cap})} \tag{4.3}$$

$$i_{Cap} = i_{Input} = \frac{p_{Output}}{(V_{Input} - v_{Cap})} \tag{4.4}$$

$$\frac{p_{Output}}{(V_{Input} - v_{Cap})} = C\left(\frac{dv_{Cap}}{dt}\right) \tag{4.5}$$

Where $i_{primary}$ is the instantaneous current being drawn by the primary inverter.

4.2.2 Inverter operating mode 2

In this mode the main sub inverter running off the input, in this case the inverter is drawing the same power it is outputting and the capacitor is neither being charged or discharged and is used during the periods of the output cycle shown in figure 4.6.

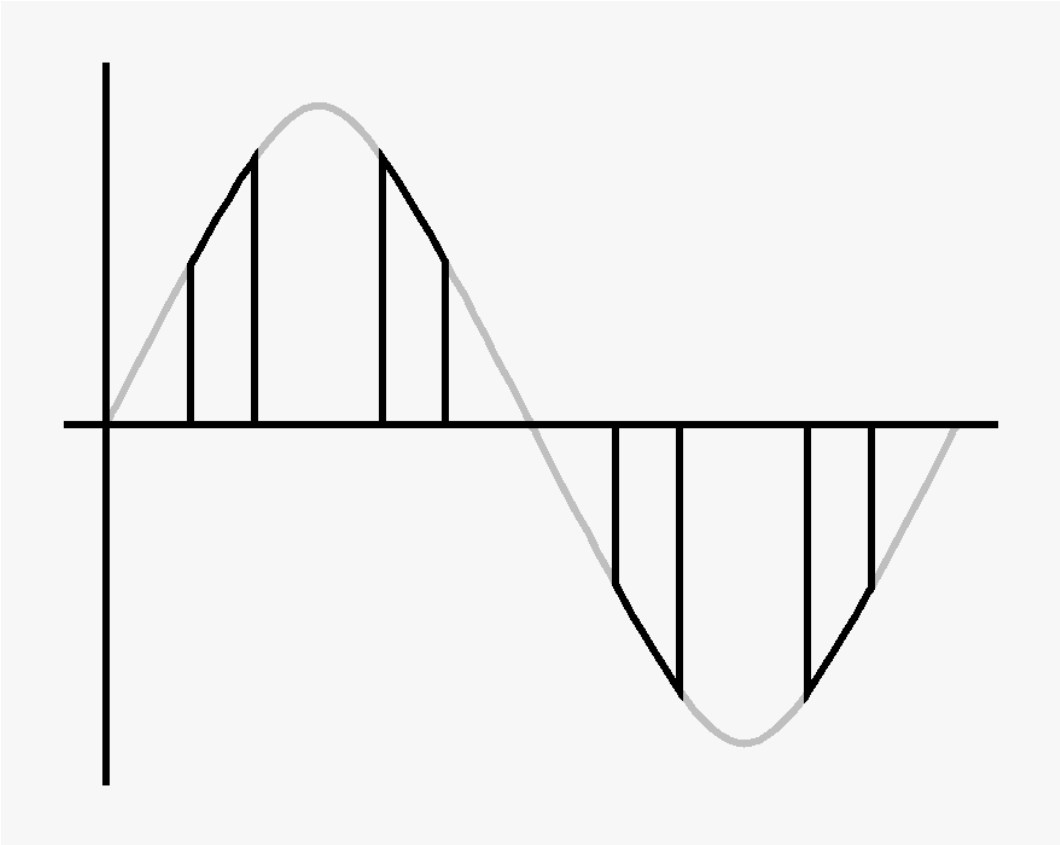

Figure 4.6:Periods of the output cycle where mode 2 is used.

Figure 4.7 shows the configuration of the inverter when running in this mode along with the input current flow, equation 4.6 gives the relationship between the instantaneous input and output power when in this mode.

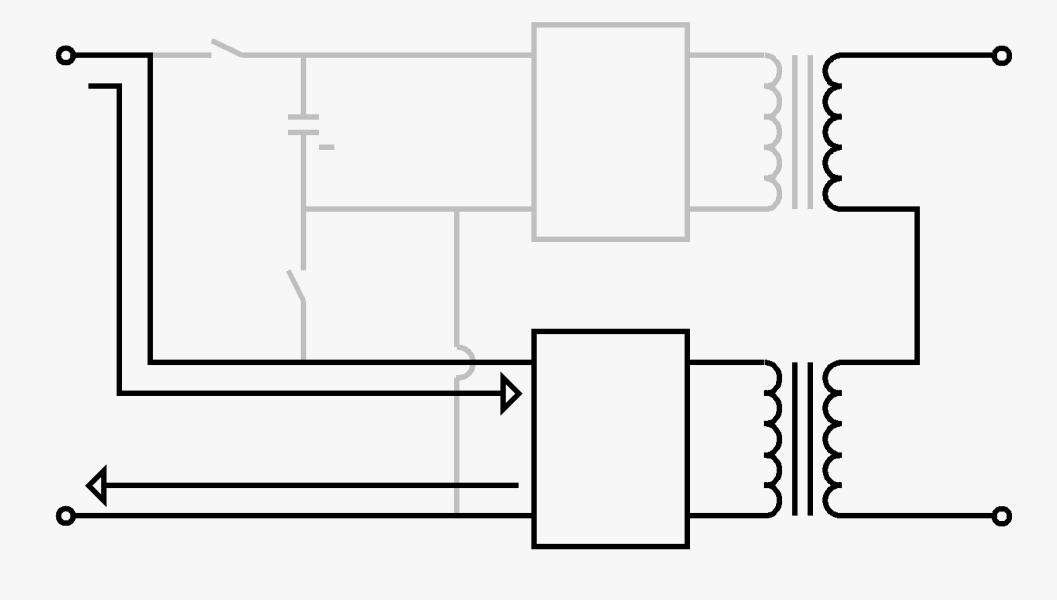

Figure 4.7: Switched supercapacitor assisted inverter during mode 2, arrows show input current flow through the inverter.

$$p_{Input} = p_{Output} \tag{4.6}$$

4.2.3 Inverter operating mode 3

In this final mode the main sub inverter running off the input and secondary sub inverter running off the capacitor, when in this mode the output power would exceed the input power without the input power dropping to zero. Figure 4.8 shows the parts of the output cycle where this mode is used, indicated is the portion of each sub-inverter as they add to the output. As mentioned in the part detailing the mode 1, the total energy drawn from the capacitor during this mode over any given half-cycle must be equal to the energy stored over that same half-cycle. Figure 4.9 shows the configuration of the inverter when running in this mode along with the input current flow into both sub-inverters, grayed-out areas indicate

unused parts of the inverter. The relationship between the instantaneous input and output power when operating in this mode is given by equations 4.7, with the rate of change in capacitor voltage given by equations 4.8-4.9.

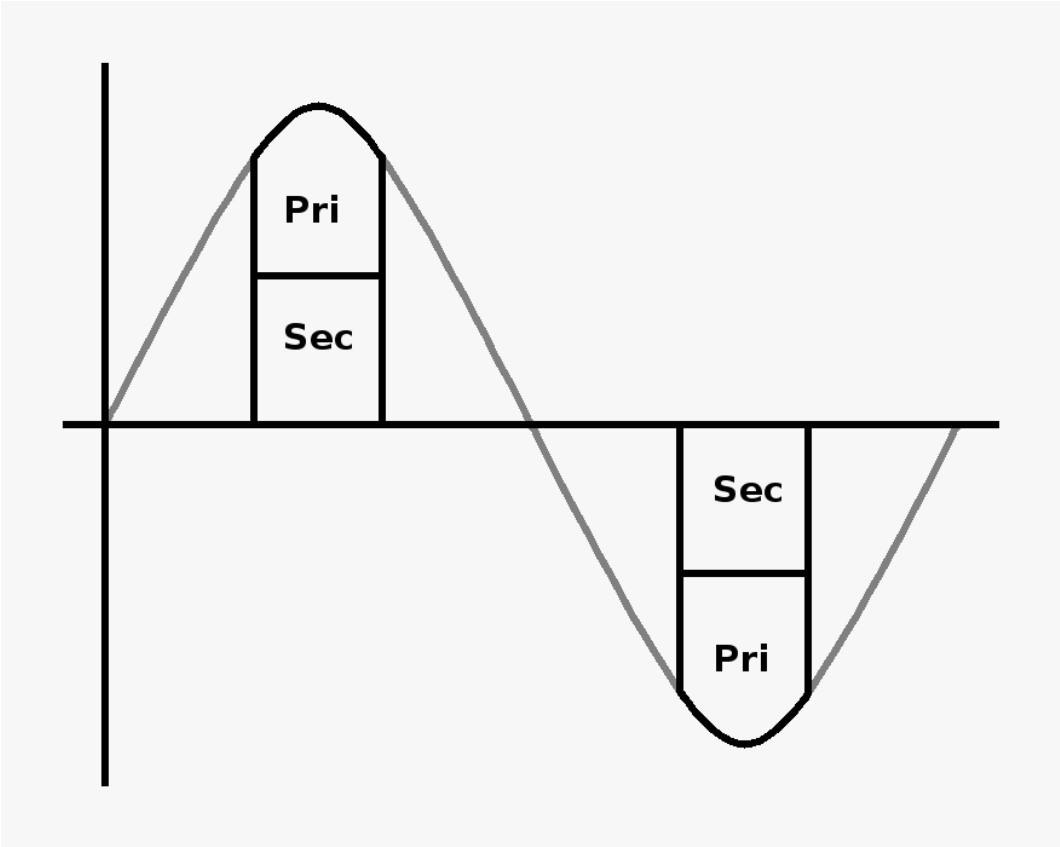

Figure 4.8: Periods of the output cycle where mode 3 is used, indicated is the ratio of the two sub-inverters and how they add to provide the total output.

$$p_{Input} = p_{Output} - p_{Secondary} \tag{4.7}$$

$$p_{Secondary} = -i_{Cap} \cdot v_{Cap} \tag{4.8}$$

$$\frac{-p_{Secondary}}{v_{Cap}} = C\left(\frac{dv_{Cap}}{dt}\right) \tag{4.9}$$

Where $p_{secondary}$ is the power output by the secondary sub-inverter.

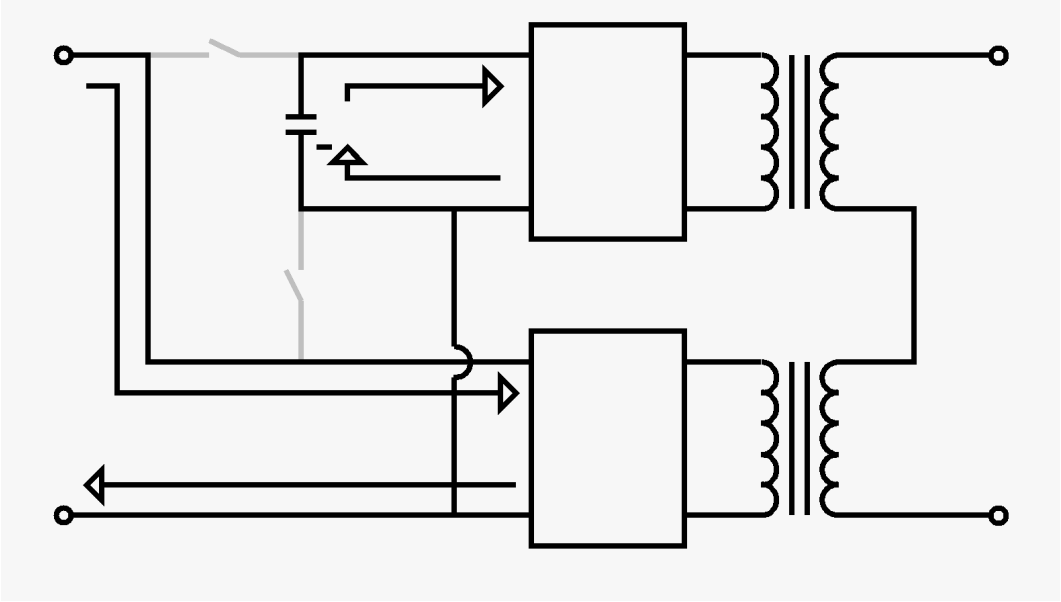

Figure 4.9: Switched supercapacitor assisted inverter during mode 3, arrows show input current flow through the two sub-inverters.

4.3 Ripple control, capacitor energy balance, and capacitor voltage conservation

The three modes could be used to actively control input ripple to the inverter, with mode 1 being used during periods of low output power in order to increase the input power, mode 2 used when the output power is near the average, and mode 3 when the output power is at its peak of the cycle in order to reduce the input power. In order to avoid situations where the inverter cannot output the required voltage without switching to a less desirable operating mode, the two sub-inverters would need to each be able to output more than half the maximum output voltage with an input voltage of half the inverter supply voltage. Furthermore the primary sub-inverter would also need to be able to operate on the full inverter supply voltage without issue.

As mentioned, it is important to maintain capacitor charge balance, in order to do this, over any given half cycle the total energy stored in the capacitor by the primary sub-inverter when operating in mode 1 must equal the energy drawn from it by the secondary sub-inverter during mode 3.

In order to demonstrate how charge balancing would work the case of a simple 50Hz 3-step modified sine wave will be examined, the waveform for this is shown in figure 4.10.

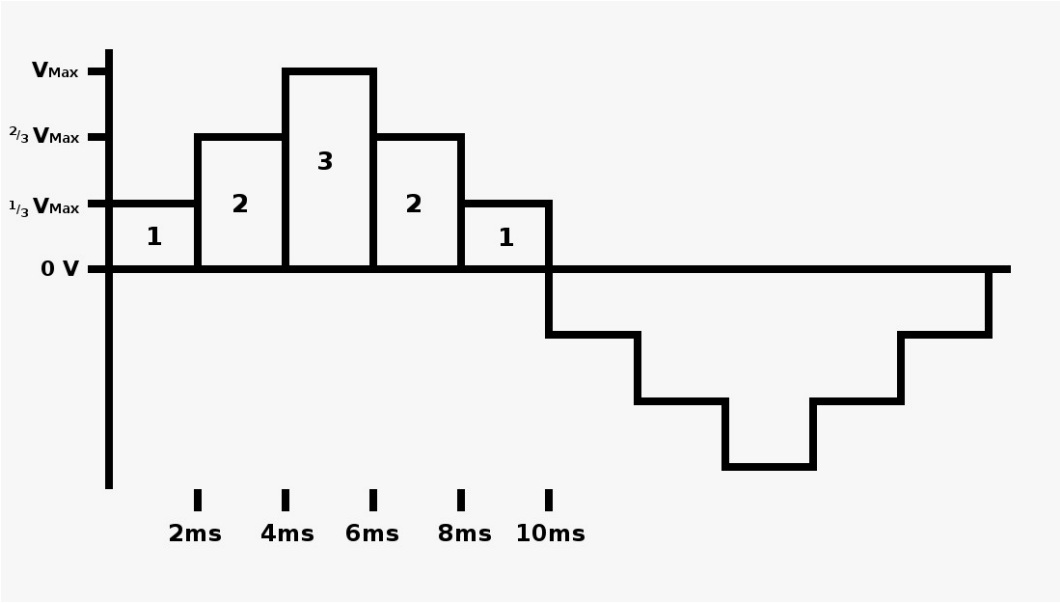

Figure 4.10: Simple 3-step modified sine wave.

If the capacitor is charged to half the operating voltage then the total energy stored in it over the half-cycle is equal to the energy output by the main sub-inverter when in mode 1, this given by equations 4.10-4.11.

$$E_{Store} = \int_{0}^{2} \frac{\left(\frac{1}{3}V_{Max}\right)^2}{R_{Load}} + \int_{8}^{10} \frac{\left(\frac{1}{3}V_{Max}\right)^2}{R_{Load}} \tag{4.10}$$

$$E_{Store} = 2 \cdot \frac{\left(\frac{1}{3}V_{Max}\right)^2}{R_{Load}} \cdot 2x10^{-3}s \tag{4.11}$$

Where R_{Load} is the load resistance.

A more general equation for the energy stored in the capacitor is given by equation 4.12.

$$E_{Store} = \int_{t0}^{t1} \frac{(v_{out}(t))^2}{R_{Load}} dt + \int_{t4}^{t5} \frac{(v_{out}(t))^2}{R_{Load}} dt \tag{4.12}$$

The change in capacitor voltage over each of these periods is given by equation 4.13-4.14.

$$E_{Store} = \frac{1}{2}C(v_{Cap}(t_2))^2 - \frac{1}{2}C(v_{Cap}(t_1))^2 \tag{4.13}$$

$$\frac{\left(\frac{1}{3}V_{Max}\right)^2 \cdot 4x10^{-3}s}{C \cdot R_{Load}} = (v_{Cap}(t_2))^2 - (v_{Cap}(t_1))^2 \tag{4.14}$$

Where $v_{Cap}(t_1)$ is the capacitor voltage at the start of the charging periods (0ms and 8ms), and $v_{Cap}(t_2)$ is the capacitor voltage at the end of the charging periods (2ms and 10ms).

The energy drawn from the capacitor over the half-cycle when operating in mode 3 is given by equations 4.15-4.16, where $V_{Primary}$ is the output voltage

of the primary inverter during this mode.

$$E_{Draw} = \int_{4}^{6} \frac{(V_{Max} - V_{Primary})^2}{R_{Load}} dt \tag{4.15}$$

$$E_{Draw} = \frac{(V_{Max} - V_{Primary})^2}{R_{Load}} \cdot 2\,x\,10^{-3}\,s \tag{4.16}$$

A general form of equation 4.15 is given by equation 4.17.

$$E_{Draw} = \int_{t2}^{t3} \frac{(v(t) - v_{Primary}(t))^2}{R_{Load}} dt \tag{4.17}$$

The change in capacitor voltage over this period is given by equation 4.18-4.19.

$$E_{Draw} = \frac{1}{2} C (v_{Cap}(t_1))^2 - \frac{1}{2} C (v_{Cap}(t_2))^2 \tag{4.18}$$

$$-\frac{(V_{Max} - V_{Primary})^2 \cdot 4\,x\,10^{-3}\,s}{C \cdot R_{Load}} = (v_{Cap}(t_2))^2 - (v_{Cap}(t_1))^2 \tag{4.19}$$

Where $v_{Cap}(t_1)$ is the capacitor voltage at the start of the discharging period (4ms), and $v_{Cap}(t_2)$ is the capacitor voltage at the end of the discharging period (6ms).

Since over any given cycle E_{Store} must be equal to E_{Draw}, this gives equations 4.20-4.21, with the general form shown in equation 4.22.

$$2 \cdot \frac{\left(\frac{1}{3} V_{Max}\right)^2}{R_{Load}} \cdot 2\,x\,10^{-3}\,s = \frac{(V_{Max} - V_{Primary})^2}{R_{Load}} \cdot 2\,x\,10^{-3}\,s \tag{4.20}$$

$$2\cdot\left(\frac{1}{3}V_{Max}\right)^2=\left(V_{Max}-V_{Primary}\right)^2 \tag{4.21}$$

$$\int_{t0}^{t1}\frac{v(t)^2}{R_{Load}}dt+\int_{t4}^{t5}\frac{v(t)^2}{R_{Load}}dt=\int_{t2}^{t3}\frac{\left(v(t)-v_{Primary}(t)\right)^2}{R_{Load}}dt \tag{4.22}$$

This means that the primary sub-inverter output operating voltage during mode 3 is given by equation 4.23.

$$V_{Primary}=\left(1-\frac{\sqrt{2}}{3}\right)V_{Max} \tag{4.23}$$

The change in capacitor voltage over a half-cycle must total to zero, this is represented by equations 4.24-4.26.

$$\begin{gathered}\left(\left(v_{Cap}(2ms)\right)^2-\left(v_{Cap}(0ms)\right)^2\right)+\left(\left(v_{Cap}(6ms)\right)^2-\left(v_{Cap}(4ms)\right)^2\right)\\+\left(\left(v_{Cap}(10ms)\right)^2-\left(v_{Cap}(8ms)\right)^2\right)=0\end{gathered} \tag{4.24}$$

$$\begin{gathered}\frac{\left(\frac{1}{3}V_{Max}\right)^2\cdot 4x10^{-3}s}{C\cdot R_{Load}}-\frac{\left(\frac{\sqrt{2}}{3}V_{Max}\right)^2\cdot 4x10^{-3}s}{C\cdot R_{Load}}\\+\frac{\left(\frac{1}{3}V_{Max}\right)^2\cdot 4x10^{-3}s}{C\cdot R_{Load}}=0\end{gathered} \tag{4.25}$$

$$2\cdot\left(\frac{1}{3}V_{Max}\right)^2-\left(\frac{\sqrt{2}}{3}V_{Max}\right)^2=0 \tag{4.26}$$

The above equations demonstrate that under the correct configuration both the total energy stored and drawn from the capacitor over a single cycle is equal and the total change in voltage is zero. Since the voltage across the capacitor is proportional to the charge stored by that capacitor this means that the change in charge over any given cycle is also zero.

Note that for simplification purposes the change in capacitor voltage due to charging is assumed to be negligible compared to the input voltage. This means the effect of capacitor voltage change during charging and discharging when calculating energy stored and drawn from the capacitor during modes 1 and 3 is ignored. Due to the large capacitances of supercapacitors (>1F for even small supercapacitors) and the small time periods (~2ms) this assumption isn't far from what would actually occur in such a device. The equations also assume that all components are ideal, including the capacitor.

Using equations 4.3, 4.6, 4.7, and 4.15, the power draw during the three modes can be calculated, they are given by equations 4.27-4.32.

Mode 1:

$$p_{Input} = \frac{\left(\frac{1}{3}V_{Max}\right)^2}{R_{Load}} \cdot \frac{V_{Input}}{\left(V_{Input} - \frac{1}{2}V_{Input}\right)} \tag{4.27}$$

$$p_{Input} = \frac{2}{9} \cdot \frac{V_{Max}^2}{R_{Load}} \tag{4.28}$$

Mode 2:

$$p_{Input} = \frac{\left(\frac{2}{3}V_{Max}\right)^2}{R_{Load}} \tag{4.29}$$

$$p_{Input} = \frac{4}{9}\frac{V_{Max}^2}{R_{Load}} \tag{4.30}$$

Mode 3:

$$p_{Input} = \frac{V_{Max}^{\ 2}}{R_{Load}} - \frac{\left(1-\left(1-\frac{\sqrt{2}}{3}\right)V_{Max}\right)^{2}}{R_{Load}} \tag{4.31}$$

$$p_{Input} = \frac{\left(\left(1-\frac{\sqrt{2}}{3}\right)V_{Max}\right)^{2}}{R_{Load}} \tag{4.32}$$

Compare this to a conventional inverter ($p_{Input} = p_{Output}$) outputting the same modified sine wave, equations 4.33-4.35 represent the power draw inverter over these same periods.

Mode 1:

$$p_{Input} = \frac{1}{9} \cdot \frac{V_{Max}^{\ 2}}{R_{Load}} \tag{4.33}$$

This is less than the switched supercapacitor inverter, this shows that the topology is capable of increasing the power draw during low output periods.

Mode 2:

$$p_{Input} = \frac{2}{9} \cdot \frac{V_{Max}^{\ 2}}{R_{Load}} \tag{4.34}$$

This is the same as the switched supercapacitor inverter, which is expected since during this mode the inverter is acting as a conventional

inverter.

Mode 3:

$$p_{Input} = \frac{V_{Max}^{\ 2}}{R_{Load}} \tag{4.35}$$

This is far higher than the switched supercapacitor inverter, this shows that the topology is capable of reducing the input power during periods of high power output.

Comparing the power draws with the modified sine wave in the case of the switched supercapacitor inverter with the ideal inverter, the supercapacitor topology is capable of manipulating its input power to control its input ripple. This shows that the topology is capable of performing the required task.

Chapter 5

5.1 The proof of concept inverter

In order to test if the concept of switching a supercapacitor between being in series with a main inverter for charging and in parallel with a secondary inverter for discharging would reduce the input ripple, a simple proof of concept device was designed and made. To simplify the device the inverters were made in half-bridge configuration, this allowed a single microcontroller to operate both inverters which avoided unnecessary complexity.

As some of the MOSFETs which switch the capacitor bank never have their drain go to ground conventional bootstrap drivers couldn't be used without added complexity, instead photocouplers (opto-isolators with a photodiode array instead of a phototransistor for the output) were used to drive the gates. The photocouplers generate a voltage on their output and allow the microcontroller to turn on and off each gate individually by simply driving the LED in the device. The loads for the individual inverters were separate bulb loads in order to avoid any issues with connecting the outputs of the two inverters. The disadvantage of using optocouplers to drive the MOSFETs is the poor on/off time, the cause of this is due to not only the optocouplers having a relatively low maximum current output but they have no way to discharge the MOSFET when it needs to turn off. Because the optocoupler can not turn off the MOSFET once it is turned on

a resistor is required between the gate and source to perform this task, ideally a small resistor would be used to lower turn off time but as the equivalent circuit is a parallel RC circuit being driven by a constant current source this will increase the time required to charge the gate capacitor. The circuit diagram for the proof of concept inverter is shown in figure 5.2 with the manufactured design shown in figure 5.1.

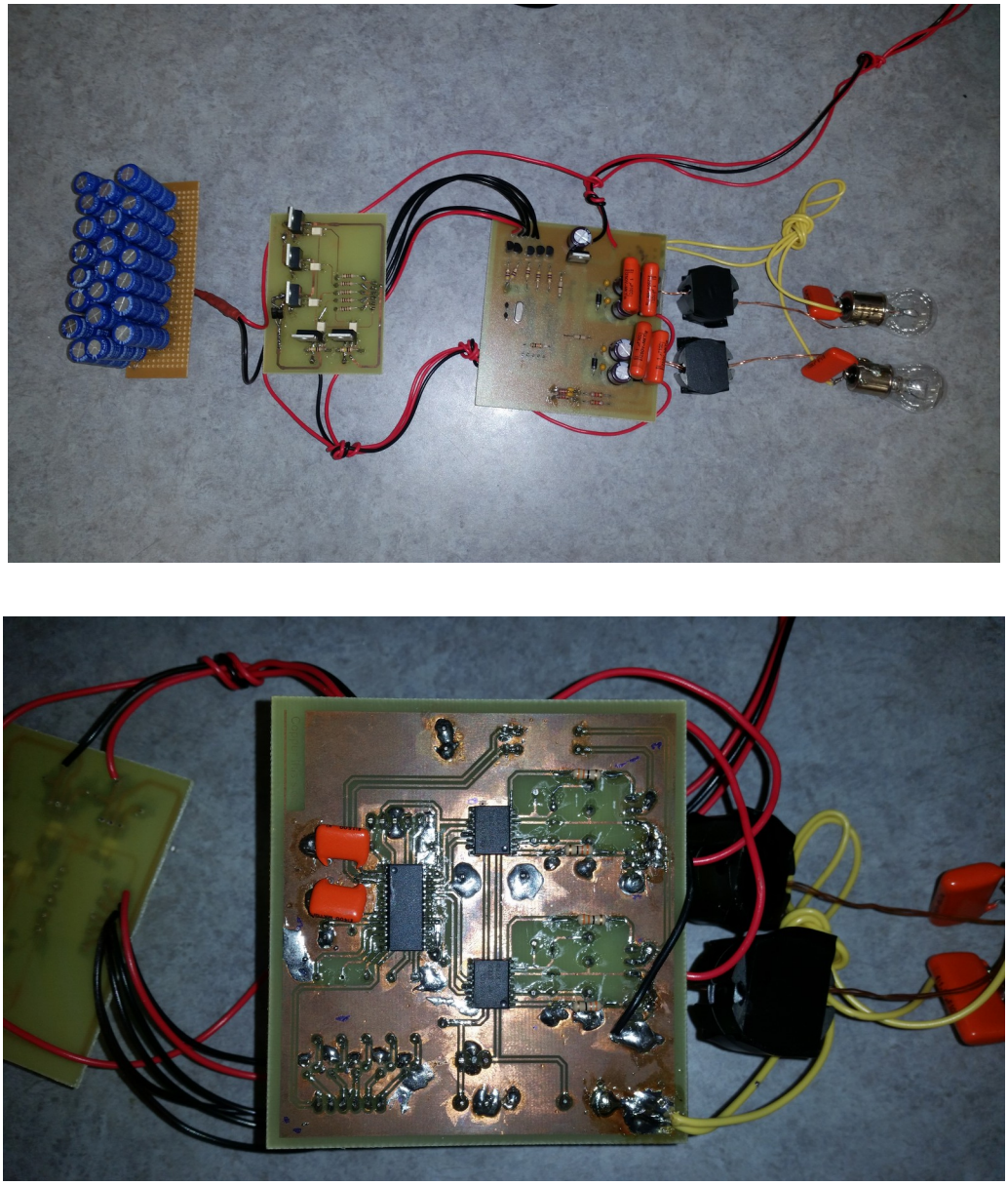

Figure 5.1: Completed proof of concept inverter, top is the overall inverter and bottom is the underside of the main board showing the microcontroller and MOSFET drivers.

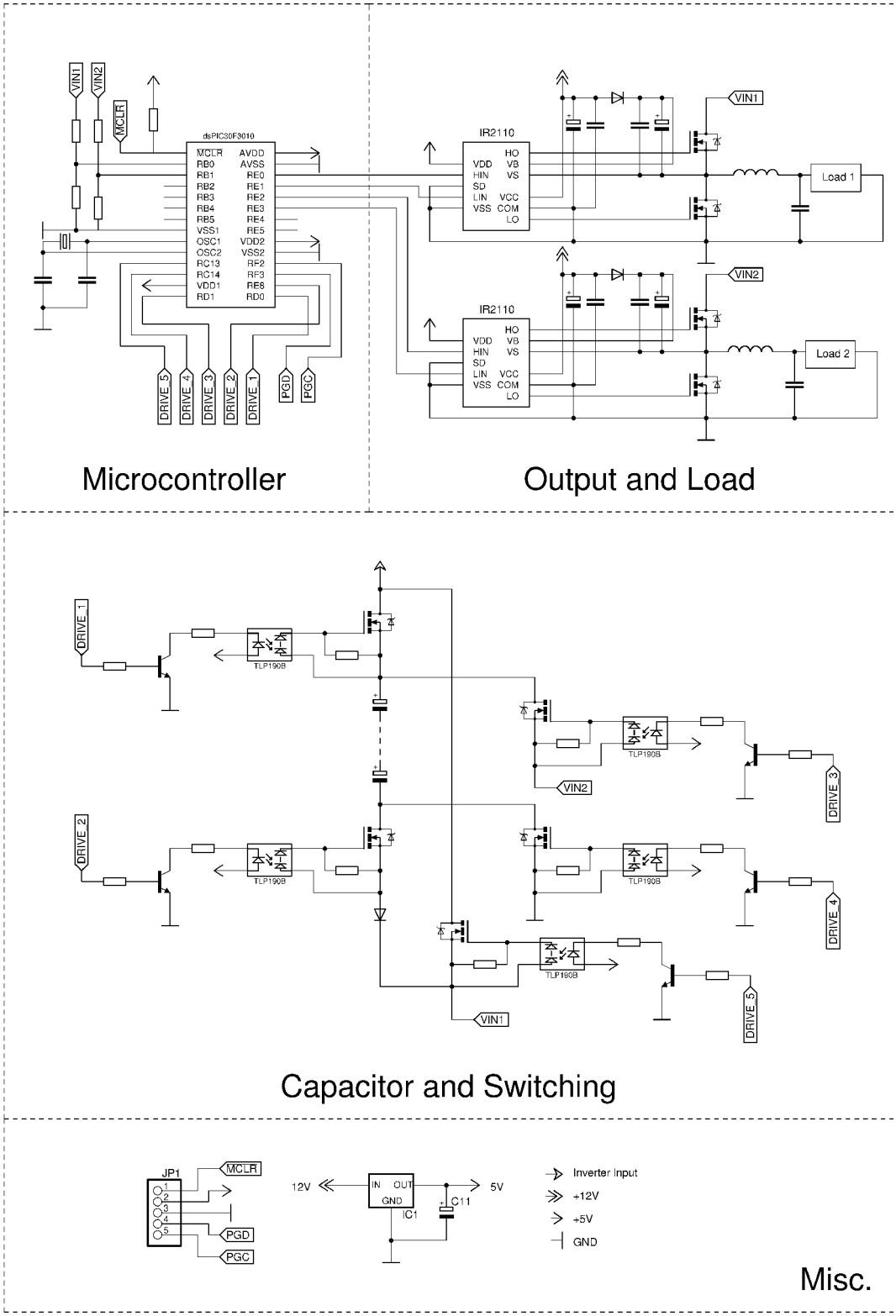

Figure 5.2: Switched supercapacitor assisted inverter proof of concept circuit diagram.

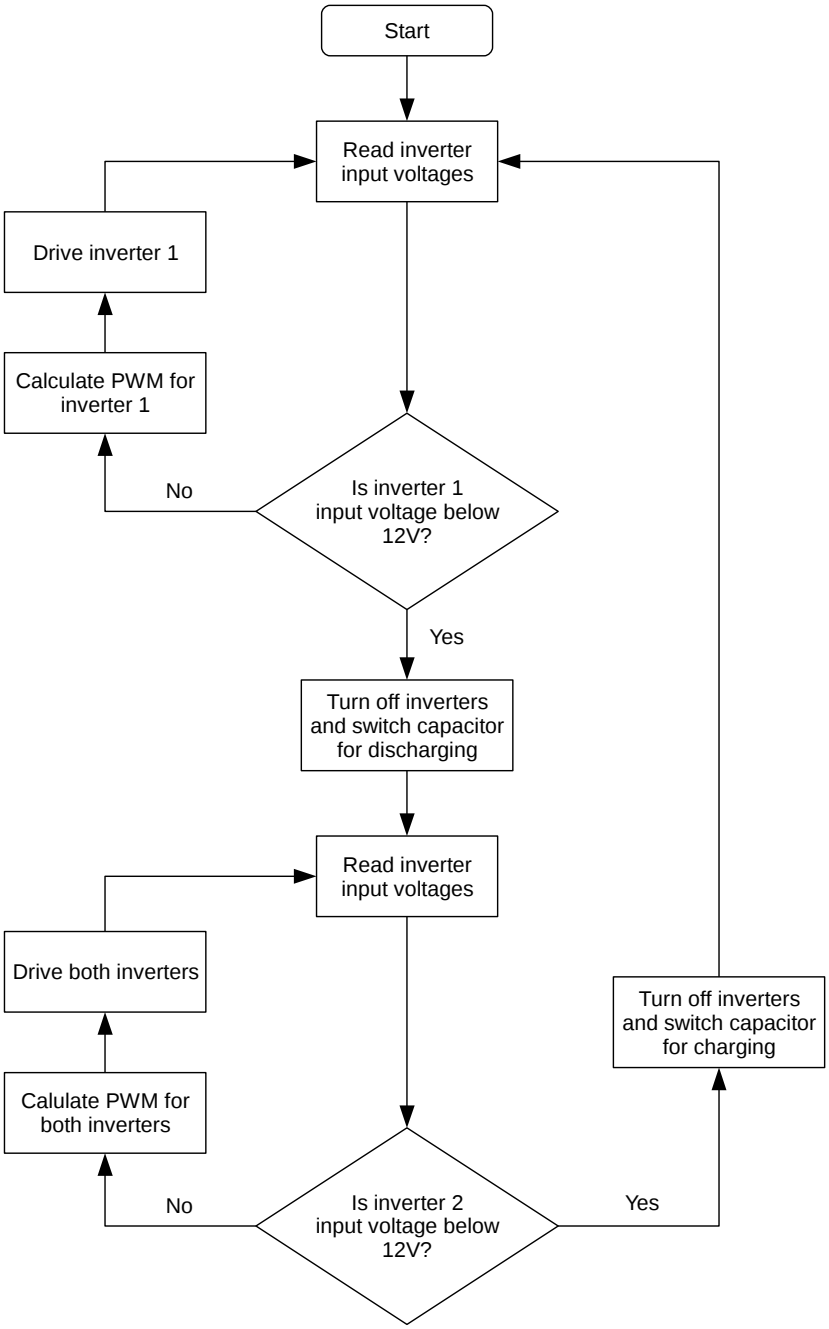

Figure 5.3: Proof of concept inverter microcontroller code flowchart.

The flowchart for the microcontroller code is shown in figure 5.3,in simple terms it alternates between the states 1 and 3 listed in section 4.2. Rather than attempting to output a sine wave like waveform each inverter attempts to output a constant voltage when it is running, in this sense the combined voltage (and therefore power) doubles when the supercapacitor is switched and the secondary inverter is running.

5.2 Concept evaluation

The test setup for the proof of concept inverter is shown in figure 5.4, the input current probe is a hall-effect type and the two output voltages are added together to show the total output. Since the input voltage is constant the measured input current represents the power input, the controller and drive circuitry input voltage is 12V and the inverter voltage is 30V. For measurement purposes a simple LC filter was placed on the input to remove the switching frequency input ripple.

When the inverter was first powered on there was an initial period where only the main inverter ran while the supercapacitor bank charged to the operating voltage before the device started switching between the two operating modes. The frequency of this switching was approximately 1Hz. The waveforms captured by the oscilloscope are shown in figure 5.5.

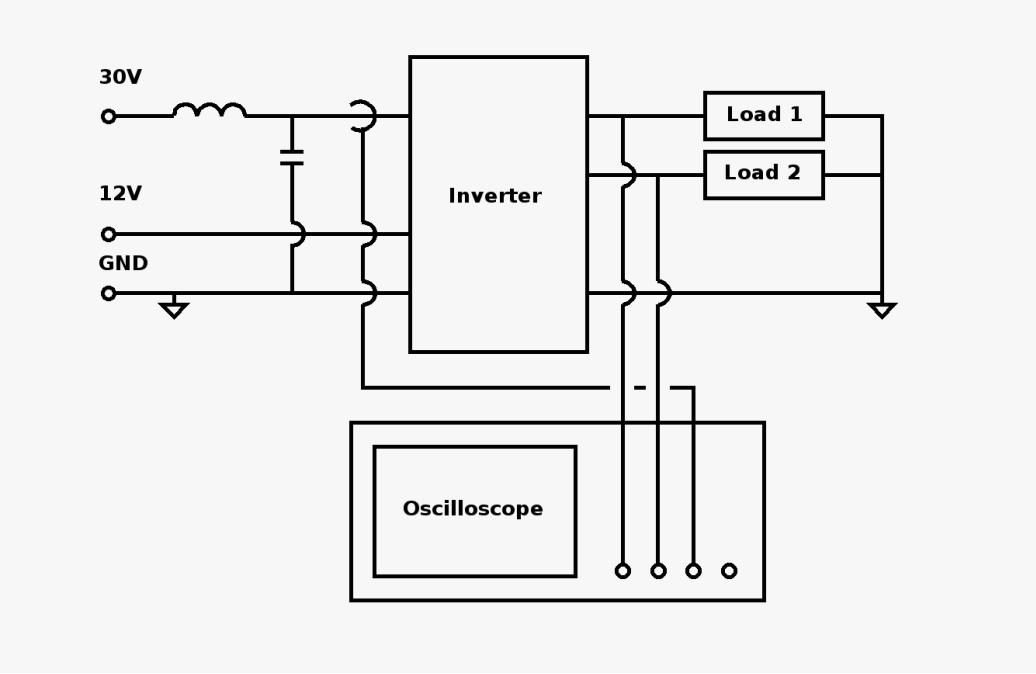

Figure 5.4: Test setup for the proof of concept inverter.

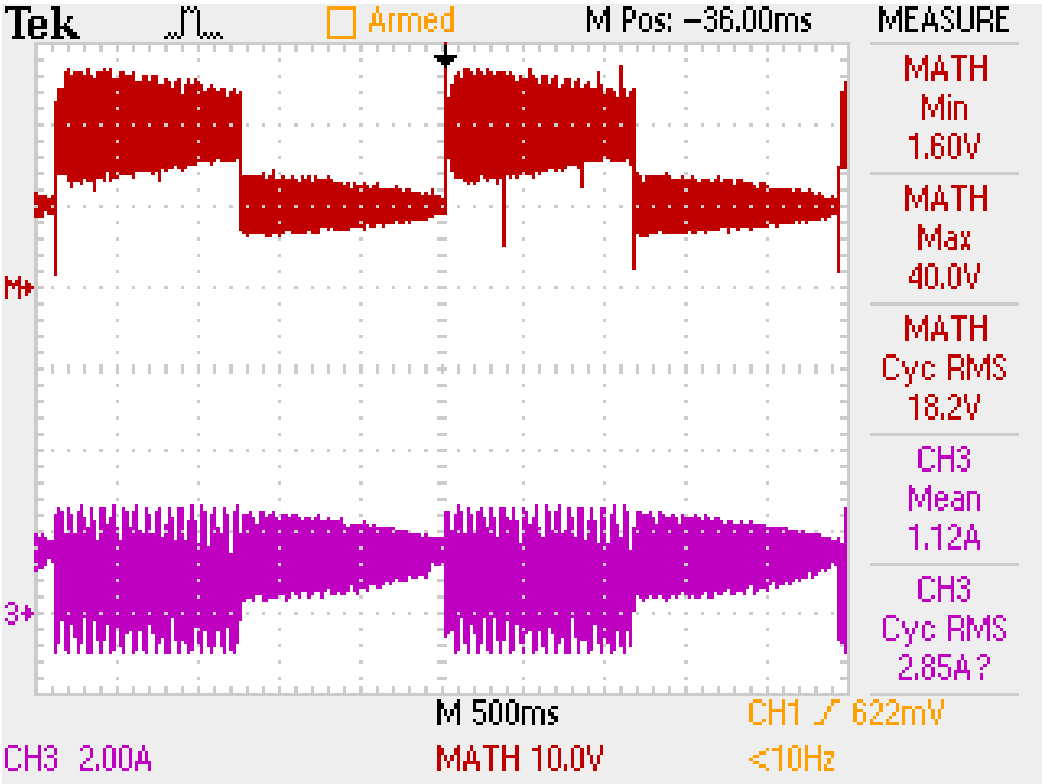

Figure 5.5 Operating waveforms of the proof of concept inverter, shown is the sum of the output voltages of the two sub inverters (top trace) and the inverter input current (bottom trace).

As the waveforms show, not only does the concept work at its intended role of reducing the input ripple but the inverter actually draws less power when both inverters are running, in other words when the output power doubles there is a decrease in the input power. This makes sense as when the capacitor is being charged the main sub-inverter must draw approximately twice the current in order to output the same power and when it is running directly from the input the higher voltage results in lower current draw for the same power. In theory the main sub-inverter could be programmed to output twice the power during the period when the secondary sub inverter was running, this would result in the power output tripling with minimal change in input current during the discharge period.

Based on the results obtained from this proof of concept inverter the basic idea of charging a capacitor in series with an inverter in order to increase the current draw during periods of low power output, then discharging it in parallel with a secondary inverter to boost the output during periods of high power output to actively alter the input current waveform works.

5.3 Development of a full bridge AC inverter

The proof of concept inverter developed isn't so much an inverter but more like a two DC-DC converters in that it could only output a a voltage in one direction separately from its two switching circuits. The next step is to develop a fullbridge inverter in order to output an AC waveform and couple the two sub-inverters together for a single output.

In order to output an AC waveform the output circuitry was converted to a full bridge configuration, this was done by taking the existing half bridge output and filter design and duplicating it on the other side of the load, the circuit diagram for this is shown in figure 5.6. As the dsPIC used as the controller does not have enough outputs to control all 8 switches in the 2 full-bridges, an FPGA was programmed to act as a logic circuit to take the 4 complementary PWM outputs from the dsPIC as well as a 'direction' signal and convert it to the 8 drive signals to be used by the MOSFET drivers. The truth tables for the FPGA are shown in figure 5.7.

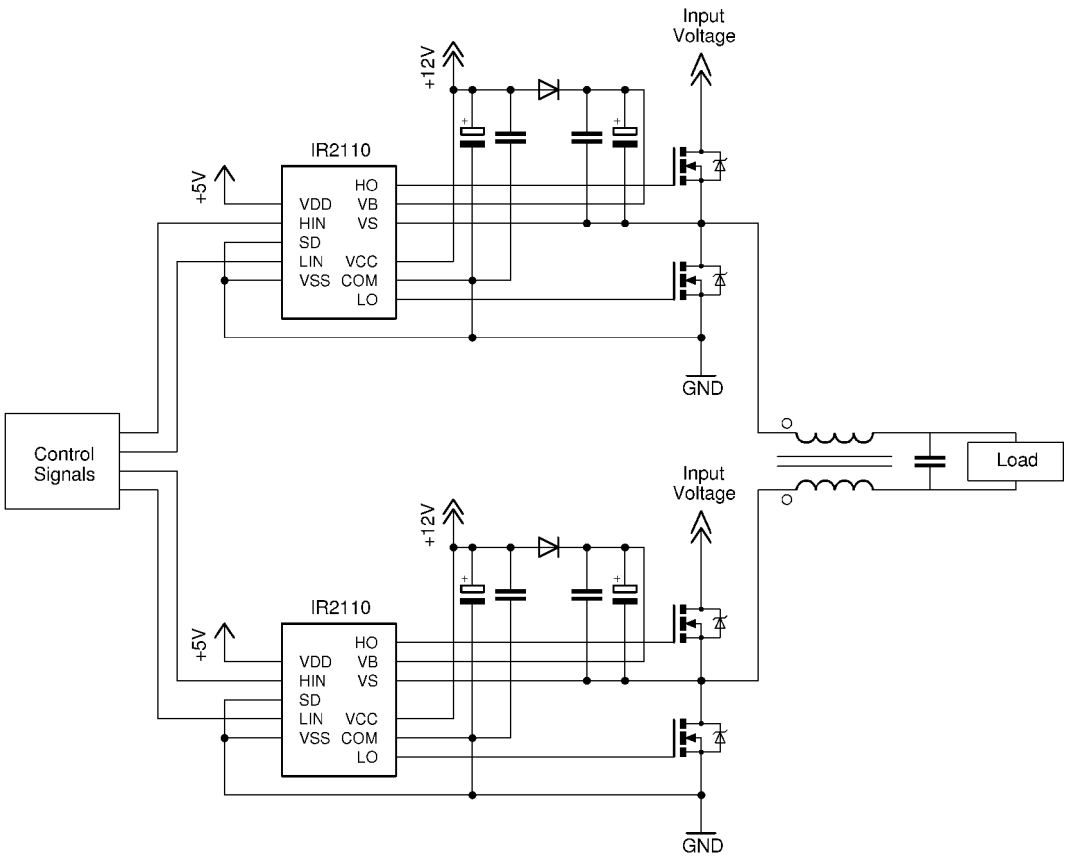

Figure 5.6: Fullbridge output driver and output filter, made by taking two half bridge drivers and combining the outputs.

Side	Lo Hi	LL	LH	RL	RH
0	1 0	1	0	1	0
	0 1	1	0	0	1
1	1 0	1	0	1	0
	0 1	0	1	1	0

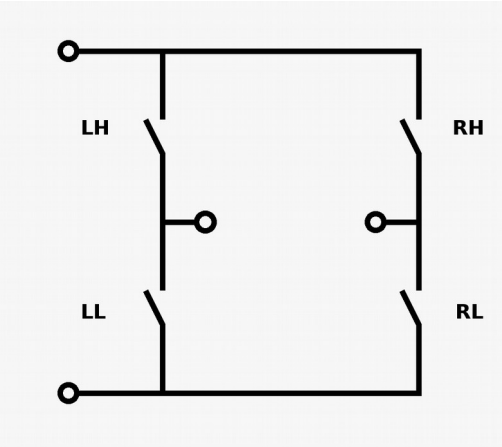

Figure 5.7: FPGA truth table. Side, Lo, and Hi are input signals. LL, LH,RL, and RH are MOSFET drive signals associated with a particular switch on the fullbridge.

By using an FPGA to generate the additional control signals the complication of using separate microcontrollers to drive the two full-bridges is avoided as they would need to communicate between them in order to synchronize their outputs.

The supercapacitor switching circuit was also simplified, removing three switches and replacing them with two diodes in order to simplify the drive circuitry. Furthermore additional optocouplers were added to the two remaining MOSFETS to improve their on/off switching time, this is important when moving from the sub 1Hz switching frequency to 50Hz as switching time will ultimately limit how much the inverters can be operating over a given cycle. The simplified capacitor switching circuit is shown in figure 5.8.

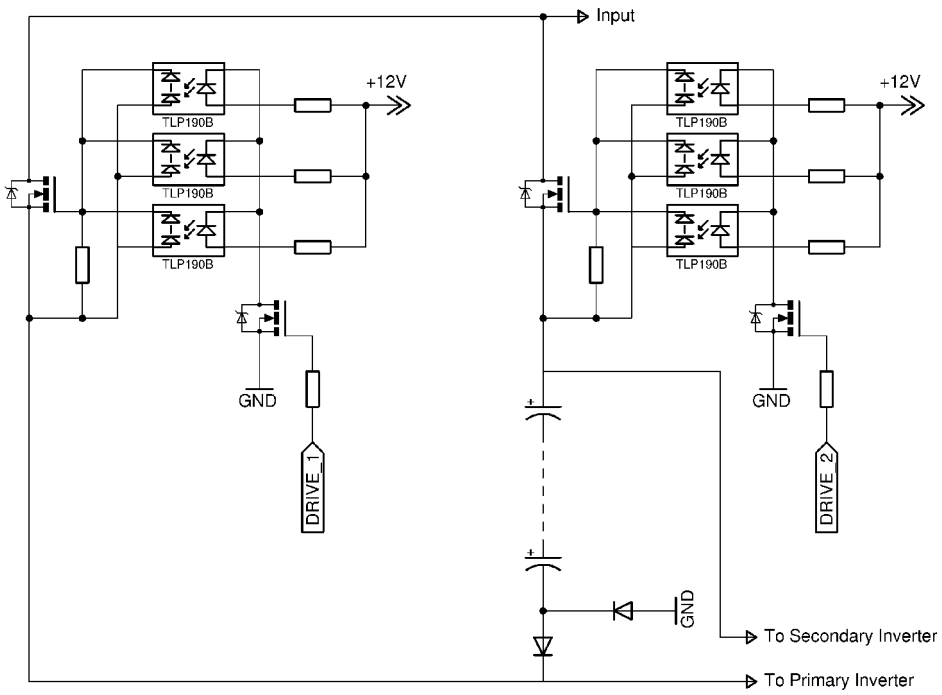

Figure 5.8: Simplified capacitor switching circuit.

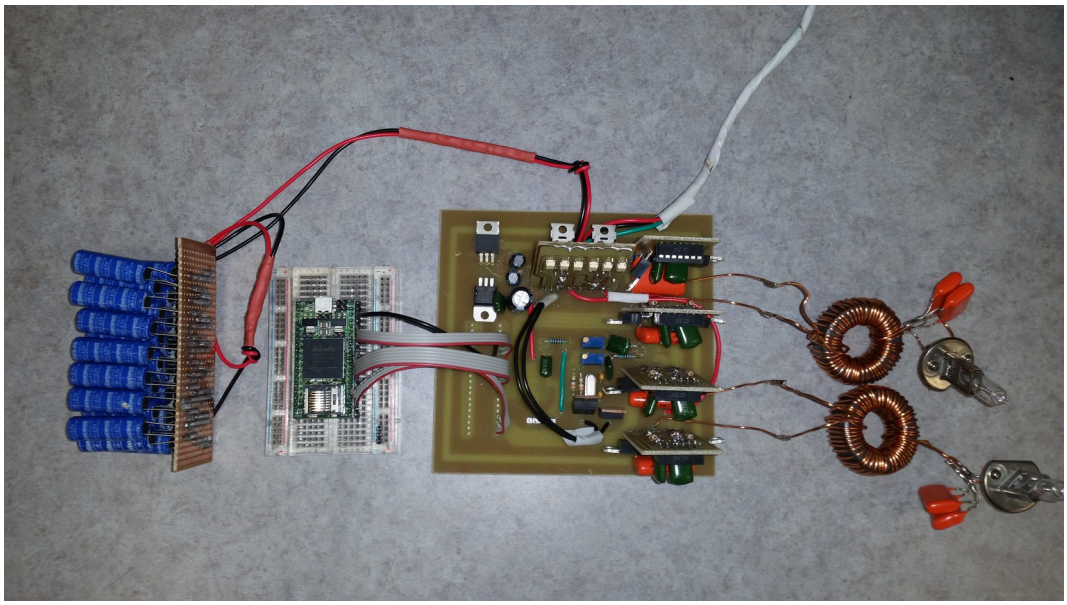

Figure 5.9: Switched capacitor fullbridge AC inverter.

As with the proof of concept inverter the full bridge design was built and is shown in figure 5.9, the loads used for this design are 40W automotive headlight bulbs. To reflect the circuit changes and desire for an AC waveform the microcontroller code was updated, shown in figure 5.5 is the flowchart for the new microcontroller code. Aside from the update to produce an AC waveform the main difference is that instead of monitoring the the inverter input voltages to determine when to switch it now is delay based to produce an output waveform with a frequency close to 50Hz. A minor change done to the code was to make primary sub-inverter double its output when the capacitor is being discharged, this results in the output tripling when both inverters are on and the input current being near constant.

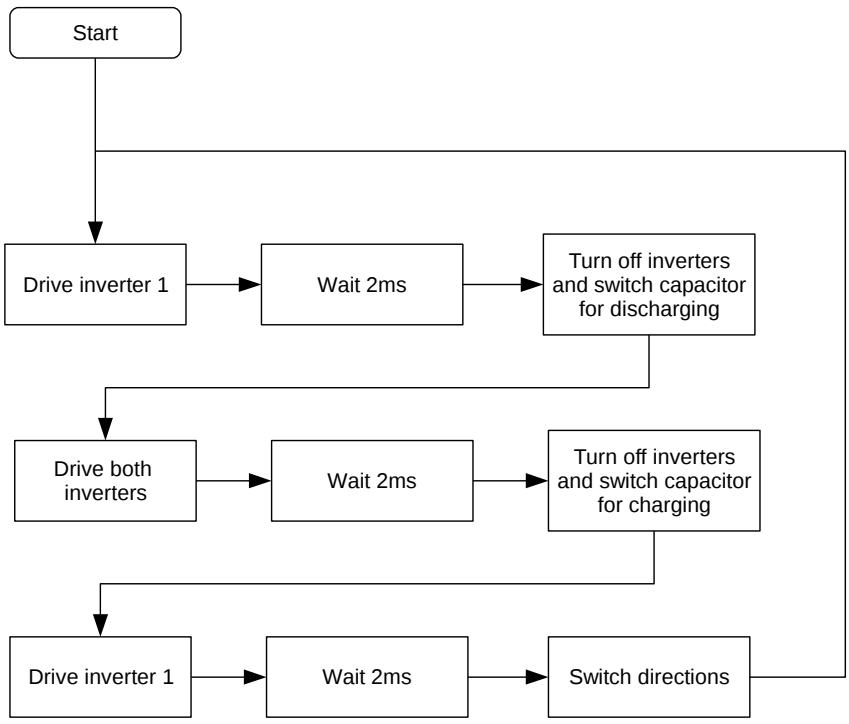

Figure 5.10: Switched capacitor fullbridge inverter microcontroller code flowchart.

The fullbridge design was tested in the same way as the proof of concept inverter, however as the outputs are now AC rather than DC the voltage is taken across the load rather than with respect to ground. As the oscilloscope used has isolated inputs this does not produce grounding issues.

The operating waveforms of the inverter are shown in figure 5.11, as before the input voltage is 30V and the two AC outputs are summed on the oscilloscope to give the total output. As this shows the inverter is capable of not only outputting an AC waveform as required but the changes made to the code result in the input current having minimal ripple.

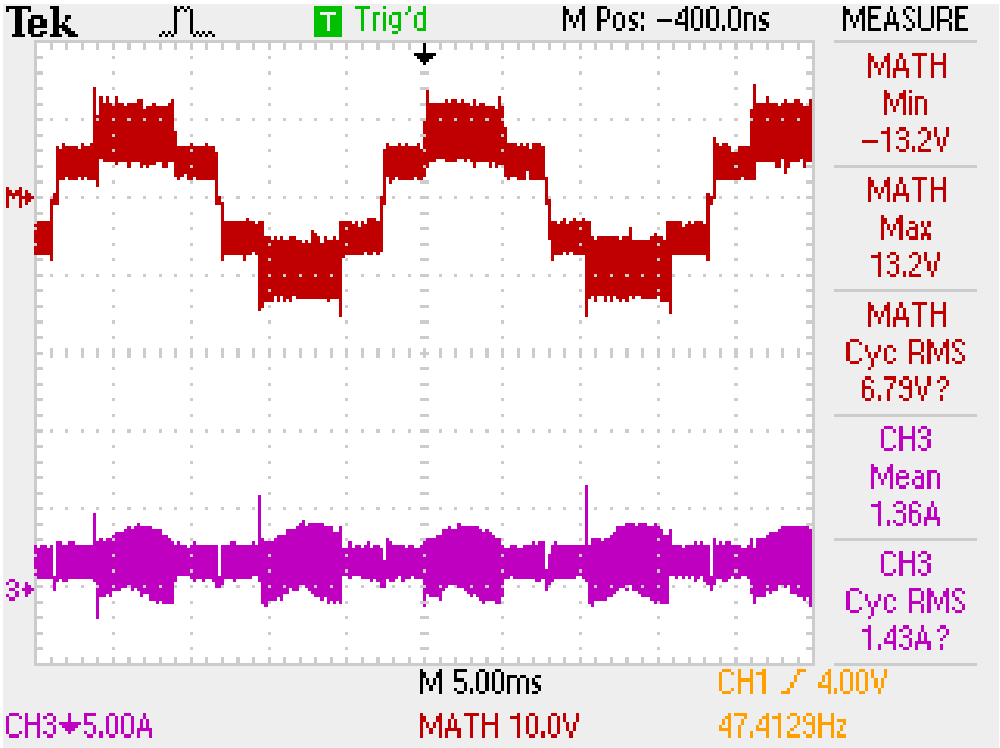

Figure 5.11: Switched capacitor fullbridge inverter operating waveforms.

5.4 Coupling the outputs

Separate sub-inverter outputs are not particularly useful for the final inverter, what is needed is to couple the two outputs so that instead of outputting power to two separate loads it can power one (that load ideally being the mains grid).

As the two sub-inverters operate with their negative input with respect to ground it should be possible to couple the two outputs via a choke setup, the idea being to try and use the core magnetic flux to prevent current from flowing out of the inverter with the higher input voltage and into the other rather than going into the load. The circuit designed to couple the two sub-inverter outputs is shown in figure 5.12.

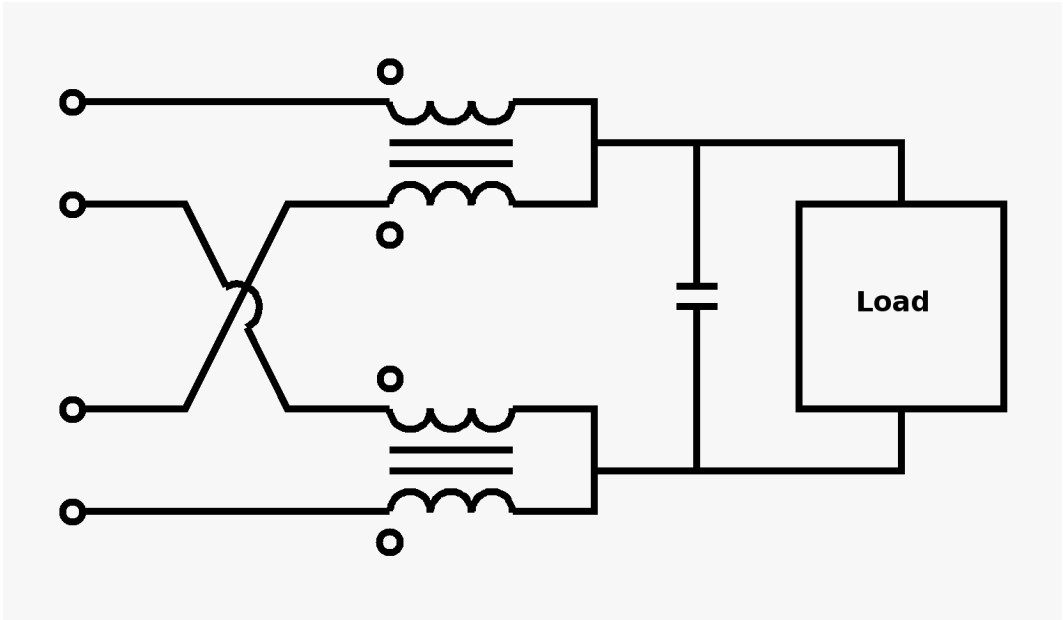

Figure 5.12: Sub-inverter coupling circuit.

By using choke based circuit, rather than the more obvious transformer with multiple windings, allows the device to physically far smaller as instead of energy being transferred through the magnetic core it is instead being used to block current from flowing in the opposite direction. Figure 5.13 shows the switched capacitor inverter with the choke coupling circuit, the load is the same two 40W globes from previously but are now combined in parallel.

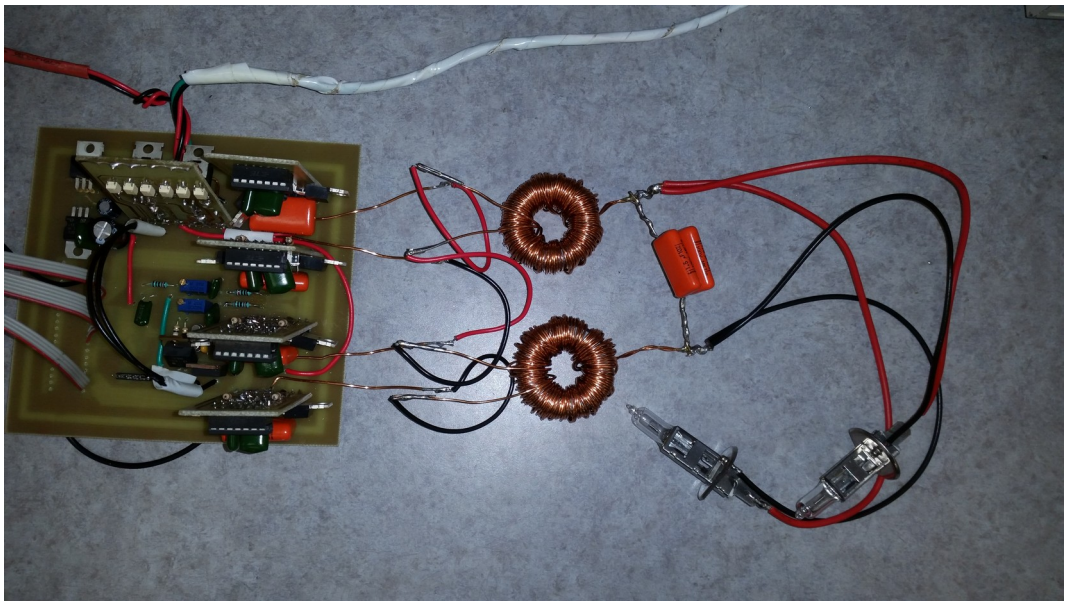

Figure 5.13: Switched capacitor fullbridge inverter with the choke based output coupling circuit.

The inverter was tested in the same way as before except instead of the single output is shown rather than the sum of the two sub-inverters, the operating waveforms are shown in figure 5.14.

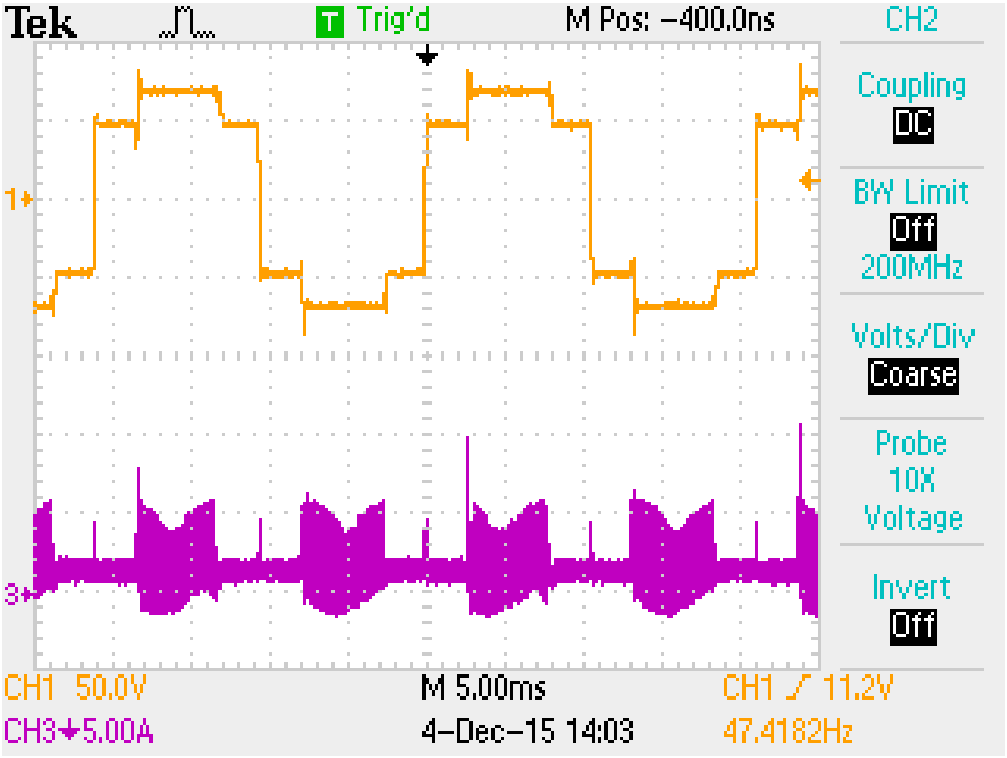

Figure 5.14: Switched capacitor fullbridge inverter with choke coupling circuit operating waveforms.

Based on the results above the choke based coupling circuit is incapable of preventing current from flowing back into the sub-inverter with the lower input voltage. What is occurring is when the secondary sub-inverter is turned on the primary sub-inverter is powered by the full input voltage which is far higher than the voltage the capacitor is charged to, this causes a significant amount of the current output from the primary to flow back into the secondary and charge the capacitor. In the inverters current configuration this would occur even if the secondary sub-inverter was turned off as the current would flow though the body diodes in the MOSFET switches.

In order to solve this problem the choke based coupling circuit was replaced with a toroidal power transformer made for 230V with two output windings. The sub-inverters were connected to these secondary windings separately and is shown in figure 5.15, note the physical size of the transformer relative to the previous choke based setup, the load for this is a 100W 230V incandescent bulb due to the transformer stepping up the voltage.

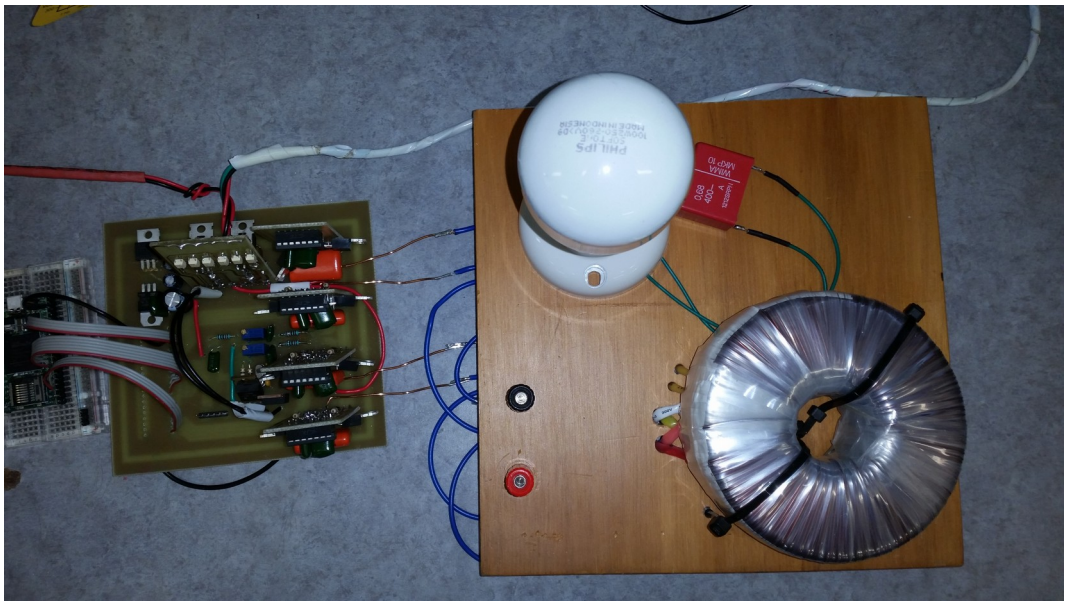

Figure 5.15: Switched capacitor inverter with transformer based output coupler.

The circuit was tested in the same way as before with the operating waveforms are shown in figure 5.16, as it shows the transformer coupling has eliminated the current flow back into the secondary sub-inverter. However there is an issue with the efficiency of the overall circuit, the uncoupled version had acceptable efficiency which indicates the issue is caused by the transformer being used outside its intended application.

With the 56.8Vrms output voltage the 100W bulb provides a load of approximately 25W, with the 30V input voltage and an input current of 1.34A this gives an input power of 40W, giving an efficiency of 63%.

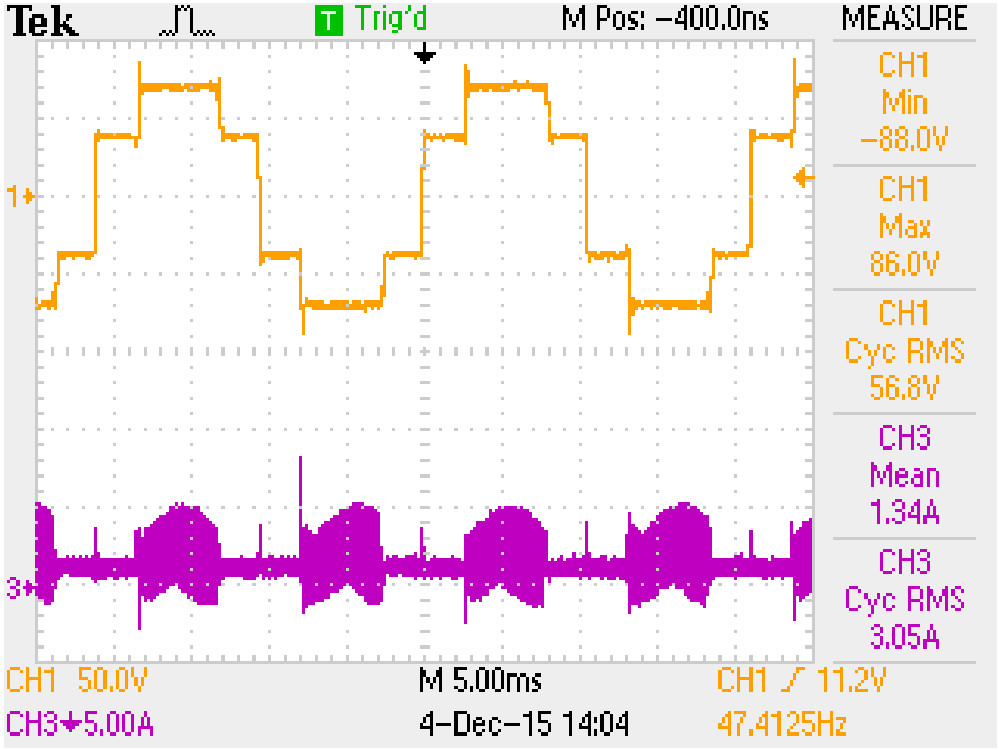

Figure 5.16: Switched capacitor fullbridge inverter with transformer coupling operating waveforms.

While the use of a more conventional transformer arrangement (one with multiple windings so that the two sub-inverters can 'add' their outputs) solved the issue of coupling the sub-inverters the next logical step is to modify the design to produce a pure sine wave output rather than a two step modified sine wave. However there is a less obvious but fundamental issue with the switched capacitor bank topology which has only just been realized by the thought of moving away from an output waveform with two

or more discrete voltages to a range of voltages which is required for a pure sine wave output.

5.5 Issues with a switched capacitor

As noted in the previous section there are fundamental issues with the hard switching of the capacitor bank between charging and discharging when moving from a the current output waveform to a pure sine wave.

This issue is the fact that the switched capacitor topology only allows for three discrete operating modes as discussed in chapter 4 section 2, these modes allow the inverter to manipulate its input power to three distinct levels with respect to its output power (assuming ideal efficiency). The relationships between input and output power between the three modes are shown in equations 5.1-5.3.

Mode 1 – Primary sub-inverter charging capacitor.

$$p_{Input} = p_{Output} \cdot \frac{V_{Input}}{(V_{Input} - v_{Cap})} \tag{5.1}$$

Mode 2 – Primary sub-inverter running directly from inverter input.

$$p_{Input} = p_{Output} \tag{5.2}$$

Mode 3 – Primary sub-inverter running directly from inverter input and secondary sub-inverter discharging capacitor.

$$p_{Input} = p_{Output} - p_{Secondary} \tag{5.3}$$

While mode 3 is capable of manipulating the input power over a wide range compared to the other two modes it can only be used for brief periods of the output cycle in order to maintain capacitor charge balance.

The reason this is an issue is that when moving to an output waveform that doesn't have several discrete voltage levels the need for the inverter to manipulate the input current over a range becomes important. This is because unlike the modified sine wave in a pure sine wave does not have large periods of the output cycle where the output power is static, instead it varies. If the current inverter was to be used this variation in output power would be seen on the input when operating in modes 1 and 2.

For the purposes of input ripple control it is advantageous to develop a topology which is capable of operating over a range rather than in three distinct modes.

Chapter 6

6.1 The switchless topology

While not immediately obvious, the solution to the issue discussed at the end of chapter 5 of the inverter only being able to operate in three fixed modes is to remove the capacitor switching. However this is not possible with the circuit in its current configuration as the capacitor negative terminal must be switched to ground where the negative input for the secondary sub-inverter is for discharge but obviously must be at the positive input for the primary sub-inverter for charging. Furthermore the positive input to the primary sub-inverter must be connected to the input during capacitor discharge for it to be able to operate, which is essential as the input power would drop to zero during this time otherwise.

The two problems associated with the removal of the capacitor switching stem from the same assumption, that the negative input of secondary sub-inverter must be at ground. While this is true in the previous two inverters due to the fact that both sub-inverters ran from a single controller and all the control signals needing to be with respect to ground, if each sub-inverter has its own controller then the signals would be with respect to the negative input of that sub-inverter.

With the negative input of the two sub-inverters no longer needing to be at ground they are now able to be placed anywhere in the circuit as

functional blocks, making the issue of removing the capacitor switching possible to solve. The so called 'switchless' inverter topology is shown in figure 6.1, here the two inverters are in series with each other with the capacitor placed in parallel with the secondary sub-inverter and in series with the primary.

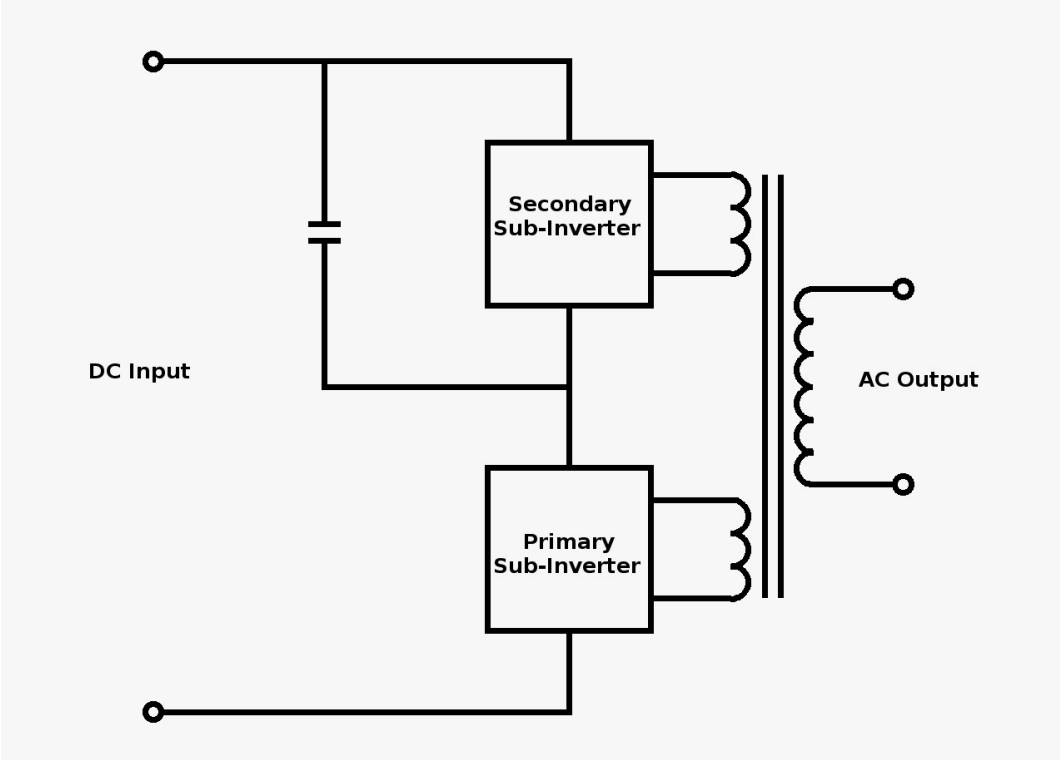

Figure 6.1: The switchless supercapacitor assisted inverter topology.

In this circuit the rate of capacitor charging or discharging is set by the ratio of the current draw of the two sub-inverters. Should the primary consume more current than the secondary the difference will be drawn through the capacitor, charging it, and should the secondary consume more than the primary then the difference will be drawn from the capacitor, discharging it. If the current draw of the two sub-inverters are the same

then the capacitor will neither charge or discharge. Figure 6.2 shows the current flow though the inverter under these different operating conditions, with equation 6.1 giving the rate of change in capacitor voltage.

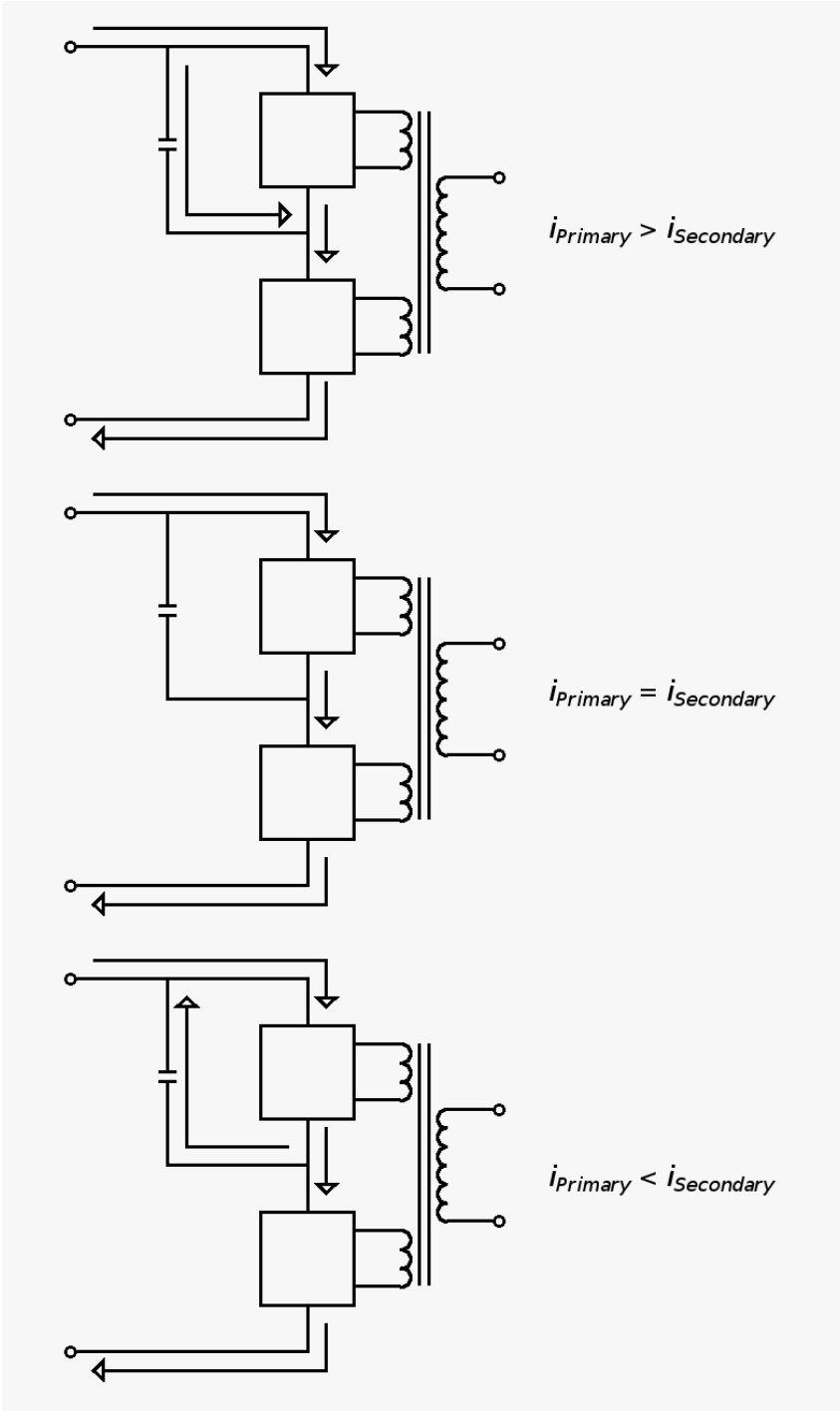

Figure 6.2: Current flow through the switchless inverter during the possible operating conditions.

$$\frac{dv_{Cap}}{dt} = \frac{i_{Primary} - i_{Secondary}}{C} \quad (6.1)$$

Where $i_{Primary}$ and $i_{Secondary}$ are the instantaneous primary and secondary sub-inverter current draws respectively.

What is special about this topology is that the current draw of the two sub-inverters can be varied over a wide range, allowing the inverter to manipulate its instantaneous power draw over a range with respect to the output power rather than the three fixed values of the previous switched topology. Equation 6.2 gives the range over which the switchless inverter can manipulate its input power with respect to its output power and equations 6.3-6.5 give the power input with respect to power output and the sub-inverter currents.

$$0 \leqslant p_{Input} \leqslant p_{Output} \frac{V_{Input}}{V_{Input} - v_{Cap}} \quad (6.2)$$

$$p_{Input} = V_{Input} \cdot i_{Main} \quad (6.3)$$

$$p_{Output} = (V_{Input} - v_{Cap}) \cdot i_{Main} + v_{Cap} \cdot i_{Secondary} \quad (6.4)$$

$$p_{Input} = p_{Output} + V_{Cap}(i_{Main} - i_{Secondary}) \quad (6.5)$$

The rate of change in capacitor voltage with respect to the input and output power is given by equation 6.6.

$$\frac{dv_{Cap}}{dt} = \frac{p_{Input} - p_{Output}}{C \cdot v_{Cap}} \quad (6.6)$$

6.2 Construction of a basic switchless supercapacitor assisted inverter

The construction of an inverter utilizing the switchless topology is slightly different than the switched topology, the key differences are that each sub-inverter now needs its own microcontroller as the negative input to the secondary sub-inverter is no longer at ground and that in order for the two sub-inverters to be properly synchronized with each other there needs to be a way for the two controllers to communicate between each other.

Having separate controllers for the sub-inverter actually simplifies the circuit with the current microcontrollers as they each have enough PWM outputs to control their respective full-bridges without the need for an FPGA or similar circuitry, the circuit diagram for the sub-inverters is shown in figure 6.3.

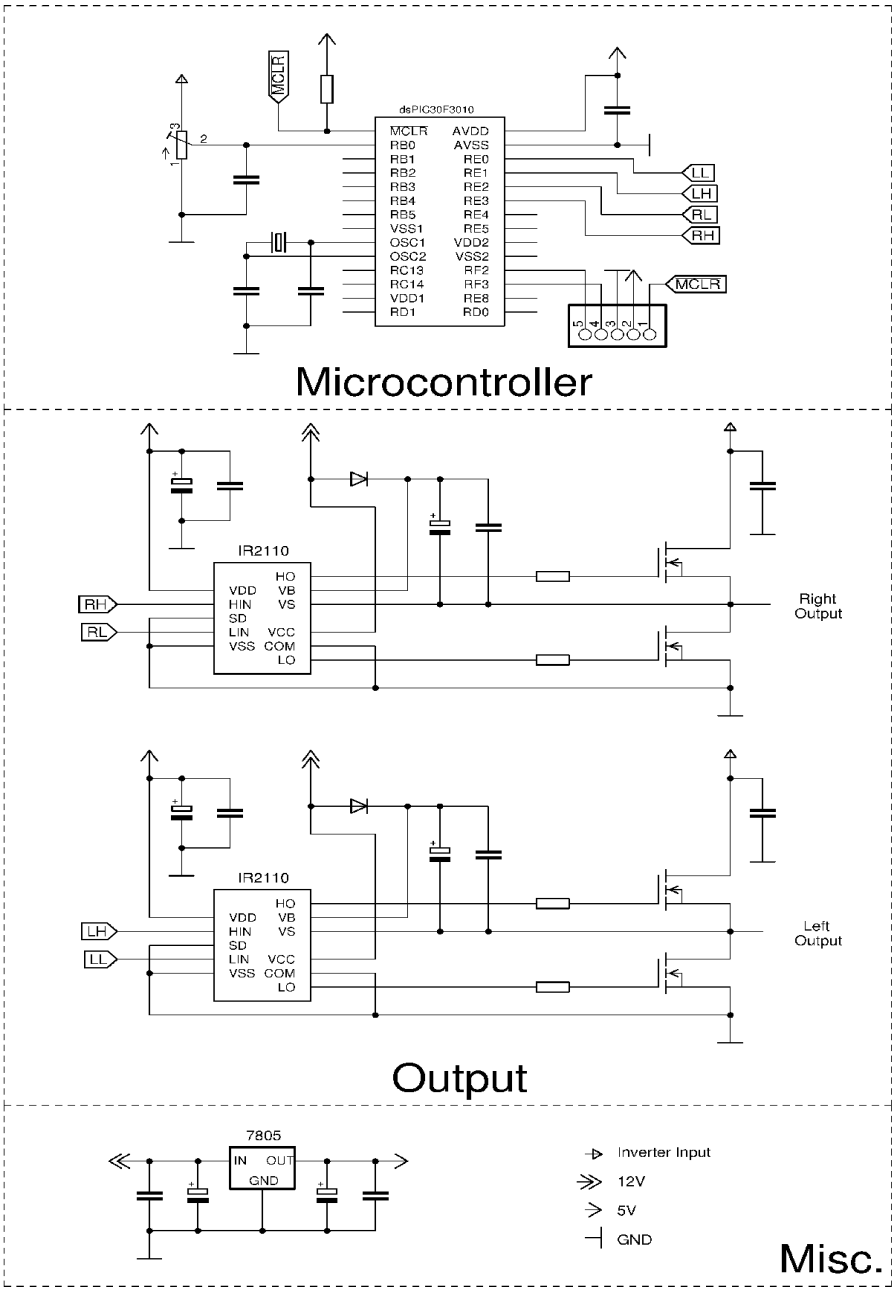

Figure 6.3: Switchless inverter sub-inverter circuit diagram.

Because the secondary sub-inverter negative input is at the positive input to the primary in order for the two controllers to communicate an isolator is needed, this is made from two opto-isolators and several resistors and is shown in figure 6.4. The different 5V and GND are from the respective sub-inverters and are not connected.

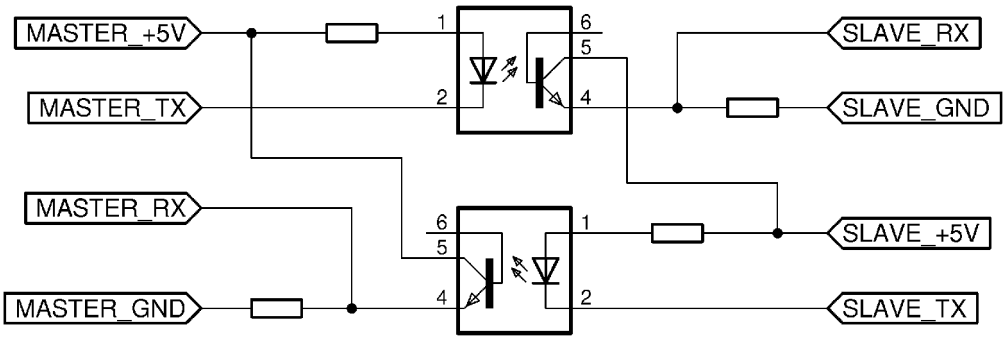

Figure 6.4: Serial communications isolater for the switchless inverter topology.

To couple the two sub-inverter outputs the transformer used in the switched full-bridge design will be used in the same configuration, the completed inverter with its load shown in figure 6.5.

The programming for the switchless inverter is much the same as the switched design except the secondary is setup as a slave that outputs the PWM desired by the primary which acts as a master. As before the inverter is programmed to output a modified sine wave however it is now a three step rather than a two step waveform.

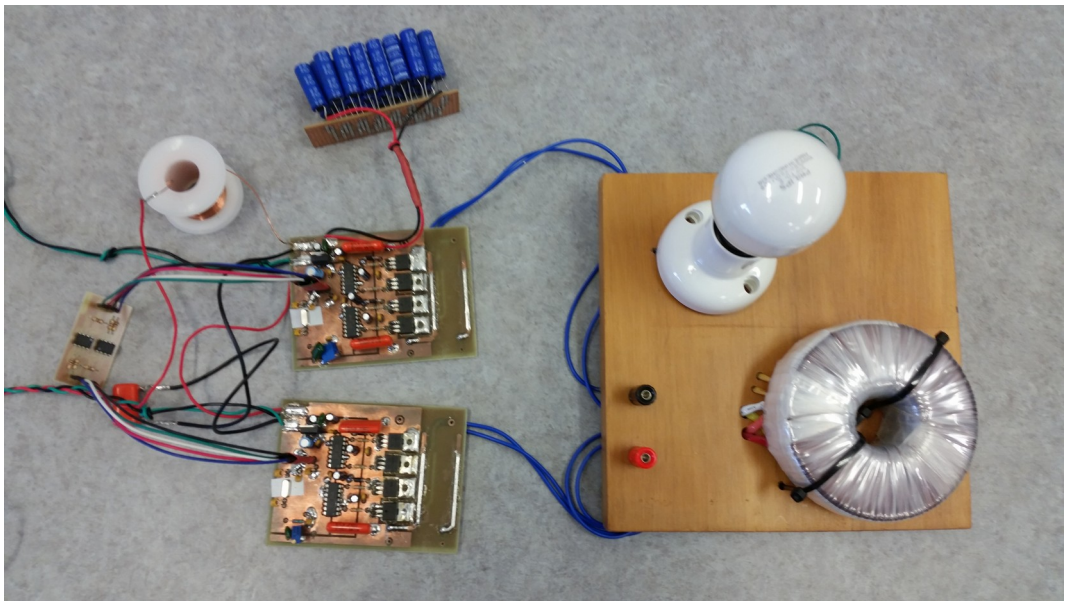

Figure 6.5: Completed switchless inverter with load, shown in LC input filter used for previous tests.

6.3 Performance analysis of the switchless inverter

The switchless inverter was tested with a 40V input from a benchtop supply and 100W 230V light bulb for a load, in order to supply the separate controllers in each sub-inverter an additional benchtop supply was used to provide 12V for the logic and switching. The operating voltage for the supercapacitor was 20V, half the input voltage.

The input current and output voltage waveforms for the inverter is shown in figure 6.6, as this shows the inverter is capable of controlling the input ripple well with near constant input irrespective of the output.

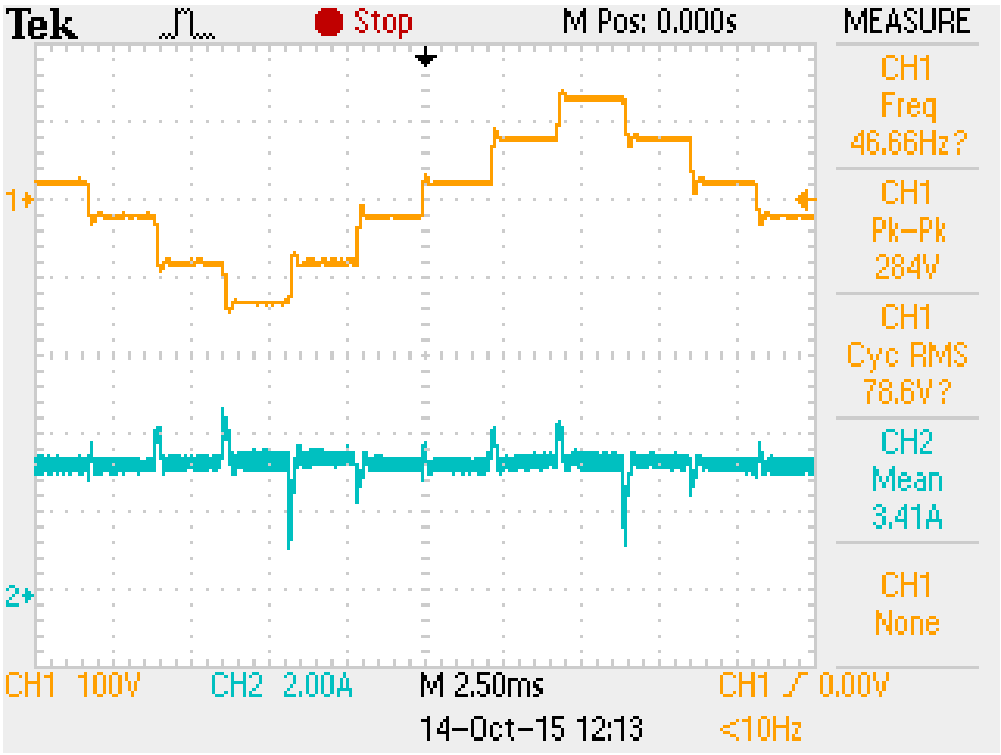

Figure 6.6: Input current (bottom trace) and output voltage (top trace) waveforms of the switchless inverter.

The small positive and negative spikes in input current correlate with changes in output power, with the positive spikes matching with the increase in output power and the negative spikes matching with the decreases in output power. One thing to note is, like the transformer coupled switched inverter this topology also has poor efficiency, with the 78.6Vrms output voltage the 100W/230V light bulb provides a load of approximately 40W, with an input power of 120W this results in an efficiency of 33%. The cause of this poor efficiency is likely one of two things, either it is a fundamental issue related to the topology, or a result of the transformer used to couple the two sub-inverters being non-ideal for this task.

In order to identify the cause of the low efficiency, the transformer was replaced with separate output filters and loads for the two sub-inverters, these were the choke and automotive headlight units used to test the uncoupled switched AC inverter in chapter 5. Like with the uncoupled switched AC inverter the two output voltages were added on the scope to show the total output voltage, the waveforms for the inverter in this configuration is shown in figure 6.7. The total load for the inverter in this configuration is approximately 80W, with a mean input current of 2.1A the input power is 88W which produces an efficiency of 91%, significantly higher than the previous 33%.

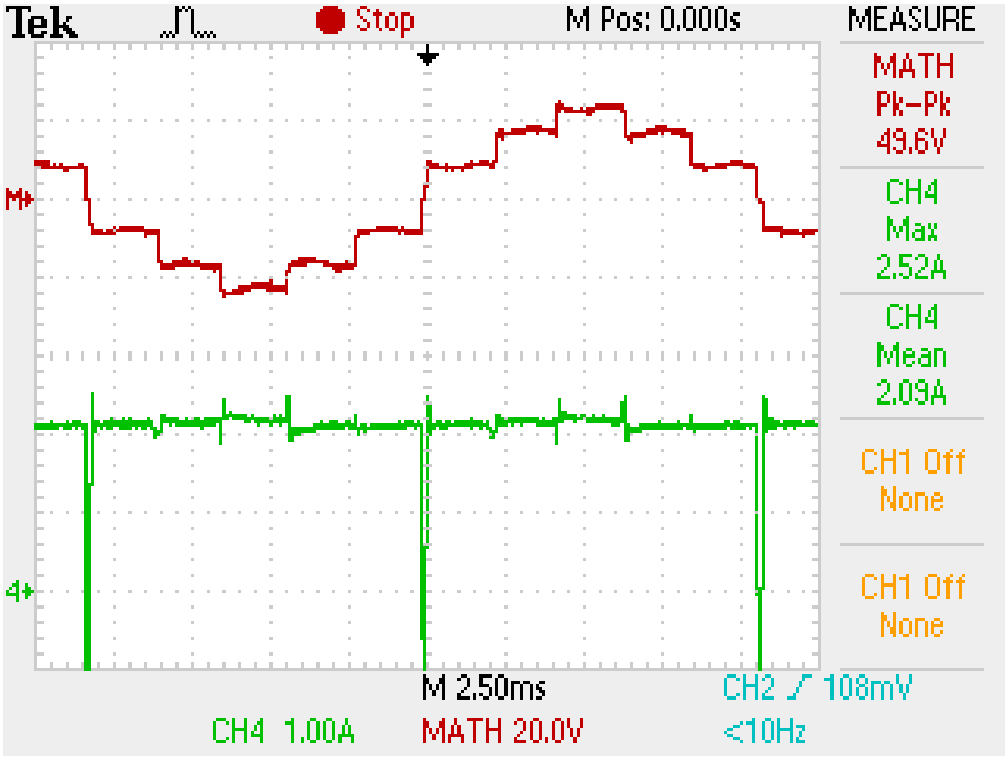

Figure 6.7: Input current(bottom trace) and sum of output voltages (top trace) of the switchless inverter with separate loads.

This result indicates that the poor efficiency of the inverter in the configuration with the coupled outputs is caused by the transformer being non-ideal for the task of coupling the two sub-inverter outputs. With suitably designed coupling transformers the efficiency could potentially be be far higher.

6.4 Comparison of switchless inverter input ripple with the conventional commercial inverter.

To verify that the switchless inverter topology is effective at controlling the input ripple it will be compared to the pure sine wave inverter investigated in chapter 3. The reason for choosing the pure sine wave inverter is because its output waveform is the one which closest matches that of the switchless inverter.

From figure 3.12, with the 100W load the pure sine wave inverter had a mean input current of 9.74A and a peak to peak current of 5A, this is a ripple percentage of 51%. From figure 6.7, with an 80W load the mean input current to the switchless inverter with the uncoupled outputs is 2.09A, if the small (<0.5ms) spikes in input current are ignored the peak to peak input current is approximately 0.05A, this gives gives a ripple percentage of 5%. Compared to the conventional inverter, the switchless inverter has significantly better input ripple performance.

Chapter 7

7.1 Discussion of the switchless inverter ripple performance

While crude the switchless inverter is capable of controlling the input ripple, with the input power being near constant while the output stepped through 3 separate power levels to produce a sine-like waveform. The topology works as predicted, with the ratio between the output power of the two inverters being used to manipulate the input power with respect to the output. By operating the primary sub-inverter at a higher power than the secondary the input power can be increased with respect to the output, with the difference being stored in the supercapacitor, and conversely by operating the secondary sub-inverter at a higher power than the primary the input power can be decreased with respect to the output, with the difference being drawn from the supercapacitor.

There is however an issue with the inverter in its current form due to the non-ideal transformer used to couple the outputs of the two sub-inverters. The transformer used for this task was a mains toroidal power transformer with two secondary output windings, each one connected to one of the two sub-inverters. With the transformer coupled outputs and a load of 40W the inverter shows poor efficiency of around 33%, the issue may be the common core shared by the two windings causing energy to flow back into

the inverter with the lower power output, effectively wasting it. To verify the transformer was at fault and that it wasn't an inherent issue with the topology the inverter was tested with separate loads for the two sub-inverters. By summing the two outputs the inverter was shown to have a much higher efficiency of 91% with a higher load of 80W, showing the previous poor efficiency was due to the non-ideal transformer. The ripple performance of the inverter in this configuration is 5%, significantly better than the pure sine wave inverter which was investigated in chapter 3 which with a load of 100W had a ripple of 51%.

At this stage the topology has been developed into a basic inverter capable of driving a resistive load with a 3-step sine-like waveform, in order to take this to a functional pure sine wave inverter capable of driving any load further development is necessary.

7.2 Potential future developments of the current topology

In order for the controller to accurately manipulate input and output current several changes and additions must be made.

7.2.1 Input and output current Sensors

Currently the inverter can only handle resistive loads as the controller programming assumes the current output is in phase with the voltage

output, any large inductive or capacitive loading would shift these out of phase which would cause issues with the total energy charged and discharged by the capacitor over a cycle. The assumption that the voltage and current output are in phase is due to not being able to tell if that is not the case as the inverter in its current state lacks the ability to monitor the input or output currents. A solution to this is to include current sensors on the input and output so the controller can analyze these waveforms and adjust its operation accordingly, figure 7.1 shows where these sensors could be placed. Due to isolation reasons these sensors would have to be hall-effect, where the current is determined by measuring the magnetic flux produced by it, rather than resistive types, where the voltage drop across a known resistance is measured to determine current.

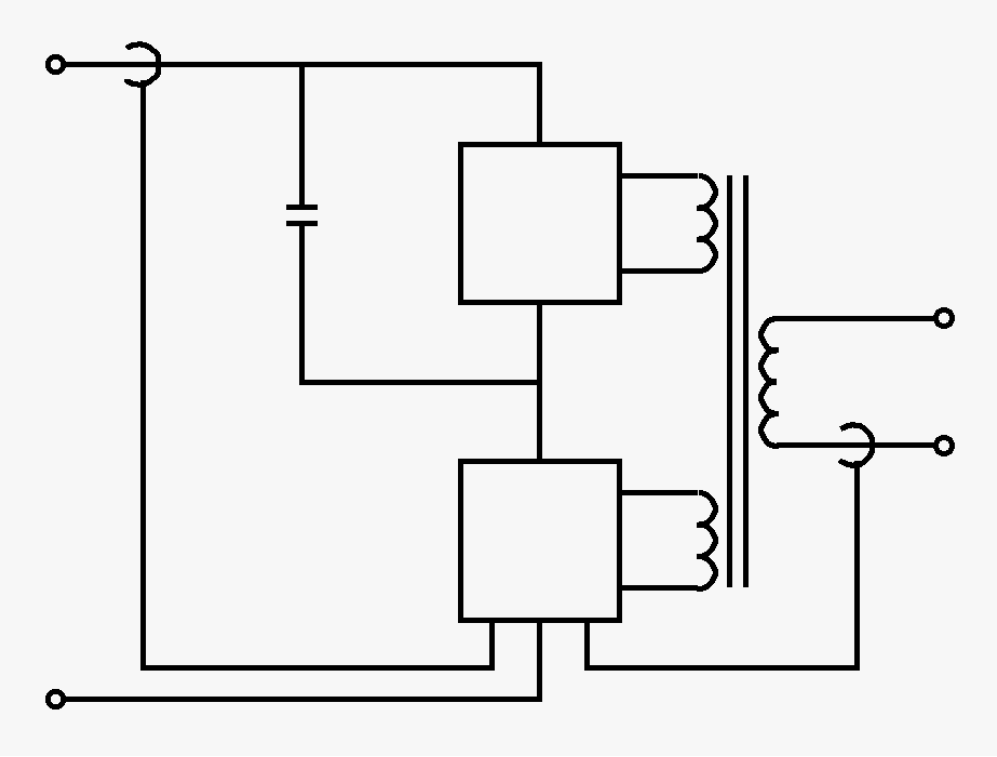

Figure 7.1: Potential current sensor locations.

7.2.2 Circuitry to store energy when output is zero

In its current configuration the topology has a major flaw which is not evident with the current 3 step sine-like waveform which would be observed in the case of a pure sine output. That is the inverter lacks a way of storing energy during periods of very low or zero output power, such as when the output voltage is close to the 0V point with a resistive load. This is because the topology in its most basic form can only manipulate the input current as a ratio to the output current, if no power is being drawn by the primary sub-inverter then the input power is also zero.

There are several ways to allow the inverter to draw energy when the output is zero, such as a switch placed on the missing 'leg' of the inverter as shown in figure 7.2 or the inductor and switch placed on the input as shown in figure 7.3.

Both of these will allow the inverter to draw current when the output is zero, with the switch placed in series with the capacitor in figure 7.2 allowing the inverter to connect the supercapacitor directly to between the two inputs by shorting it to ground, which due to its lower voltage would immediately begin charging. The circuit in figure 7.3 stores energy in the inductor by shorting it to ground to prevent the current flow though it dropping to zero, this is the similar to how power-factor-correction in domestic appliances is performed. Both of these methods are not efficient at storing energy though so alternate methods should be investigated.

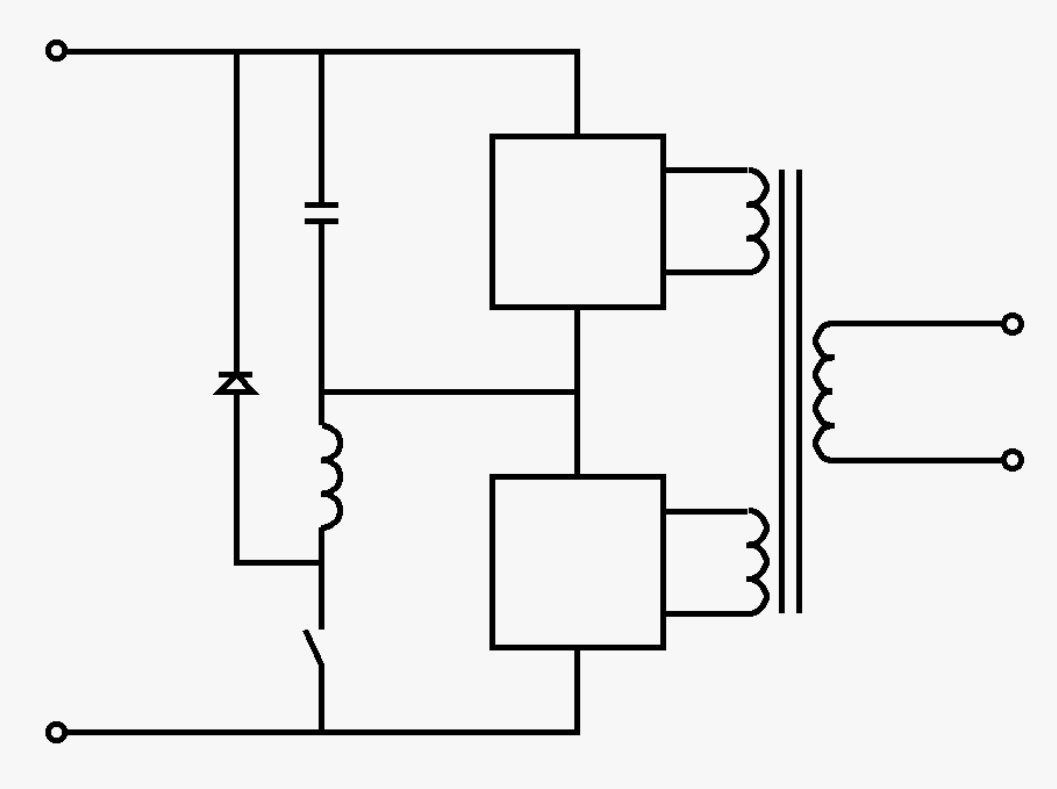

Figure 7.2: 'Missing Leg' style inductor placement.

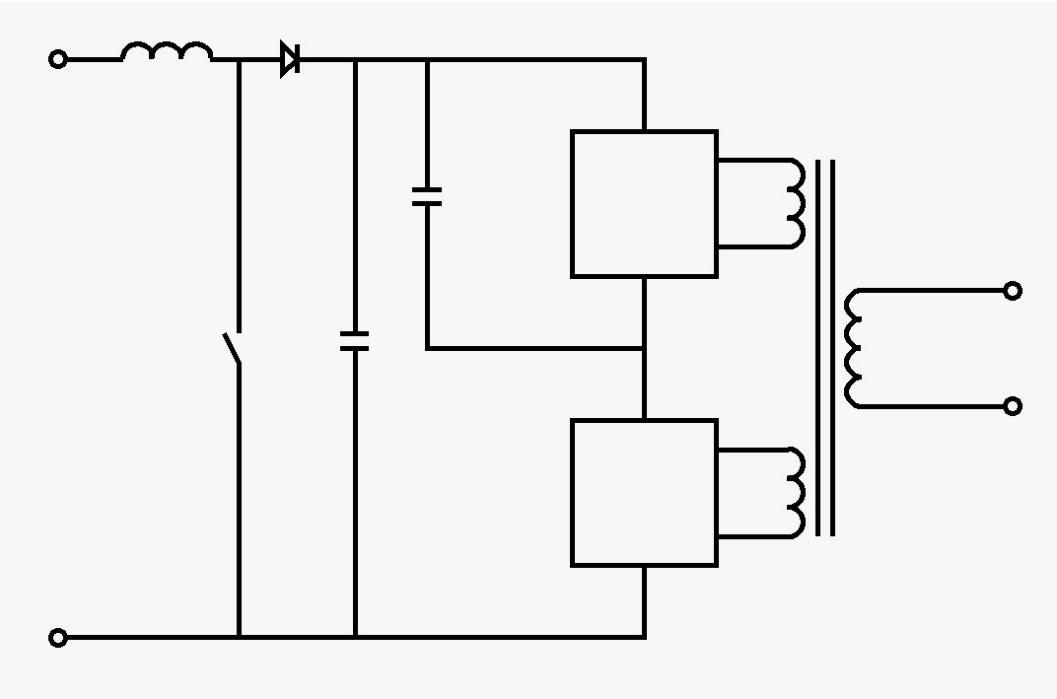

Figure 7.3: 'PFC' style inductor placement.

7.3 Developments to the topology

From the performance results of the switchless inverter it is evident that a more suitable way of coupling the two inverters is required, aside from the obvious solutions such as an appropriately designed transformer setup there exists major changes which could be made to the topology, one such possibility is shown in figure 7.4.

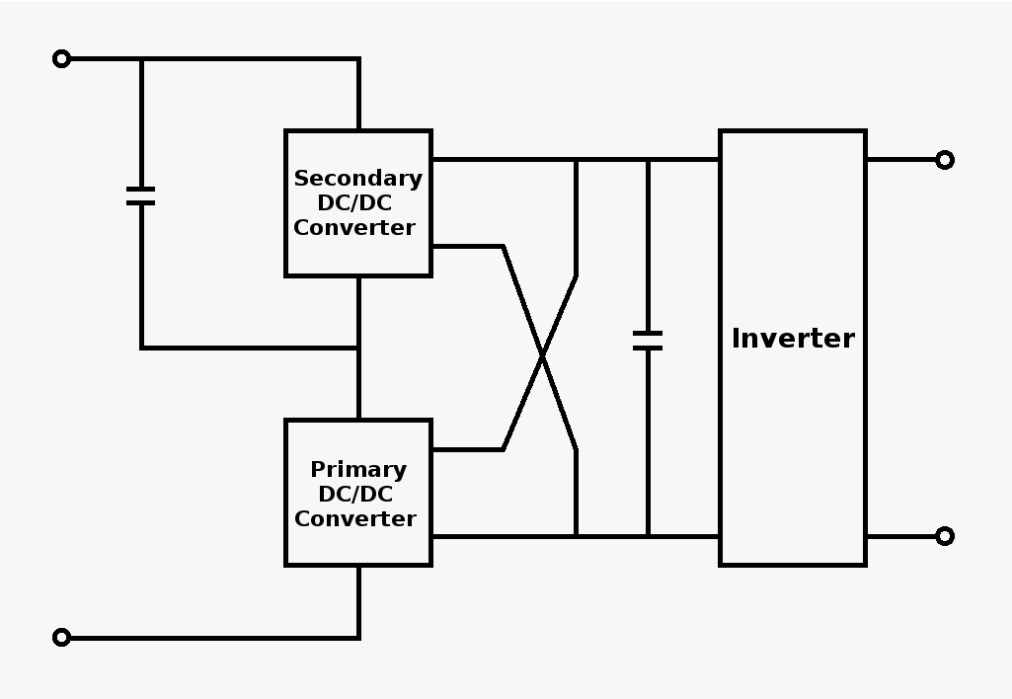

Figure 7.4: Alternate topology with the sub-inverters replaced with DC-DC converters.

Here the two sub-inverters are replaced with isolated DC/DC converters whose outputs combine, this then powers a dedicated inverter circuit which no longer needs a transformer for its output. There are several advantages offered by this topology over the existing switchless topology, namely a far higher power density, simpler microcontroller code, and the ability to setup the circuit to more easily manipulate the input power with

respect to the output power.

The higher power density offered by this circuit comes from largely the same sources as the DC-DC converter isolated inverter discussed in chapter 2, that is as the output from the isolation stage no longer needs to be a 50Hz sine wave a much higher frequency can be used, which means higher power for any given transformer size.

The simpler microcontroller code is due to separate controllers for the DC-DC and DC-AC conversion stages, as the isolation and voltage conversion stage no longer needs to perform the DC-AC conversion only the output voltage, capacitor voltage, and input current need to me monitored. This means that potentially a simple PID control loop could be used to perform the input current manipulation. Furthermore, the controller performing the DC-AC conversion would in theory only need to monitor the voltage produced by the DC-DC converter to properly perform its task.

The circuit could also more easily manipulate the relationship between its input and output powers, this is because the ratio between the nominal input voltage and the working capacitor voltage can be easily adjusted by the designer to adjust the range over which the topology can manipulate the ratio between its input and output. While this is possible with the current topology this method allows some room for the inverter to further adjust it on the fly.

References

[1] Carr, G. (2012, November). "Sunny Uplands." *The Economist*. Internet: http://www.economist.com/news/21566414-alternative-energy-will-no-longer-be-alternative-sunny-uplands [Jan. 19, 2016]

[2] Hunt, T. (2014, November). "Swanson's Law and Making US Solar Scale Like Germany." *Green Tech Media*. Internet: https://www.greentechmedia.com/articles/read/Is-there-really-a-Swansons-Law [Jan. 19, 2016]

[3] DeMeo, D. et al. “Electrodeposited Copper Oxide and Zinc Oxide Core-Shell Nanowire Photovoltaic Cells” in *Nanowires – Implementations and Applications*. Hashim, A (Ed.). 2011.

[4] Renogy. "RNG-Mono Series Solar Panels." Internet: http://www.enfsolar.com/ApolloF/solar/Product/pdf/Crystalline/522e9c35531c4.pdf

[5] Cubas, J. et al. "Explicit Expressions for Solar Panel Equivalent Circuit Parameters Based on Analytical Formulation and the Lambert W-Function." *1st International e-Conference on Energies*, 2014.

[6] Singh, A. et al. “Voltage Fed Full Bridge DC-DC and DC-AC Converter for High-Frequency Inverter Using C2000.” *Texas Instruments*. Internet: http://www.ti.com/lit/an/sprabw0b/sprabw0b.pdf

[7] Sclocchi, M. “Input Filter Design for Switching Power Supplies.” *Texas Instruments*. Internet: http://www.ti.com/lit/an/snva538/snva538.pdf

[8] Tarampvoch, S. (2012, January). "Teardown: The power inverter – from sunlight to power grid." *EDN Network*. Internet: http://www.edn.com/design/power-management/4368876/Teardown-The-power-inverter--from-sunlight-to-power-grid [Jan. 19, 2016]

[9] Rozenblat, L. “PUSH-PULL DC-AC INVERTERS.” Internet: http://www.smps.us/inverters.html [Jan. 19, 2016]

[10] Bower, W. at al. “Evaluation of Islanding Detection Methods for Utility-Interactive Inverters in Photovoltaic Systems.” *Sandia National Laboratories*. Internet: http://prod.sandia.gov/techlib/access-

control.cgi/2002/023591.pdf

[11] National Instruments. “Maximum Power Point Tracking.” Internet: http://www.ni.com/white-paper/8106/en/ [Jan. 19, 2016]

[12] Zipp, K. (2011, October). "Where microinverter and panal manufacturer meet up." *Solar Power World*. Internet: http://www.solarpowerworldonline.com/2011/10/where-microinverter-and-panel-manufacturer-meet-up/ [Jan. 19, 2016]

[13] Knoth, S. (2014, May). "Simplifying solar-based battery charging." *EE Times*. Internet: http://analog-eetimes.com/en/simplifying-solar-based-battery-charging.html?cmp_id=71&news_id=222906361 [Jan. 19, 2016]

[14] Woodbank Communications Ltd. "Battery Performance Characteristics." Internet: http://www.mpoweruk.com/performance.htm [Jan. 19, 2016]