Development of a Supercapacitor based Surge Resistant Uninterruptible Power Supply

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Te Whare Wānanga o Waikato

Abstract

Uninterruptible Power Supplies (UPSs) provide short-term power back-up to sensitive electronic and electrical equipments, where an unexpected power loss could lead to undesirable outcomes. They usually bridge the connected equipment between the utility mains power and other long term back-up power systems like generators. A UPS also provides a "clean" source of power, meaning they filter the connected equipment from distortions in electrical parameters of the mains power like noise, harmonics, surges, sags and spikes.

A surge resistant UPS or SRUPS is one that has the capability to withstand surges, which are momentary or sustained increases in the mains voltage, and react quickly enough to offer protection to the connected equipment from the same.
Usually UPSs run off battery power when the utility mains power is absent. But the SRUPS developed in this design project uses super capacitors instead of battery packs. The reason for this is that the high energy-densities and medium power-densities offered by super capacitors allow for it to serve two purposes. One is to provide the DC power to operate the UPS in the absence of mains power, as an alternative to batteries. Secondly, super capacitors can withstand heavy momentary high current/voltage surges due to its high energy-density characteristics. Also as the life-time of super capacitors is much higher than that of conventional batteries and as they do not need regular topping-up or inspection, the end result is a truly maintenance-free UPS.

Most commercial UPSs do not have inherent surge protection capabilities. The UPS is one entity while a discrete surge protection module is inserted between the utility mains and the UPS to provide for transient surge suppression. In the proposed SRUPS, the super capacitor, because of their inherent capability to absorb transient surges, forms a protective front end to the actual UPS rather than needing to have the involvement of discrete protection devices.

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Acknowledgements

First off, I dedicate this thesis to my parents whose unwavering love and support made me what I am today. Words can't express my gratitude for all they have provided me with.

I am very much indebted to my academic supervisor, Mr. Nihal Kularatna, without whose brilliance, this research project wouldn't have taken form. He was the guiding light who unfalteringly led me through thick and thin, whose support and enthusiasm was quintessential for the successful completion of my Masters of Engineering degree at The University of Waikato.

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A hearty thanks to everyone at College Hall, for being my family in New Zealand, for all the good times I had, and providing me with a vibrant atmosphere for me to study and work.

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Nomenclature

AC	**Alternating Current**
DC	**Direct Current**
EMI	**Electro-Magnetic Interference**
ESR	**Effective Series Resistance**
GDT	**Gas Discharge Tube**
LED	**Light Emitting Diode**
MOSFET	**Metal Oxide Semiconductor Field Effect Transistor**
MOV	**Metal Oxide Varistor**
PIC®	**Peripheral Interface Controller**
PWM	**Pulse Width Modulation**
RMS	**Root Mean Square**
SC	**Super Capacitor**
SRUPS	**Surge Resistant Uninterruptible Power Supply**
TVSS	**Transient Voltage Surge Suppressor**
UPS	**Uninterruptible Power Supply**

Chapter 1

Introduction

1.1 OVERTURE

Super capacitors (SCs) or ultra capacitors are electrochemical double layer capacitors that have high power densities with limited energy density as compared to conventional batteries. Their beginnings can be traced back to the laboratories of Sohio Corporation of Cleveland, New Jersey some 40 years ago [2]. Nowadays SCs with capacitance values in the range of thousands of farads are commercially available, thus making them a promising energy storage device for niche power electronics applications. SCs are a reliable alternative to batteries in the sense they have enhanced life cycles as their operation involves only non-faradaic electrostatic phenomenon.

Recent research carried out by the author's supervisor opened up a previously uncharted application area for SCs. Their extremely high capacitance values theoretically allow them to absorb large amounts of energy which practically can be interpreted as surge endurance. Table 1.1 summarizes test results obtained from surge testing SCs from different vendors by exposing them to short duration surges with energy values specified in IEEE C62-41 and IEC 61000-4-5 and similar standards.

Table 1.1: Super capacitor data summary and summary of test results (Kularatna, 2010)

Parameters as per data sheets	**Cap-XX**	**Nesscap**	**Maxwell Boostcap**
Capacitance	0.18 F	90 F	230 F
Rated DC Voltage	2.3 V	2.7 V	2.5 V
Effective Series Resistance	45 mΩ	0.33 mΩ	2.2 mΩ
Operating Temperature Range	-40 - 70 °C	-40 - 65 °C	-40 - 70 °C
Leakage Current	3.5 µA	0.75 mA	0.45 mA
Surges persevered before failure	150-250	Didn't fail after 600 hits	Didn't fail after 1000 hits

These results show that SCs with higher capacitances have extended surge withstanding capabilities. Therefore, SCs, with their increased functionality, life cycle costs, reliability and surge resistance capabilities offer the perfect energy storage solution to make successful mission-critical power backup systems.

1.2 SCOPE

The project aimed at developing a prototype super capacitor based on-line, double-conversion surge resistant uninterruptible power supply (SRUPS) to provide a clean and efficient reserve source of power for sensitive electronic equipments. The principal intention of this project is to demonstrate the feasibility of SCs, both as energy storage devices for power back up as well as its surge resistance capability when used as proposed in the system.

The prototype shall consist of a solid state AC-DC step-down converter, super capacitor based power reserve, a microcontroller based super capacitor bank switching circuit, a solid-state inverter, an automatic solid-state surge detection and isolation circuit and a static by-pass switch. As a prototype, the system is designed to work off the 230V/50Hz utility mains power and deliver clean useable power of at least100W at the load at 230V/50Hz using three consecutively switched super capacitor banks as the energy storage elements for providing power backup and as a system front end to offer surge protection.

The project was originally undertaken with funding from WaikatoLink, the commercialization and technology transfer arm of The University of Waikato with a view to visualize commercially viable patentable applications of SCs that haven’t been developed elsewhere.

1.3 UNINTERRUPTIBLE POWER SUPPLIES

UPSs arose by the turn of the century from the apparent need for clean and “break-free” power for electronic equipments that had ever increasing system complexities and sensitivities. UPSs act as a bridge and a back-up to stand between the utility mains power supply and the equipment. They generally have rechargeable batteries as the energy storage elements for use as the backup power source. Most UPSs are not inherently resistant to power surges or other line

anomalies. They have discrete suppression and filtering modules that are inserted in their initial stages to tackle these issues.

Figure 1.1 shows the basic building blocks of a UPS which are iterated in different topologies to create different types of UPSs.

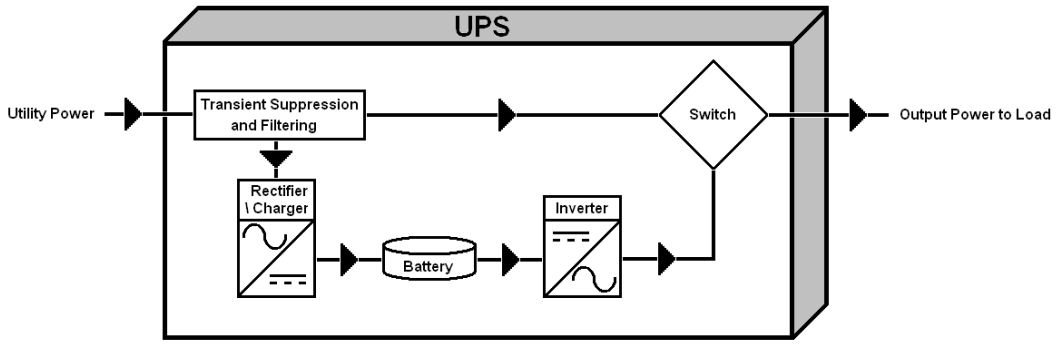


Figure 1.1: Block diagram of a basic UPS

In a layman's point of view, there are only two types of UPS systems, namely the standby UPS and the online UPS, their operation being obvious from their naming terminology. But from a design approach point of view, UPSs can be classified as:

- Standby / Off-line
- Line Interactive / Standby Ferro
- Standby-Ferro
- On-Line

1.3.1 STANDBY / OFF-LINE UPS

This UPS is commonly found in domestic household environments. Figure 1.2 shows the operation of the standby UPS. The transfer switch normally connects the filtered AC input as the primary power source to run the load and in the event of a utility power failure, switches to the battery / inverter as the backup. The inverter is only operational when the power fails, hence the name "standby". These UPSs are cheap, offer high efficiency, and serves its intended purpose for low sensitivity equipmental power backup requirements. The level of utility line filtering and surge suppression available in standby UPSs are price dependent and may be even absent in low-end versions which make them highly unreliable when operated in environments prone to line transients and surges.

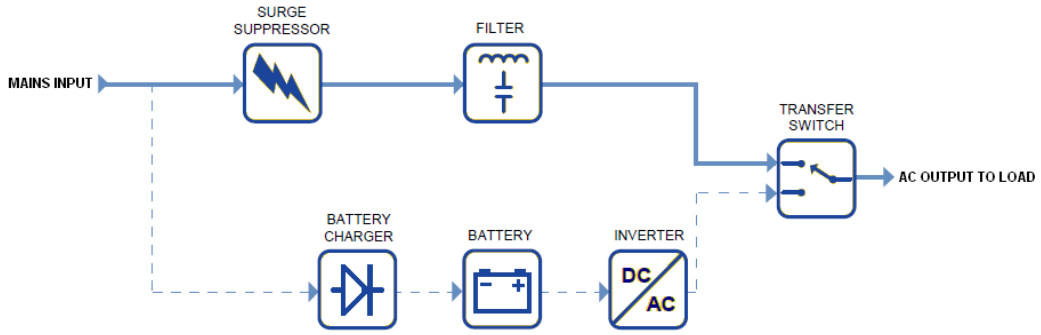


Figure 1.2: Block diagram of a standby/off-line UPS

1.3.2 LINE INTERACTIVE / STANDBY-FERRO UPS

These were formerly the prevailing type of UPSs used in the 0.5-15KVA range. This design relies on a special saturating transformer that has three windings, two bifilar wound primaries and a secondary. The primary power path runs from the mains AC input, through a transfer switch, via one of the transformer primaries and onto the connected load. In case of power failure, the transfer switch opens and the inverter picks up the output load via the second primary winding of the transformer. Here, the inverter is in standby mode during normal operation. The transformer, along with the isolation it provides, also has a special "ferro-resonant" capability that ensures limited voltage regulation and output waveform "shaping" . As these transformers are quite large, heavy and inherently inefficient these UPSs are large and generate a great deal of heat. Figure 1.3 demonstrates the standby-ferro topology.

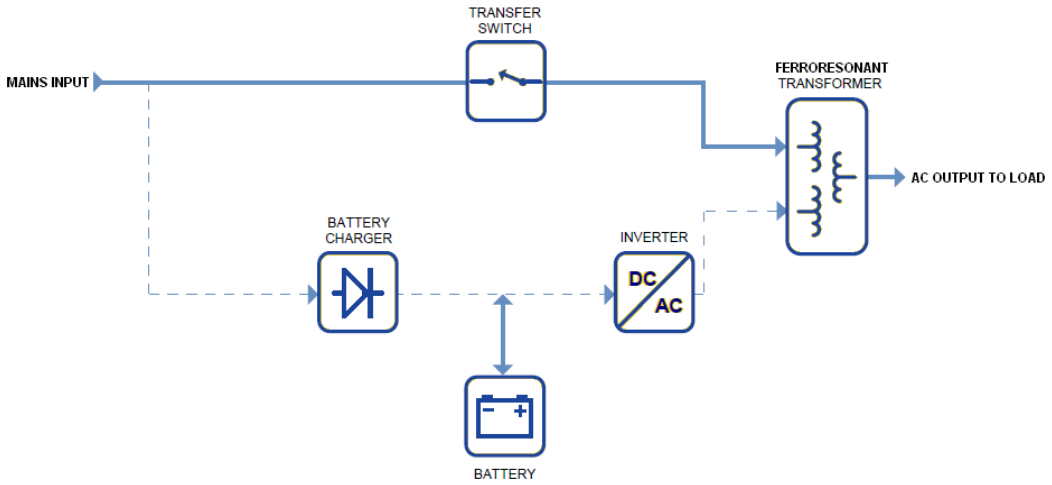


Figure 1.3: Block diagram of a line interactive / standby-ferro UPS

1.3.3 ON-LINE UPS

These UPSs are mainly used where power requirements exceed 10KVA. Here, there is no transfer switch as the connected load always runs off the inverter. The inverter runs directly off the rectified mains AC during normal operation and when there is a power failure, the inverter runs off the battery. The changeover switch is negated as the battery is always floating. If a low voltage battery bank is used, the UPS is called a Double-Conversion on-line UPS as the utility mains is rectified and stepped down to charge the battery and the battery power is boosted to the mains voltage before being fed to the inverter. For high power on-line UPS systems, high voltage battery banks (similar to utility mains voltage) are arranged and an active power factor correction circuit serves as the mains rectifier as its output DC voltage is automatically adjusted to float charge the battery bank and drive the inverter. These designs are called Delta-Conversion on-line UPSs. The working of on on-line UPS is depicted in Figure 1.4

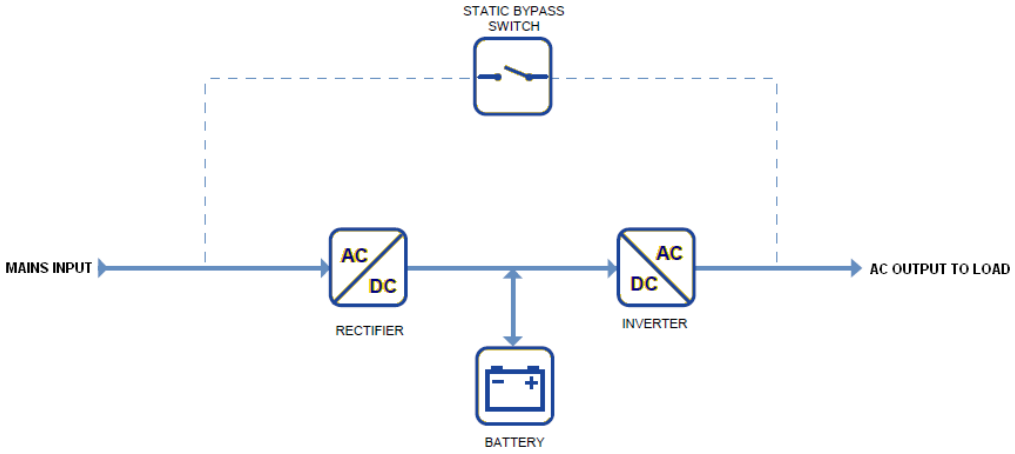


Figure 1.4: Block diagram of an on-line UPS

Tables 1.2 and 1.3 describe the main characteristics of the different types of UPSs that have been discussed so far.

Table 1.2: Characteristics of different types of UPSs

Type of UPS	**Practical Power Range (KVA)**	**Voltage Conditioning**	**Cost per VA**
Standby/Off-line	0-0.5	Low	Low
Standby-Ferro / Line Interactive	0.5-15	High	High
On-Line	5-5000	High	Medium

Table 1.3: Operational characteristics of different types of UPSs.

Type of UPS	Efficiency	Inverter Always Operating	Benefits	Limitations
Standby /Off-line	Low	No	Low cost, High efficiency, compact	Uses battery during brownouts, Impractical over 2kVA
Standby-Ferro / Line Interactive	High	No	Excellent voltage conditioning, high reliability	Low efficiency, unstable in combination with some loads and generators
On-Line	High	Yes	Excellent voltage conditioning, high efficiency	Impractical under 5kVA

1.4 RESEARCH OBJECTIVES AND SPECIFICATIONS

The intention of this research is to develop a prototype 230V/50Hz on-line double-conversion UPS that utilizes SC banks as its energy storage element. The prototype must be able to deliver at least 100W of useable power at the load side at 230V/50Hz. Three SC banks are proposed to power the system consecutively to enhance the backup capability of the UPS. Also as the SC banks form the front end of the UPS system, its inherent capability to withstand surges will be put to use as the surge suppression element in the system to ultimately create a surge resistant UPS.

The main objectives in developing the super capacitor based surge resistant uninterruptible power supply (SRUPS) are as follows:

- Runs off the utility mains power supply of 230v / 50Hz
- Run a connected 230v / 50Hz AC load at 100w
- Withstand surges as per IEEE C62-41 and IEC 61000-4-5 specifications
- Fast surge detection and system isolation

- Synthesized pure sinusoidal output AC
- Reliable with a high operational mean time between failure (MTBF) hours
- Economical with relation to component count and costs

1.5 SYSTEM DESCRIPTION

The SRUPS consists of six major parts.

- Basic surge protection block
- Solid-state surge detection and isolation circuit
- Solid-state AC-DC step-down converter
- Microcontroller based super capacitor bank switching circuit
- Three 21.6v / 81.25F super capacitor banks
- Microcontroller based synthesized sine-wave PWM full-bridge inverter
- Static bye-pass switch

Off the shelf transient voltage surge suppression devices form the initial surge protection. Opto-couplers and solid state switches are used in the surge detection and isolation circuit. A high-end power MOSFET is used in a buck converter based configuration for the AC-DC step-down converter to charge the SC banks. Eight 2.7v/650F Maxwell BOOSTCAP super capacitors connected in series are used in each of the three SC banks. A PIC® microcontroller based control and monitoring circuit incorporating MOSFET switches is used for switching between the charge/idle/discharge states of the SC banks. A MOSFET driven PIC® microcontroller based synthesized sine wave pulse width modulated full-bridge inverter is used for efficient DC-AC conversion. In the event that the UPS must be taken off-line for maintenance of UPS, or unforeseen emergency situations, the critical load shall be transferred to the utility mains source via the static switch.

The complete functional block diagram of the SRUPS is demonstrated in Figure 1.5.

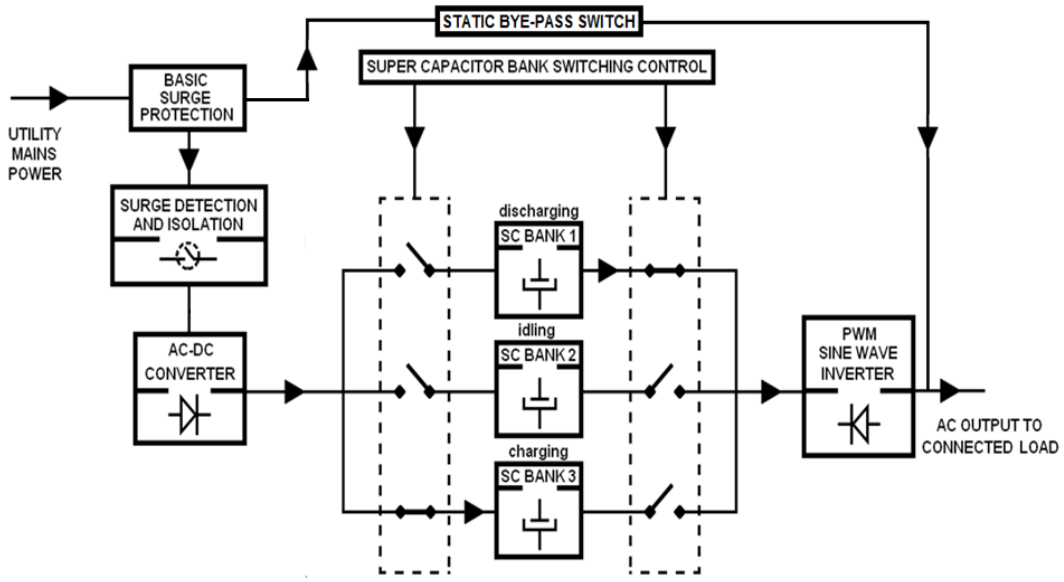


Figure 1.5: Functional block diagram of SRUPS

1.6 THESIS OUTLINE

Chapter One: Introduction. A basic outline and scope of the project is discussed and the background on the inception of the idea of using super capacitors as energy storage elements in power back–up systems and how the same could be used to offer protection against power line surges is brought to light. Also briefed are the different types of UPSs in existence. Finally a rundown of the overall system functionality of the proposed SRUPS is also given.

Chapter Two: Background. Here, the two main topics discussed will be super capacitors and transient surges. The literature survey carried out on these topics form the backbone for the ideologies used in the development of the prototype SRUPS. This chapter sheds light on the working and operational characteristics of super capacitors and then moves on to briefly explain principles of transient surges, surge protection and surge testing.

Chapter Three: Theoretical Synopsis of the Design Approach. The theories concerned in the design of the various electronic circuits involved in the different stages of the SRUPS are discussed in this chapter. The reasons why the circuits used to implement these stages are the better design choices amongst other available technologies are also brought to light.

Chapter Four: System Implementation. This chapter deals with how the individual modules involved in the SRUPS were realized and tested and then integrated to one single entity to form the complete operational system, which is the super capacitor based surge resistant uninterruptible power supply.

Chapter Five: Performance Evaluation and Results. After the implementation of the SRUPS, tests and measurements carried out to determine its operational performance characteristics and the corresponding results obtained are categorized in this chapter.

Chapter Six: Conclusion and Future Developments. The SRUPS developed in this research project is a prototype. There are certain areas in the modules of the SRUPS that could be fine-tuned to improve the overall performance and efficiency of the system. Technological and other constraints that limited the design of the SRUPS are also discussed. This chapter concludes with general idea that went into the SRUPS and what future improvements could be incorporated to progress on the prototype developed.

Chapter 2

Background

2.1 SUPER CAPACITORS

Electrochemical double layer capacitors are also known as super capacitors or ultra capacitors. Super capacitors (SCs) are reversible energy storage devices that have higher instantaneous power densities than conventional batteries and higher energy densities than electrostatic dielectric capacitors as can be seen depicted in Figure 2.1. Energy density is the amount of energy stored per unit mass. Power density is the maximum amount of power that can be supplied per unit mass. An SC stores energy via an electrostatic process by polarizing an electrolytic solution. Though it is an electrochemical device there are no chemical reactions involved in its energy storage mechanism. This mechanism is highly reversible, allowing the SC to offer high charge-discharge cycling capabilities, making them well suited in power conditioning and back-up applications.

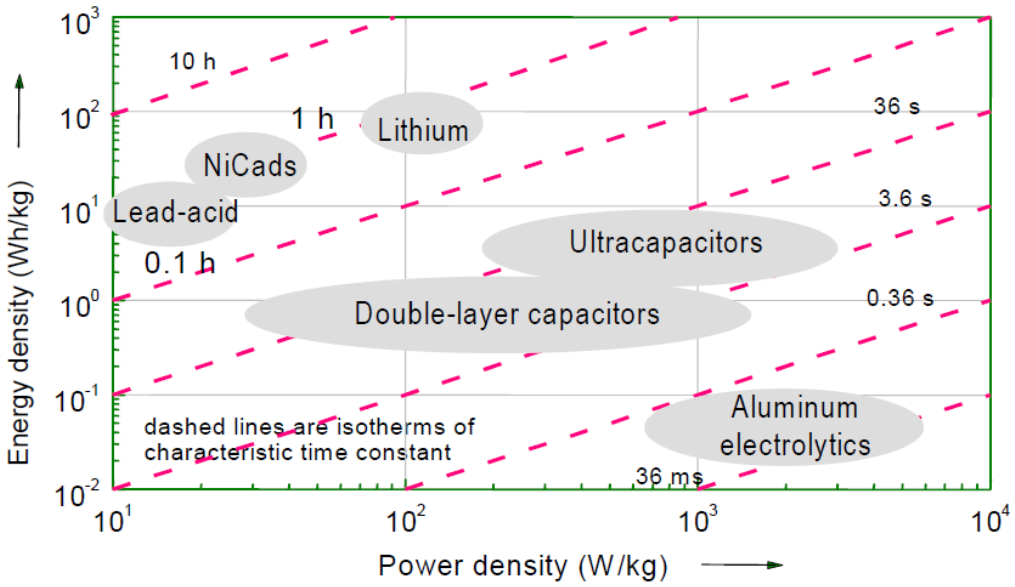


Figure 2.1: Ragone chart of various energy storage devices (Nesscap Co. Ltd., 2008)

An SC can be visualized as two nonreactive porous plates suspended within an electrolyte with an applied voltage across the plates. This is shown in figure 2.2.

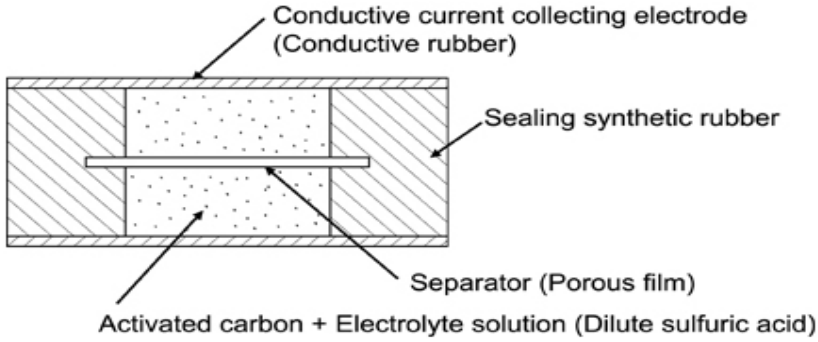


Figure 2.2: Layered structure of a super capacitor (NEC Corp. 1994-2011)

The applied potential on the positive plate attracts the negative ions in the electrolyte, while the potential on the negative plate attracts the positive ions. This effectively creates two layers of capacitive storage, as shown in figure 2.3, one where the charges are separated at the positive plate, and another at the negative plate, thus the terminology electrochemical double layer capacitors.

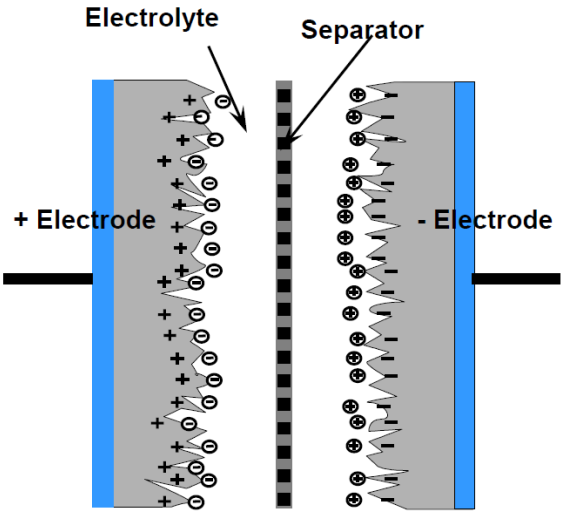


Figure 2.3: Charge separation in super capacitors (Maxwell Technologies, 2006)

The capacitance (C) of a parallel plate capacitor with permittivity of the dielectric (ε), area of the plates (A) and inter-plate separation (d) is given as:

$$C = \varepsilon \frac{A}{d} \quad (1)$$

Conventional electrolytic capacitors storage area is derived from thin plates of flat, conductive material. High capacitance is achieved by winding great lengths of material. Further increases are possible through texturing on its surface, increasing its surface area. A conventional capacitor separates its charged plates with a dielectric material: plastic, paper or ceramic films. The thinner the dielectric the more area can be created within a specified volume. The limitations of the thickness of the dielectric define the surface area achievable. An SC on the other hand derives its area from a porous carbon-based electrode material. The porous structure of this material allows its surface area to approach 2000 square meters per gram, much greater than can be accomplished using flat or textured films and plates. An SC's charge separation distance is determined by the size of the ions in the electrolyte, which are attracted to the charged electrode. This charge separation (less than 10 angstroms) is much smaller than can be

accomplished using conventional dielectric materials. The combination of enormous surface area and extremely small charge separation gives the super capacitor its outstanding capacitance relative to conventional capacitors.

The energy storage (E) for a capacitor with a capacitance (C) and voltage rating (V) is given as:

$$E = \frac{1}{2}CV^2 \quad (2)$$

2.1.1 APPLICATIONS OF SUPER CAPACITORS

Typical applications of SCs span from a requirements of a few milliamps of current or milliwatts of power to several hundred amperes of current or several hundred kilowatts of power needs. Industries employing SCs have included: consumer electronics, traction, automotive, and industrial.

2.1.1.1 PULSE POWER

SCs are ideally suited for pulse power applications. As the energy storage is not a chemical reaction, the charge/discharge behavior of the capacitors is efficient. Since SCs have low internal impedance they are capable of delivering extremely high currents and are often placed in parallel with batteries to level the loading of the batteries, extending battery life. The SC buffers the battery from seeing the high peak currents experienced in the application. This methodology is employed for devices such as digital cameras, hybrid drive systems and regenerative braking (for energy recapture).

2.1.1.2 BRIDGE POWER

SCs are utilized as temporary energy sources in many applications where immediate power availability may be difficult. This includes UPS systems utilizing generators, fuel cells or flywheels which function as the main power backup for applications. All of these systems require a definite though short start up time before they are fully functional and can switch over the load, thereby generating momentary power interruptions. SC systems are utilized to provide the appropriate amount of ride-through time until the primary backup power source kicks in and becomes available to take up the load.

2.1.1.3 MAIN POWER

SCs are perfectly suitable to be used as the primary source of power for applications requiring power for only short periods of time or if it is only acceptable to allow short charging time before use. Examples of such applications include toys, emergency flashlights, institutional paging devices, solar charged accent or mood lighting, and powering emergency access points.

2.1.1.4 MEMORY BACKUP

When an application has an available power source to keep the SCs trickle charged as in computer systems, they may be suited for memory backup, system shutdown operations, or event notifications. The SCs can be maintained at its full charged state and can act as a power reserve to perform critical functions in the event of loss of power. This may include automatic monitoring and reporting systems for reporting power outage, micro-controllers based embedded systems and mother board memories in computers.

2.1.2 SIZING THE CAPACITANCE REQUIREMENT FOR AN APPLICATION

Determination of the proper capacitor and number of capacitors is dependent on the intended application. For sizing the system correctly a number of factors should be known. These factors include the maximum and minimum operating voltage of the application, the average current or power, the peak current or power, the operating environment temperature, the run time required for the application, and the required life of the application. Every super capacitor has a rated voltage (V_R). Since SCs are low voltage devices, this rated voltage is generally less than what the required application voltage is. Knowing the maximum application voltage (V_{MAX}) will determine how many capacitor cells are required to be series connected. The number of series connected cells (N) is determined by:

$$N = \frac{V_{MAX}}{V_R} \tag{3}$$

Next, by knowing the average current (I) in amps, the required run time (dt) in seconds and the minimum working voltage (V_{MIN}) for the application, an approximate capacitance required to power the system (C_{SYS}) can be calculated.

$$C_{SYS} = I * \frac{dt}{dV} = I * \frac{dt}{(V_{MAX} - V_{MIN})} \tag{4}$$

The total system capacitance requires is comprised of the capacitance of all the series connected capacitors for achieving V_{MAX}. For capacitors connected in series the total capacitance (C_{TOT}) is determined by:

$$\frac{1}{C_{TOT}} = \frac{1}{C_1} + \frac{1}{C_2} + \cdots + \frac{1}{C_n} \quad (5)$$

For n SC cells of equal capacitance (C) connected in series, the total capacitance is given by:

$$C_{TOT} = \frac{C}{n} \quad (6)$$

It may also be necessary to place one or more capacitors in parallel to attain the needed energy requirements. For n capacitors connected in parallel the equivalent capacitance (C_{EQ}) is determined by:

$$C_{EQ} = C_1 + C_2 + \ldots + C_n \quad (7)$$

There are many other items to consider for properly sizing the capacitance value required for an application. This includes the internal resistance of the capacitor to account for the instantaneous voltage drop associated with an applied current, the ambient operating temperature which affects the internal resistance and the capacitor life, and the lifetime expected of the application. The super capacitor performance requirement at end of life of the application is necessary to ensure proper initial sizing for the system.

2.1.3 SUPER CAPACITOR SPECIFICATIONS

Given below are the technical specifications and ratings that need to be kept in mind and considered before and during the selection and application of super capacitors in a system.

- **Capacitance** – the measurement of energy storage capacity in joules.
- **Voltage** – the maximum operating voltage for a single capacitor. It is possible for the capacitors to experience voltages in excess of the rated voltage. The impact is dependent on the time and temperature during this exposure. At no time should the capacitor be subjected to voltages in excess of 10% of the rated voltage.
- **Internal Resistance, DC** – the resistance corresponding to all the resistivecomponents within the super capacitor. It is compromised of resistive components attributed to contacts, electrode, electrolyte, and other material resistances.

- **Internal resistance, 100 hz or 1 khz** – the measure of the high frequency resistance component and is mainly attributed to contact resistance. Because of the time constant of the super capacitors, operation at this frequency is highly inefficient.
- **Thermal Resistance** – this may be used to determine the heat generation within the SC at any given current load and duty cycle. This value is based on free convection and would be considered for the worst case scenario. Forced convection would improve the thermal resistance.
- **Short Circuit Current** – momentary current delivery possible by the SC if it is short circuited. This is intended purely for cautionary purposes and not for nominal usage.
- **Leakage Current** – the stable parasitic current that is expected when the SC is held indefinitely on charge at its rated voltage. This value is voltage and temperature dependent.
- **Operating Temperature Range** – represents the operating temperature range of the S and may not reflect the ambient temperature.
- **Storage Temperature Range** – represents the safe storage temperature without affecting ultracapacitor performance when no voltage is applied to the ultracapacitor.
- **Endurance Capacitance** – the maximum capacitance change expected when the SC is held at rated voltage for a specified life-time and temperature, which is intended to be considered as the upper operational limit.
- **Endurance Resistance -** the maximum resistance change expected if the SC is held at rated voltage for a specified life-time and temperature, which is intended to be taken as the upper operational limit.
- **Maximum Energy** – the maximum energy available for SC while it is new, when it is discharged from its maximum rated working voltage to zero volts fully discharged condition
- **Peak Power Density** – measurement of the instantaneous power from full rated voltage V_R to $V_R^2/4R_{AC}$ where R_{AC} is the AC resistance. This value does not represent the sustainable power.
- **Power density** – gravimetric power density calculated between the ranges of a 20% to 40% voltage drop from the rated voltage of SC.

- **Life Time** – expected performance change for the super capacitor if held at rated voltage and 25°C for 10 years.
- **Cycle Life** – expected performance change after cycling half to one million times from rated voltage to half the rated voltage. Cycling is to be performed at a duty cycle resulting in no heating of the super capacitor with the SC maintained at 25°C.

2.1.4 SUPER CAPACITOR AS A CIRCUIT ELEMENT

The circuit schematic in Figure 2.4 represents the first-order model for a super capacitor. It is comprised of four ideal circuit elements, which include a capacitance C, a series resistor R_S, a parallel resistor R_P, and a series inductor L. R_S is called the equivalent series resistance (ESR) and contribute to energy loss during capacitor charging and discharging. R_P simulates the energy loss due to capacitor self-discharge. It is often referred to as the leakage current resistance. Inductor L results primarily from the physical construction of capacitor and is usually small. However, it cannot be neglected in many applications, particularly those operating at high frequencies or subjected to hard switching.

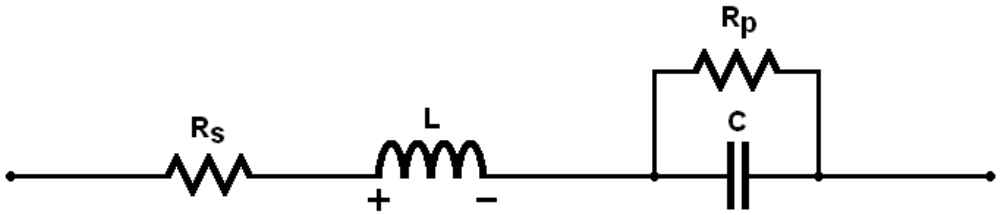


Figure 2.4: The first-order circuit model of a super capacitor

Resistor R_P is always much higher than R_S in practical capacitors. Thus it can often be neglected, particularly in high-power applications. In that case, the impedance of the first-order circuit model Z is:

$$Z = R + i(2\pi fL - \frac{1}{2\pi fC}) \quad (8)$$

The impedance is purely resistive when $2\pi fL - \frac{1}{2\pi fC} = 0$, or $f = \frac{1}{2\pi\sqrt{LC}}$.

This particular frequency f is referred to as the resonance frequency of the super capacitor. Thus, the impedance of circuit is simply the resistance at self-resonance. However, SCs exhibit non-ideal behavior, which result primarily from the porous material used to form the electrodes that causes the resistance and capacitance to be distributed such that the electrical response mimics more of a

transmission line like behavior. The various parameters in this ladder circuit approximation; L, Rp,R_1, R_2,...R_n,C_1, C_2,…C_n can be derived by using the nonlinear least-squares fitting algorithm.Therefore, it would be more suitable to use a more generalized circuit as shown in Figure 2.5 for representing a more realistic electrical response of an SC.

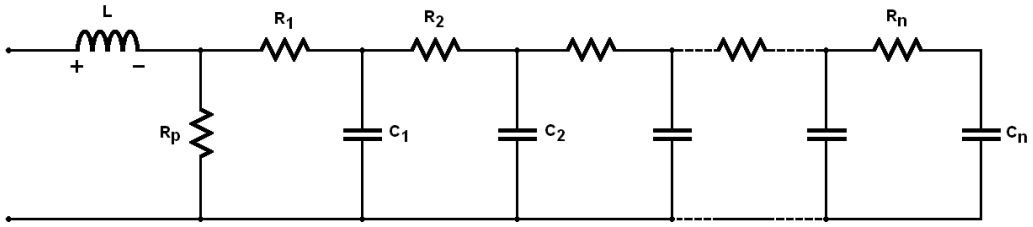


Figure 2.5: The transmission line model equivalent circuit of an SC

2.1.5 CHARGING AND DISCHARGING OF SUPER CAPACITORS

Charging of SCs is simple while at the same time may present some unique challenges. Unlike batteries, SCs may be charged and discharged at similar rates. An SC with zero charge looks like a short circuit to the charging source. So day-to-day power supplies which fold back the output current in response to a perceived short circuit are not suitable for charging SCs.

A DC-to-DC constant current regulator is the simplest form of active charging for an SC. The power losses due to SC heating are proportional to current squared times the duty cycle of the converter.

When charge time is critical, constant power charging provides the solution for the fastest charging. Constant power charging can transfer all the available power from the charging source onto the SC.

The graph in Figure 2.6 courtesy of Maxwell Technologies shows the charging characteristics for a 100F/50V super capacitor module in constant current and constant power charging topologies. In constant current mode, the module is charged from a 50 V, 20 amp power supply. In the constant power mode, it is charged at a constant power of 1000 watts with a voltage limiter of 50v. The constant 20 amp charge current required 250 seconds to charge the module to 50 volts while the 1000 watt constant power charger required 145 seconds to charge the module to 50 volts.

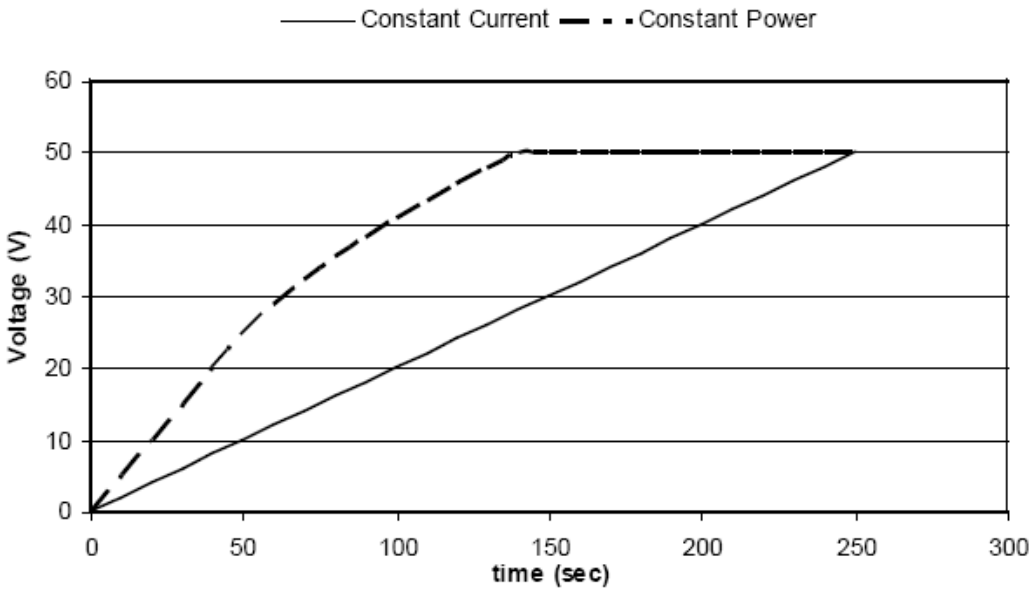


Figure 2.6: Constant current vs. constant power charging of a super capacitor (Maxwell Technologies, 2005)

The setup shown in Figure 2.7 was used for timing the charging and discharging characteristics of the 21.6v/81.25F super capacitor module that is employed in the SRUPS.

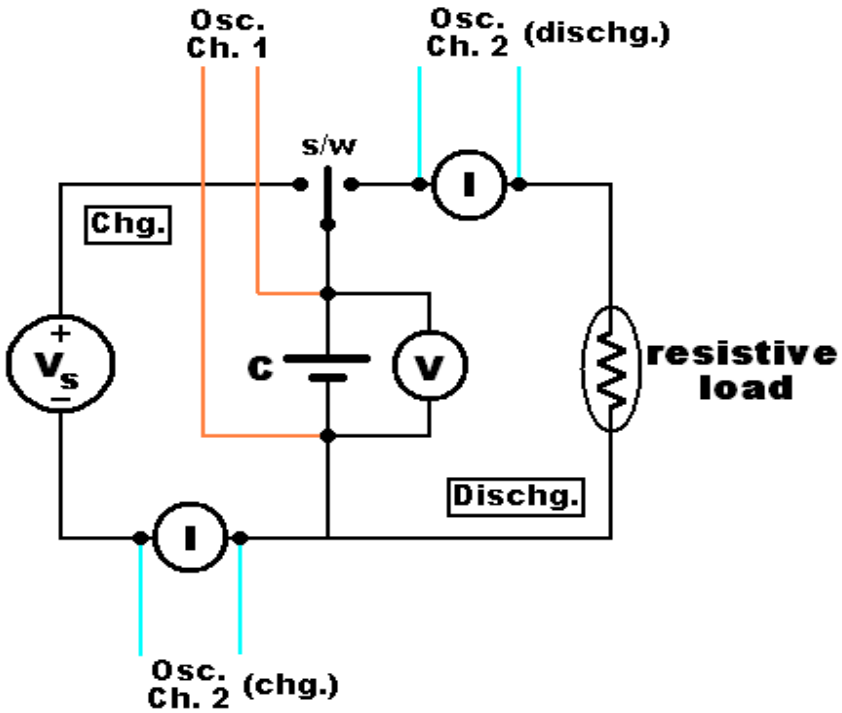


Figure 2.7: Setup for testing charging/discharging characteristics of SC

The constant current charging circuit used in the charger section of the SRUPS was employed to perform the charging. This charger is a 15A constant current charger with a voltage limiter set at 21.6V. For a constant current charger, the

momentary increase in voltage with respect to time (ΔV/Δt) is a constant. When Q denotes the charge, C is the capacitance and I is the current, ΔQ = I x Δt and ΔV = ΔQ / C, we get

$$\frac{\Delta V}{\Delta t} = \frac{I}{C} \tag{9}$$

The time taken for a capacitor to charge from 0 to 63% of its rated voltage is called the capacitor time constant τ. When R and C is the corresponding total resistance and capacitance of the charging circuit where V_S is the source voltage, τ is equated as

$$\tau = R \times C \tag{10}$$

and the capacitor voltage during charging V_C is derived as

$$V_C = V_S(1 - e^{-t/RC}) \tag{11}$$

From this equation, the charge time t_r required for charging the capacitor to .99 V_S is found to be $t_r = 5$ RC.

The discharge characteristics of super capacitors are similar to the charging curves. The voltage of the capacitor V_C discharging through a resistor from an initial voltage of V_i follows the equation derived the same way as equation (11).

$$V_C = V_i(e^{-t/RC}) \tag{12}$$

The discharge test was performed using a resistive load and not a constant current sink load. The load was a wire wound rheostat set at 0.9Ω to mimic a 200w load that draws 15A, which is the same as the current limit on the charger. The fully charged 81.25F SC module at 21.6V was discharged to 0V for the test.

Shown below in Figures 2.8 and 2.9 are the oscilloscope screenshots for the charge and discharge tests.

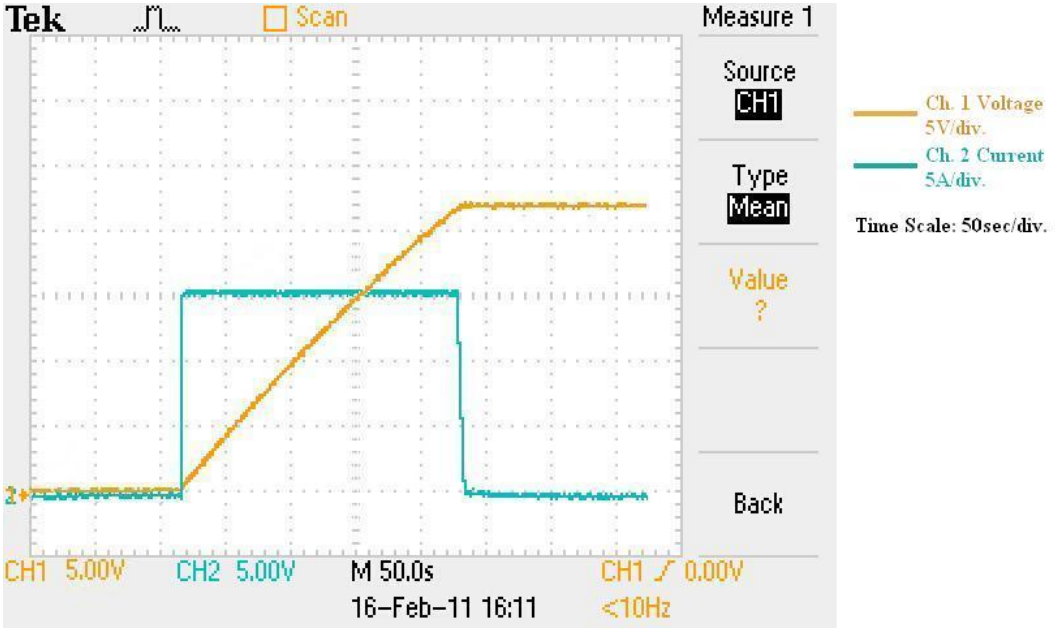


Figure 2.8: Oscilloscope screenshot of constant current charging of SC bank

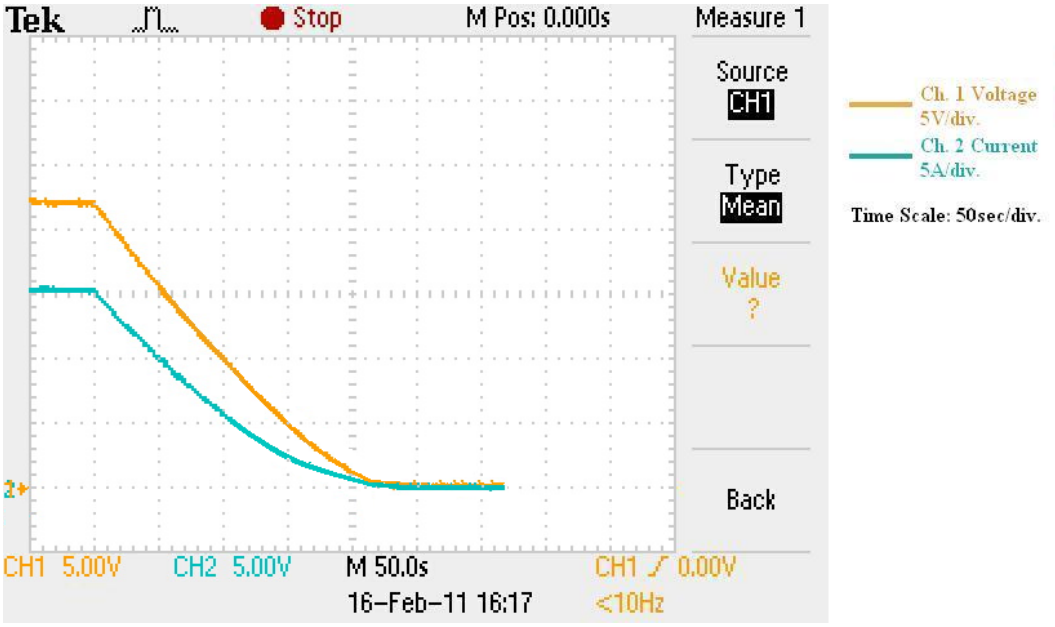


Figure 2.9: Oscilloscope screenshot of SC bank discharging through a resistive load

The tests conducted on the 21.6V / 81.25F super capacitor bank showed that constant current charging at from 0V to full rated voltage at 15A took ~210 seconds while discharging through a 200W resistive load from full rated voltage to 0V took ~215 seconds which are more or less similar.

2.1.6 VOLTAGE EQUALIZATION IN SERIES CONNECTED SUPER CAPACITORS

Many system applications require that capacitors be connected together, in series and/or parallel combinations, to form a "bank" with a specific voltage and capacitance rating as their voltage ratings are generally low. Because sustained over voltage can cause an SC to fail, the voltage across each cell in a series stack must not exceed the maximum continuous working voltage rating of individual cells in the stack. Provisions for either reducing the "rate of charge" being delivered to a cell, or to completely stop charging a cell whose voltage approaches its surge voltage rating should be made. The easiest way to reduce the current that is charging an SC cell is to divert some of it around the cell. One such method employs a passive bypass component. The other, more complicated procedure uses an active bypass circuit. After the stack has been held at a voltage for a period of time, voltage distribution becomes a function of internal parallel resistance. The cells with higher leakage current would have lower cell voltages, and vice versa in a series stack of SCs. One technique to compensate for variations in parallel resistance is to place a bypass resistor in parallel with each cell, sized to dominate the total cell leakage current. This effectively reduces the variation of equivalent parallel resistance between the cells. The active balancing circuit has an active switching device, like a bipolar transistor or a MOSFET, connected in series with each bypass element ladder. The switches are controlled by voltage-detection circuits that only turn a switch "on" when the voltage across that particular cell approaches a value just slightly below the continuous working voltage rating of the cell. This is called the bypass threshold voltage. Figure 2.10 depicts a typical block diagram of an active charging-current diversion circuit.

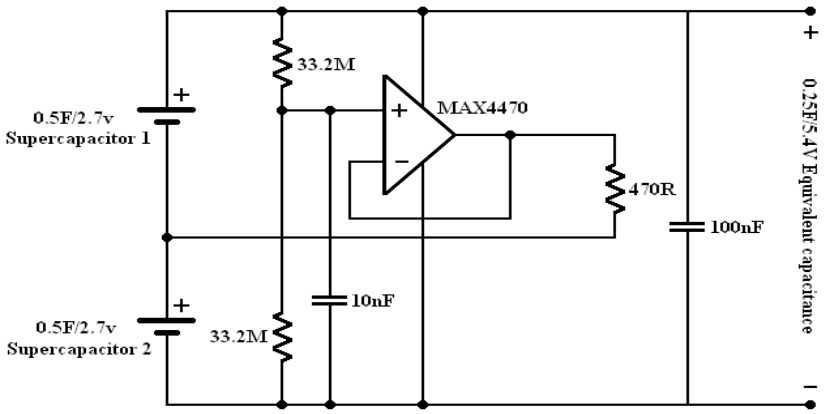


Figure 2.10: Active voltage balancing circuit for super capacitors (Cap-XX Limited, 2008)

2.2 TRANSIENTS AND SURGES

The trend towards even smaller components and ever lower signal levels increases the susceptibility of electronic circuits to interference due to electrostatic disturbance. Electronic systems and circuits containing integrated circuits (IC) are sensitive to overvoltage transients such as ESD (electrostatic discharge) pulses. These pulses can enter an electrical device when the device port is touched or its connector is removed. Ports and connectors are probably the most common routes through which an ESD pulse can be introduced into a device. The pulse travels through the connector to the printed circuit board. It then propagates down the data and/or supply lines to the components on the board. Without sufficient protection, these components may become inoperable or even be destroyed.

Disturbances that electronic equipments have to be protected from can be broadly classified into three.

- Transients
- Noise and harmonics
- Voltage fluctuations

Voltage fluctuations mainly comprise of increase or decrease in the utility mains (root mean square) RMS voltage levels. They can be either momentary fluctuations that typically last from about 15 milliseconds to half a second in which case an over voltage is called a surge while an under voltage is called a sag, or if they last more than two seconds they are just referred to as over or under voltages. Under voltage situations cause brown-outs whereas a total power supply failure is termed a blackout.

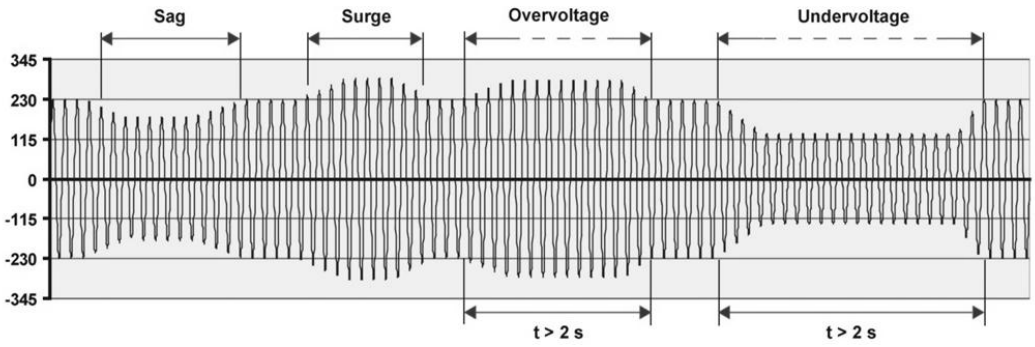


Figure 2.11: Waveform representation of surge, sag, overvoltage and under voltage conditions

Noise disturbances may be caused by radio frequency interferences (RFI) or electro-magnetic interferences (EMI). These are high frequency elements in the order or kilohertz and megahertz at which conditions these are picked up by power lines, as transmission lines tend to act as antennas in this frequency spectrum. Noise usually is not critical is a strictly electrical sense, but can cause severe data malfunctions in electronic or magnetic data storage media.

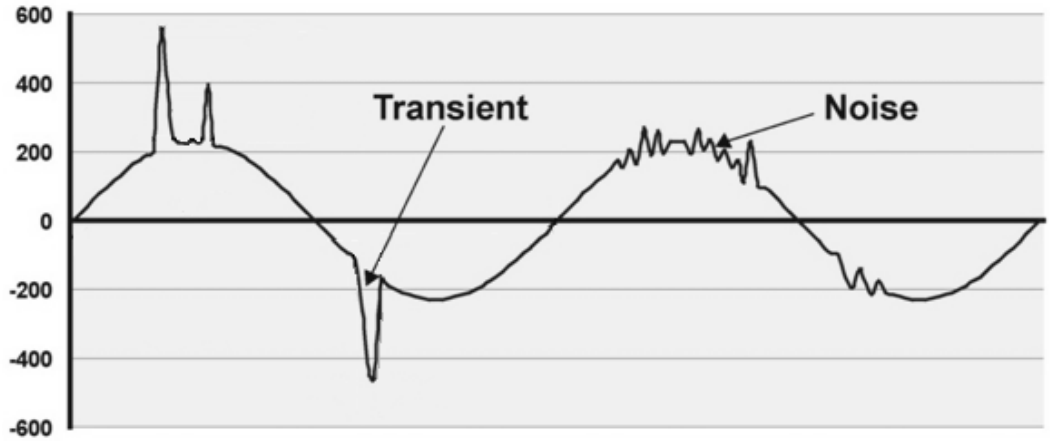


Figure 2.12: Waveform representation of transients and noise on a power line

Harmonics are currents or voltages with frequencies that are integer multiples of the fundamental power frequency. They are generally the result of operation of non-linear loads on the utility power by end users which draw current in a non-sinusoidal fashion from the power line. In such situations when there are distortions in the current and voltage waveforms, harmonics are injected back into the power line. Major causes of harmonic distortions are switched-mode power supplies using DC rectification and adjustable-speed drives. To counter this, standards and specifications laid out by authoritative agencies require active power factor correction in these systems so that current and voltage drawn are linearized with the intention that harmonic injection into the power line is kept to a minimum. Harmonics usually cause data corruption, false tripping of circuit breakers and general computer and telecom system down-times.

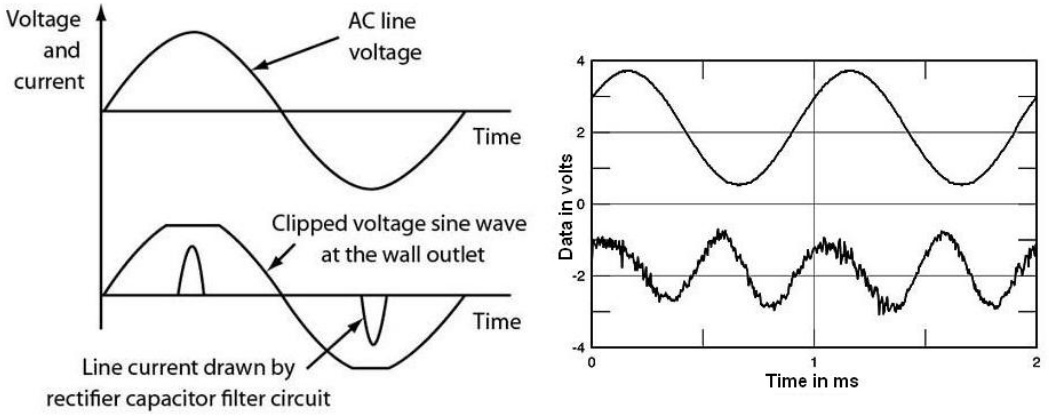


Figure 2.13: Harmonics generated non-linear loads

Transients are very sharp fluctuations that are formed in the power supply waveform. These have the appearance of spikes. Although there isn't an exact definition for a transient voltage surge (TVS), it can be considered a transient with voltage levels greater than 2000V and current levels greater than 100 ampere. It is not uncommon for the voltage levels to be 15kV to 20kV in amplitude and the current surge to exceed 2000Ampere. The IEEE and ANSI standards groups have defined two wave forms which are used to evaluate open circuit (voltage) and short circuit (current) transients. The voltage waveform is 1.2x50µsec, and the current waveform is 8x20µsec. These numbers indicate the rise time and duration of the waveform. Therefore, the rise time for the voltage waveform is 1.2µsec to the peak voltage and the duration to 50% of the wave form is 50µsec and for the current waveform the rise time to reach peak current is 8µsec and the time taken to reach 50% of the waveform is 20µsec.

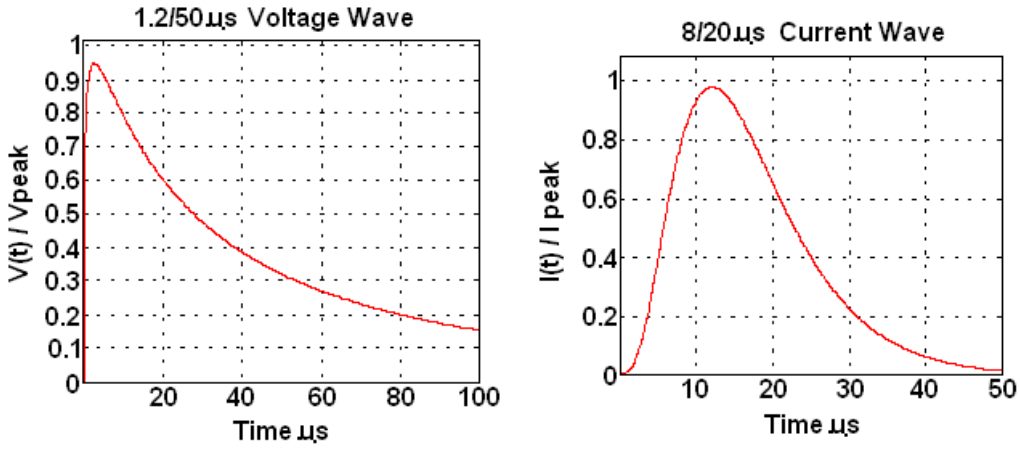


Figure 2.14: Voltage and current surge waveforms

Transient voltage surges are usually caused by:

a) Switching of lighting and the starting and stopping of motors.
b) Electrical fault conditions (equipment failure which passes high currents to ground or from phase to phase).
c) Power failure and the subsequent return of power.
d) Lightning strikes that hit the electrical system in your nearby geographical area.
e) Lightning strikes that induce transients through radiation of electromagnetic fields (without hitting the electrical system).

Peak current for lightning strikes generally range from 2000 to 400,000 amps. The strongest strikes for three phase systems will induce currents of up to 320,000 amps per phase and up to 1,200,000 amps total.

Typically used transient voltage surge suppression (TVSS) devices are gas discharge tubes (GDT), metal oxide varistors (MOV), silicon avalanche breakdown diodes or combinations of these devices in order to aid in protecting electrical equipment from power line surges.

Each of these TVSS elements has its own strengths and weaknesses:

- The GDT can handle very large voltage (~20kV) and current (~2500A) surges, but relatively speaking is slow (~1µsec) in responding to a transient surge.
- The MOV is very fast (~50nsec) responding, but has difficulties with large (~100Amp) currents which shorten the life cycle of the MOV.
- Silicon avalanche breakdown devices are fast (~1nsec) and can handle large (~1000Amp) currents, but are susceptible to dv/dt (instantaneous rate of change of voltage with time) and peak voltage failure modes.
- Other combinational products may use resistors, capacitors and/or SCRs in conjunction with these TVSS elements, which make them prone to the respective failure characteristics.
- Choke coils are inductors designed to block higher frequencies in an electrical transmission line. They use their property of self inductance to

attenuate electromagnetic interference and radio frequency interference from power supply lines

In some cases, MOVs and GDTs are connected in series or parallel as a single package that forms a device which has the speed of the MOV and the current handling capability of the GDT.

Manufacturers usually stack different types of clamping components across the power line in the hope that if one fails to clamp then the others might take over the clamping. Unfortunately, the device with the lowest clamping voltage will conduct all the current while the higher voltage devices will sit idle unless the lower voltage device blows out. This is why most surge protection units have low amperage fuses to blow out when such a situation arises.

Figure 2.15: Transient surge suppression devices

Given below are some of the criterions that should be taken into consideration while selecting a transient voltage surge suppression (TVSS) product:

- What Voltage levels of TVSS are expected?
- What Current levels of TVSS are expected?
- Will a high potential test need to be performed on the system?
- What type of life expectancy is required of the protection device?
- Does the system require other noise protection as well as TVSS?

The following are the major ratings used to describe TVSS devices**:**

- Joules - indicates the amount of energy that the suppressor can dissipate. If the incoming energy exceeds the suppressor's ability to dissipate, the suppressor will be damaged and the excess energy will be passed to the protected equipment.

- Peak Surge Current in Amperes - maximum current allowed to pass without damage to the suppressor for a single standard test impulse. Surge currents exceeding that value will be passed to the protected equipment.
- Peak Let-Through Voltage - The true effectiveness of a suppressor is given by the Let-Through Voltage rating, which is the maximum peak voltage of a transient that is allowed to pass on to the protected equipment by the suppressor. The rating gives the peak voltage that occurs within 100 microseconds following the application of a test impulse. It is the maximum voltage to which the protected equipment will be exposed due to the transient.

The Category B Impulse Test as defined by ANSI/IEEE C62.41 is the most widely used test standard for testing TVSS devices. It includes a 6000 volt, 3000 amp pulse which will rise to 90% of its peak voltage in 1.2 microseconds and will fall to 50% of peak in 20 microseconds.

2.2.1 PROPAGATION MODES FOR TRANSIENTS AND NOISE

Power line disturbances, namely transients and electrical noise can propagate through the power line as a super-imposition on the utility voltage. This happens in two modes, that is differential mode and common mode. Consider a three wire single phase AC mains utility line. The three wires consist of the two supply wires which are the line or live and the neutral; and the third wire which is the ground or earth. Any transient or noise appearing between the two supply lines, that is, when the wire-to-wire voltage is compromised, is termed normal mode or differential mode. A common mode transient occurs when the voltage differential appears between the ground and either of the two supply lines.

According to IEEE/ANSI Standard C62.41-1991, the worst normal mode surge expected inside a building is a 6,000V, 3,000A, 90 joule (J) combination wave. A normal mode surge is one that occurs between the hot (line) and neutral wires. This standard also states that the worst common mode surge — referred to in the standard as neutral-ground mode — is only found far from the service entrance and is a very weak 3,000V, 100A, 0.645J ring wave. This worst-case common-mode surge is already about nine times smaller than the suppressed surge left over

after typical suppression, also referred to as the let-through surge. Component audio and video systems are interconnected by cables that, for safety reasons, are often connected in some way to the electrical ground wire circuit. Their signals can be degraded by even mill volts of noise. On the other hand, computer systems may be able to tolerate several volts of noise on the ground system and continue to operate without problems

Most switch-mode power supplies, as used in most modern equipment, are inherently immune to common-mode surges and noise, due principally to the high-frequency transformers and filters used in these supplies. Hence, due to their relatively weak nature, common-mode surges do not deserve much attention and protection from differential or normal mode surges take higher priority. Surge protectors which have TVSS devices between live, neutral and ground divert energy to both neutral and ground, and will contaminate both the neutral and the ground wires. The safety ground is the same as the equipment chassis and system ground, and surges diverted to ground will allow energy to flow in chasses and cables that join interconnected equipment. Dumping surge energy onto the system ground instead of blocking and containing it can result in high-voltage energy travelling along interconnecting cables and causing permanent damage to input or output stages. Surge protectors which have TVSS devices only between live and neutral divert energy only to neutral and do not contaminate the ground wire, but they are also not effective at completely protecting equipment. Not having any shunt devices to ground, they allow live and neutral to float with respect to chassis ground up to dangerously high voltage levels during a surge event. In technical terms they convert normal mode surges to common-mode surges. Common-mode surges are normally only found at low, harmless levels on branch circuits, but when generated by such a piece of equipment they can be large and damaging. Common-mode filters often have capacitors from live and neutral to ground and these capacitors will be blown out by the large common-mode surges that are generated in these situations. Figures 2.19 and 2.20 shows oscilloscope screenshots of differential mode and common mode surges.

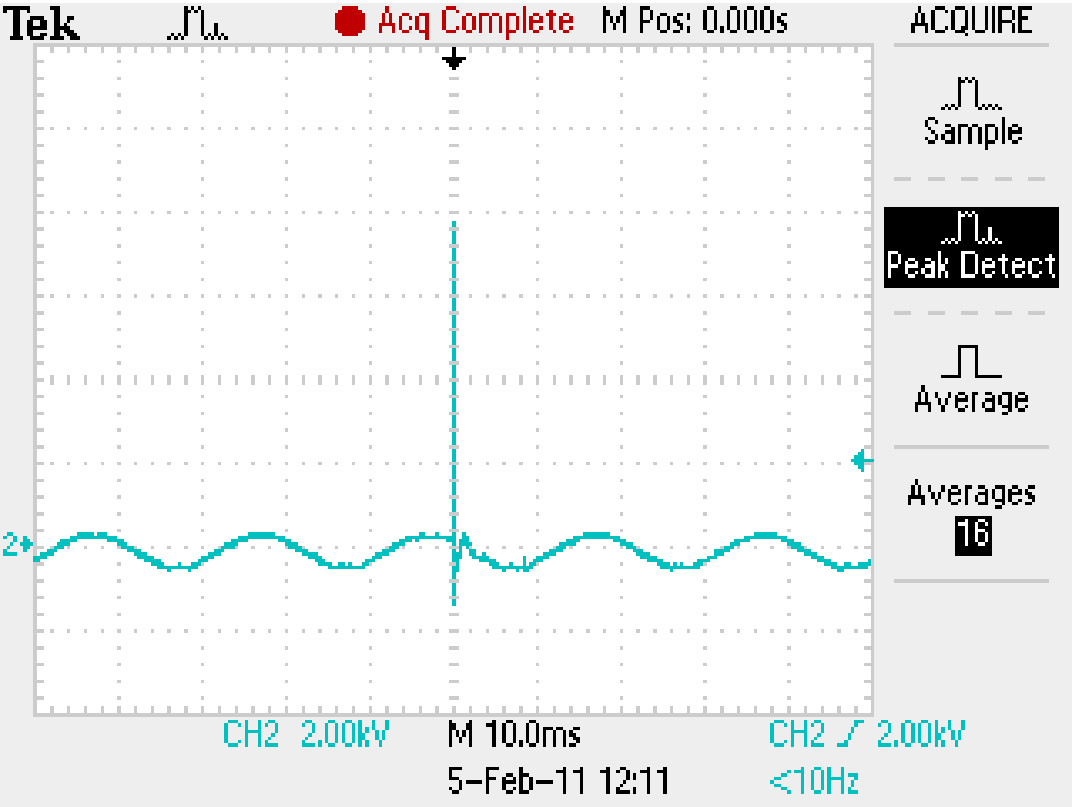


Figure 2.19: 6.8KV differential-mode surge measured between Line and Neutral wires

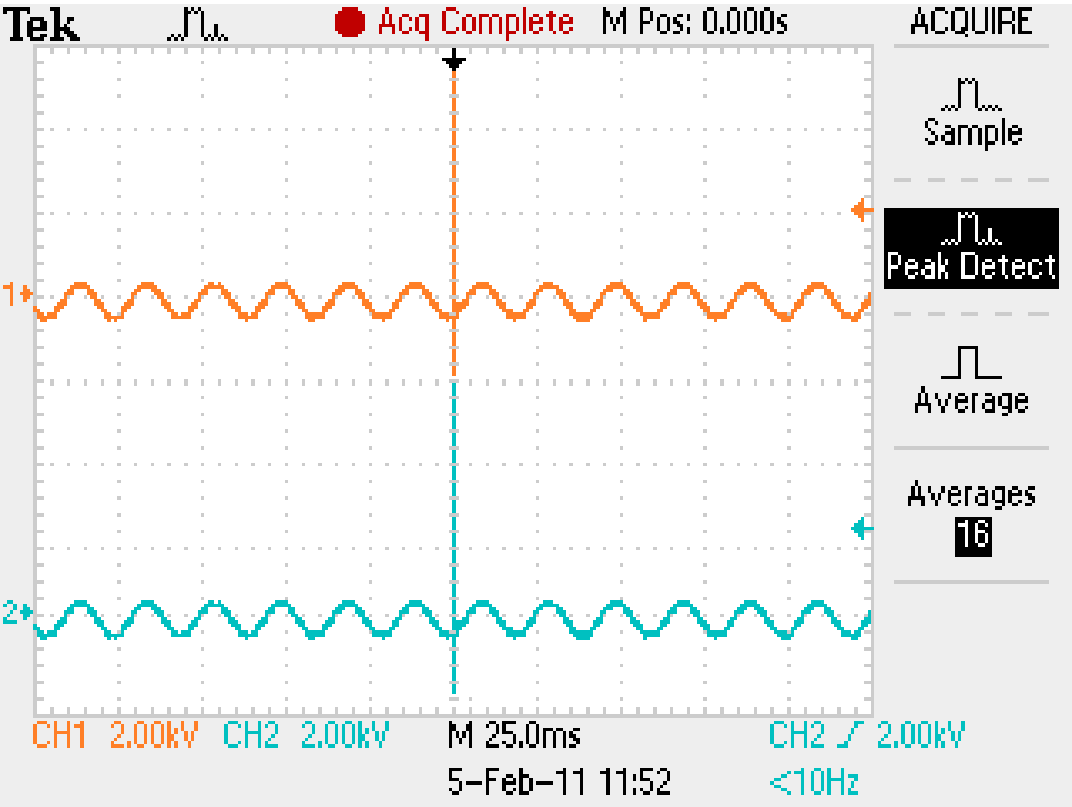


Figure 2.20: 6KV common-mode surge measured between Line/Neutral wires with respect to Ground wire

2.2.2 TRANSIENT IMMUNITY STANDARDS

Both IEC 1000-4-5: 1995 "Surge Immunity Test" and IEEE C62.41-1991 "IEEE Recommended Practice on Surge Voltages in Low-Voltage AC Power Circuits" define a "1.2/50µs - 8/20µs combination wave" surge which has a 1.2µs voltage rise time with a 50µs decay across an open circuit. The specified current waveform has an 8µs rise time with 20µs decay into a short circuit. Open circuit voltages levels from 1 to 6kV are commonly used in both the positive and negative polarities, although, under some circumstances, voltages as high as 20kV may be applied.

The InternationalElectrotechnical Commission (IEC), a worldwide organization promoting international cooperation on questions concerning standardization in electrical & electronic fields, has developed transient immunity standards which have become minimum requirements for manufacturers. Three of the IEC standards that deal with transient immunity are:

- IEC 61000-4-2 : Electrostatic Discharge (ESD)
- IEC 61000-4-4 : Electrical Fast Transient/Burst (EFT)
- IEC 61000-4-5 : Surge Immunity

2.2.2.1 IEC 61000-4-2: ELECTROSTATIC DISCHARGE (ESD) STANDARD

IEC 61000-4-2 addresses one of the most common forms of transients in electronic systems; electrostatic discharge (ESD). ESD results from conditions which allow the build up of electrical charge from contact and separation of two non-conductive materials. When the charged body is brought in proximity of another object of lower potential, energy is released in the form of electrostatic discharge. The standard defines immunity requirements for ESD which can be coupled into the equipment directly or through radiation. IEC 61000-4-2 also specifies the ESD current waveform and parameters shown in Figure 2.18. The rise time is extremely fast, defined as 0.7 to 1ns, with a second peak at 30ns and a total duration of only 60ns. The total energy contained within the pulse is approximately a few hundred micro joules.

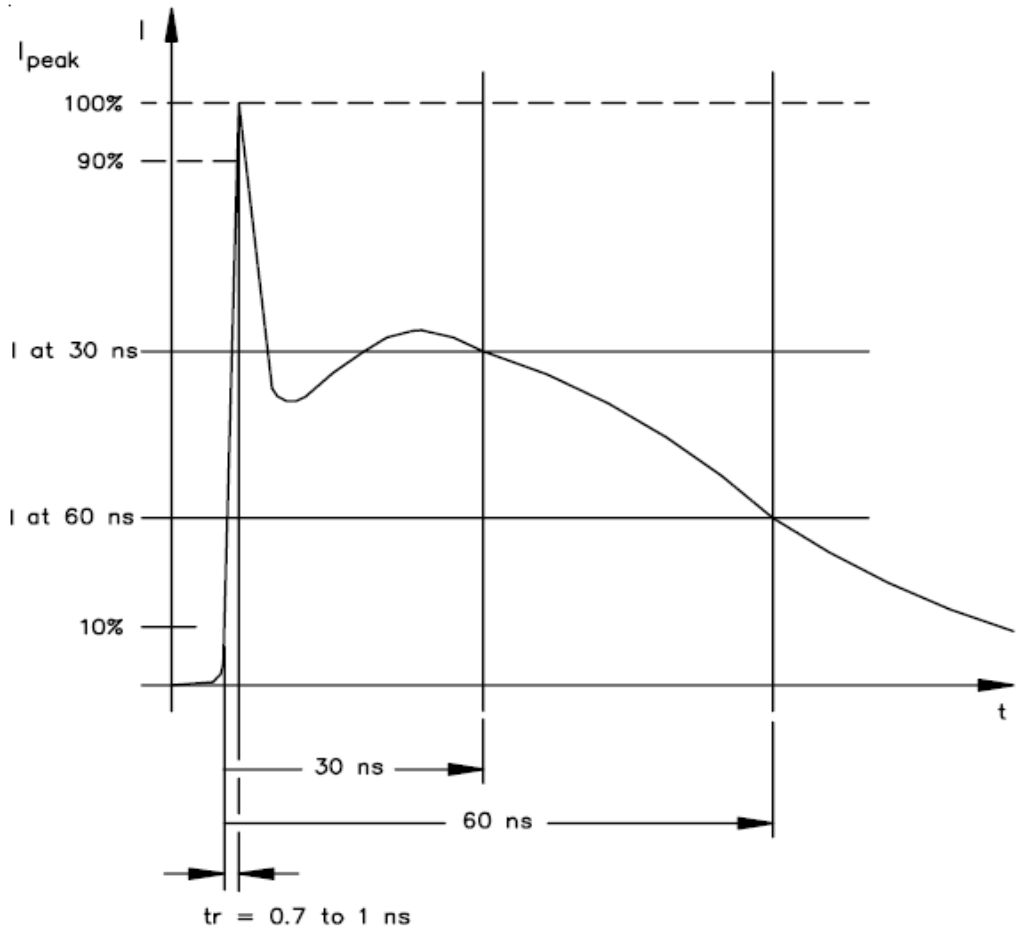


Figure 2.18: ESD Waveform

2.2.2.2 IEC 61000-4-4: ELECTRICAL FAST TRANSIENT/BURST (EFT) STANDARD

Electrical fast transients occur as a result of arcing contacts in switches and relays. EFT disturbances are common in industrial environments where electromechanical switches are used to connect and disconnect inductive loads. IEC 61000-4-4 specifies the EFT threat in both power and data lines. The electrical fast transient is described in terms of a voltage across a 50Ω load from a generator having a nominal dynamic source impedance of 50Ω. The output occurs as a burst of high voltage spikes at a repetition rate ranging from 2 KHz to 5 KHz. The burst length is defined as 15ms with bursts repeated every 300ms. Each individual burst pulse is a double exponential waveform with a rise time of 5ns and a total duration of 50ns. A diagram showing the EFT waveform and the EFT burst repetition rate and burst period is shown in Figure 2.19.

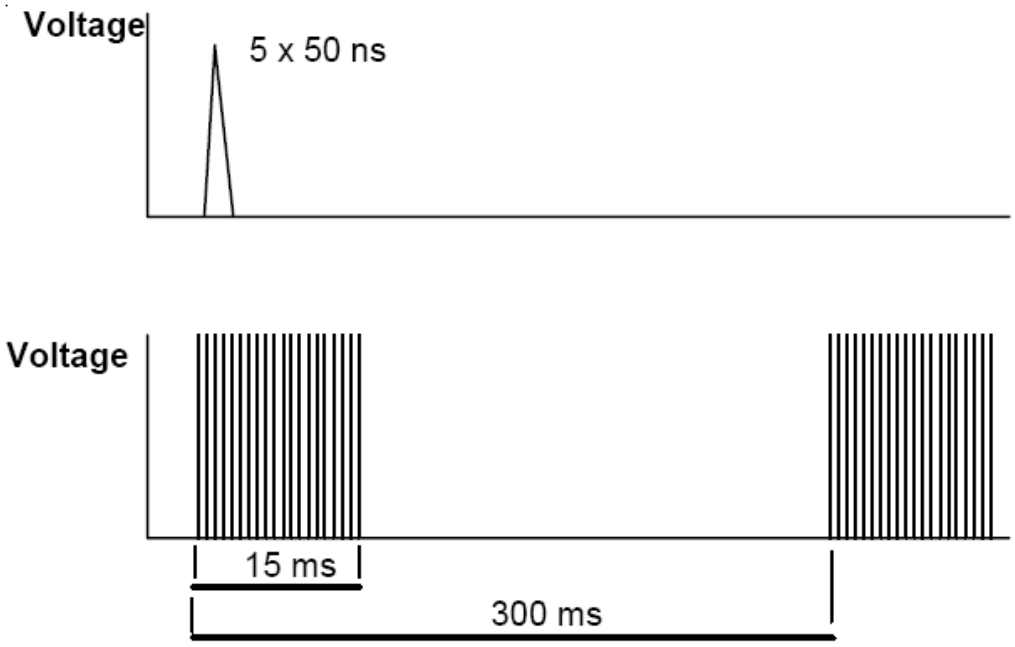


Figure 2.19: EFT burst waveform, repetition rate and burst period

2.2.2.3 IEC 61000-4-5: SURGE STANDARD

IEC 61000-4-5 addresses the most severe transient conditions on both power and data lines. These are transients caused by lightning strikes and switching. Switching transients may be the result of power system switching, load changes in power distribution systems, or short circuit fault conditions. Lightning transients may result from a direct strike or induced voltages and currents due to an indirect strike. The IEC 61000-4-5 standard defines a transient entry point and a set of installation conditions. The transient is defined in terms of a generator producing a given waveform and having specified open circuit voltage and source impedance. Two surge waveforms are specified: the 1.2x50μs open-circuit voltage waveform and the 8x20μs short-circuit current waveform; Figures2.20 and 2.21 respectively.

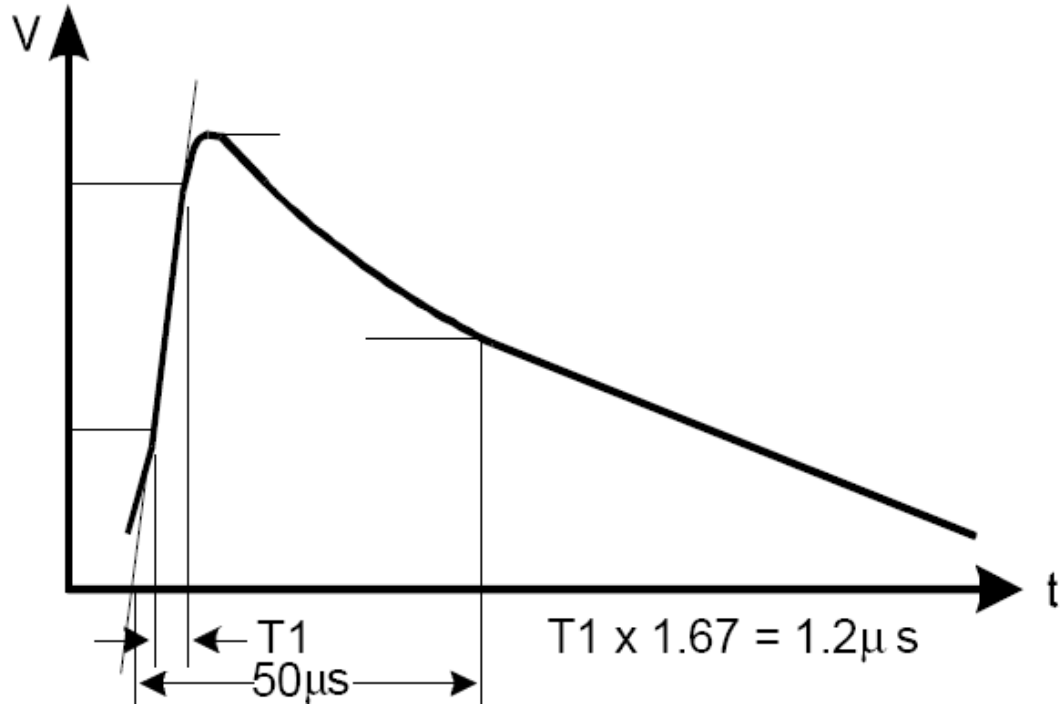


Figure 2.20: IEC 61000-4-5 Voltage impulse waveform

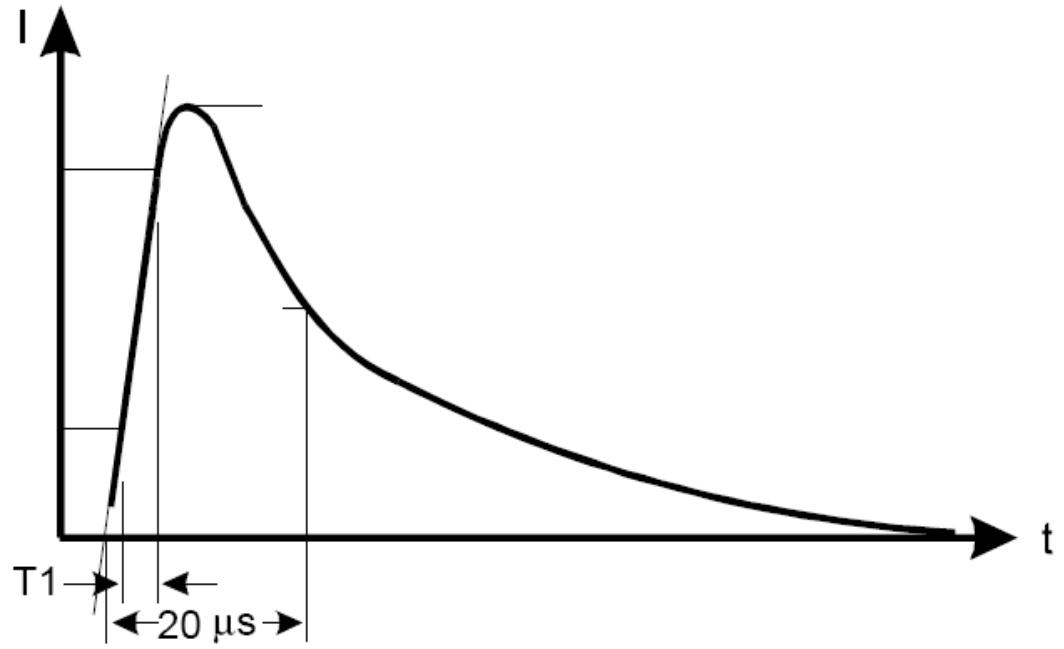


Figure 2.21: IEC 61000-4-5 current impulse waveform

2.2.3 Lightning Surge Simulator

A lightning surge simulator or LSS is used to test the surge resistance capabilities of electronic and electric circuits and components. It is basically a high voltage pulse generator that can produce high current and voltage surges which correspond to stipulations specified by the IEC/IEEE surge testing and measurement strategies. The LSS used for testing purposes in this research project

is the NoiseKen LSS-6110 that is capable of generating voltage-current combination wave surges as specified in the IEC6100-4-5 standards. Figure 2.22 shows the oscilloscope screenshot of the 6.6KV voltage surge waveform used in carrying out the surge tests.

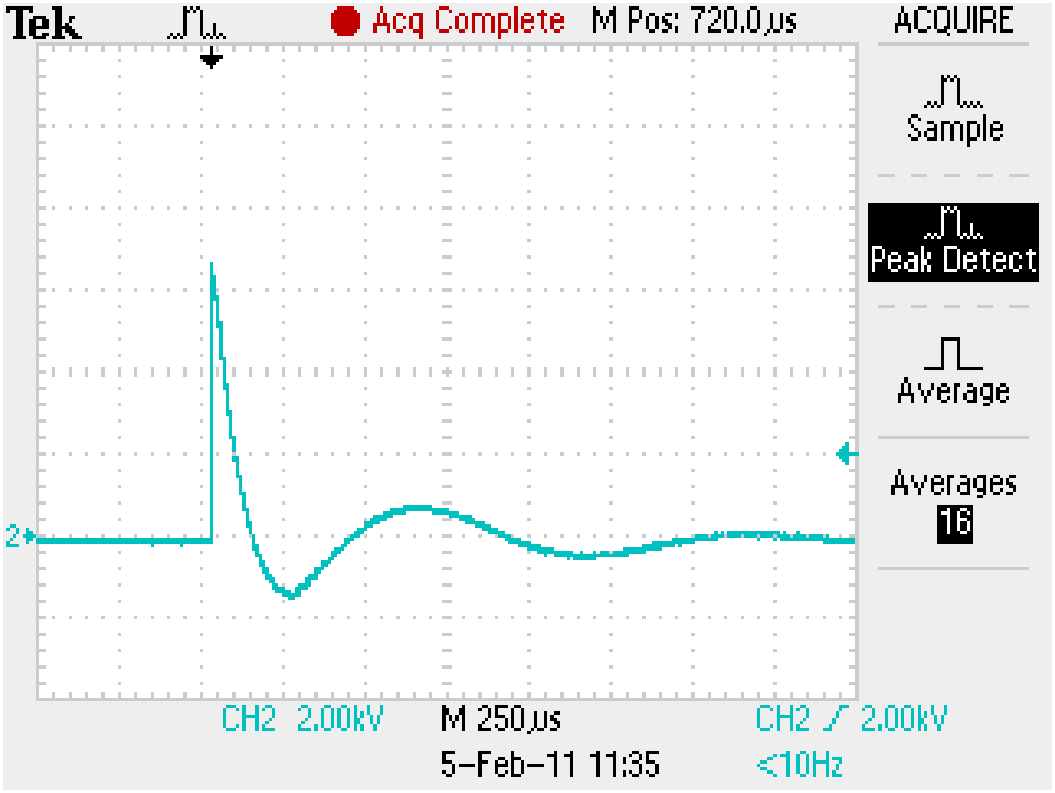


Figure 2.22: 6.6KV voltage surge generated by the NoiseKen LSS-6110

Figure 2.23 gives a basic understanding into the surge generator circuit that is employed inside an LSS.

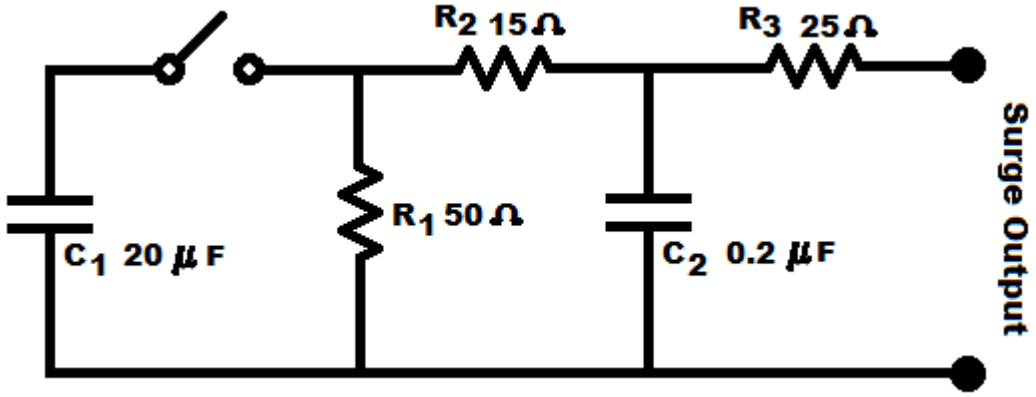


Figure 2.23: Basic surge generator circuit

The surge generator can generate a high voltage surge when it is in open circuit Figure 2.24 shows the parameters of the 12/50µs voltage surge generated by the surge generation circuit when configured in open circuit mode.

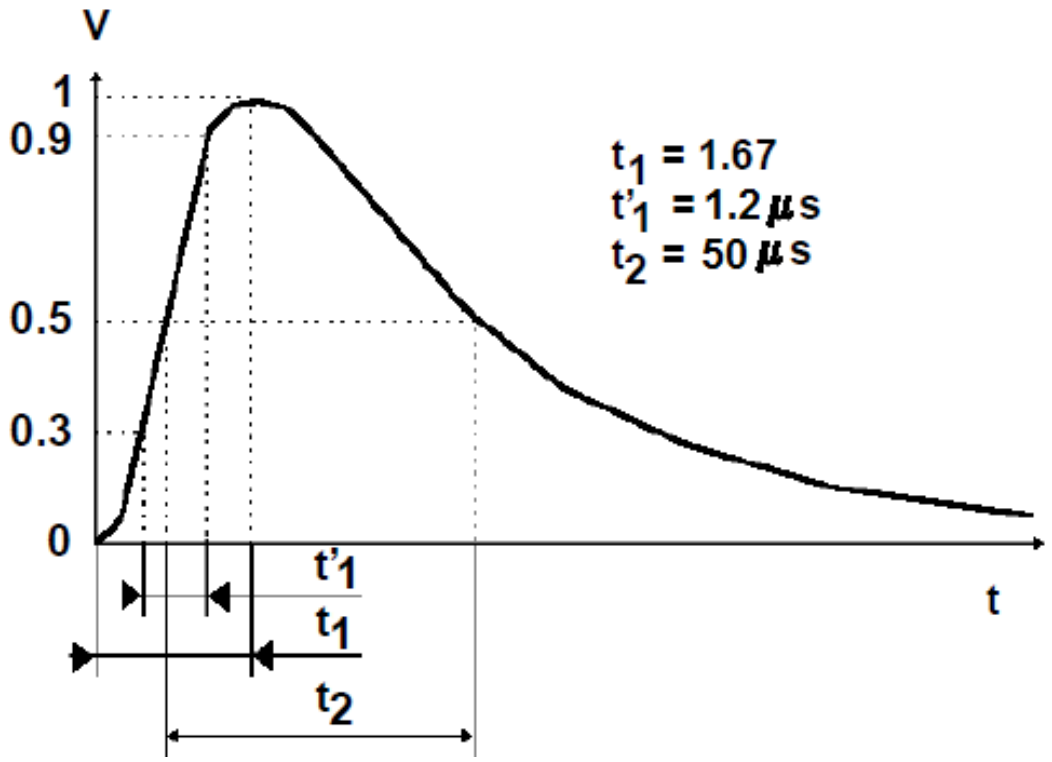


Figure 2.24: Voltage surge waveform parameters

The equation for the rise time of the voltage surge waveform is as follows:

$$v(t) = V_p (1 - \exp(-t/T))$$

$$\Rightarrow t = -T \log n (1 - (v(t)/V_p)) \quad (13)$$

In this case the time constant T is essentially due to R_2 and C_2 and hence T may be estimated as :

$$T = R_2 * C_2$$

So $t_{(0.3)}$ and $t_{(0.9)}$ will be calculated respectively with $v(t)/V_p=0.3$ and $v(t)/V_p= 0.9$ where $t_{(0.3)} = 0.1$ µs $t_{(0.9)} = 0.8$ µs and so

$$t_1 = 1.67 (t_{(0.9)} - t_{(0.3)})$$

$$t_1 = 1.169\mu s \approx 1.2\mu s$$

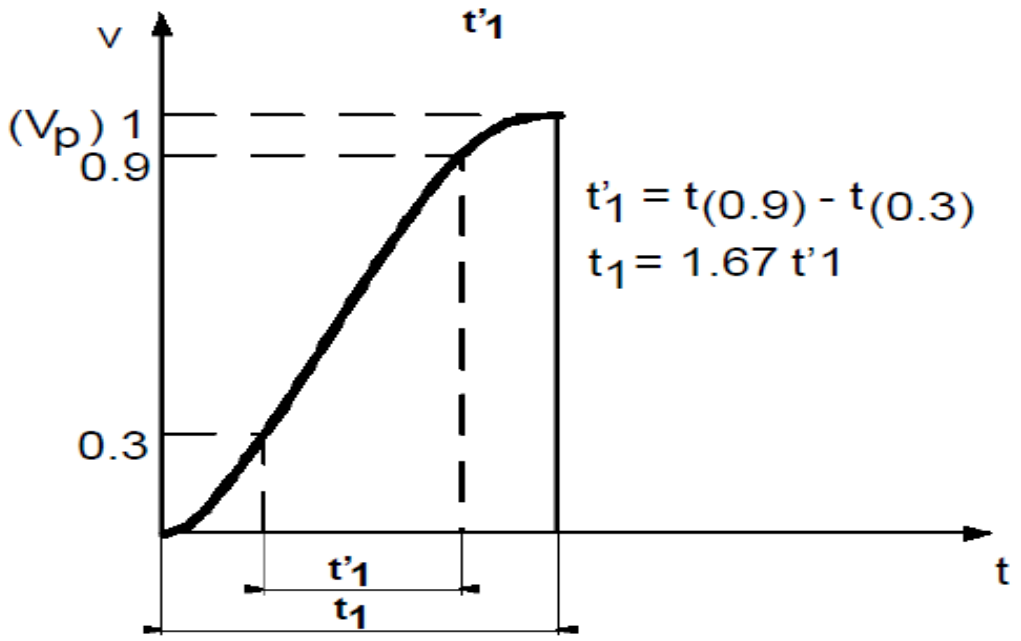


Figure 2.25: Rise time parameters for voltage surge waveform

The equation for the voltage surge duration curve can be represented as

$$v(t) = V_p \exp(-t/T)$$

$$\Rightarrow t = -T \log n\,(v(t)/V_p) \qquad (14)$$

In this case the time constant T is essentially due to R_1 and C_1 and hence T may be estimated as :

$$T = R_1 * C_1$$

So t_2 will be calculated with $v(t)/V_p = 0.5$ and so

$$t_2 = 49.3\mu s \approx 50\mu s$$

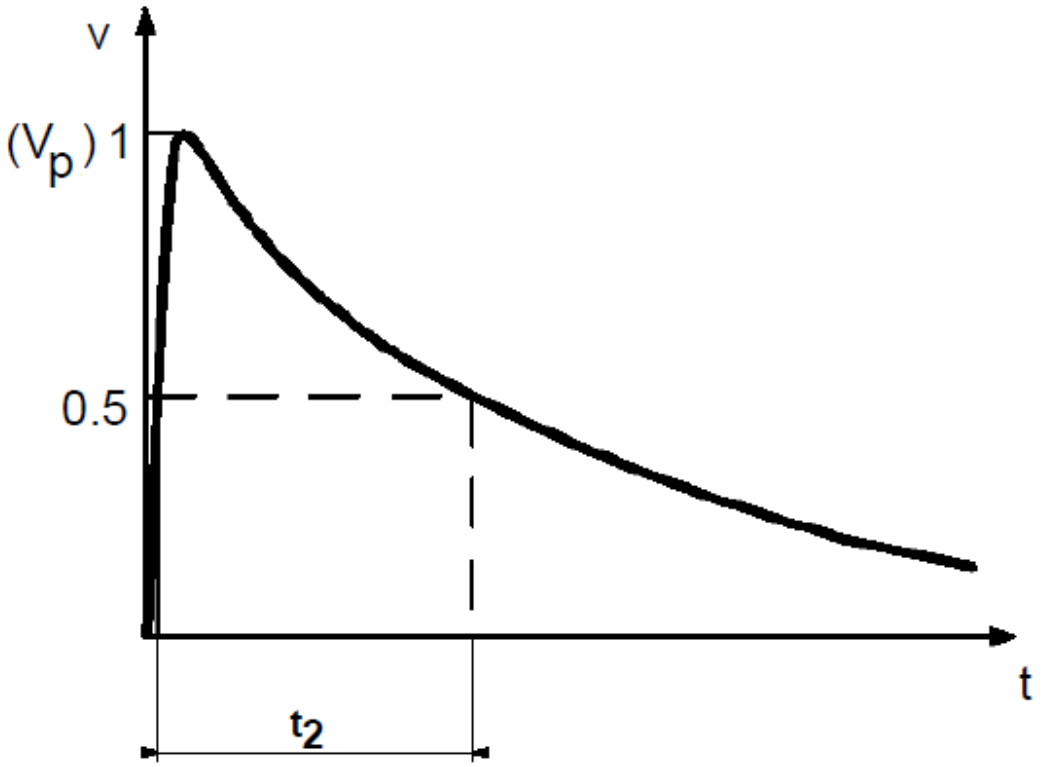


Figure 2.26: Current surge duration waveform

The surge generator can generate a high current surge when its output is short circuited as shown in Figure 2.27.

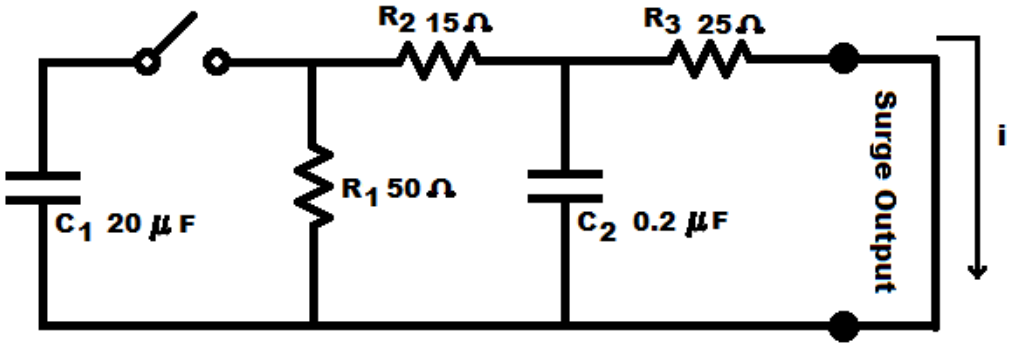


Figure 2.27: Surge generator circuit in short circuit mode for current surge

Figure 2.28 shows the parameters of the 8/20μs voltage surge generated by the surge generation circuit when configured in short circuit mode.

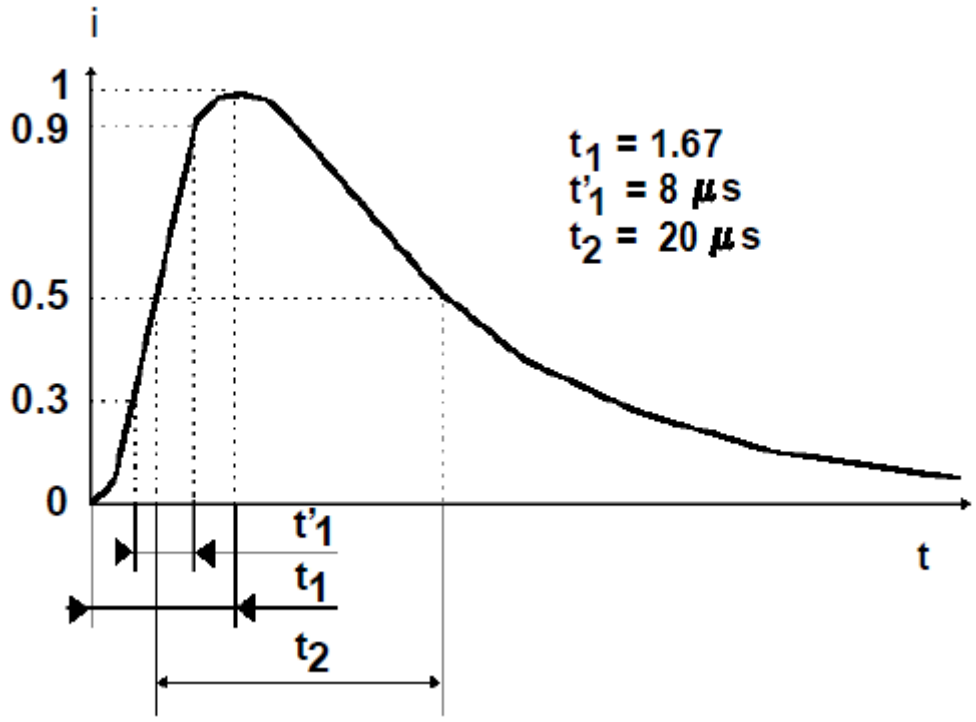


Figure 2.28: Voltage surge waveform parameters

The equation for the rise time of the current surge waveform is same as Equation (13). But in this case the time constant T must take into account the presence of R_3 along with R_2 and C_2 and hence T may be estimated as :

$$T = (R_2 * R_3 / (R_2 + R_3)) * C_2 \quad (15)$$

So $t_{(0.3)}$ and $t_{(0.9)}$ will be calculated respectively with $v(t)/V_p = 0.3$ and $v(t)/V_p = 0.9$ where $t_{(0.3)} = 0.57$ µs $t_{(0.9)} = 5.3$ µs and so

$$t_1 = 1.67\ (t_{(0.9)} - t_{(0.3)})$$

$$t_1 = 7.899\mu s \approx 8\mu s$$

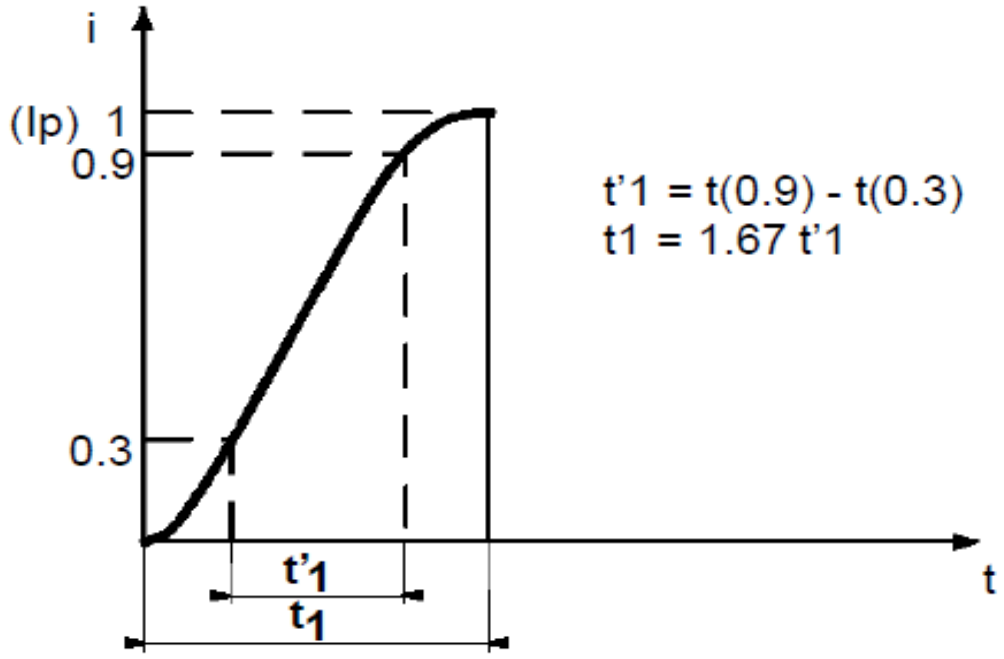


Figure 2.29: Rise time parameters for current surge waveform

The equation for the current surge duration curve is same as equation (14), but the time constant T is now due to C_1 with R_1 in parallel with R_2 and $R_3$and hence T may be estimated as :

$$T = (R_1 (R_2+R_3) / (R_1+R_2+R_3)*C_1 \quad (16)$$

So t_2 will be calculated with $v(t)/V_p=0.5$ and so

$$t_2 = 19.7\mu s \approx 20\mu s$$

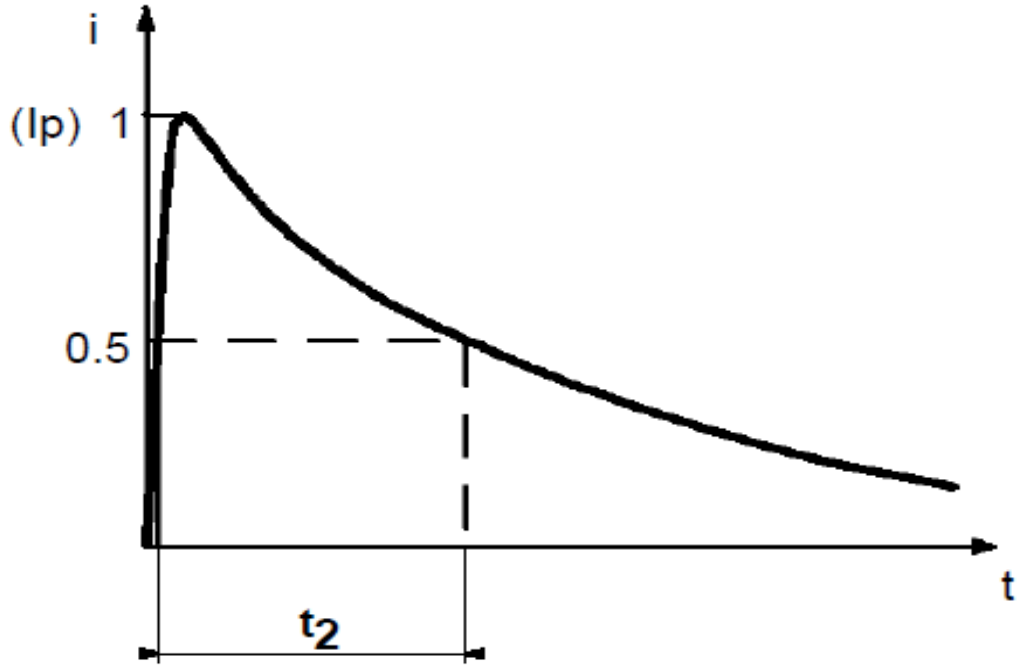


Figure 2.30: Current surge duration waveform

Chapter 3

Theoretical Synopsis of the Design Approach

3.1 BASIC SURGE PROTECTION BLOCK

The most widely used surge protection systems employed in commercial equipments consist of metal oxide varistors (MOV), gas discharge tubes (GDT) and avalanche transient voltage surge suppression (TVSS) diodes. High frequency transients and electro-magnetic interferences (EMI) are taken care of by choke coils and filter capacitors.

The surge protection block making up the front end of the prototype SRUPS employs an MOV and a GDT connected in series, followed in parallel by a TVSS diode. This topology is connected between the Line/Neutral (differential mode) and Line/Earth & Neutral/Earth (common mode). Directly after the TVSS section comes the differential and common mode suppression choke coils that filter out high frequency transients and EMI. Figure 3.1 shows the graphical representation of how the surge protection block works.

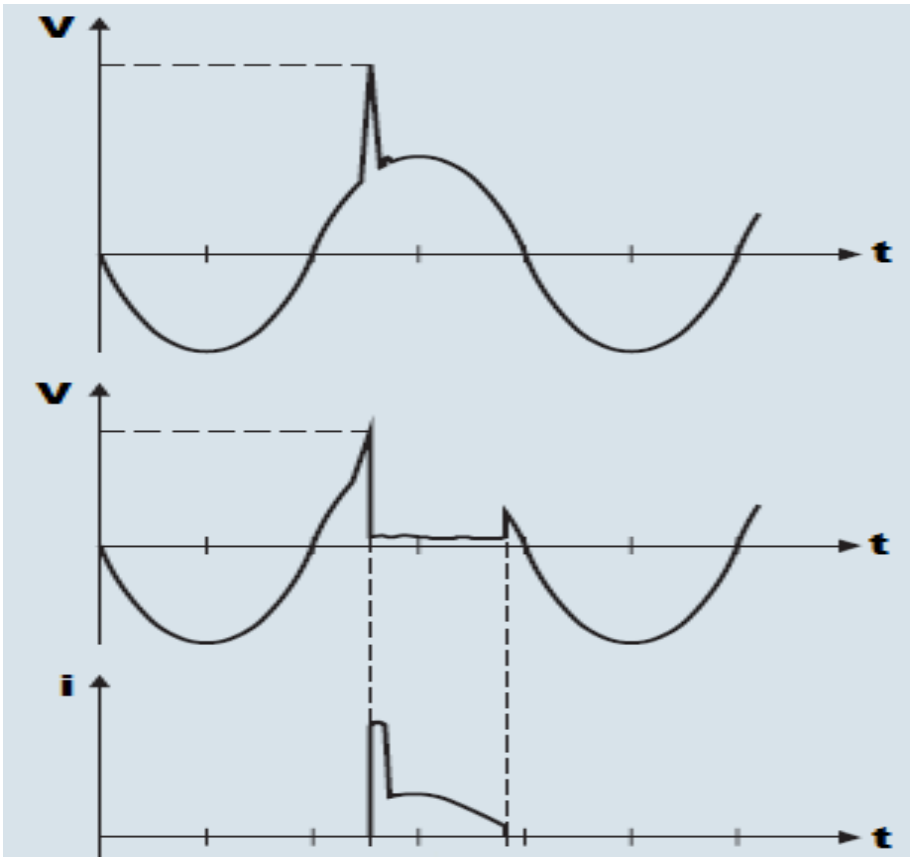


Figure 3.1: Graphical representation of surge suppression (EPCOS AG, 2008)

As gas discharge tubes have extremely low internal resistance, an excessive current which as a rule exceeds the permissible follow current would flow through

the ignited GDT. The GDT no longer extinguishes and can reach very high temperatures and create a short-circuit condition. So a metal oxide varistors is connected in series with the GDT for limiting the follow current. To stop the series combination of the GDT and MOV from responding during normal course of operation, a permissible tolerance on the line voltage of +10% and a possible de-rating of the surge arresters of –20% are taken into account. The TVSS diode is basically a pair of back to back AC zener diodes and they usually have a tolerance of 5%. Their current handling capability is limited and a heavy transient would certainly blow them, but their advantage is that they can maintain their clamping voltage throughout their current range. This is the reason why they are inserted after the MOV and GDT combination. The differential and common mode choke reactor coils are provided for absorbing and dissipating remnant high frequency transients and EMI appearing on the utility lines. Figure 3.2 depicts the setup for the basic surge protection block.

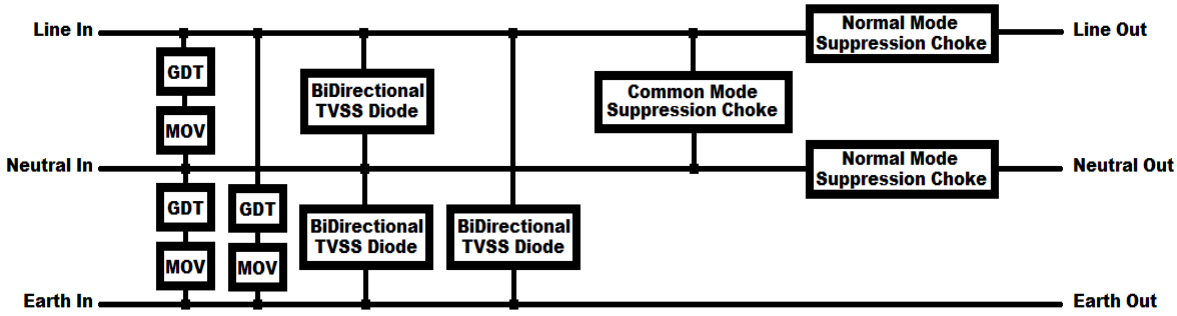


Figure 3.2: Basic surge protection block

3.2 SOLID-STATE SURGE DETECTION AND ISOLATION CIRCUIT

The surge detection and isolation circuit acts upon the first occurrence of a surge and isolates the SRUPS from the mains utility for a preset time period so that consecutive surges, if any during this interval, do not pose a threat to the system. It consists of a detector circuit that senses the appearance of a surge on the power line and a second isolation circuit that will isolate the SRUPS from the mains utility. Solid state switches are employed in the isolation circuit to provide fast isolation. A bridge and a MOSFET make up the solid-state switches employed in this circuit. The time interval for which the isolation circuit operates is variable and set according to design constraints by altering the time period for which the detection circuit triggers the isolation circuit Figure 3.3 shows the topology of the surge detection and isolation circuit.

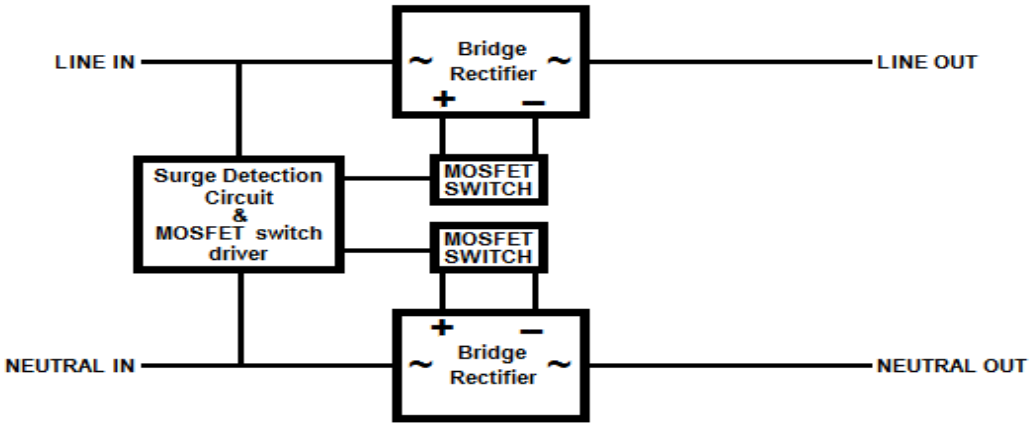


Figure 3.3: Surge detection and isolation scheme

A bidirectional TVSS avalanche diode is used as the sensing element in this circuit. When a voltage surge appears across the line and neutral that exceeds the cut-in threshold of the diode, the diode shorts out absorbing the surge. When the diode shorts out, it conducts through a bridge rectifier that turns on a pair of opto-couplers. A bridge whose DC output pins are connected to a MOSFET acts as the solid state switch in this circuit. The DC pins are shorted out during normal operation by the MOSFET, allowing a closed conduction path across the AC terminals of the bridge. But when a surge appears, the opto-couplers are set up in such a way that they switch off the MOSFET, thereby opening the DC terminals of the bridge causing it to open the path between its AC terminals. This breaks the conduction path across the bridge. For complete isolation of the succeeding circuits from the mains utility, a bridge is connected in series with both the line and the neutral wires. The time interval for which the isolation is provided by the circuit is set by deciding for how long the opto-couplers stay lit up after the TVSS diode has struck through upon the facing of the surge.

3.3 SOLID-STATE AC-DC STEP-DOWN CONVERTER

The AC to DC step-down converter forms the charger section in the SRUPS. A solid state transformer less constant-current charger design was incorporated to satisfy the charging requirements of the super capacitor banks used in the system. The charger was developed specifically for this project and is one of a kind. The existing buck-converter configuration forms the basic ideology of this AC-DC converter. A novel approach was undertaken to modify the buck converter configuration used mainly in DC to DC converters to develop this unique MOSFET based AC to DC converter.

The timing constraints imposed on charging the 21.6V / 80F super capacitor banks required the constant-current charger to have a current limit of no less than 15A. As the SRUPS is proposed to deliver at least 100W of useful power at the load, the average discharge current drawn from the SC banks was calculated to be 10A and hence the charging current was set at 15A so that the SC banks can be replenished faster than the time it takes to discharge it. At full load, the inverter takes nearly 50 seconds to discharge the SC bank from 20V to 15V, while it takes the charger 30 seconds to charge the bank from 15V to 20V at a constant current of 15AThe voltage limit for the charger is set at 21V. Figure 3.4 demonstrates the functional block diagram of the solid state AC-DC step-down converter.

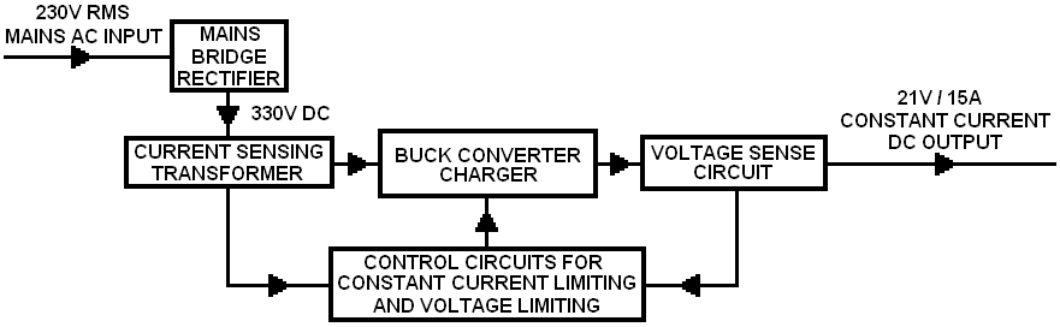


Figure 3.4: Solid-state AC-DC step-down converter

The mains AC voltage is rectified by a bridge rectifier and fed to the buck converter charger section via a current sensing transformer which senses the current drawn by the charger to limit the output current to 15A. A voltage sense circuit at the output of the charger limits the voltage delivered to the load at 21v.

3.4 MICROCONTROLLER BASED SUPER CAPACITOR BANK SWITCHING CIRCUIT

In order to extend the backup time provided by the SRUPS and also provide complete isolation of the inverter side from the charger side, three SC banks are employed. The three banks are consecutively switched between their three operational states, namely, charging, idle and discharging. An 8-bit PIC® 16F690 microcontroller is used to control the MOSFET switches that switch the SC banks between their operational states. The discharge window for the banks is from 20V to 15V and the charging window during start-up is from 0V to 20V assuming all banks are discharged fully when the system is powered on. During normal operation the charging window is from 15V to 20V. Figure 3.5 gives a brief idea on the functioning of the bank switching circuit.

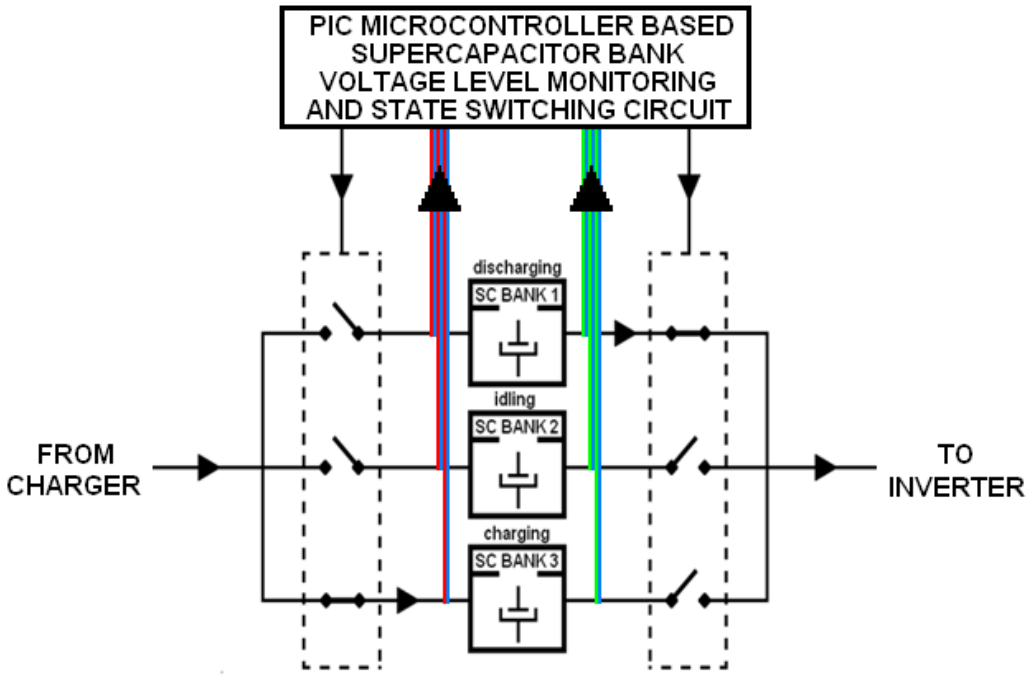


Figure 3.5: Microcontroller based super capacitor bank switching scheme

The upper voltage limit for a charged SC bank is set at 20V while 15v is set as lower discharge limit for the bank. At system start-up, the voltage monitor section of the controller monitors the voltage level of each of the three SC banks and consecutively charges then to 20V. After this, the first bank is set to discharge mode by connecting it to the inverter while the other two stay at idle. After the first bank is discharged to 15V, it is taken off the inverter and connected to the charger while the second bank is taken from idle and connected to the inverter. This process is cycled across the three capacitor banks. This allows the SRUPS to have a back-up time of thrice what would have been achieved if there was only a single capacitor bank as the reserve power source. Also as the bank that is connected to the charger is never simultaneously connected to the inverter, the inverter which is driven off another bank and the connected load is completely isolated from the utility mains end of the SRUPS.

3.5 THREE 21.6V / 81.25F SUPER CAPACITOR BANKS

The SRUPS utilizes three super capacitor banks as its back-up power source and also as a surge suppression element due to its low internal resistance and high energy density characteristics. Figure 3.6 shows one of the super capacitor banks that are employed in the SRUPS.

Figure 3.6: A single 81.25F / 21.6V super capacitor bank

As per the power requirements for the efficient operation of the SRUPS, each SC bank was required to be capable of delivering at least 7000 Joules of energy while it was discharging through a window of 5V. As the inverter section would take about 50 seconds to make a bank discharge through 5V and the charger had to replenish the bank charge within this time window, the capacitance of the SC bank was chosen accordingly. Therefore the SRUPS is capable of delivering a power back-up of nearly 150 seconds at full load with the combined reserve of the consecutively switched three SC banks. So it was decided that a bank would consist of eight 2.7V Maxwell BOOSTCAP 650F capacitors connected in series yielding an equivalent capacitance of 81.25F at 21.6V.with a total internal effective series resistance of 6.4 milliohms as per corresponding datasheet specifications. Each bank of eight super capacitors use four proprietary Maxwell active voltage stabilization units for performing voltage balancing of individual super capacitors during series integration.

3.6 MICROCONTROLLER BASED SYNTHESIZED SINE-WAVE PWM FULL-BRIDGE INVERTER

An 8-bit PIC® 16F684 microcontroller based sine wave synthesized inverter is used for the DC to AC conversion in the SRUPS. This technique is used because of its increased efficiency and reduced switching losses compared to other AC-DC inverter topologies. The microcontroller generates the PWM drive signals to drive the full bridge driver that driver the full H-Bridge power MOSFET switches

which in turn drives a step-up transformer Figure 3.7 gives the basic block diagram for the inverter.

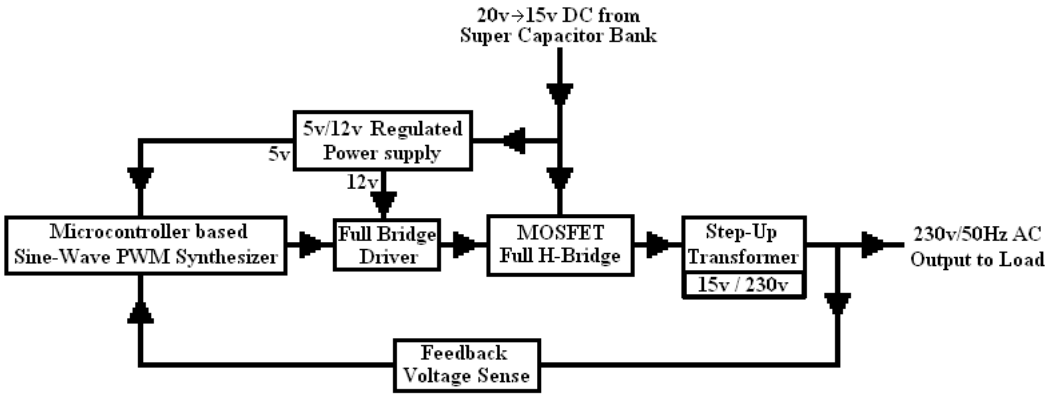


Figure 3.7: Block diagram of the inverter

The HIP4081AIP full bridge driver requires four pulse width modulated drive signals to drive the four individual power MOSFETS in the full H-bridge. The PIC® 16F684 is configured in full-bridge PWM mode to generate the four individual PWM drive signals for two high-side and two low-side power switch drivers in the full-bridge driver. The 12V required to operate the HIP4081AIP and 5V to power the PIC®16F684 is extracted and regulated from the 20V to 15V voltage window obtained from the discharging super capacitor banks. The same discharging voltage window is switched by the full H-bridge and fed to the step-up transformer. As the lower discharge limit for the SC banks is 15V, a 15V to 230V step-up transformer is used for the up-conversion. Also as the inverter is operating through a dropping input voltage window from 20V to 15V, the output voltage at the load is sensed and fed back to the microcontroller for regulation of the pulse widths driving the H-bridge so that the output AC voltage remains constant.

3.7 STATIC BYE-PASS SWITCH

In the event that the SRUPS must be taken off line due to an overload condition or failure or to allow safe and reliable maintenance, the critical load shall be transferred to the bypass AC mains utility source via the static switch without interruption of power to the critical load. The switch is a Make-Before-Break type change-over switch so as to ensure maximum load reliability and personnel safety. The static switch derives its power from an upstream bypass feed contactor that comes right after the preliminary surge protection block internal to the SRUPS

module so that even in bye-pass condition, the connected load has a robuts surge suppression system working for it. The static switch is also capable of supplying the SRUPS rated load current and also provide fault clearing current. As the implementation of a sensing logic to automatically energize the static bye-pass switch was out of the scope of the project, a manual make-before-break change-over switch is employed. Figure 3.7 shows the configuration of the static bye-pass switch.

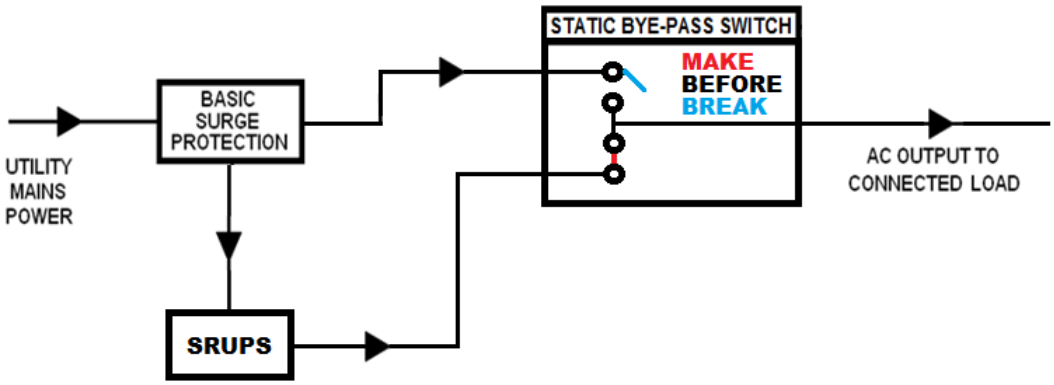


Figure 3.7: Static bye-pass switch configuration

Chapter 4

System Implementation

4.1 BASIC SURGE PROTECTION BLOCK

The surge protection block is the very first element in the SRUPS that is exposed directly to the utility mains, which is 230V RMS, the off-the-shelf components used herein are all rated at 230V as its nominal operating voltage. Surge testing of this block at 6.6KV yielded results that showed that the voltage levels at the output after clamping was in the region of 550V.

The following are the main components used:

- MOV used is the S20K250 by Siemens which is rated at 250VRMS AC / 320V DC with 8000A maximum surge current handling capability on a 8/20 µs current surge and power dissipation capability of 1W.
- GDT used is the EC350 07 O by EPCOS with a DC spark over voltage of 350V and a 20KA 8/20 µs current surge arresting capability.
- TVSS diode used is the1.5KE440CA by ST Microelectronics with a bi-directional breakdown voltage of 440V and maximum clamping voltage of 776V at 13A on an 8/20 µs surge.
- Common-mode choke used is rated at 250V/4A with two 47mH windings.
- Differential-mode choke used is rated at 250V/4A with a winding inductance of 550 µH.

Figure 4.1 gives the schematic of the basic surge protection block.

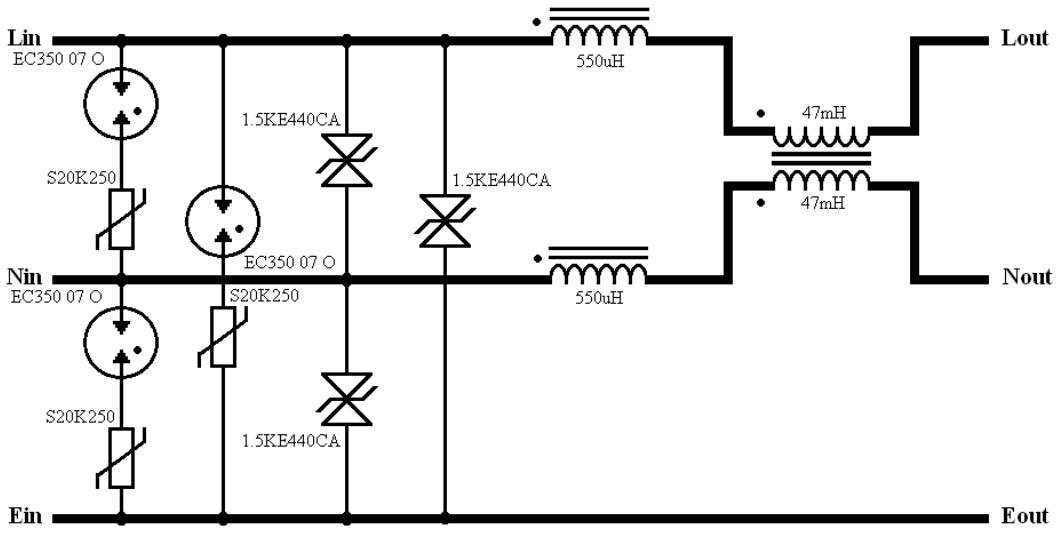


Figure 4.1 Circuit schematic for the basic surge protection block

4.2 SOLID-STATE SURGE DETECTION AND ISOLATION CIRCUIT

The input of the surge detection and isolation circuit is protected by the basic surge protection block which clamps surge voltages to an upper limit of 550V. So the components used at this stage are de-rated accordingly. The sensing circuit is connected between the Line and Neutral wires and the isolation switch is inserted into both the Line and Neutral wire to provide complete isolation in the event of a surge being detected.

The components used in the detection circuit are:

- TVSS diode 1.5KE440CA by ST Microelectronics with a bi-directional breakdown voltage of 400V and maximum clamping voltage of 706V at 14 A on an 8/20 µs surge.
- 2.2KΩ high voltage metal ceramic resistor rated at 10W.
- Ultrafast diode bridge rectifier made of four UF4007 diodes by Vishay with a rated RMS reverse breakdown voltage of 700V at 1A.
- 4N25 opto-couplers by Vishay with rated isolation voltage of 5KV, photo-diode forward current of 60mA and photo-transistor collector current of 50mA.

The time delay for which the detection circuit triggers the isolation circuit is set to 25 seconds by the 0.1µF capacitors connected across the photo-diodes of the opto-couplers.

The components used for the solid-state isolation switch are:

- 1N5929 bridge rectifier by Vishay rated at 500V RMS reverse breakdown voltage at 10A.
- 2SK1120 by Toshiba which is an N-channel enhancement mode power MOSFET with a drain current of 8A at a drain-source voltage of 800V and a low drain-source ON resistance of 1.5Ω.

As the opto-coupler employed does not have enough current handling capability to trigger the MOSFET, a general-purpose 2N2222 npn transistor is used to drive the MOSFET. The drive circuit derives its power from an externally connected 9V battery.

Figure 4.2 depicts the schematic employed in the detection and isolation circuit.

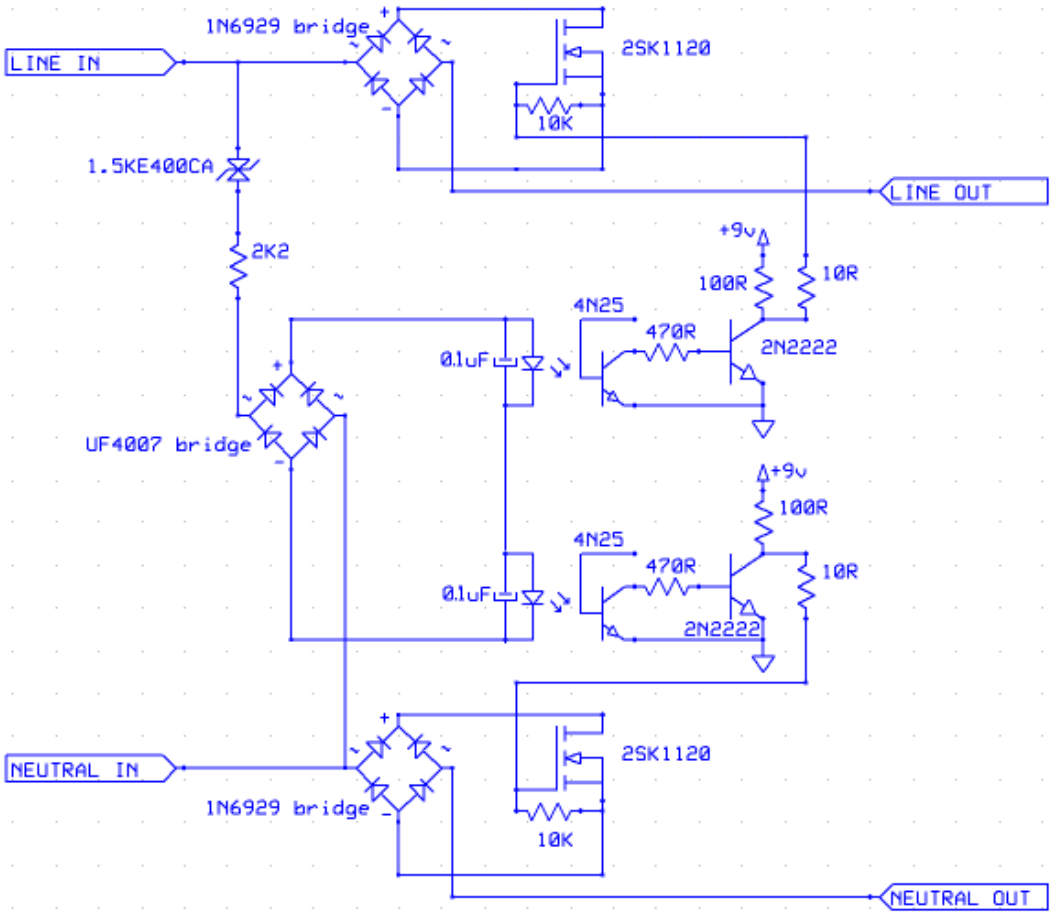


Figure 4.2: Circuit schematic for the surge detection and isolation circuit

4.3 SOLID-STATE AC-DC CONVERTER

The constant current charger circuit employed in the SRUPS is made entirely of discrete components as it offers better resistance to remnants of the transient surges that propagate through system circuits in the aftermath of a surge attack. Also as this prototype AC-DC converter is a unique transformer-less direct AC line charging scheme, with future-plans for developing application specific integrated circuits for the same purpose, discrete components have been preferred.

The charger consists of the following sections:

- High Voltage AC-DC Rectifier and Filter
- Low Voltage synthesis
- Buck Converter
    - Astable Multivibrator
    - Totem-Pole Driver
    - Power MOSFET Switch
    - Inductor and Commutation Diode

- Voltage Sense and Limiter
- Current Sense and Limiter
- Dummy Load

4.3.1 HIGH VOLTAGE AC-DC RECTIFIER AND FILTER

A bridge rectifier rated at 1KV and capable of handling 50A is used to rectify 230V RMS utility mains AC to 335V DC. A 1 µF/250V X-rated polyester capacitor is used to filter out high frequency noise on the line and a 100 µF/450V high ripple-current rated electrolytic capacitor is used to smooth out the rectified DC from the bridge. A 5A quick blow fuse is inserter on the mains side for short circuit protection and a negative temperature coefficient resistor is also inserted to limit in-rush current at system startup. Figure 4.3 shows the corresponding schematic.

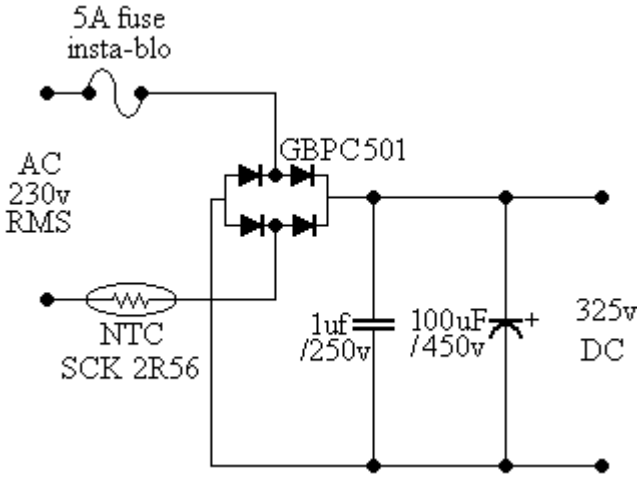


Figure 4.3: Circuit schematic for high voltage AC-DC rectifier and filter

4.3.2 LOW VOLTAGE SYNTHESIS

This circuit synthesizes a regulated 9.1V DC from the high voltage DC bus to power the low-power control, monitoring, switching and drive circuits in the charger. A high voltage 3.3KΩ wire-wound 10W ceramic resistor is used to drop the voltage and limit the current flowing through these circuits to 100mA. A9.1V zener diode is used to provide a crude voltage regulation and a 0.1µF polyester capacitor and a 470µF electrolytic capacitor forms the filter in this stage. Figure 4.4 gives the schematic for the low voltage synthesis stage.

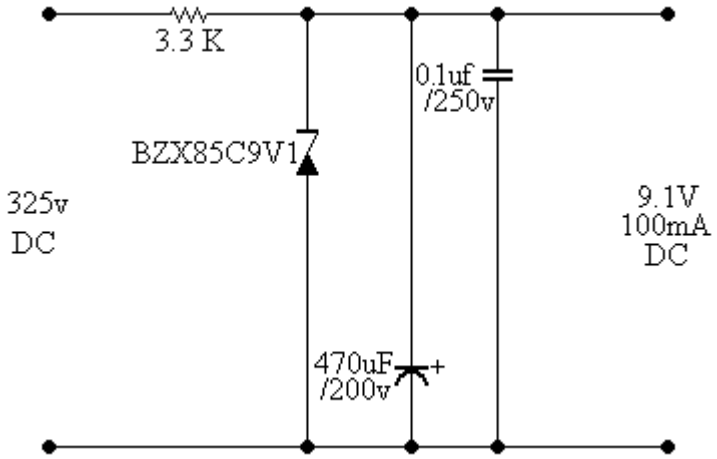


Figure 4.4: Circuit schematic for the low voltage synthesis stage

4.3.3 BUCK CONVERTER

The buck converter is a high efficiency step-down DC/DC switching converter. The converter uses a transistor switch, typically a MOSFET, to pulse width modulate the input voltage into an inductor. Rectangular pulses of voltage into an inductor result in a triangular current waveform. This charger uses a buck converter in continuous current mode, in that the current through the inductor never reaches zero. Figure 4.5 shows a basic buck converter scheme.

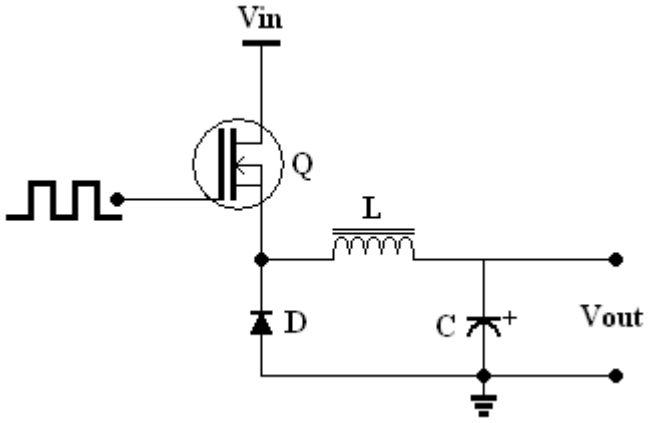


Figure 4.5 Buck converter configuration

4.3.3.1 INDUCTOR SELECTION

Calculating the inductor value is most critical in designing a buck switching converter. For a converter in continuous current mode, the inductor does not fully discharge during the switch-off time. Equation (17) assumes an ideal switch with zero on-resistance, infinite off-resistance and zero switching time and an ideal diode:

$$L = (V_{in_{max}} - V_{out}) * \frac{V_{out}}{V_{in_{max}}} * \frac{1}{f_{sw}} * \frac{1}{LIR * I_{out_{max}}} \quad (17)$$

where f_{SW} is the buck-converter switching frequency and LIR is the inductor-current ratio expressed as a percentage of I_{OUT} (e.g., for a 300-mA_{p-p} ripple current with a 1-A output, LIR = 0.3 A/1 A = 0.3 LIR).

The peak operating current through the inductor is calculated as follows:

$$I_{peak} = I_{out_{max}} + \frac{\Delta I_{inductor}}{2}$$

Where

$$\Delta I_{inductor} = LIR * I_{out_{max}} = (V_{in_{max}} - V_{out}) * \frac{V_{out}}{V_{in_{max}}} * \frac{1}{f_{sw}} * \frac{1}{L} \quad (18)$$

Using these equations, the inductance for the buck converter is calculated to be 50µH.

4.3.3.2 OUTPUT CAPACITOR SELECTION

Output capacitance is required to minimize the voltage overshoot and ripple present at the output of a buck converter. As the output load of the charger is a super capacitor, it is meaningless to include the output capacitor in-circuit. Instead a dummy load is included for eliminating undue ripples and voltage overshoot. The dummy load consists of a 1.1KΩ 10W resistor in parallel with a 1µF polyester capacitor and a 180µF/250V electrolytic capacitor.

4.3.3.3 COMMUTATION DIODE SELECTION

Power dissipation is the limiting factor when choosing a diode. Also the commutation diode must be able to operate efficiently at the switching frequency of the circuit. For reliable operation over the input-voltage range, the reverse-repetitive maximum voltage for the diode should be greater than the maximum input voltage The forward-current specification for the diode must meet or exceed the maximum output current Hence an ultra-fast recovery diode DSEP 30-10A which is rated to operate at 1KV/30A with a 95W power dissipation capability is used in the design.

4.3.3.4 POWER MOSFET SWITCH

The MOSFET used as the switching element must be one capable of operating at the switching frequency require by the converter and also should be rated to

operate at the current and voltage levels involved in the circuit. Power dissipation in the MOSFET is caused by on-resistance and switching losses. So an IXFK30N100Q2 N-channel enhancement mode MOSFET rated at 1KV/30A with a low drain to source ON resistance of 400mΩ and 735W power dissipation capability is selected.

4.3.3.5 ASTABLE MULTIVIBRATOR AND TOTEM-POLE DRIVER

An astable multivibrator is used to generate the switching frequency used to drive the power MOSFET switch in the buck-converter design. The frequency for the buck-converter design can be calculated if the duty-cycle of the switching pulses is known. The required duty-cycle for the converter is governed by the following relation:

$$V_{out} = V_{in} * \frac{T_{on}}{T} \tag{19}$$

where V_{out} is the required output voltage, V_{in} is the input voltage, T_{on} is the ON duration of the switching pulses and T is the time period. Using this relation, the frequency of the multivibrator is set as 30KHz with a duty-cycle of 10%. But as the astable multivibrator by itself can not provide pulses with enough current (~1A) for the hard switching of the power MOSFET, the astable multivibrator is fed to a totem-pole drive section which in turn drives the power MOSFET. For safety reasons pertaining that when the oscillator circuit is shut down, the power MOSFET has to be normally in OFF condition. Otherwise a failure in the oscillator circuit would result in the MOSFET being switched ON permanently leading to a disastrous short circuit condition. So the totem-pole driver is configure in an inverted state. Hence for proper operation of the buck converter, the astable multivibrator has to generate an inverted pulse train which will then be inverted once again by the totem-pole driver to provide the propped switching pulses to the power MOSFET. Hence the astable multivibrator is configured to generate 30KHz pulses with 90% duty cycle. Figures 4.6 shows the corresponding circuit schematics for the astable multivibrator and inverted totem-pole driver. Figure 4.7 shows the oscilloscope waveforms at the multivibrator and totem-pole driver outputs. The time period T for the astable multivibrator is given by:

$$T = T_{ON} + T_{OFF} \tag{20}$$

where $T_{ON} = 0.69R_3C1$ and $T_{OFF} = 0.69R_2C_2$ and $R_1 = R_4$.

On this basis for a 90% duty cycle R_1, R_2, R_3, R_4, C_1 and C_2 were obtained as 1KΩ, 15KΩ, 3.9KΩ, 1KΩ, 22nF and 1nf respectively.

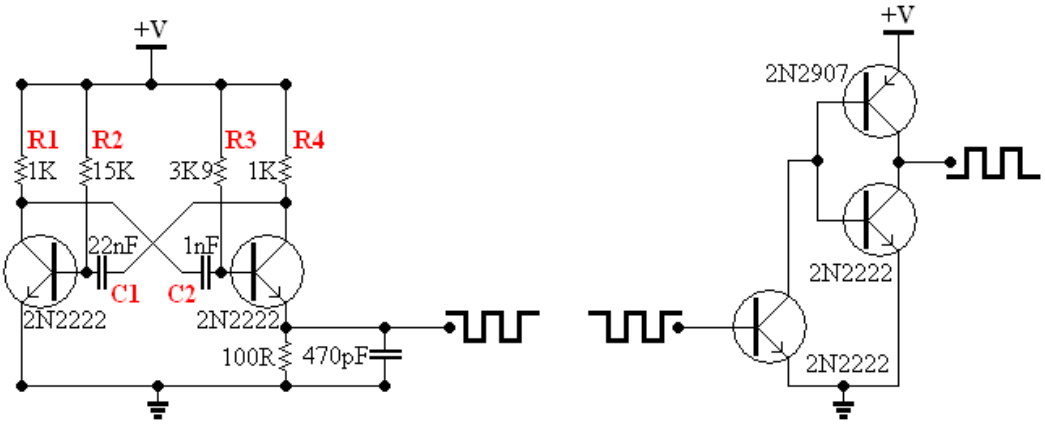


Figure 4.6: Schematics for astable multivibrator and totem-pole driver

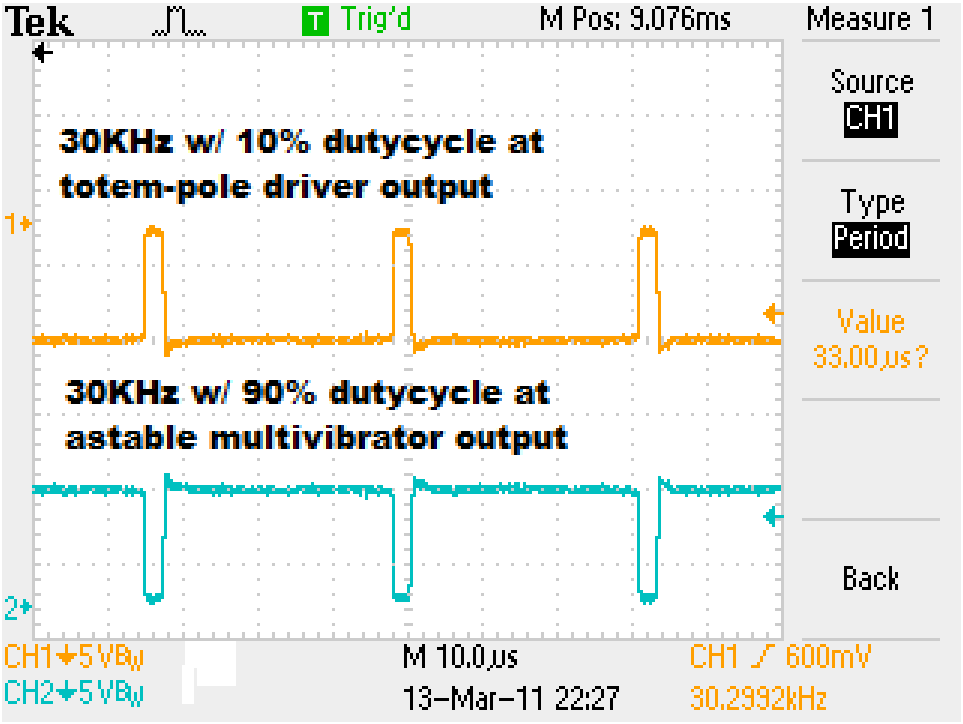


Figure 4.7: Multivibrator and driver output waveforms

4.3.4 VOLTAGE SENSE AND LIMITER

The super capacitor banks are rated at 21.6V. So the output voltage of the charger has to be limited so that it does not exceed the maximum rated value of the SC banks. The voltage sense and limiter circuit senses the voltage at the output terminals of the charger and limits it to the set value of 20V. A photodiode in an opto-coupler is used to sense the voltage at the output terminals. This is then

compared to a 4.3V zener diode based voltage reference. A 4.3V zener is used as it is has the best temperature compensation characteristics amongst low voltage zener diodes. A potentiometer is used to trim the reference voltage limit to 20V. Once the voltage through the photodiode exceeds the set reference value, it conducts and triggers its coupled phototransistor which in turn switches off the totem pole driver thereby killing the switching pulses going to the power MOSFET. Figure 4.8 shows the schematic for the voltage sense and limiter circuit.

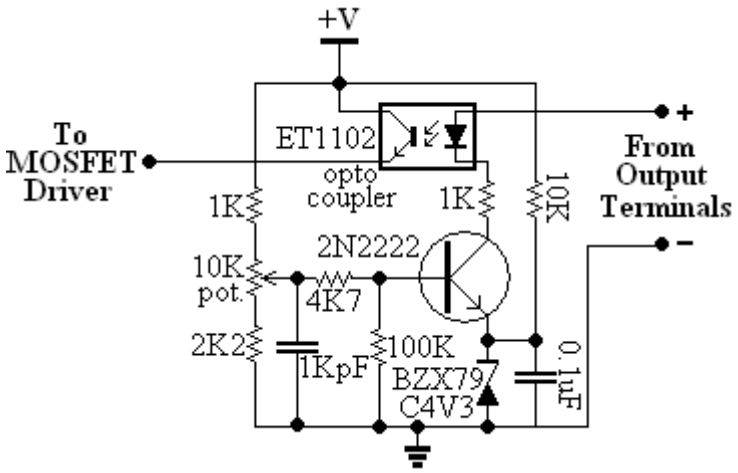


Figure 4.8: Circuit schematic for voltage sense and limiter circuit

4.3.5 CURRENT SENSE AND LIMITER

The current sense and limiter circuit limits the current drawn by the load at the output terminals of the charger to 15A. Hence the buck converter configuration is transformed to a constant current source. A current sense transformer is used to provide an isolated sensing element. One winding of the current sense transformer is connected is series to one of the output lines of the charger. The voltage generated at the secondary winding is used as the reference to trigger a transistor that when conducting turns off the totem-pole drive stage of the power MOSFET switch. A potentiometer is used to set the triggering voltage such that it corresponds to the condition when the load is drawing 15A of current from the charger circuit. Figure 4.9 depicts the circuit employed in the current sense and limiter.

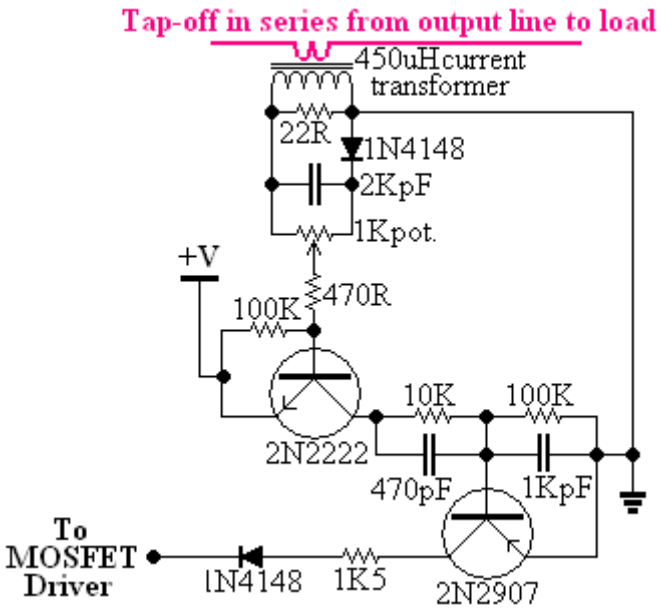


Figure 4.9: Circuit schematic for current sense and limiter circuit

4.4 MICROCONTROLLER BASED SUPER CAPACITOR BANK SWITCHING CIRCUIT

This circuit consists of two sub circuits. One is the 8-bit PIC® 16F690 microcontroller based monitoring and control circuit that senses the voltages of the three super capacitor banks and decides which of the three states, namely charge, discharge or idle, the bank should be in. To perform the actual switching of the bank states, the PIC® controller sends active-high control signals to the second sub circuit which houses the switching MOSFETS and their corresponding totem-pole drive circuits as the microcontroller signals do not have capability to switch the MOSFETs directly. Figures 4.10 and 4.11 show the flow chart of the routines running inside the firmware of the microcontroller.

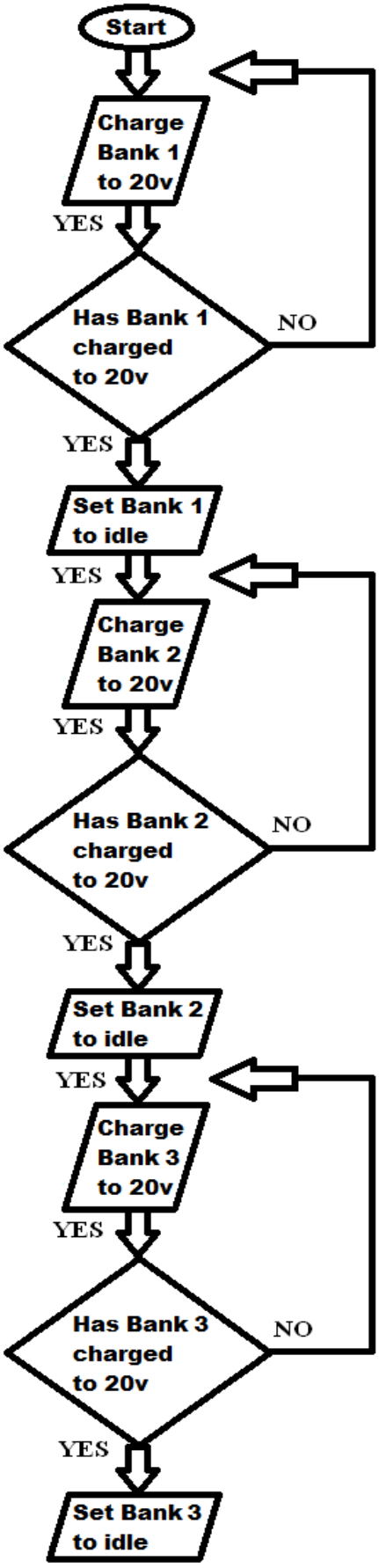


Figure 4.10: Start-up routine running in the PIC®16F690 microcontroller

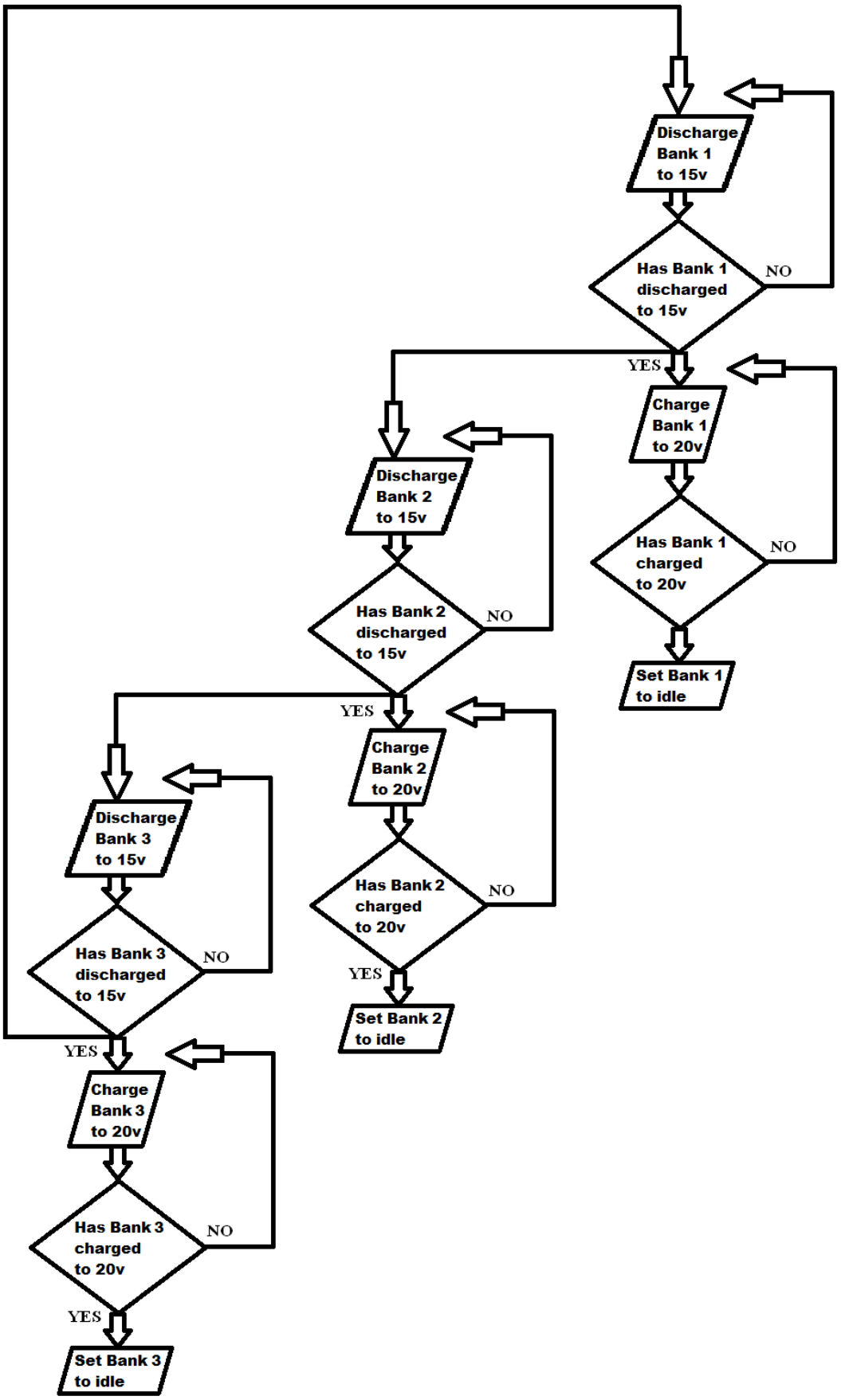


Figure 4.11: Sub-routine for normal SRUPS operation running in the PIC® 16F690 microcontroller

The analogue to digital converter (ADC) of the PIC® microcontroller is used to measure the super capacitor bank voltage. The ADC of the 16F690 comes in two modes: 8 bit and 10 bit.10 bit conversion is used to measure the voltage across the bank accurately. The reference voltage used in here is the regulated supply voltage of 5V. The resolution of the measurement is;

$$\frac{1}{1024} X\ 5V = 4.8\ mV$$

This resolution is sufficient to read the charging or discharging voltage across the super capacitor bank with reasonable accuracy. To read the correct voltage across the bank, 40 consecutive ADC readings are taken and averaged. Averaging the measurements eliminates any wrong readings resulting from spurious noise spikes. The voltage sense input lines to the microcontroller is via opto-couplers so that absolute electrical isolation from any transients that may appear across the SC banks do not affect the control circuitry. Table 4.1 is the state table for the different operational states of the super capacitor banks.

Table 4.1: Description of states of super capacitor banks

Current State	Previous State	Following State	Description	Voltage at Start	Voltage at End
Charge	Discharge	Idle	SC bank is charged to 20V by the charger	15V	20 V
Idle	Charge	Discharge	SC bank is neither connected to charger or inverter. It retains its charge acquired in previous cycle.	20V	15V
Discharge	Idle	Charge	SC bank is discharged to 15V through the inverter which generates 230 V AC to the critical load.	20V	15V

Figures 4.10 and 4.11 present the flow charts for the start-up routine and the sub-routine during normal operation of the system running in the PIC®16F690 microcontroller. The controller board has red and green LEDs that show the state in which a particular SC bank is in at an instant. Table 4.2 describes the status detailed by the LEDs.

Table 4.2: Description of LED status lights on controller board

Red LED	Green LED	State of Super Capacitor bank
On	On	Idle
On	Off	Charge
Off	On	Discharge
Off	Off	Bank voltage is less than 15V

The switching circuit consists of 80V/30A rated n-channel MOSFETS, two for each SC bank, one connecting the bank to the charger and the other transferring the connection to the inverter. Each MOSFET has its own totem-pole driver which is driven by the active-high control lines of the microcontroller via opto-couplers so that the sensitive microcontroller board is isolated from any switching transients that may arise. The schematics for the controller board and the switching circuit can be found in the schematics appendices.

4.5 MICROCONTROLLER BASED SYNTHESIZED SINE-WAVE PWM FULL-BRIDGE INVERTER

Synthesized sine-wave pulse width modulation technology is the most efficient mode of AC to DC conversion available for inverters. Minimized switching losses and low total harmonic distortion in the output AC waveform are a few of the benefits. The inverter section used in the SRUPS uses a PIC®16F684 internally configured to operate in the full-bridge PWM mode to generate the individual drive signals for each of the four MOSFET switches in the full bridge. As the PIC® signal lines can not drive the MOSFETs directly; a full-bridge driver HIP4081AIP by Intersil is used. 12V required to power the full-bridge driver and 5V required to power the microcontroller are obtained from the DC power supplied by the discharging super capacitor banks using an LM7812 and LM7805 voltage regulators respectively. The firmware in the microcontroller is coded to generate a 16KHz PWM to synthesize a 50Hz sine wave from a sine look-up table. Dead-time control to prevent shoot-through in the full-bridge is included as well. The coding also includes the modulation scheme to vary the pulse widths for output voltage regulation when the inverter is loaded. 80V/30A MOSFETs are the power switches used in the full bridge. The four MOSFET switches work in a boot-strapped configuration to generate the bi-polar waveform that is fed to the step-up transformer. The transformer used is an E-I lamination core type with a

15V primary winding and a 230V secondary with a 150W power rating. The transformer has a second secondary winding whose output is rectified and voltage-divided and fed back to the ADC of the microcontroller to modulate the pulse width so as to regulate the output voltage during loading of the inverter. And also as the DC power supplied to the inverter by the discharging SC banks is falling through a 5V window from 20V to 15V, a feedback for voltage regulation is absolutely necessary. The circuit schematic for the inverter can be found in the schematics appendix. Figure 4.12 shows the full-bridge PWM signals generated by the microcontroller. Figure 4.13 is the waveform at the output of the full H-bridge at no-load condition. Figure 4.14 is the waveform at the secondary of the step-up transformer at full-load condition.

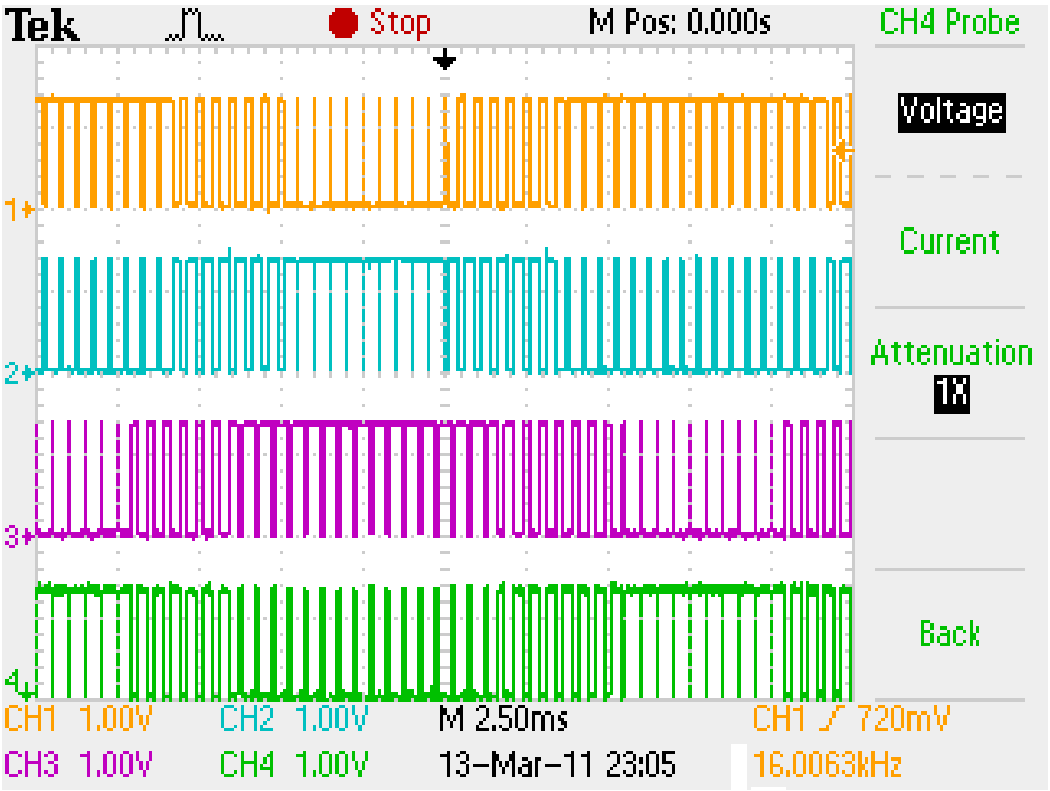


Figure 4.12: Full-bridge PWM mode drive signals

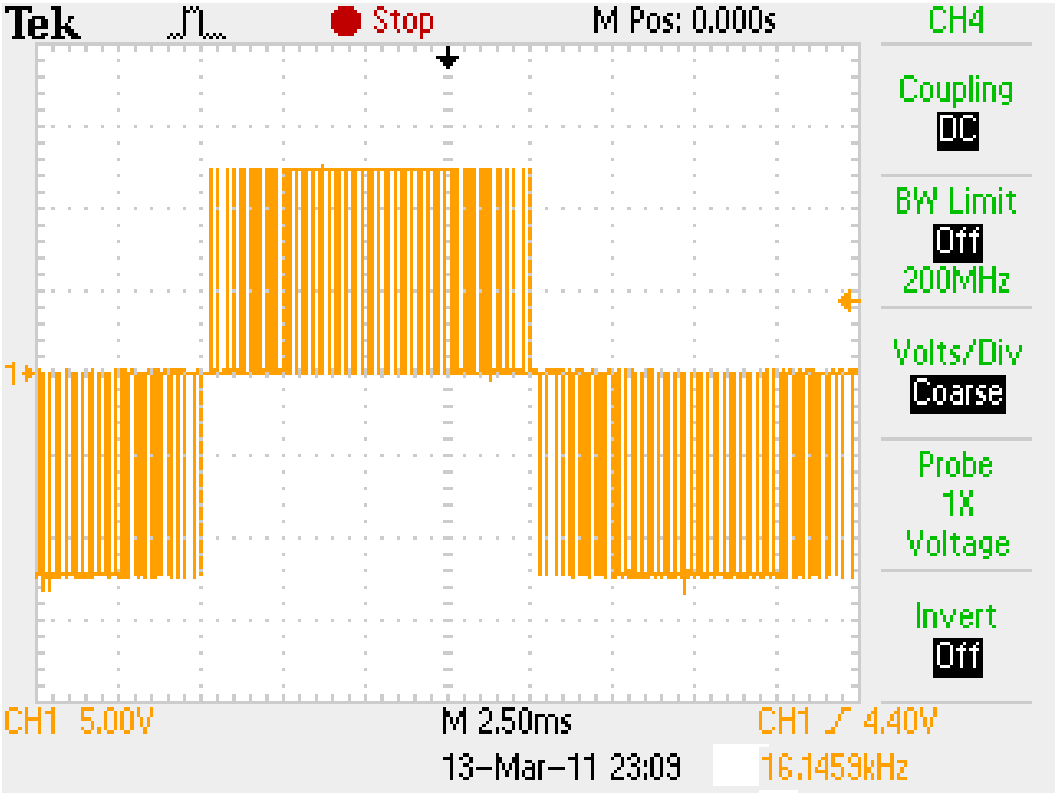


Figure 4.13: No-load waveform at full H-Bridge output

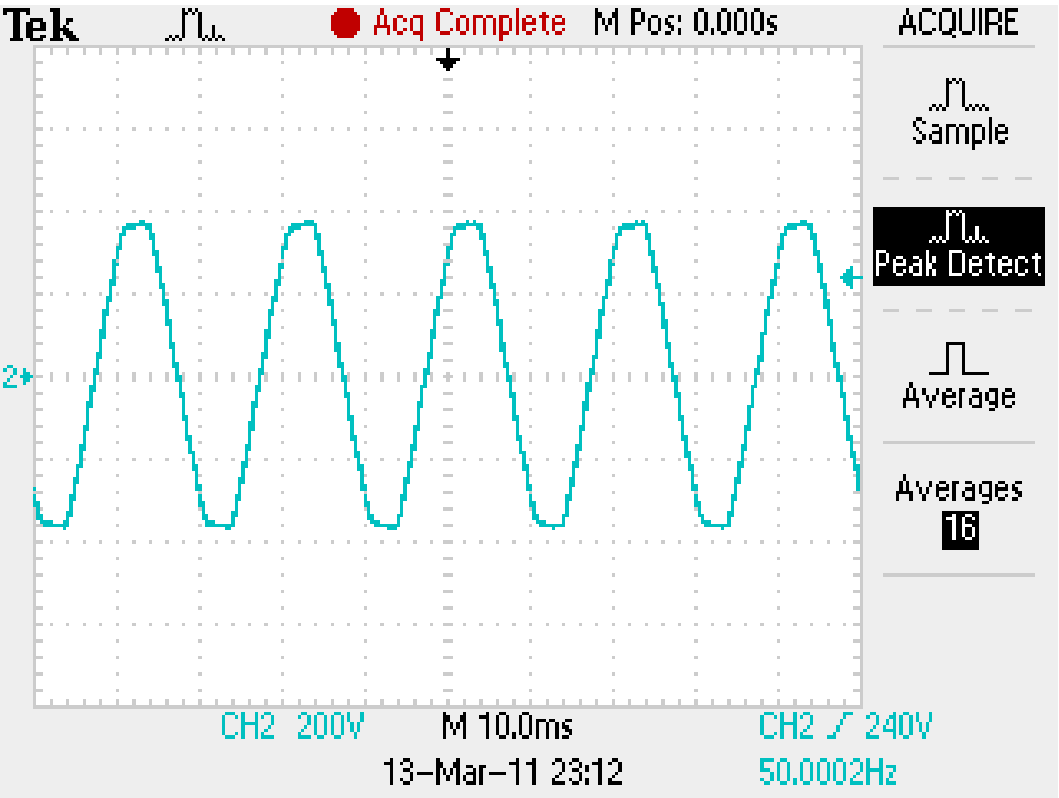


Figure 4.14: Full-load output waveform at secondary of step-up transformer

Chapter 5

Performance Evaluation and Results

The complete SRUPS system was set up to as per the topology shown in figure 5.1 to perform the test and measurement procedures for the performance evaluation.

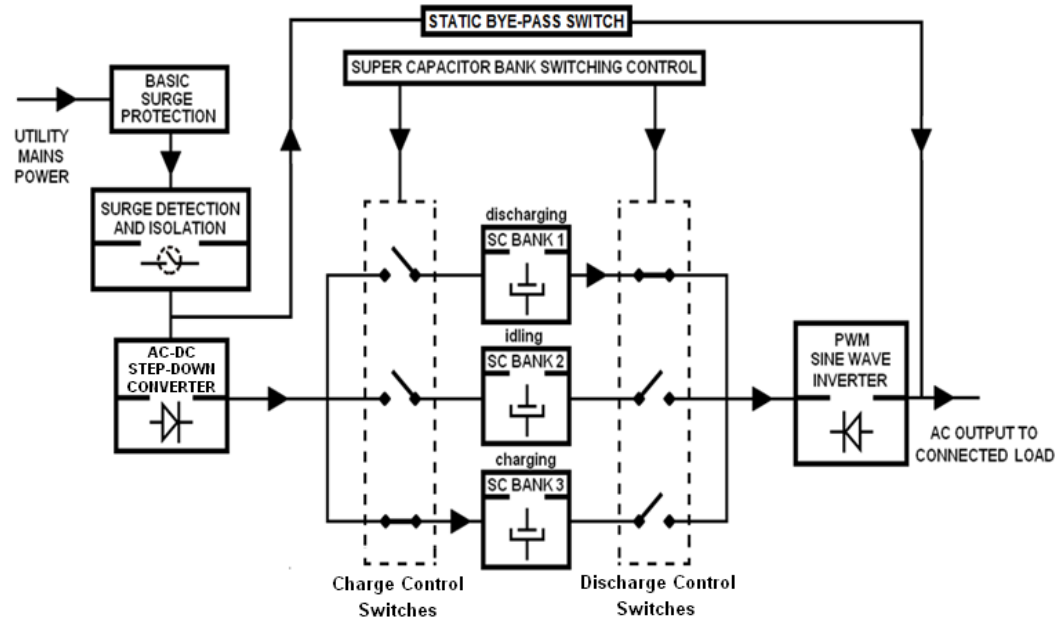


Figure 5.1: Block diagram of the final revision of the SRUPS system

The following tests and measurements were carried out on the SRUPS system:

- Surge testing of the basic surge protection block to measure the surge suppression offered
- Surge testing of the surge detection and isolation circuit to measure the response and isolation offered
- Charge testing of the AC-DC step-down converter to measure its efficiency and timing for constant current charging of the super capacitor banks
- Surge testing of the AC-DC step-down converter to measure its surge withstanding capability
- Testing of the SC bank switching control circuitry to verify if the switching scheme works as intended
- Discharge testing of the SC banks via the inverter to measure the inverter efficiency as well as the timing the back-up offered by the SC banks when at full-load condition

All surge testing was performed using the NoiseKen LSS-6110 lightning surge simulator power via a 230V/1KW isolation transformer as shown in figure 5.2 and

the measurements were read off the Tektronix TPS 2024 digital storage oscilloscope with four isolated inputs which is shown in figure 5.3.

Figure 5.2: Photograph of the NoiseKen LSS-6110 lightning surge simulator

Figure 5.3: Snapshot of the Tektronix TPS2024 digital storage oscilloscope

5.1 SURGE TESTING OF THE BASIC SURGE PROTECTION BLOCK

Figure 5.4 shows the connection topology used in this test procedure.

Figure 5.4: Connection topology for surge testing of the basic surge protection block

Figure 5.5: Snapshot of the basic surge protection block

Differential mode surge testing was performed using 6.6KV 1.2/50µs voltage surge superimposed on the 230V RMS mains AC utility voltage. Common mode surge testing was not performed as common-mode surges in reality are relatively weak unless there is a direct lightning strike on the wiring connected to an equipment, and do not deserve much attention and protection from differential or normal mode surges take higher priority Figure 5.6 is the oscilloscope screenshot of the waveform at the output of the surge protection block.

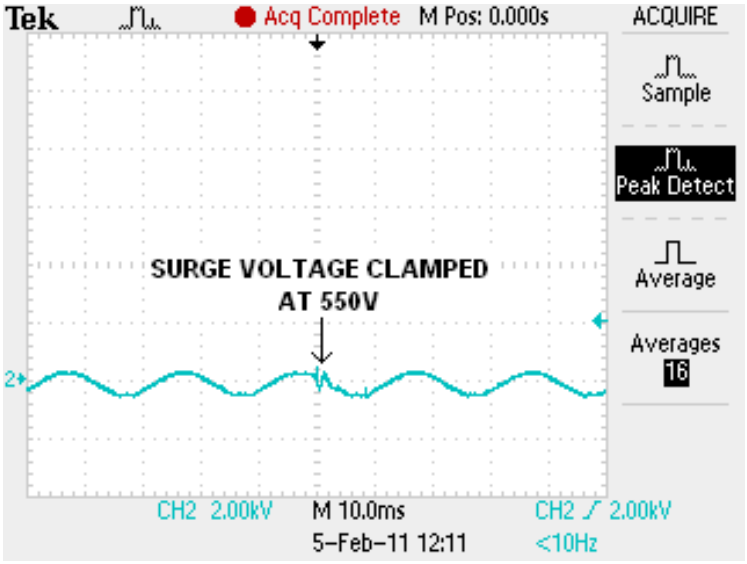


Figure 5.6: Oscilloscope screenshot of surge suppression by basic surge protection block

The voltage waveform at the output of the basic surge protection block displayed a mains AC voltage with the 6.6KV surge clamped to a voltage of ~550V. Repeated surging resulted in the MOV GDT combination blowing out after an average of 4 surges thereby leading to the blowing of the TVSS diode in the consecutive surge.

5.2 SURGE TESTING OF THE SURGE DETECTION AND ISOLATION CIRCUIT

The surge testing of the surge protection block gave the result that remnant transients on the mains line is in the order of half a kilovolt after the surge propagates through the block. So surge testing was performed directly on the surge detection and isolation block at 0.6KV as the components used in the circuit are suitably over-rated. Figure 5.7 shows the connection topology used in this test procedure.

Figure 5.7: Connection topology for surge testing of the surge detection and isolation circuit

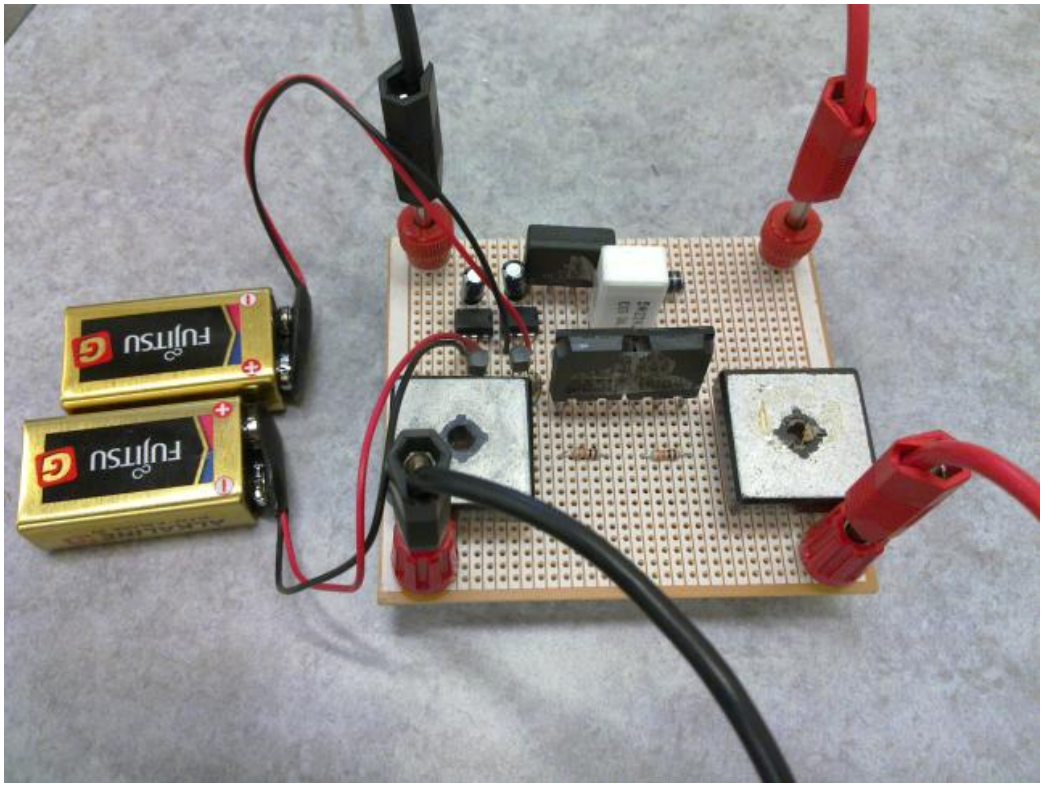


Figure 5.8: Snapshot of the surge detection and isolation circuit

The surge simulator was configured to generate a common mode surge over the mains utility with the surge injected on both the Line and Neutral wires with the Earth wire taken as the return path. Figure 5.9 shows the screenshot of the voltage waveform at the output of the surge detection block. It is seen that both the solid-state switches that lie on the Line and Neutral wires were opened once the surge was confronted, isolating both the mains utility wires. The switches resumed normal operation after the pre-set time delay of 25 seconds.

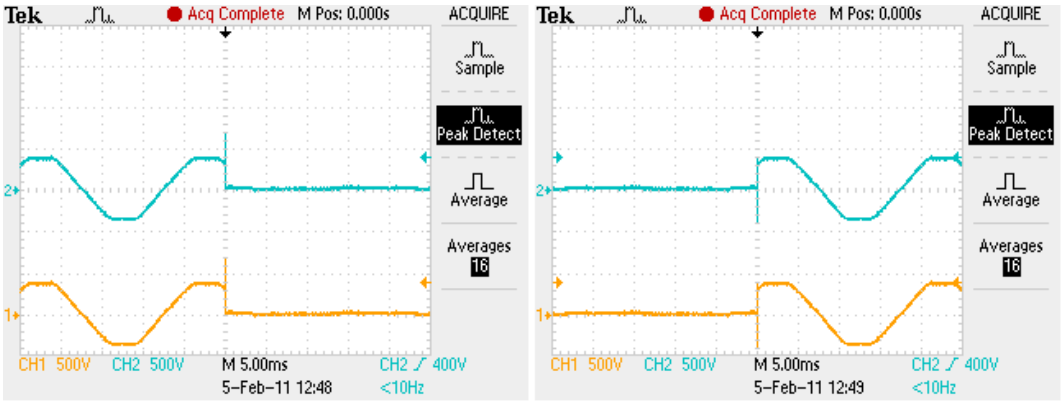


Figure 5.9: Oscilloscope screenshost of the operation of the surge detection and isolation circuit

5.3 TESTING OF THE AC-DC CONVERTER

The tests conducted on the charger section were to determine whether the constant current and voltage limiters were working as intended, whether it can charge the SC banks within the timing constraints. Figure 5.10 depicts the setup for the charging tests.

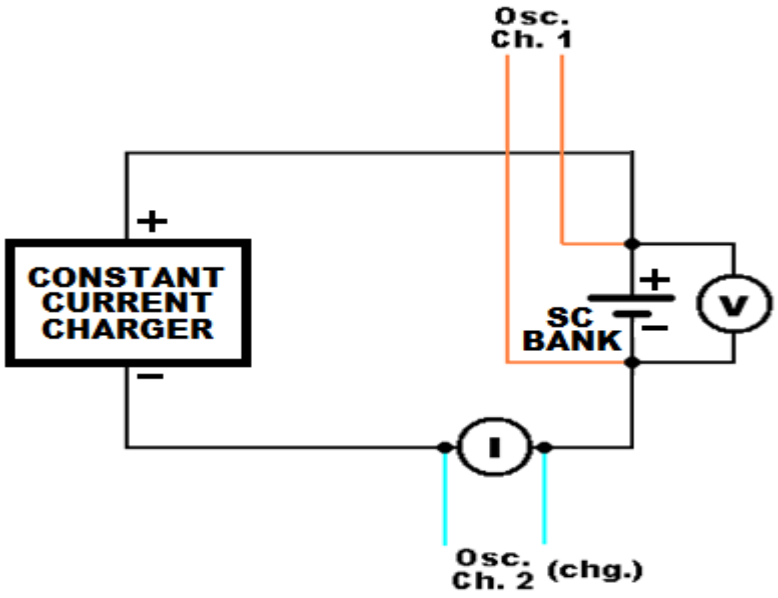


Figure 5.10: Test setup for charging test of AC-DC converter

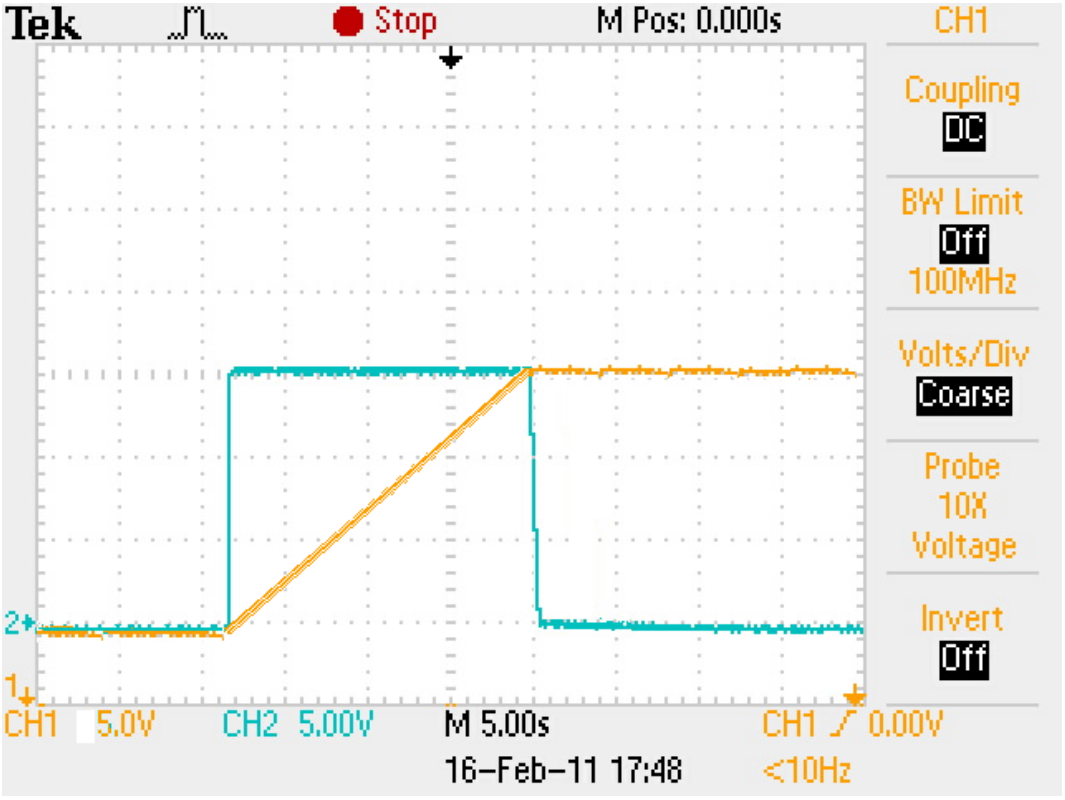


Figure 5.11: Waveform for charge testing

The charging test conducted resulted in a super capacitor bank being charged from 15V to 20V in 15 seconds at a constant current of 15A. The operational efficiency of the charger circuit was also measured. The following are the operational efficiency parameters.

Mains Voltage = 242V, 50Hz

Charger Output Voltage = 15V DC.

Load at 20V = 1.3ohm.

Load Current drawn = 15A

Load Power = 300W.

Mains Current Drawn = 1.09A.

Input Power=1.09x242 = 264W.

Efficiency = (264/300)x100 = 88%.

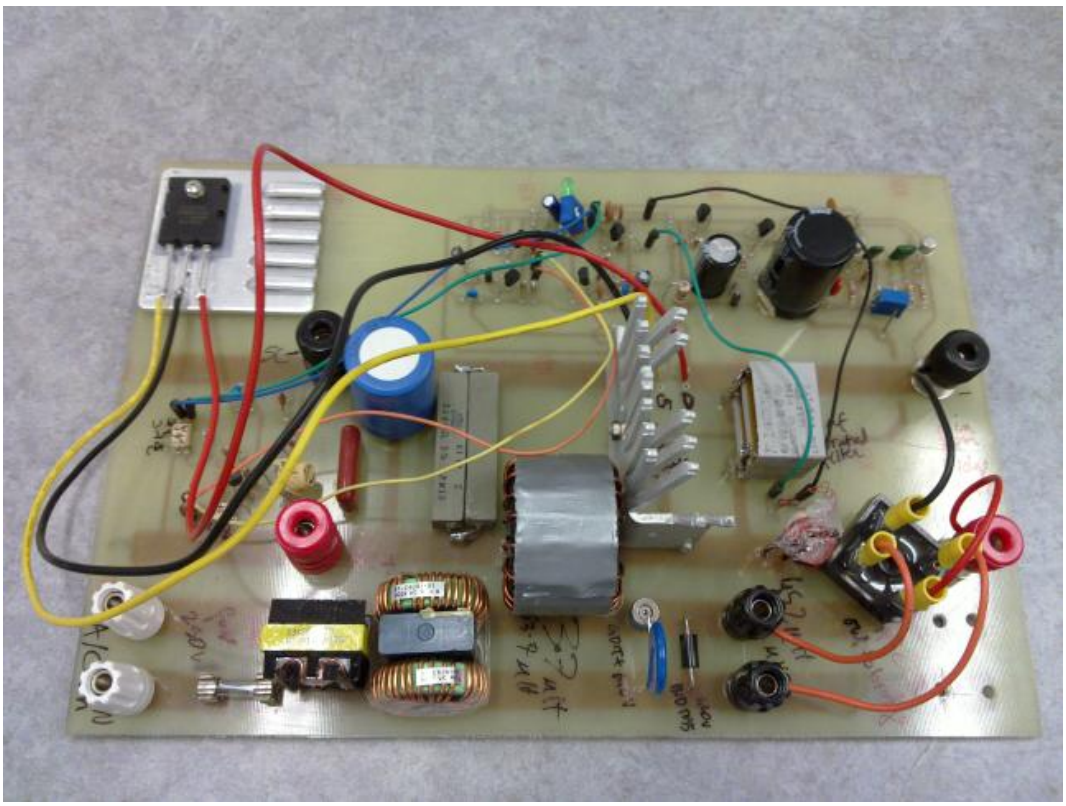


Figure 5.11: Photograph of the charger circuit

The charger circuit utilizes a 1KV rated bridge rectifier, power MOSFET and commutation diode. So the charger was surge tested at 0.8KV 1.2/50µs pulses and ever after 100 consecutive hits, there was no damage recorded to any of the circuit components and there was no variation in the output voltage either as the vulnerable components have already been over rated and under usual circumstances, the remnants of the surge that propagates through the surge protection block comprises of voltage levels of 0.5KV which makes the charger circuit completely resistant to the surge tests performed on it. And as there is no surges transients that appeared at its output terminals, the rest of the SRUPS system is protected. Even if some seepage does occur, as the charger is connected to the super capacitor banks with very low ESR, the load connected to the SRUPS is completely safe.

5.4 TESTING OF THE BANK SWITCHING CONTROLLER

The bank switching controller was tested to verify whether the sub-routines it was running in its firmware were operating as it was meant to be. Figures 5.13 and 5.14 show the functional waveforms of the start-up routine and the nominal operation subroutine. For the start-up routine, the control circuit consecutively checks the voltage level of each SC bank and charges it to 20V as shown in figure 5.13. During the normal operation, the subroutine, starts discharging the first bank through the inverter, and once its voltage drops to 15V, it switches the bank over to the charger while seamlessly allotting the second bank to the inverter. Once the first bank is charged it is kept on idle. This process is cycled through all the three banks and then the whole process starts over again.

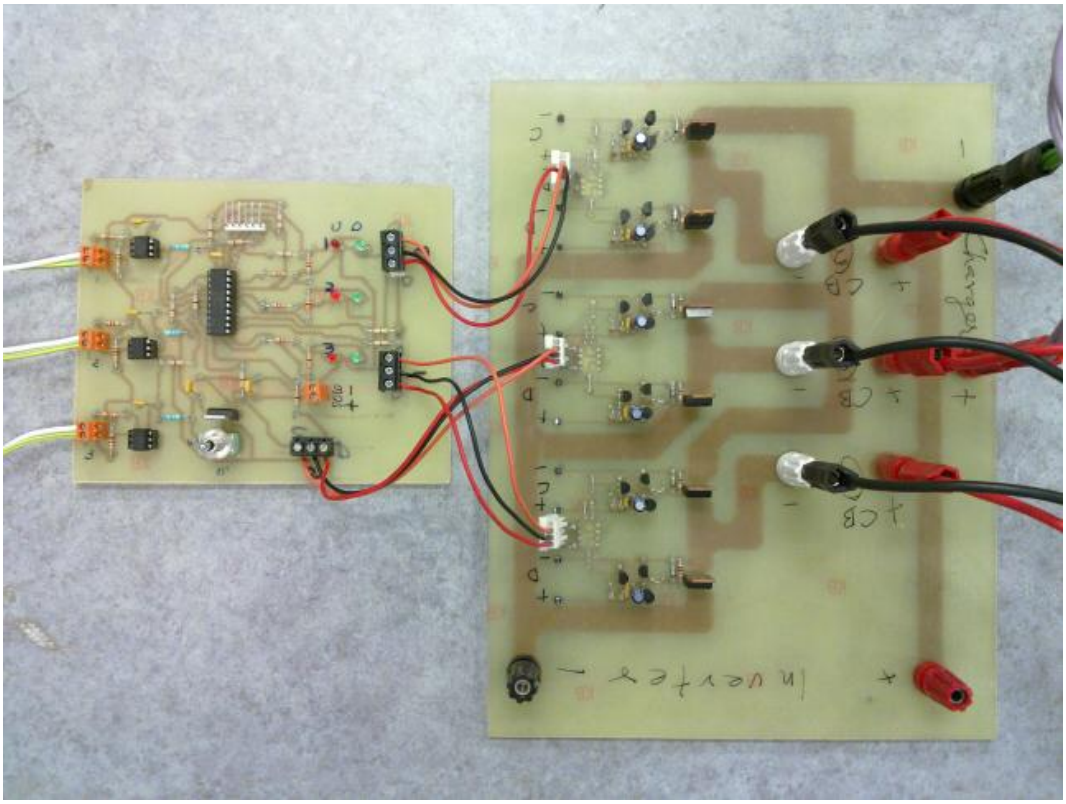


Figure 5.12: Photograph of the bank switching controller and MOSFET switches

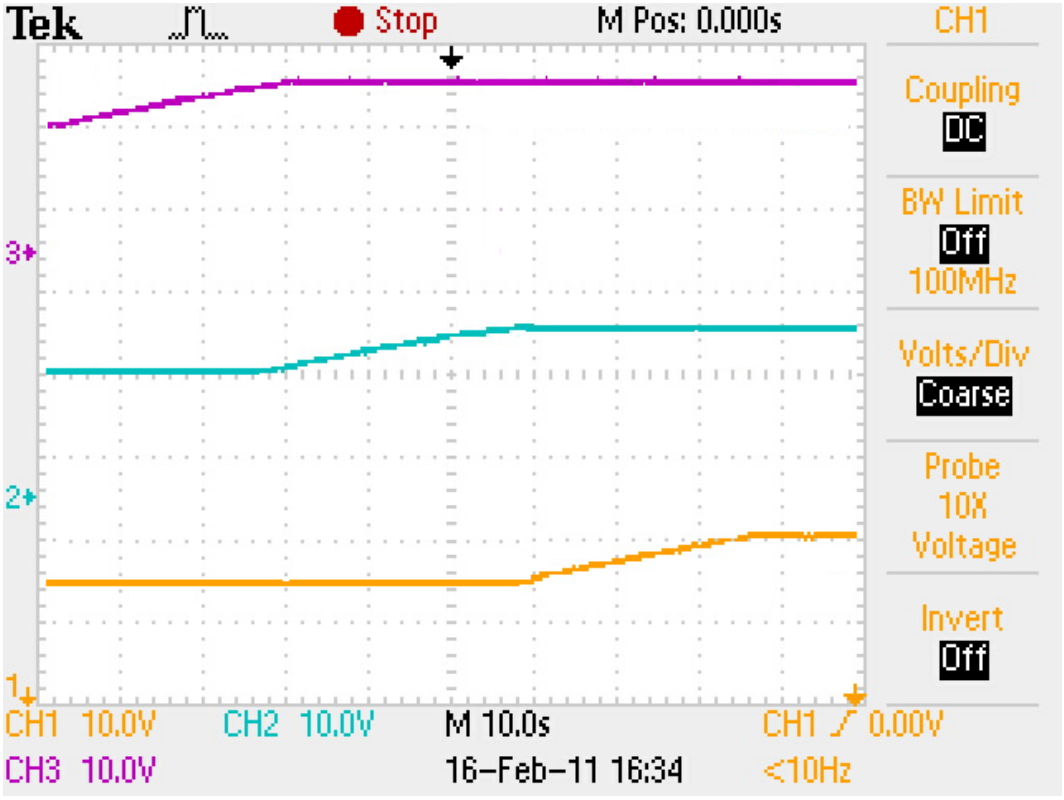


Figure 5.13: Waveform for start-up routine

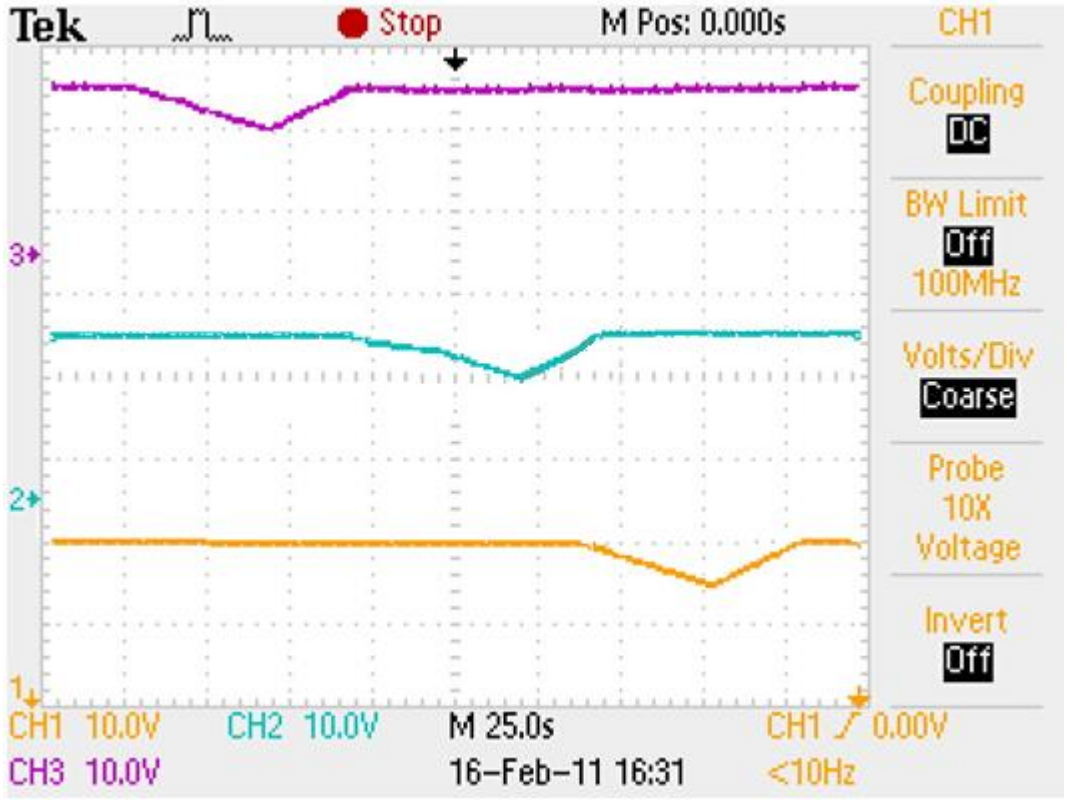


Figure 5.14: Waveform for nominal operation sub-routine

5.5 TESTING OF THE SINE WAVE PWM INVERTER

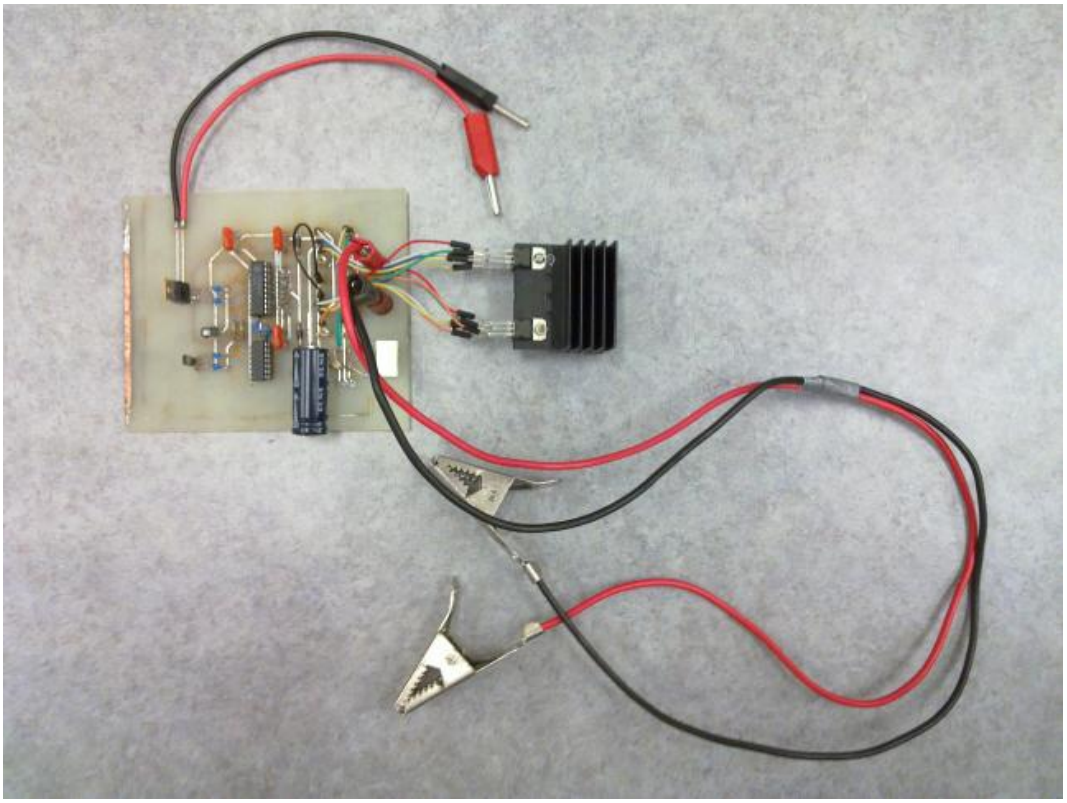


Figure 5.15: Photograph of the first revision inverter

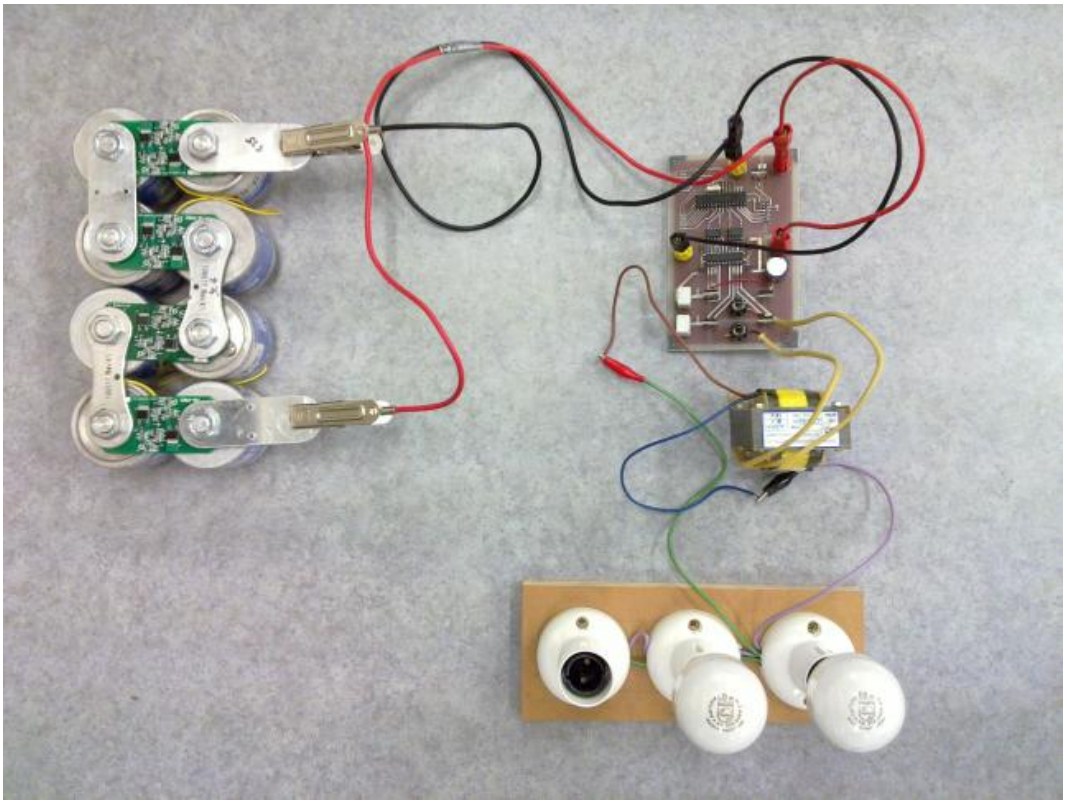


Figure 5.16: Photograph of the second revision inverter

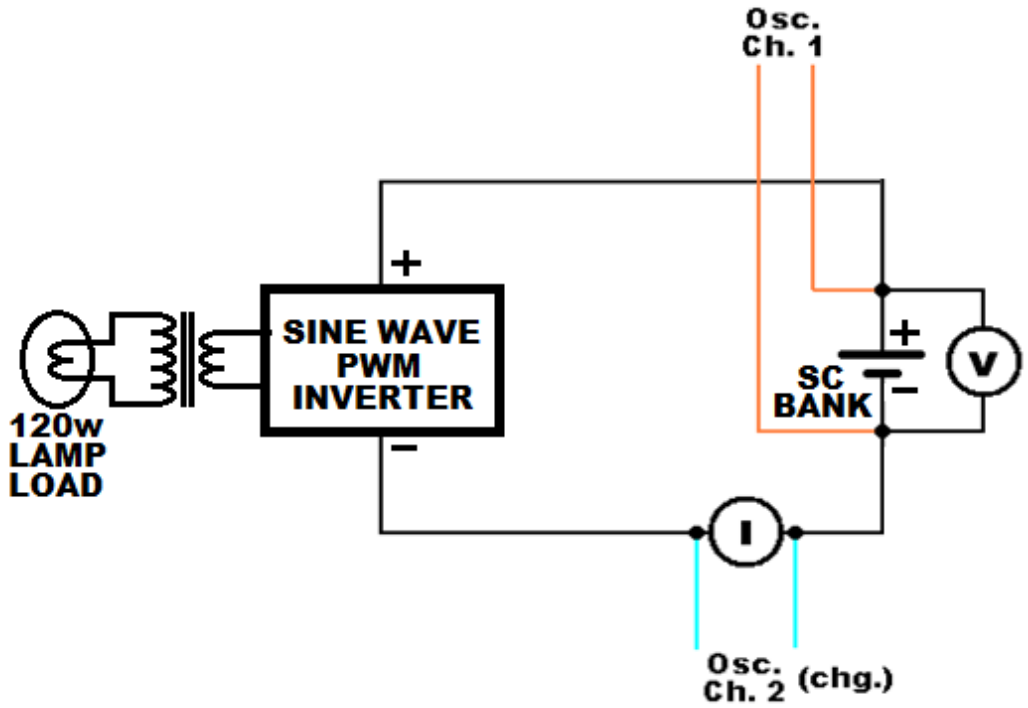


Figure 5.17: Setup for the discharge testing

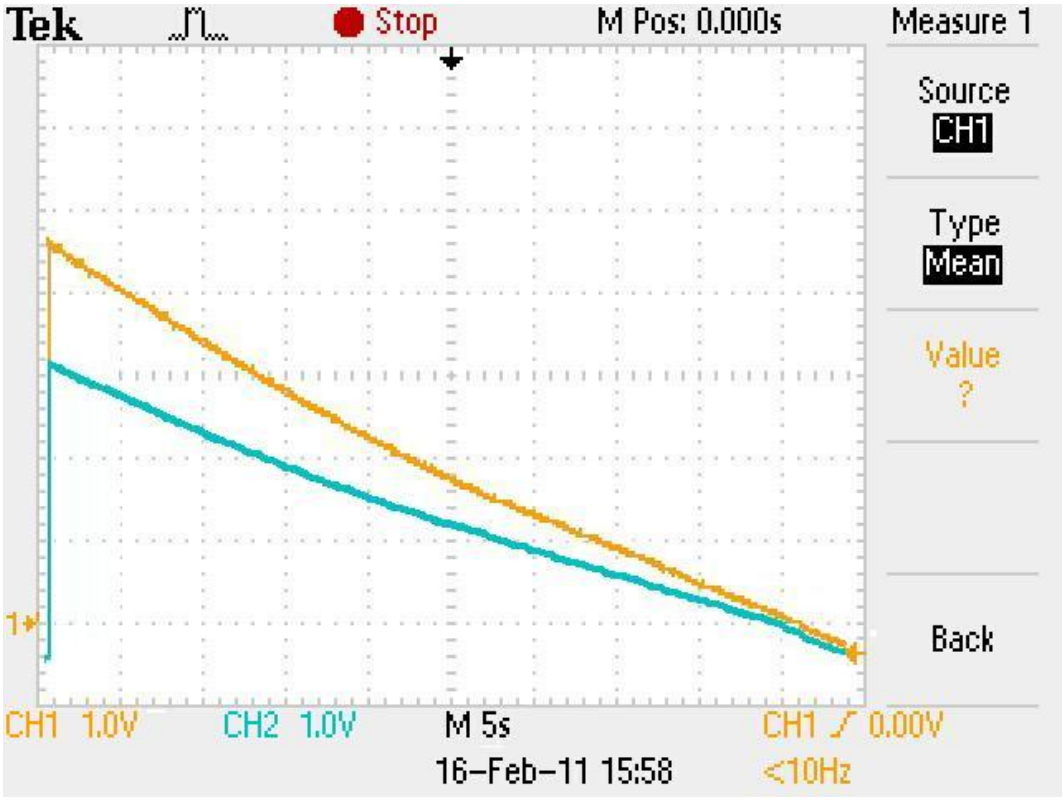


Figure 5.18: Discharge test waveform

Figure 5.17 shows the setup that was used to conduct the discharge tests and figure 5.18 is the oscilloscope screenshot of the discharge waveform. The

discharge tests were conducted by connecting a super capacitor bank that was charged to 20V to the inverter and loading the inverter with a 120W lamp load. The bank was allowed to discharge to 15V and the time taken was noted to be 46 seconds, which is well within the time constraints as the charger requires only 15 seconds to replenish the charge in the bank from 15V to 20V. At a load of 120W, each bank provides 46seconds of back-up, thereby taking the total back-up provided by the SRUPS which employs three super capacitor banks to138 seconds.

Inverter Output AC Voltage = 230V, 50Hz
Load Current drawn = 1.9A
Load Power drawn = 120W.
Input Current drawn = 7.68A
Input voltage supplied = 17.5V
Input Power = 17.5x7.68 = 134.5W.
Efficiency = (120/134.5)x100 = 89.2%.

Figure 5.19 shows the waveforms of utility mains AC fed to the SRUPS and the output AC waveform delivered by the SRUPS.

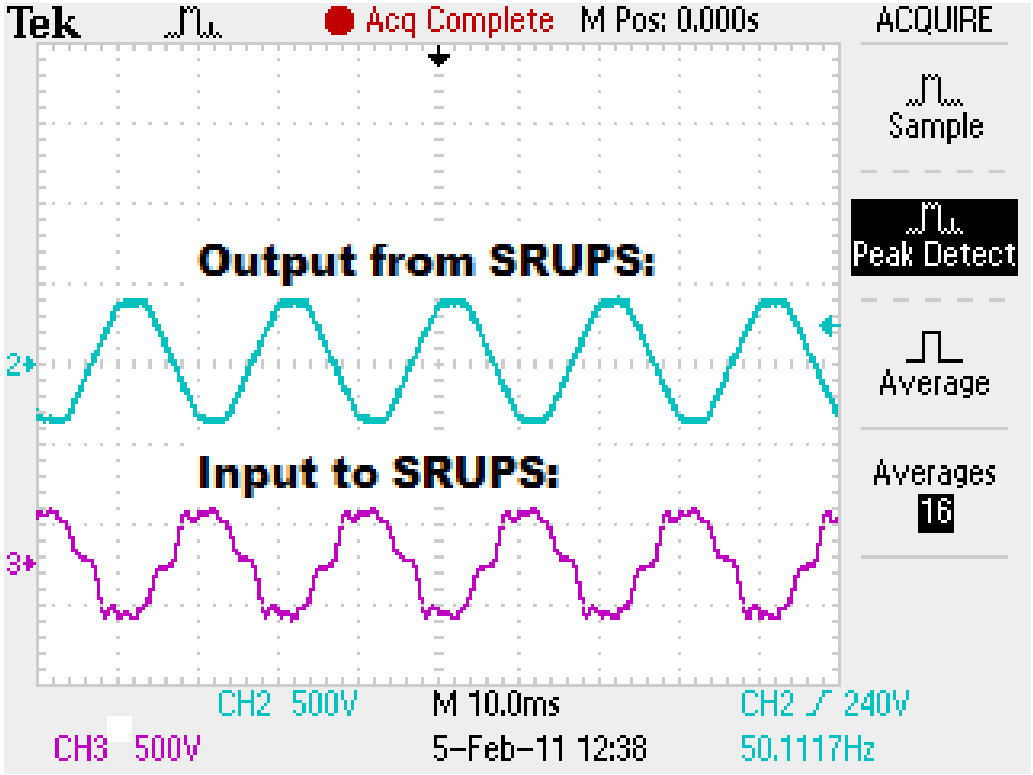


Figure 5.19: SRUPS input AC vs. output AC waveforms

Chapter 6

Conclusion and Future Developments

6.1 CONCLUSION

The surge resistant uninterruptible power supply developed for this research project is a unique endeavor in that it utilizes commercially available super capacitor technology in a whole new light. The property of super capacitors that they can withstand heavy momentary voltage and current surges due to their high energy density characteristics and very low internal effective series resistance has been exploited in this project in two perspectives. One is that they can be charged and discharged in similar linear fashion which means energy can be re-circulated quickly and efficiently in a system employing more than one super capacitor, thereby enabling it to be used as a reserve power source. The other is that as a super capacitor can endure exposure to transient surges, a system which has a super capacitor based front end has the inherent ability to survive the same.

The SRUPS developed is an on-line version where an AC-DC step-down converter consecutively charges three SC banks which in turn drive a step-up DC-AC converter which in turn drives the connected load.

The idea behind the project was to create a back-up power source that provides absolute protection to the connected load from any anomalies that should arise in the utility mains power supply. This plan has come to fruition because the three SC banks that are employed in the SRUPS employs that are consecutively switched to power the system. When one bank is being charged, the second bank is at idle while the third bank powers the inverter. Hence the connected load is powered from an inverter which is completely isolated from the mains utility as the only section that is connected to the mains supply is the charger which is charging a different SC bank. Any transient that appears on the utility power line trickles down in the worst case scenario to the SC bank that is being charged, which will be successfully absorbed by that bank.

The developed SRUPS was successfully surge tested as per IEC/IEEE transient immunity standards and the overall efficiency of the system is par with commercially available UPS systems. This project dealt with a prototype development and there is certainly scope for much development in the future.

6.2 FUTURE DEVELOPMENTS

The SRUPS developed in this project is by no means complete in its development. There are several areas that can be fine-tuned to improve upon the basic ideology.

As super capacitor technology is still in its infancy, it is a costly option compared to alternative power sources like batteries; thereby currently making an SC based UPS system commercially infeasible. SC's currently have very low voltage ratings in the range of a few volts and hence need to be connected in series to obtain an appreciable voltage level capable enough to drive an inverter efficiently. This compromises the value of capacitance achieved, making the back-up time that can be provided by an SC based power supply very limited. In the future with the advance in manufacturing technology, cost of SC's would come down and also high voltage SC's could be a reality. Then such a system would be a commercially viable option.

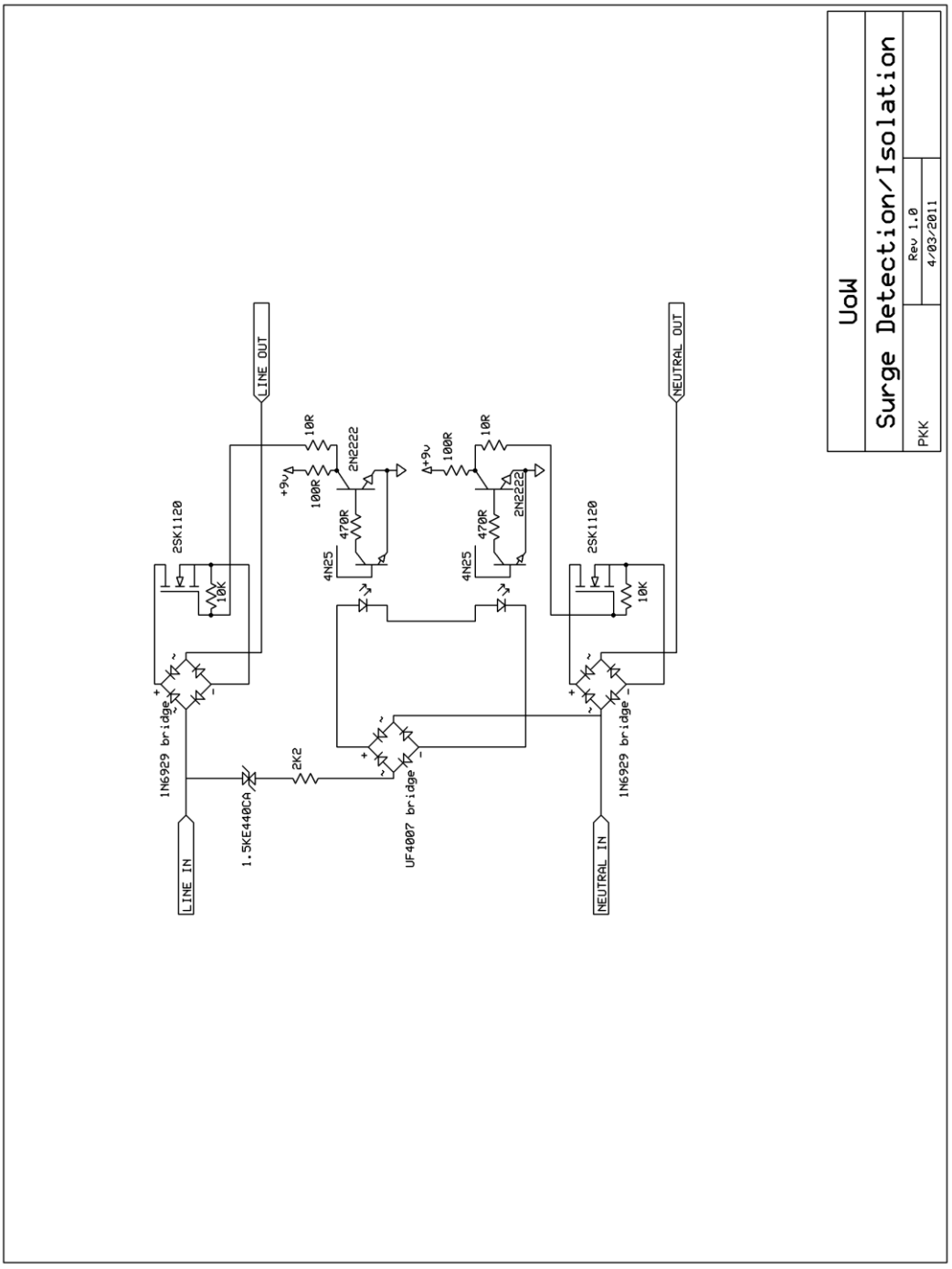
The various parts comprising the SC based SRUPS also have much leeway for improvement. Presently the over-rated components that have been used in the system are very costly and with suitable research it would be possible to de-rate them sufficiently. The charger circuit employed is a constant current charging scheme which if replaced with a constant power scheme would make it much more efficient as SC's can be charged faster under such a scheme. The inverter section uses a lossy low frequency 50Hz transformer to step-up the voltage. An efficient inverter could be developed that uses a high frequency DC to DC boost converter to step-up the voltage level thereby negating the need for a bulky AC utility mains frequency transformer. Also the different modules employed in the system uses individual microcontrollers for monitoring and control operations. Integration of these modules onto a central control system could further reduce the system complexity.

A lot was discovered and learnt during the course of the development of this project which if incorporated into the future prototyping process could vastly improve upon the present design.

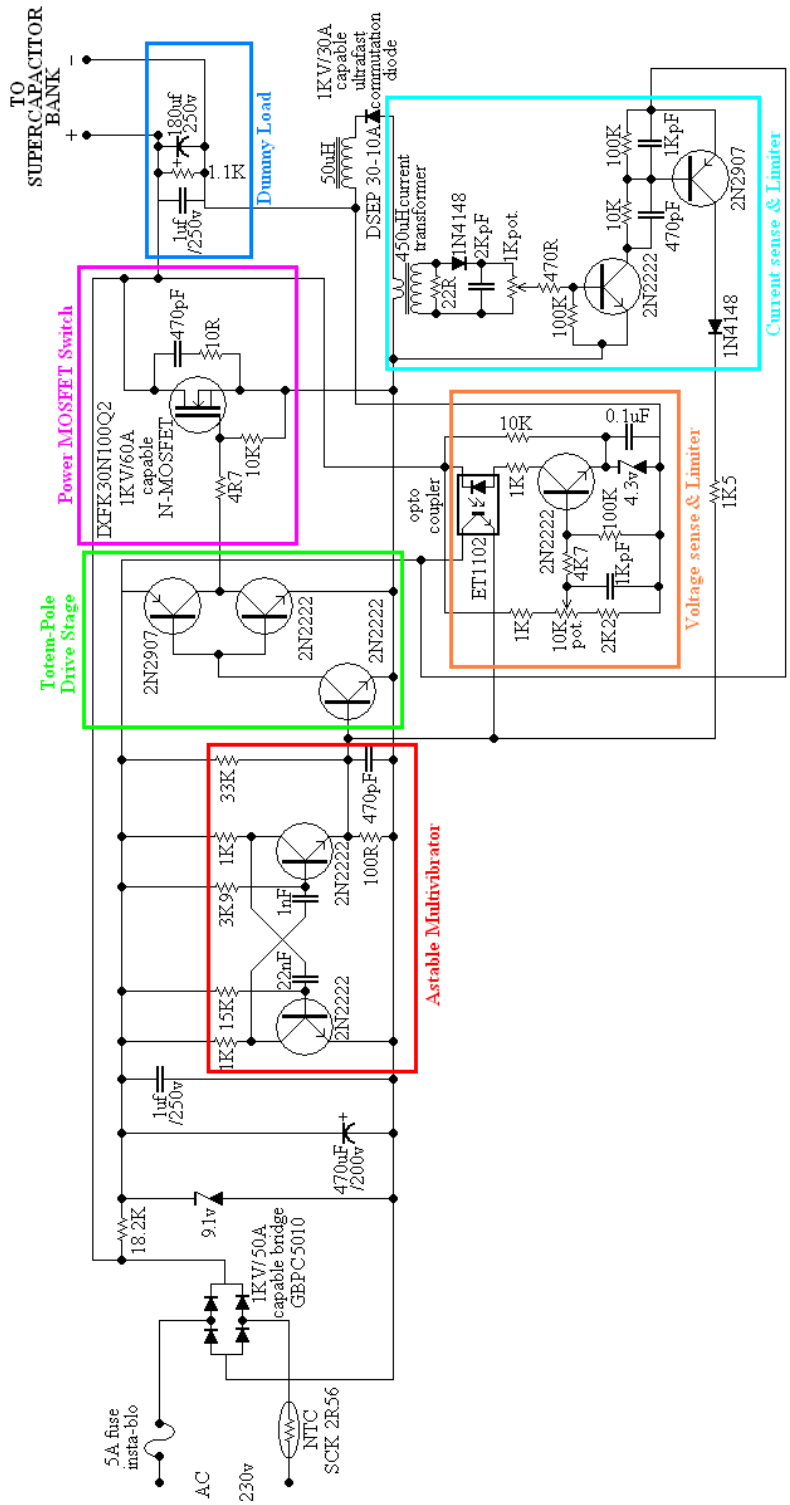
Appendices

APPENDIX 1: SCHEMATICS

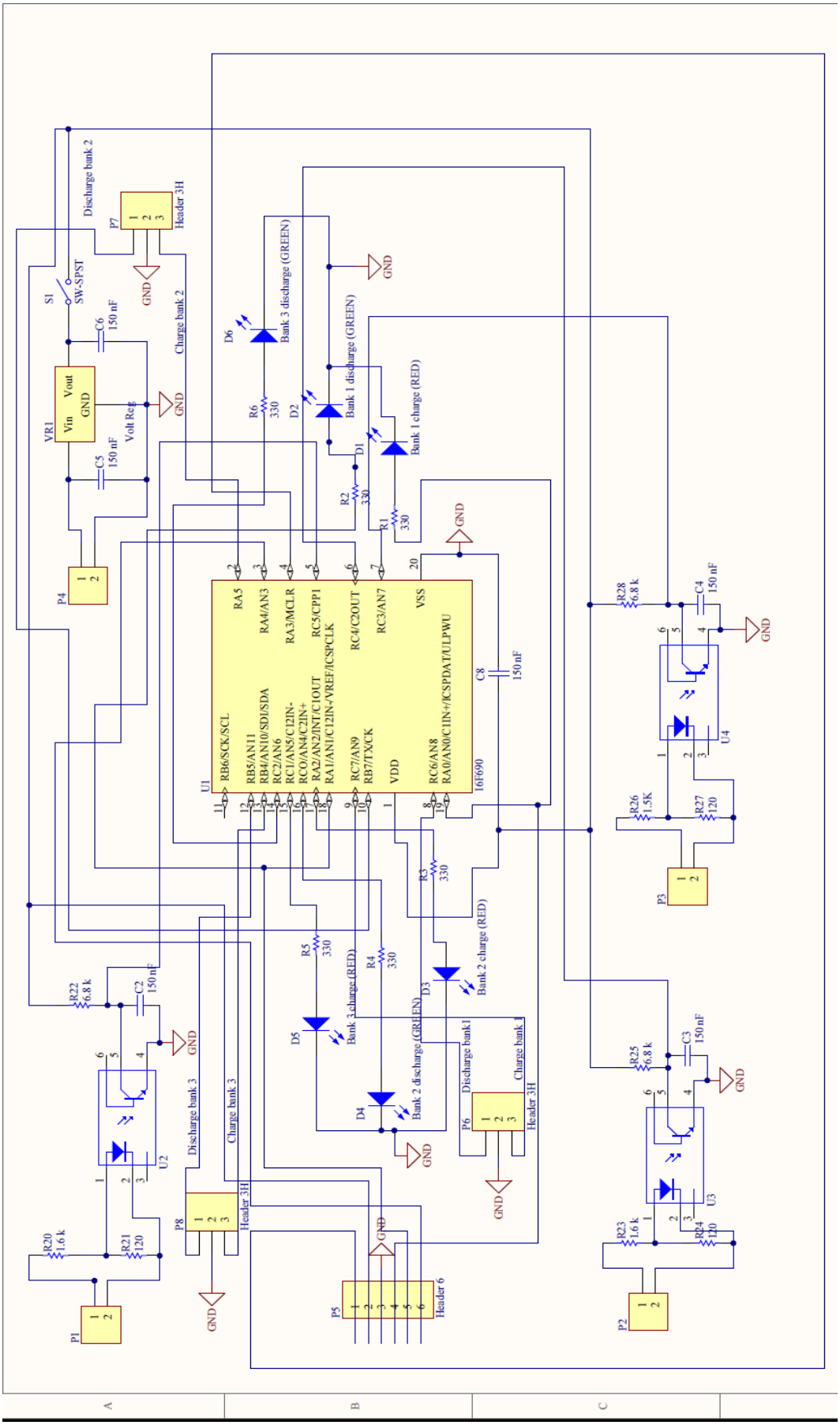
1-A) SURGE DETECTION AND ISOLATION MODULE



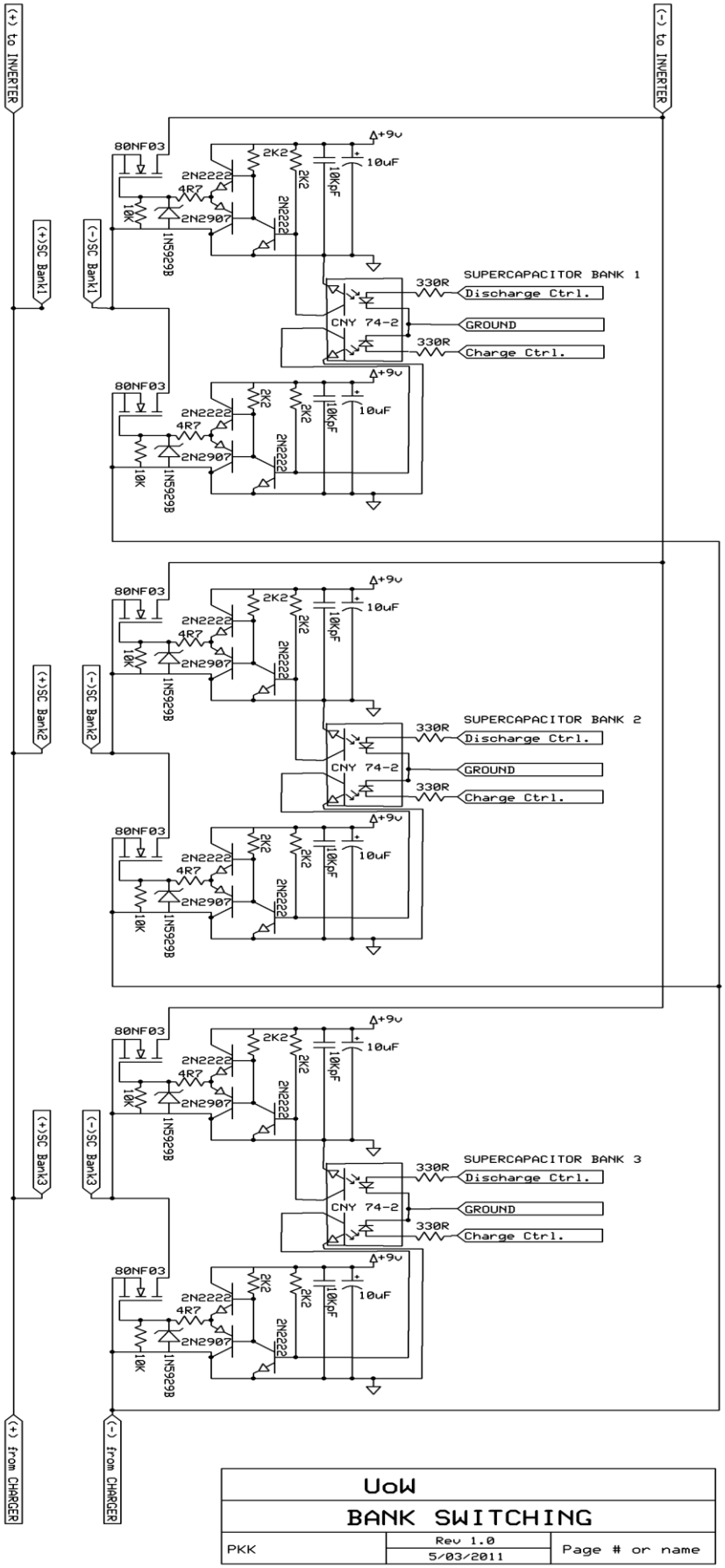
1-B) AC-DC STEP-DOWN CONVERTER



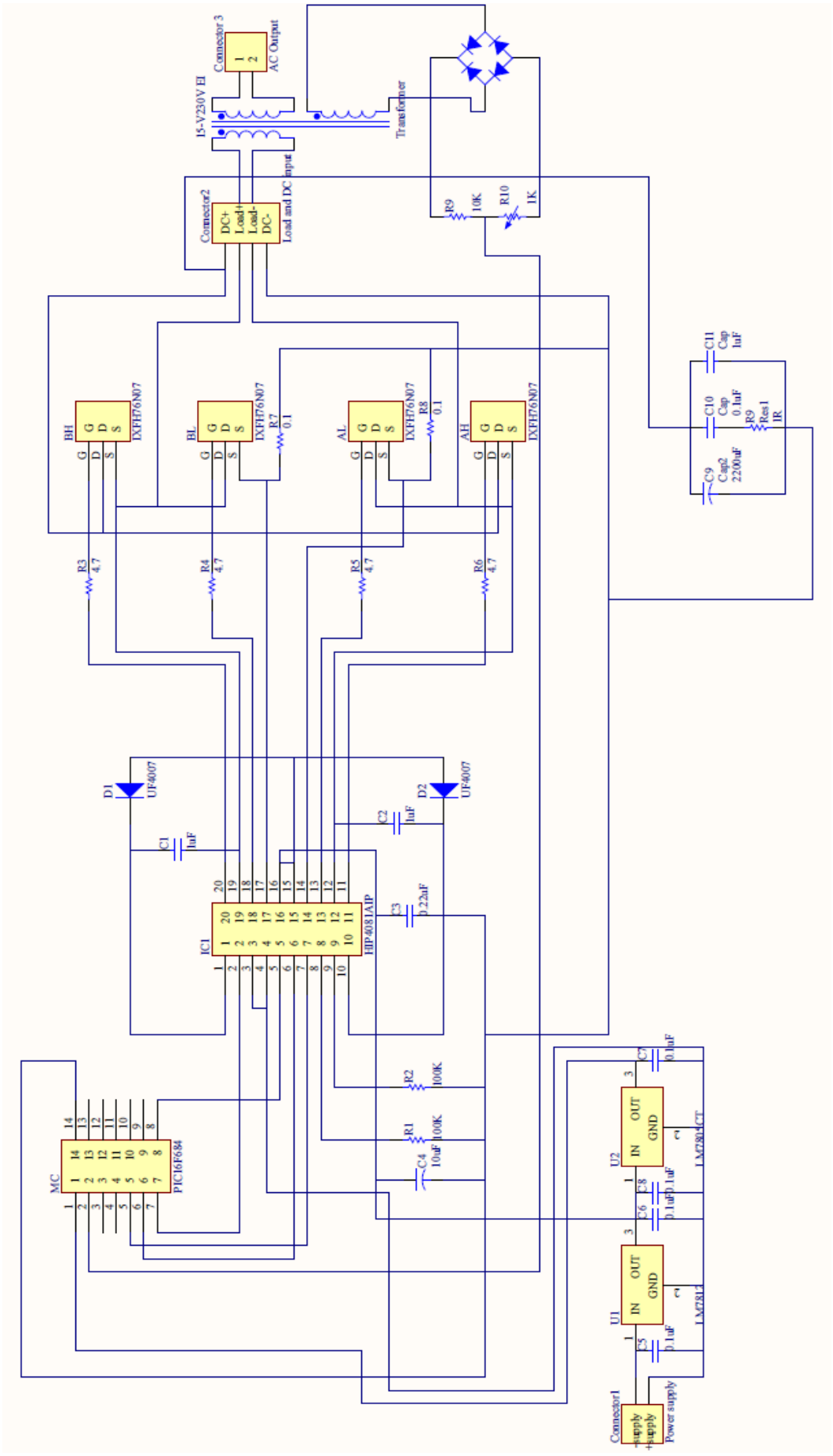
1-C) BANK SWITCHING CONTROLLER



1-D) BANK SWITCHING CIRCUIT



1-E) INVERTER


Connector3
AC Output
15-V230V EI
Transformer
Connector2
DC+
Load+
Load-
DC-
Load and DC input
R9
10K
R10
1K
BH
BL
AL
AH
IXFH76N07
R7
0.1
R8
0.1
C11
Cap
1uF
C10
Cap
0.1uF
R9
Res1
1R
C9
Cap2
2200uF
R3
4.7
R4
4.7
R5
4.7
R6
4.7
D1
UF4007
D2
UF4007
C1
1uF
C2
1uF
C3
0.22uF
IC1
HIP4081AIP
MC
PIC16F684
R2
100K
R1
100K
C4
10uF
C7
0.1uF
U2
IN
OUT
GND
LM7805CT
C8
0.1uF
C6
0.1uF
U1
IN
OUT
GND
LM7812
C5
0.1uF
Connector1
+supply
-supply
Power supply

APPENDIX 2:MICROCONTROLLER CODING

2-A)BANK SWITCHING CONTROLLER

```
/*
Filename :              SC16F690.c
Author   :                  PKK
Date     :              01.10.2010
Description:      Super Capacitor Bank Switching Controller
*/
#include <pic.h>
#include <stdlib.h>
__CONFIG(INTIO & WDTDIS & MCLRDIS & UNPROTECT &
PWRTDIS & BORDIS);
//Led's to display status of each banka charge status is shown by RED LED
//discharge status is shown by GREEN LED
#define BANK1_CHARGE_DISP       RA0
#define BANK1_DISCHARGE_DISP    RA1
#define BANK2_CHARGE_DISP       RA2
#define BANK2_DISCHARGE_DISP    RC0
#define BANK3_CHARGE_DISP       RC1
#define BANK3_DISCHARGE_DISP    RC2
//Input signal to 2 MOSFET in each SC bank.One to charge the SC and the
other
//to discharge the SC
#define BANK1_CHARGE            RC4
#define BANK1_DISCHARGE             RC5
#define BANK2_CHARGE            RA5
#define BANK2_DISCHARGE             RB7
#define BANK3_CHARGE            RB4
#define BANK3_DISCHARGE             RB5
//Bank 1 sense is RC6/AN8
//Bank 2 sense is RC7/AN9
//Bank 3 sense is RC3/AN7
#define ON_MOSFET 1
#define OFF_MOSFET 0
```

```
//ADC 10 bit values
#define HIGH_READING 976                    //75
#define LOW_READING  1023   //978
//Defining common definitions
#define ON 1                                        //Define ON
as digital 1
#define OFF 0
        //Define OFF as digital 0
#define CLEAR 0
        //Define CLEAR as digital 0
#define TIMER1 TMR1ON                               //Set this bit
start the timer and vice versa.
//Variables
short unsigned int pTMR1 @ 0x0E;            //16 bits of timer1
are named as pTMR1
short unsigned int i;                               //Used in loop
short unsigned int j;
unsigned char final_voltage_reading;
unsigned char voltage_reading[10];
unsigned short int bank1_final_voltage;
unsigned short int bank2_final_voltage;
unsigned short int bank3_final_voltage;
//short unsigned int pTMR1 @ 0x0E;
unsigned int timer1_tick;
bit bank1_charged;
bit bank1_discharged;
bit bank2_charged;
bit bank2_discharged;
bit bank3_charged;
bit bank3_discharged;
unsigned int average_voltage;
char temp;                                          //Used
to ADC value generate by the switches
//Defining functions
```

```
//Function which returns the 8 bit adc value when called.Remember to set the
proper chanel
//before calling this function.
unsigned short int read_adc(void)
{
unsigned short int temp_adc_results;        //Used in read_adc function
GODONE = 1;
while(GODONE);
temp_adc_results = 0;                                   //Reset
temp_adc_results
temp_adc_results = ADRESH;                              //Copy 8 bit
ADRESH to temp_adc_resutls.
temp_adc_results <<=8;
temp_adc_results = temp_adc_results|ADRESL;
return temp_adc_results;                            //Return 8 bit ADC value
}//read_adc
delay_a_bit(void){
for(j=0;j<10000;j++);
}unsigned short int average_adc_value(void)
{
        unsigned short int voltage = 0;
        for (i=0;i<10;i++){
        voltage +=read_adc();
        }
        voltage /=10;
        return voltage;
}
select_switch_channel(void)
{
//AN0 (RA0) is connected to switches
        ADCON0 = 0B00000001;                                    //Bit 7 = 0
(Left justified)

        //Bit 6 = 0 (Reference bit VDD)
```

```
        //Bit 5 unimplemented

        //Bit 4,3,2 = 0,0,0 (Channel 00 AN0)

        //Bit 1=0 ADC conversion not yet started

        //Bit 0 = 1 ADC converter is on

}//select_switch_channel
//Function which used select the proper capacitor bank for ADC
select_bank1_sense_channel(void){
//AN5 (RC1 connected to optocoupler
        ADCON0 = 0B10100001;                    //Bit 7 = 1
(Right justified)

        //Bit 6 = 0 (Reference bit VDD)


        //Bit 5,4,3,2 = 1,0,0,0 (Channel 04 AN8)

        //Bit 1=0 ADC conversion not yet started

        //Bit 0 = 1 ADC converter is on
}//select_current_sense_channel
select_bank2_sense_channel(void){
//AN5 (RC1 connected to optocoupler
        ADCON0 = 0B10100101;                    //Bit 7 = 1
(Right justified)

        //Bit 6 = 0 (Reference bit VDD)


        //Bit 5,4,3,2 = 1,0,0,1 (Channel 04 AN9)
```

```
        //Bit 1=0 ADC conversion not yet started

        //Bit 0 = 1 ADC converter is on
}//select_current_sense_channel
select_bank3_sense_channel(void){
//AN5 (RC1 connected to optocoupler
        ADCON0 = 0B10011101;                                    //Bit 7 = 1
(Right justified)

        //Bit 6 = 0 (Reference bit VDD)



        //Bit 5,4,3,2 = 0,1,1,1 ( AN7)

        //Bit 1=0 ADC conversion not yet started

        //Bit 0 = 1 ADC converter is on
}//select_current_sense_channel
bank1_status_charge(void){
        BANK1_CHARGE_DISP = ON;
        BANK1_DISCHARGE_DISP = OFF;
}
bank1_status_discharge(void){
        BANK1_CHARGE_DISP = OFF;
        BANK1_DISCHARGE_DISP = ON;
}
bank2_status_charge(void){
        BANK2_CHARGE_DISP = ON;
        BANK2_DISCHARGE_DISP = OFF;
}
bank2_status_discharge(void){
        BANK2_CHARGE_DISP = OFF;
        BANK2_DISCHARGE_DISP = ON;
}
```

```
bank3_status_charge(void){
        BANK3_CHARGE_DISP = ON;
        BANK3_DISCHARGE_DISP = OFF;
}
bank3_status_discharge(void){
        BANK3_CHARGE_DISP = OFF;
        BANK3_DISCHARGE_DISP = ON;
}
bank1_status_idle(void){
        BANK1_CHARGE_DISP = ON;
        BANK1_DISCHARGE_DISP = ON;
}
bank2_status_idle(void){
        BANK2_CHARGE_DISP = ON;
        BANK2_DISCHARGE_DISP = ON;
}

bank3_status_idle(void){
        BANK3_CHARGE_DISP = ON;
        BANK3_DISCHARGE_DISP = ON;
}
bank1_status_dead(void){
        BANK1_CHARGE_DISP = OFF;
        BANK1_DISCHARGE_DISP = OFF;
}
bank2_status_dead(void){
        BANK2_CHARGE_DISP = OFF;
        BANK2_DISCHARGE_DISP = OFF;
}
 bank3_status_dead(void){
        BANK3_CHARGE_DISP = OFF;
        BANK3_DISCHARGE_DISP = OFF;
}
void main(void){
//Initialize variables
```

```
i = 0;
j = 0;
//Speed is 8 Mhz
IRCF2 = 1;
IRCF1 = 1;
IRCF0 = 1;
//Setup ADC clock
ADCON1 = 0B01010000;                    //Bit 6,5,4 =
101(Fosc/16)
//Set up Digital ports
ANSEL = 0B10000000;                     // AN7
is analog input
ANSELH = 0B00000011;                    //AN 8 and
AN9 are analog inputs
//Set up Port A
TRISA = 0;                              //All
porta pins are outputs
TRISB = 0;                              //All
portb pins are outputs
TRISC = 0B11001000;
        //RC7,RC6 and RC3 are inputs.All other outputs
BANK1_CHARGE = OFF_MOSFET;
BANK1_DISCHARGE = OFF_MOSFET;
BANK2_CHARGE = OFF_MOSFET;
BANK2_CHARGE = OFF_MOSFET;
BANK3_CHARGE = OFF_MOSFET;
BANK3_DISCHARGE = OFF_MOSFET;
BANK1_CHARGE_DISP = 1;
for(i=0;i<8000;i++);
BANK1_CHARGE_DISP = 0;
for(i=0;i<8000;i++);
BANK1_DISCHARGE_DISP = 1;
for(i=0;i<8000;i++);
BANK1_DISCHARGE_DISP = 0;
for(i=0;i<8000;i++);
```

```
BANK2_CHARGE_DISP = 1;
for(i=0;i<8000;i++);
BANK2_CHARGE_DISP = 0;
for(i=0;i<8000;i++);
BANK2_DISCHARGE_DISP = 1;
for(i=0;i<8000;i++);
BANK2_DISCHARGE_DISP = 0;
for(i=0;i<8000;i++);
BANK3_CHARGE_DISP = 1;
for(i=0;i<8000;i++);
BANK3_CHARGE_DISP = 0;
for(i=0;i<8000;i++);
BANK3_DISCHARGE_DISP = 1;
for(i=0;i<8000;i++);
BANK3_DISCHARGE_DISP = 0;
//Determining status of SC bank
1*****************************************************************
select_bank1_sense_channel();
bank1_final_voltage = average_adc_value();
if(bank1_final_voltage<HIGH_READING){                    //Capacitor
already charged to required value
        bank1_charged = 1;                              //Clear charged flag
//change everthing to bank1_charged
        bank1_discharged = 0;                           //Clear discharged
flag
        bank1_status_idle();
}
delay_a_bit();
select_bank2_sense_channel();
bank2_final_voltage = average_adc_value();
if(bank2_final_voltage<HIGH_READING){                    //Capacitor
already charged to required value
        bank2_charged = 1;                              //Clear charged flag
//change everthing to bank1_charged
```

```
        bank2_discharged = 0;                    //Clear discharged
flag
        bank2_status_idle();
}
delay_a_bit();
select_bank3_sense_channel();
bank3_final_voltage = average_adc_value();

if(bank3_final_voltage<HIGH_READING){            //Capacitor
already charged to required value

        bank3_charged = 1;                       //Clear charged flag
//change everthing to bank1_charged
        bank3_discharged = 0;                    //Clear discharged
flag
        bank3_status_idle();

}
select_bank1_sense_channel();
bank1_final_voltage = average_adc_value();
bank1_status_charge();
while(bank1_final_voltage>HIGH_READING){         //If the
capacitor is not charged do this while loop
        BANK1_CHARGE = ON_MOSFET;
        bank1_final_voltage = average_adc_value();//until it is charged

}
bank1_status_idle();
BANK1_CHARGE = OFF_MOSFET;
select_bank2_sense_channel();
bank2_final_voltage = average_adc_value();
bank2_status_charge();
while(bank2_final_voltage>HIGH_READING){         //If the
capacitor is not charged do this while loop
```

```
        BANK2_CHARGE = ON_MOSFET;
        bank2_final_voltage = average_adc_value();//until it is charged
}
bank2_status_idle();
BANK2_CHARGE = OFF_MOSFET;
select_bank3_sense_channel();
bank3_final_voltage = average_adc_value();
bank3_status_charge();
while(bank3_final_voltage>HIGH_READING){                    //If the
capacitor is not charged do this while loop
        bank3_status_charge();
        BANK3_CHARGE = ON_MOSFET;
        bank3_final_voltage = average_adc_value();//until it is charged
}
bank3_status_idle();
BANK3_CHARGE = OFF_MOSFET;
//All the capacitors are charged now start discharging capacitor 1
select_bank1_sense_channel();
bank1_final_voltage = average_adc_value();
bank1_status_discharge();
//Wait till bank 1 discharges
while(bank1_final_voltage<LOW_READING){
        bank1_status_discharge();
        BANK1_DISCHARGE = ON_MOSFET;
        bank1_final_voltage = average_adc_value();
}
BANK1_DISCHARGE = OFF_MOSFET;
//bank 1 is discharged.Now discharged bank 2 while charging bank 1
while(1==1){
        bank1_status_charge();
        bank2_status_discharge();
        BANK1_CHARGE = ON_MOSFET;
        BANK2_DISCHARGE = ON_MOSFET;
        select_bank1_sense_channel();
        bank1_final_voltage = average_adc_value();
```

```
        select_bank2_sense_channel();
        bank2_final_voltage = average_adc_value();
        while((bank2_final_voltage<LOW_READING) |
(bank1_final_voltage>HIGH_READING)){
                select_bank1_sense_channel();
                bank1_final_voltage = average_adc_value();

                if(bank1_final_voltage<HIGH_READING){
                        bank1_status_idle();
                        BANK1_CHARGE = OFF_MOSFET;
                }
                select_bank2_sense_channel();
                bank2_final_voltage = average_adc_value();
                if(bank2_final_voltage > LOW_READING){
                        bank2_status_dead();
                        BANK2_DISCHARGE = OFF_MOSFET;
                }
        }
        //At this point bank 1 is in idle.Bank 2 is discharged and bank 3 has
started to discharge.Now
        //charge bank 2 while discharging bank 3.
        bank2_status_charge();
        bank3_status_discharge();
        BANK2_CHARGE = ON_MOSFET;
        BANK3_DISCHARGE = ON_MOSFET;
        //bank 1 is discharged.Now discharged bank 2 while charging bank 1
        select_bank2_sense_channel();
        bank1_final_voltage = average_adc_value();
        select_bank3_sense_channel();
        bank3_final_voltage = average_adc_value();
        while((bank3_final_voltage<LOW_READING) |
(bank2_final_voltage>HIGH_READING)){
                select_bank2_sense_channel();
                bank2_final_voltage = average_adc_value();
```

```
                if(bank2_final_voltage<HIGH_READING){
                        bank2_status_idle();
                        BANK2_CHARGE = OFF_MOSFET;
                }

                select_bank3_sense_channel();
                bank3_final_voltage = average_adc_value();

                if(bank3_final_voltage > LOW_READING){
                        bank3_status_dead();
                        BANK3_DISCHARGE = OFF_MOSFET;
                }
        }
        //At this point bank 2 is idle.Bank 3 is full discharge .Now discharge
bank 1 while chargign bank 3
        bank3_status_charge();
        bank1_status_discharge();
        BANK3_CHARGE = ON_MOSFET;
        BANK1_DISCHARGE = ON_MOSFET;
        //bank 1 is discharged.Now discharged bank 2 while charging bank 1
        select_bank3_sense_channel();
        bank3_final_voltage = average_adc_value();
        select_bank1_sense_channel();
        bank1_final_voltage = average_adc_value();
        while((bank1_final_voltage<LOW_READING) |
(bank3_final_voltage>HIGH_READING)){
                select_bank3_sense_channel();
                bank3_final_voltage = average_adc_value();
                if(bank3_final_voltage<HIGH_READING){
                        bank3_status_idle();
                        BANK3_CHARGE = OFF_MOSFET;
                }
                select_bank1_sense_channel();
                bank1_final_voltage = average_adc_value();
                if(bank1_final_voltage > LOW_READING){
```

```
                    bank1_status_dead();
                    BANK1_DISCHARGE = OFF_MOSFET;
                }
        }
        bank1_status_dead();
}//while
while(1==1){
//bank1_status_discharge();
//delay_a_bit();
//bank1_status_dead();
//delay_a_bit();
}
}//main
```

2-B) INVERTER

```
/*
Filename :          SC16F684.c
Author     :            PKK
Date     :          01.04.2010
```

```
Description:        Inverter
*/

#include <p16F684.h>

#define     TRUE        1;
#define     FALSE           0;
#define     RUN_LED         LATBbits.LATB4

//---------------------------------------------------------------------------

void main (void);
void Initialise(void);
void InitialisePWMValues(void);
void InterruptHandlerHigh (void);

unsigned char       PWMIndexA;
unsigned char       PWMIndexB;
volatile char   UpdatePWM;
volatile int    mSecCounter;
int     LegA[80];
//int   LegB[80];

//---------------------------------------------------------------------------
void main()
{
        Initialise();

        InitialisePWMValues();

        RUN_LED = 1;
        PWMIndexA = 0;
        PWMIndexB = 40;
        mSecCounter = 0;
        UpdatePWM = FALSE;
```

```
PTCON1bits.PTEN  = 1;     //        PWM time base is ON.

while(1)
{
        if(UpdatePWM)
        {
                LATCbits.LATC3 = 1;

                UpdatePWM = FALSE;

                PDC0L         = LegA[PWMIndexA];
                PDC0H         = (LegA[PWMIndexA]>>8);
                PDC1L         = LegA[PWMIndexB];
                PDC1H         = (LegA[PWMIndexB]>>8);
                PWMIndexA += 2;
                PWMIndexB += 2;

                if(PWMIndexA >= 80)
                {
                        PWMIndexA = 0;
                        PWMIndexB = 40;
                }
                if(PWMIndexB >= 80)
                {
                        PWMIndexB = 0;
                }
        }

        if(mSecCounter >=100)
        {
                ClrWdt();

                mSecCounter = 0;
```

```
                    if(RUN_LED == 0)
                    {
                        RUN_LED = 1;
                    }
                    else
                    {
                        RUN_LED = 0;
                    }
                }

        }       //      End of while()

}

//---------------------------------------------------------------------------

void Initialise()
{

        TRISA       = 0b00000000;
        TRISB       = 0b00000000;
        TRISC       = 0b00000000;
        LATC = 0b00000000;

        RCONbits.IPEN     = 1;    //      Enable priority levels on
Interrupts.
        INTCON      = 0b11100000;       //      Enable interrupts.

        TMR0L       = 0xF0;       //      Set TMR0 H/L = 0xD8F0
(55536dec) for 1ms interrupt.
        TMR0H       = 0xD8;
        T0CON       = 0b10001000;

        DTCON       = 0b01000100;               //      Dead time 4*100nS=
400nS
```

```
        FLTCONFIG = 0b00000000;             //      Disable FLTA and
FLTB pins.

        PTPERL      = 0xC4;             //      PTPER H/L = 0x09C4 =
2500DEC = 250uS @ 10MHz.
        PTPERH      = 0x09;

        PTMRL       = 0x00;
        PTMRH       = 0x00;

        PDC0L       = 0xE2;
        PDC0H       = 0x04;
        PDC1L       = 0xE2;
        PDC1H       = 0x04;
        PTCON0      = 0b00000010;       //      PWM in UP/DOWN mode.
        PWMCON0     = 0b00110000;       //      PWM0..3 enabled in
complementry mode.

        PIE3bits.PTIE       = 1;    //      Enable PWM Timebase interrupt;
        IPR3bits.PTIP       = 1;    //      Set PWM Timebase interrupt high
priority.
        PIR3bits.PTIF       = 0;    //      Clear interrupt.

}

//---------------------------------------------------------------------------

void InitialisePWMValues()
{
        int i;

        LegA[0] = 1291;
        LegA[1] = 1364;
        LegA[2] = 1451;
        LegA[3] = 1513;
```

LegA[4] = 1606;

LegA[5] = 1657;

LegA[6] = 1752;

LegA[7] = 1791;

LegA[8] = 1884;

LegA[9] = 1913;

LegA[10] = 2000;

LegA[11] = 2020;

LegA[12] = 2096;

LegA[13] = 2109;

LegA[14] = 2170;

LegA[15] = 2177;

LegA[16] = 2220;

LegA[17] = 2224;

LegA[18] = 2246;

LegA[19] = 2247;

LegA[20] = 2247;

LegA[21] = 2246;

LegA[22] = 2224;

LegA[23] = 2220;

LegA[24] = 2177;

LegA[25] = 2170;

LegA[26] = 2109;

LegA[27] = 2096;

LegA[28] = 2020;

LegA[29] = 2000;

LegA[30] = 1913;

LegA[31] = 1884;

LegA[32] = 1791;

LegA[33] = 1752;

LegA[34] = 1657;

LegA[35] = 1606;

LegA[36] = 1513;

LegA[37] = 1451;

LegA[38] = 1364;

```
LegA[39] = 1291;
LegA[40] = 1212;
LegA[41] = 1129;
LegA[42] = 1061;
LegA[43] = 970;
LegA[44] = 914;
LegA[45] = 819;
LegA[46] = 775;
LegA[47] = 680;
LegA[48] = 646;
LegA[49] = 556;
LegA[50] = 532;
LegA[51] = 450;
LegA[52] = 433;
LegA[53] = 365;
LegA[54] = 354;
LegA[55] = 302;
LegA[56] = 296;
LegA[57] = 264;
LegA[58] = 261;
LegA[59] = 250;
LegA[60] = 250;
LegA[61] = 261;
LegA[62] = 264;
LegA[63] = 296;
LegA[64] = 302;
LegA[65] = 354;
LegA[66] = 365;
LegA[67] = 433;
LegA[68] = 450;
LegA[69] = 532;
LegA[70] = 556;
LegA[71] = 646;
LegA[72] = 680;
LegA[73] = 775;
```

```
        LegA[74] = 819;
        LegA[75] = 914;
        LegA[76] = 970;
        LegA[77] = 1061;
        LegA[78] = 1129;
        LegA[79] = 1212;

        for(i=0; i<80; i++)
        {
                LegA[i] = 4*LegA[i];
        }

}

//------------------------------------------------------------------------

// High priority interrupt vector
#pragma code InterruptVectorHigh = 0x08
void
InterruptVectorHigh (void)
{
  _asm
    goto InterruptHandlerHigh //jump to interrupt routine
  _endasm
}

//------------------------------------------------------------------------
// High priority interrupt routine

#pragma code
#pragma interrupt InterruptHandlerHigh

void
InterruptHandlerHigh ()
{
```

```
        if(INTCONbits.TMR0IF)    // Check for TMR0 overflow.
   {
                INTCONbits.TMR0IF = 0;  // Clear interrupt flag.
                TMR0L       = 0xF0;         //      Reload timer.
                TMR0H       = 0xD8;         //      Set TMR0 H/L = 0xD8F0
(55536dec) for 1ms interrupt.
                mSecCounter++;
   }
        else if(PIR3bits.PTIF)              //      Check for PWM Timebase
interrupt
        {
                PIR3bits.PTIF = 0;          //      Clear interrupt.
                UpdatePWM = TRUE;
        }

}

//---------------------------------------------------------------------------
```

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