A simple microcontroller based digital lock-in amplifier for the detection of low level optical signals

Adrian A. Dorrington and Rainer Künnemeyer
Department of Physics and Electronic Engineering
University of Waikato, Private Bag 3105
Hamilton, New Zealand.
E-mail: a.dorrington@waikato.ac.nz

Abstract

Traditionally digital lock-in amplifiers sample the input signal at a rate much higher than the lock-in reference frequency and perform the lock-in algorithm with high-speed processors. We present a small and simple digital lock-in amplifier that uses a 20 bit current integrating analogue-to-digital converter interfaced to a microcontroller. The sample rate is set to twice the reference frequency placing the sampled lock-in signal at the Niquest frequency allowing the lock-in procedure to be performed with one simple algorithm. This algorithm consists of a spectral inversion technique integrated into a highly optimised low-pass filter. We demonstrate a system with a dynamic range of 103dB recovering signals up to 85dB below the interference.

1. Introduction

Detecting low-level, slowly varying optical signals, common in many optical measurement situations, is often difficult due to the presence of high-level, low frequency optical interference and low frequency (1/f) noise. A solution to this problem is to use an intensity modulated optical source and a lock-in detection system. Modulating the source shifts the measuring signal up the frequency spectrum and away form the low frequency noise. A lock-in amplifier (LIA) is then used to demodulate and recover the signal while removing the noise and interference. The history and background theory of digital and analogue LIAs is well documented elsewhere [1-4] and will not be discussed here.

Many of our optical sensor projects suffer from the above mentioned problems. We have therefore designed a simple, re-configurable, high performance, digital LIA that is small and simple enough to be included as part of a larger instrument.

Most digital LIAs use a 16-bit analogue-to-digital converter (ADC), which limits the system's dynamic range. These ADCs are run at sample rates much greater than the lock-in reference frequency requiring high speed signal processing such as a desktop computer [5,6] or a digital signal processor [4]. Our design is different to most digital lock-in systems because we chose to set our sample rate to twice the lock-in frequency, providing one sample per half cycle of the reference signal. In addition, we utilise the advantages of an integrating 20-bit ADC.

2. Optimised Digital Lock-in Algorithm

Wang [7] reports a digital lock-in amplifier that realizes the demodulation process by accumulating all samples during the positive half cycles of the reference signal and subtracts the samples during the negative half cycle. This method is computationally efficient but does not completely eliminate the low frequency noise. The underlying principle is to calculate the difference between the average of the input during each half cycle of the reference signal, thereby finding the amplitude of the signal at the reference frequency. However, this process also calculates the derivative of any low frequency input signals. This is a major disadvantage of Wang's algorithm, which limits its use in high dynamic range applications.

However, the process of accumulating samples during reference signal half cycles is still an option. It can be considered as a down-sampling process reducing the sample rate to twice the reference frequency. The reference signal and the detected modulated signal now correspond to the Niquest frequency. The principle of an analogue lock-in amplifier can now be applied using the well-known technique for spectral inversion of a sampled signal, which is swapping the sign of every second sample. A digital low-pass filter can then remove the noise that now resides in the vicinity of the Niquest frequency. This method is summarised in figure 1.

Proceedings of the First IEEE International Workshop on Electronic Design, Test and Applications (DELTA'02)
0-7695-1453-7/02 $17.00 © 2002 IEEE

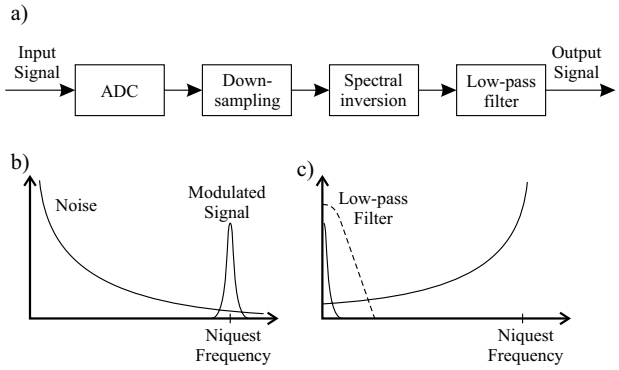

Figure 1. Conceptual illustration of proposed digital lock-in amplifier operations. Diagram a illustrates the signal flow through the system. Diagram b shows the spectrum of the input signal, and diagram c shows the spectrally inverted sampled signal and the response of the low-pass filter.

3. Microcontroller based implementation

For our optical lock-in detector system we chose the DDC112 (Texas Instruments Inc., Dallas TX, USA) as our ADC for two important reasons. This ADC has a current integrating input capable of single bit resolution as low as 94 fA (which is ideal for sampling low level photo-detector outputs) and automatically provides the accumulation process described above. It also has a 20 bit resolution providing a wide dynamic range useful for sampling low level optical signals in the presence of relatively high ambient light levels. The main disadvantages of the DDC112 are its 2 kHz maximum sampling rate and its mismatched integration capacitors.

An 89c8252 (Atmel Corporation, San Jose CA, USA) 8-bit microcontroller is interfaced to the DDC112. This microcontroller was chosen for its on-chip EEROM program memory, ease of interface to the DDC112, and compatibility with industry standard 8051 development tools.

Digital filtering can be a time consuming task, especially for an 8-bit microcontroller performing 32 bit mathematical operations. Therefore, filtering the sampled data in real time requires a highly optimised algorithm. A single pole 2.5Hz Butterworth low-pass filter (operating at a 2 kHz sample rate) was selected because its coefficients are all multiples of 1/256, which is an easy division for the microcontroller. The expression for this filter (rearranged for easier coding into the microcontroller) is

$$y_n = \frac{x_n}{256} + \frac{x_{n-1}}{256} + y_{n-1} - \frac{y_{n-1}}{256} - \frac{y_{n-1}}{256} \qquad 1$$

where y is the output, x is the input, and n is the sample number.

To conserve processor time, the spectral inversion was integrated into the filter algorithm by using two filter expressions each with one of the input terms negated. The expressions

$$y_n = -\frac{x_n}{256} + \frac{x_{n-1}}{256} + y_{n-1} - \frac{y_{n-1}}{256} - \frac{y_{n-1}}{256} \qquad 2$$

and

$$y_n = \frac{x_n}{256} - \frac{x_{n-1}}{256} + y_{n-1} - \frac{y_{n-1}}{256} - \frac{y_{n-1}}{256} \qquad 3$$

are used alternatively as a complete digital lock-in amplifier. The result is then down-sampled by averaging 200 samples providing an output with a rate of 10 Hz.

In a microprocessor, a division by any power of two (2^n where n is a positive integer) can be efficiently performed with the use of bit-shifting operations. Moreover, by performing the calculations with unsigned variables the divided by 256 value can be obtained by storing a zero in the immediately preceding memory location and reading from that location, as illustrated in figure 2. Because the program is simply reading a value from a different memory location, the division consumes no additional processor time. In C or C++ this division can be coded easily using a union.

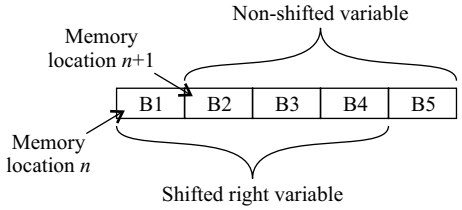

Figure 2. Memory addressing divide by 256 operation. By choosing to address a variable at location *n* or location *n*+1 either an 8 bit right shifted or a non-shifted value can be read, as long as a zero value byte is stored in location *n*.

To make efficient use of time and to provide continuous sampling the DDC112 utilises two integration capacitors, one of which is integrating charge while the charge in the other is being digitised [8]. Unfortunately, there can be a mismatch between these capacitors of up to 0.5% of the full-scale input value. When sampling a low frequency signal, the slight differences between alternating samples appears to the lock-in algorithm as a valid signal, and hence these errors significantly reduce the dynamic range of the system.

To compensate for the mismatch a calibration procedure has been implemented. A series of eight DC levels covering the full input range are applied to the DDC112, and 256 samples from each integration capacitor are averaged. For each of the DC input levels the difference between the two values is calculated. A

linear regression then provides a calibration line for the mismatch error. The coefficients generated by the regression are used to generate a look-up table that is used to correct the samples obtained from one of the capacitors in real time.

However, it is not practical to create one look-up table to accommodate all 1,048,576 possible outputs from the 20 bit ADC. Instead, the least significant 8 bits, middle 8 bits, and most significant 4 bits are treated separately by using three different look-up tables. This approach requires only 528 entries in total. The disadvantage of using three look-up tables is a decrease in accuracy. Maximum errors vary from 2 to 6 ADC counts depending on the severity of the capacitor mismatch.

4. Performance evaluation

To evaluate the performance of the system, the DDC112 was set to a resolution of 294 fA per bit and was subjected to a desired input signal summed with an interfering signal. Two tests were performed with signals of amplitudes 83 pA and 16 pA (peak-to-peak) at 0.25 Hz, modulated by the square wave reference signal. For both tests, the interfering signal amplitude was 278 nA (peak-to-peak) at 100 Hz plus 148 nA DC (almost the full-scale of the ADC). The results, illustrated in figure 3, show clearly identifiable recovered signals that were originally 70 dB and 85 dB, respectively, below the interfering signal. For a constant amplitude input signal the average uncertainty is 7 ADC counts, demonstrating a dynamic range of 103dB between full scale input noise and the output noise floor.

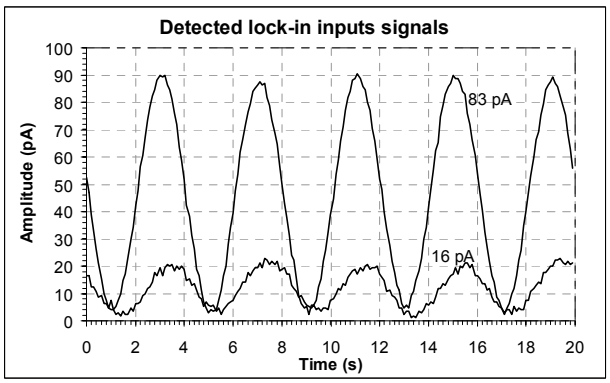

Figure 3. Detected lock-in signals. The detected signals 70 dB and 85 dB below the interfering signal.

The performance of our LIA exceeds that of commercially available digital lock-in modules (e.g. Pocket-Lockin, Electrosolutions, New Jersey, USA, or Lock-in Amplifier card model 5106, Perkin Elmer, Berkshire, UK) and approaches that of commercial DSP LIA instruments such as Perkin Elmer's Model 7280. Our device is many times smaller and cheaper but only operates at a fixed 0° phase reference and has limited ability to change the operating frequency and time constant. However, it is a unique combination of a simple, small design and high performance.

5. Conclusion

We have successfully developed a simple, high sensitivity, small, low cost digital lock-in amplifier for the detection of low-level optical signals, which has a dynamic range of 103 dB and is capable of recovering input signals in the pico-ampere range. The design contains novel solutions to problems arising form the use of a microcontroller as the central processor. Flexibility and configurability are good reasons for using a microcontroller, but the disadvantage is the poor signal processing performance. A highly optimised lock-in algorithm, based on a one sample per reference half cycle principle, has been implemented including a divide by 256 algorithm that requires minimal processor time. A real-time calibration algorithm based on multiple look-up tables has also been implemented.

6. References

[1] A. Mandelis. "Signal-to-noise ratio in lock-in amplifier synchronous detection: A generalized communications system approach with applications to frequency, time, and hybrid (rate window) photothermal measurements." *Rev. Sci. Instrum*., vol. 65, pp. 3309-3323, 1994.

[2] Analog Devices, *AD630 – Balanced Modulator/ Demodulator.* Datasheet Rev D, Analog Devices, Northwood MA, USA, 2001.

[3] P.K. Dixon and L. Wu. "Broadband digital lock-in amplifier techniques." *Rev. Sci. Instrum*., vol. 60, pp. 3329-3336, 1989.

[4] L.A. Barragan, J.I. Artigas, R. Alonso, and F. Viluendas. "A modular, low-cost digital signal processor-based lock-in card for measuring optical attenuation." *Rev. Sci. Instrum*., vol. 72, pp. 247-251, 2001.

[5] P. Probst and A. Jaquier. "Multiple-channel digital lock-in amplifier with PPM resolution." *Rev. Sci. Instrum*., vol. 65, pp. 747-750, 1994.

[6] F. Barone, E. Calloni, L. DiFiore, A. Grado, L. Milano, and G. Russo. "High-performance modular digital lock-in amplifier." *Rev. Sci. Instrum*., vol. 66, pp. 3697-3701, 1995.

[7] X. Wang. "Sensitive digital lock-in amplifier using a personal computer." *Rev. Sci. instrum*., vol. 61, pp. 1999-2001, 1990.

[8] Burr Brown, *Dual current input 20-bit analog-to-digital converter*. Datasheet, Burr Brown, USA, 2000.