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Design of SCALDO Based High-current DC Power Supply

A thesis submitted

for the degree of

Doctor of Philosophy

in Electronics Engineering

by

Thilanga Anuruddha Ariyarathna

THE UNIVERSITY OF
WAIKATO
Te Whare Wānanga o Waikato

March 2021

The University of Waikato

Abstract

Supercapacitor assisted (SCA) techniques are primarily based on supercapacitors having in the order of one million times more capacitance, together with one to two orders of magnitude smaller equivalent series resistance (ESR), compared with conventional capacitors. In the first successful SCA technique, the supercapacitor-assisted low dropout regulator (SCALDO) combined a linear regulator in series with a supercapacitor to act as a lossless voltage dropper. SCALDO created the opportunity to develop an entirely new family of highly efficient, interference-free, very-low-frequency DC-DC converters, which have evolved further into several branches over the last 6 years.

Leading data centre operators such as Google have announced their intention to move toward 48 V server rack architecture to minimise power losses in distribution lines and to improve overall operating efficiency. This thesis investigated the potential of the SCALDO technique to develop a high-current DC power supply suitable for Google server racks, meeting requirements such as electrical isolation, fast transient response, high efficiency and DC-UPS capability within the converter.

Work related to this thesis proved that by creatively extending the SCALDO technique to achieve higher current at high voltage and further developing a bulk DC-rail from AC input by extending the previously proven fast supercapacitor charger technique, a SCALDO-assisted high-current DC power supply can be achieved. As a proof-of-concept project with a DC output of 12 V (one fourth scale) at 10 A load current capability, several key circuit blocks were developed including: (i) high current discrete LDO of 10 A; (ii) four switch implementation of a SCALDO stage; and (iii) a transformer-isolated input DC stage to feed the output SCALDO stage based on a hybrid-type medium frequency switch mode. This overall implementation is expected to overcome the limitations of a direct-SCALDO stage, maintaining high end-to-end efficiency. MATLAB and LTspice simulation models were developed to observe the behaviour of these new power converter techniques.

The thesis discusses the significance of this work, related techniques, the loss-circumventing principle in the *RC* charging loop, which is the theoretical basis of SCALDO, and the design and simulation details of a novel power conversion technology. It also presents the implementation details of the prototypes built to verify this approach.

Preface

This thesis is submitted in partial fulfilment of the requirements for obtaining a PhD in Electronics Engineering at the University of Waikato, New Zealand. The work was carried out from October 2016 to March 2021 and was supervised by Associate Professor Nihal Kularatna and Associate Professor Alistair Steyn-Ross.

As outcomes of this research, three journal articles, ten peer-reviewed IEEE conference papers and a book chapter were published, as listed below.

Journal articles

1. T. Ariyarathna, N. Kularatna, K. Gunawardane, D. Jayananda, and D. A. Steyn-Ross. Development of supercapacitor technology and its potential impact on new power converter techniques for renewable energy. *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, pages 1–1, 2021
2. Thilanga Ariyarathna, Nihal Kularatna, and D. Alistair Steyn-Ross. Transformer Isolated SCALDO Based High Current DC Power Supply. *Applied Mechanics and Materials*, 884:122–128, 9 2018
3. N. Kularatna, K. Gunawardane, and T. Ariyarathna. Circumventing loss in an rc circuit leads to more efficient power converters a quick review of basic rc loop behavior. *HOW2POWER Today*, 2017

Peer reviewed IEEE conference papers

1. T. Ariyarathna, N. Kularatna, and D. A. Steyn-Ross. Upscaling supercapacitor assisted low dropout regulator for high-current and high-voltage for the 48 V DC Google rack architecture. In *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 124–129, 2020
2. T. Ariyarathna, N. Kularatna, and D. A. Steyn-Ross. Supercapacitor assisted hybrid dc-dc converter for applications powered by renewable energy sources. In *2020 2nd IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES)*, volume 1, pages 194–199, 2020
3. T. Ariyarathna, N. Kularatna, and D. A. Steyn-Ross. Batteryless ups for modern data centres: A high current extension of scaldo with distributed dc-ups. In *2020 8th International Conference on Smart Grid (icSmartGrid)*, pages 61–66, 2020
4. T. Ariyarathna, N. Kularatna, and D. A. Steyn-Ross. Supercapacitor assisted data center power architecture for 380 v dc-microgrid. In *2019 IEEE Third International Conference on DC Microgrids (ICDCM)*, pages 1–6, 2019

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9. T. Ariyarathna, N. Kularatna, and D. A. Steyn-Ross. Off-line SCALDO based high current DC power supply. In *2018 IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES)*, pages 140–145, Jan 2018
10. T. Ariyarathna, D. Jayananda, N. Kularatna, and D. A. Steyn-Ross. Potential of supercapacitors in novel power converters as semi-ideal lossless voltage droppers. In *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, pages 1429–1434, Oct 2017

Book chapter

- Thilanga Ariyarathna. Supercapacitor assisted techniques-loss management conceptswithin the resistor-capacitor loop (to be published). In *Energy Storage Devices for Electronic Systems*. Elsevier Inc, 2021

Acknowledgements

I am grateful to many individuals and institutions for making my PhD journey a success. First and foremost, I would like to express my sincere gratitude to my supervisors, Associate Professor Nihal Kularatna and Associate Professor Alistair Steyn-Ross.

Prof. Nihal Kularatna has a unique way of mentoring PhD students. He praises the practical engagement of electronics, using the motto "burning is learning". He describes "silicon seniors" as those who have burnt at least $USD 20,000 worth of components during their career. He motivated me, pointing out the light at the end of the tunnel, and encouraged us to always go the extra mile ("no pain, no gain"). He emphasised the importance of simple fundamentals and inspired me to identify innovative new solutions from a simple *RC* circuit. He mentored me to identify novel power converter topology during the early stage of my PhD. The team always benefited from his international reputation and professional network. He inspired us with tea-time stories about his early career. He created opportunities to engage with valuable industry partnerships such as the Port of Auckland LED lighting project. We were exposed to international research communities through conference travel opportunities.

Prof. Steyn-Ross mentored us with the analytical aspects of the research. He helped us to improve our academic writing skills, refining all our publications. He praised punctuality and emphasised the importance of maintaining quality. He was our guru for LaTeX and Matlab. Teaching engagement with his physics classes developed a love of the subject. Prof. Steyn-Ross's focus, commitment and professionalism were an inspiration.

I would also like to acknowledge the support received from Prof. Michael R. Mucalo, Prof. James Carson, Associate Prof. Melanie Ooi, Tanya Mete and the postgraduate office throughout this journey along with that from Prof. Jonathan B. Scott and the academic staff of the School of Engineering, Mary Dalbeth, Benson Chang, Viking Zhou, fellow member of the power electronics research group and the non-academic staff. They were always there to support us whenever we needed them. Part of the research was funded by a Waikato Doctoral Scholarship. I would like to sincerely acknowledge the support received from Gwenda Pennington and her staff in the scholarship office.

During the latter part of my PhD, I was offered an academic position at Waikato Institute of Technology (WINTEC), and the institute supported my study in many ways. I am very grateful for the generous support received from my manager, Dr. Trudy Harris, who provided the flexibility to fulfill my research commitment at the University and allocated funding to support my study.

Dedication

I dedicate this thesis—

To my wife Nayomi Udayangani
To my son Sahen Ariyarathna

for your patience throughout this journey and for sharing the hardship. Nayomi sacrificed her career to support my ambitions and take good care of our son. Sahen came to our lives in the middle of my PhD journey; he brought a lot of joy to life during this challenging time.

To my mother Mangalika Padmaseeli
To my father H.M. Ariyarathna
To my sister Thilini Nuwanthika

for taking good care of me, worrying about me from thousands of miles away and inspiring me to pursue my studies.

To my alma mater Ananda College

for giving me pride in myself and teaching me perseverance and resilience in accordance with Buddhist philosophy.

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Acronyms and Abbreviations

AC	alternating current
BBD	bidirectional break-over diodes
CPU	central processing unit
DC	direct current
DoD	depth of discharge
EDLC	electric double layer capacitor
EMI	electromagnetic interference
EPRI	electric power research institute
ESR	equivalent series resistance
ETEE	end-to-end efficiency
ICT	information and communication technology
LDO	low dropout
MOSFET	metal–oxide semiconduc-tor field-effect transistor
MOV	metal oxide varistors
NLD	nonlinear devices
PWM	pulse width modulation
RFI	radio frequency interference
rms	root-mean square
SC	supercapacitor
SCA	supercapacitor-assisted
SCAHDI	supercapacitor-assisted high density inverter
SCALDO	supercapacitor-assisted low-dropout regulator
SCALED	supercapacitor-assisted LED
SCALoM	supercapacitor-assisted loss management technique
SCASA	supercapacitor-assisted surge absorber
SCATMA	supercapacitor-assisted temperature modification apparatus
SCAWI	supercapacitor-assisted wide input
SMPS	witch-mode power supplies
SoC	state of charge
SPE	series-pass element
SRUPS	surge resistant uninterrupted power supply
UPS	uninterrupted power supply

Chapter 1

Introduction

Designing a DC power supply is a challenging task. Continuous improvements are made to achieve higher efficiency, to meet the complex requirements of modern electronics applications and to enhance the quality of output. The power supply has a direct impact on the performance of electronic appliances. This chapter discusses current trends in the power electronics world, power challenges in modern data centres, existing power converter techniques, and the need for a new design approach.

1.1 Expectations of modern power supplies and design challenges

The reliable operation of any electronic device demands a steady constant power supply through out its operation. The essential characteristics of a reliable power supply are (i) specific line and load regulation characteristics; (ii) minimum output impedance; (iii) high efficiency; (iv) predictable transient behaviour; and (v) cost-effective design [17, 18]. In addition to these primary requirements, electrical isolation, DC-UPS capability, and surge absorption are also important features.

A good-quality power supply can increase the durability of equipment and reduce electricity costs. A high-quality power supply is less than 5% of the total cost of a computer [19]. Low-quality power supplies can create issues such as freezing the computer, bad sectors on the hard disk, "blue screen of death" errors, and random resets. Low-quality power supplies can thus create severe problems in the computer, which are difficult to solve.

Personal computers have now become part of our lives, and have improved significantly since the 1980s, when computers were mainly used for small text-processing tasks or simple calculations. Today computers are used for much more complicated tasks, such as video editing, gaming, simulations, and playing music and videos. With the evolution of the computer processor, power consumption has also rapidly increased. The computer power supply needs to be capable of producing stable power and maintaining it throughout the operation. Figure 1.1 illustrates the energy utilization inside a computer. The CPU is the most power-hungry component. Figure 1.2 depicts the trend data for microprocessors over the last 40 years.

Processor manufacturers such as Intel publish specifications for power supplies with their products. Typical standards for power supplies have DC output voltage regulation requirement, typical power distribution requirements such as efficiency, physical dimensions and maximum allowed electromagnetic interference (EMI) levels [21]. Also power supplies require protection against input over current, input under-voltage, catastrophic failure, short circuit, over-voltage

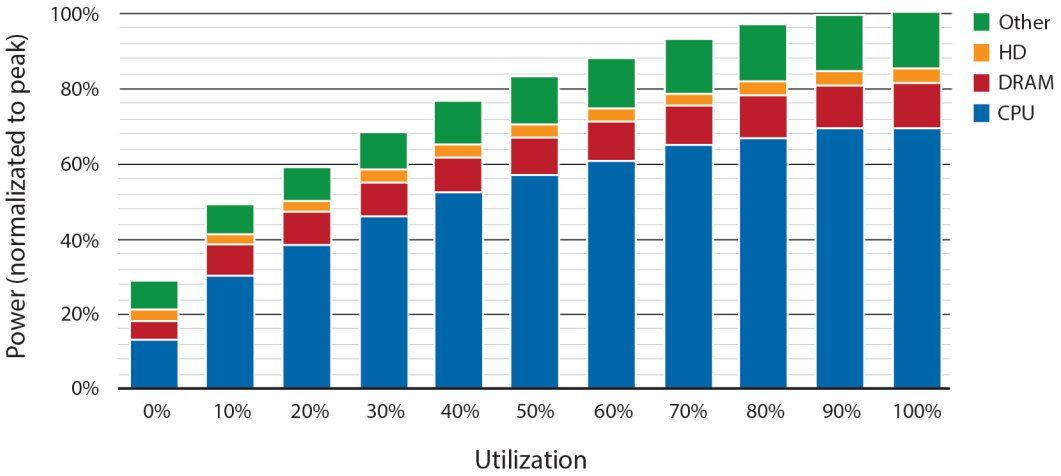


Figure 1.1: Energy utilisation inside a computer [20]

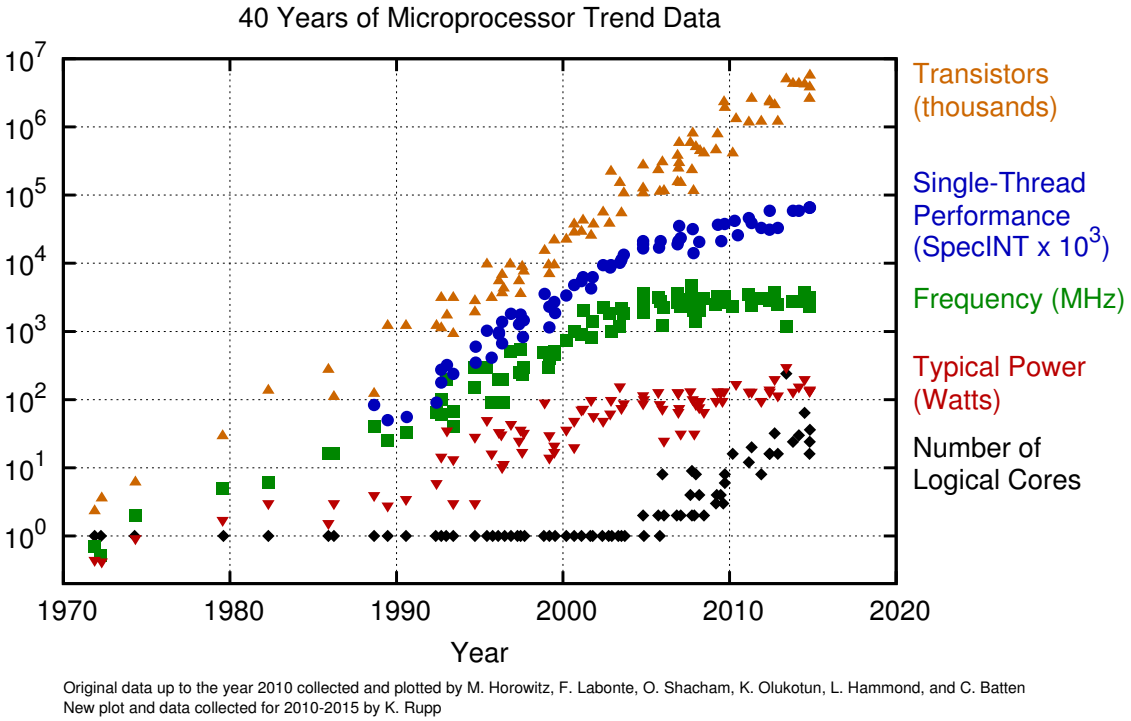


Figure 1.2: 40 years of microprocessor trend data [20]

and over-current conditions [21]. Such specifications are essential to enable power supply manufactures to provide solutions tailored to the requirements of new processors. The power density of electronic devices has also shown exponential growth over time, as shown in Figure 1.3 [22]. Power supplies should be able to meet these growing demand in future.

1.2 Power challenges in modern data centres

Since 2009, emerging areas in Information and Communication Technology (ICT) such as cloud computing, high-speed wireless access, and thin client solutions such as smartphones have had

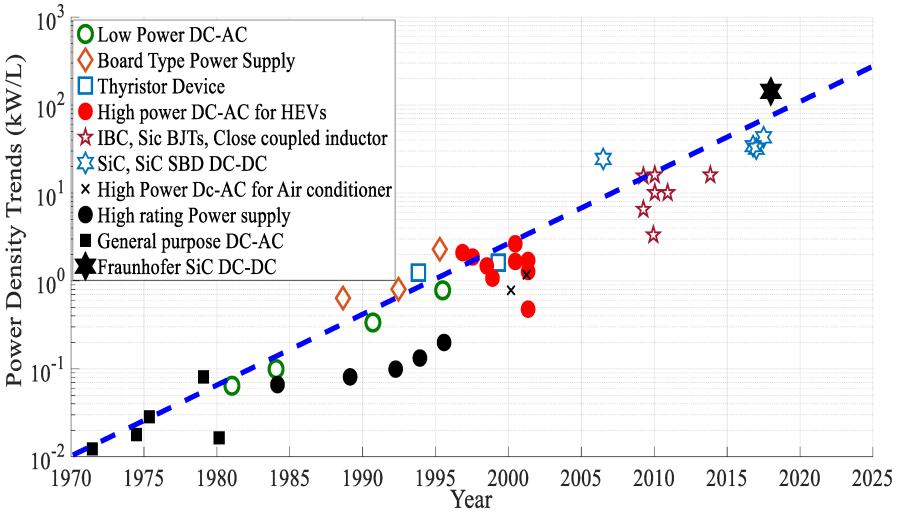


Figure 1.3: projected growth of power density in power electronics devices [22]

a disruptive impact on energy consumption [23]. The USA holds a huge share of the cloud computing market, and it is the home of giants such as Amazon, IBM, Apple, Cisco, and Google. The main operational cost for cloud computing businesses is powering their data centres. Data centre power consumption issues are compounded at the national level: according to data published by Electric Power Research Institute (EPRI), the USA data centre power market is growing at over 10% annually [24].

A few years ago, data centres were designed around 4-to-5-kW server racks. However, today these racks are designed for 10 kW, and rack power consumption is expected to grow up to 30 kW per rack in coming years [25]. A 1% efficiency improvement can save hundreds of watts at the rack level and several kilowatts at the data centre level. Existing server racks are fed from a utility power supply and converted to lower DC voltage at the rack. Existing 12 V, 1 kW power supplies draw over 80 A and the distribution bus should have a low ohmic drop at these currents. Once the rack-power levels approach 30 kW, ohmic loss can be unaffordable since it increases with the square of the current.

According to the New Climate Economy, investments made in the next 15 years will determine the future of the planet's climate system. Investments made in electricity and communication technology infrastructure will be significant as they represent major segments of world energy consumption and are expected to grow in coming years. This trend is illustrated in Figure 1.4, while Figure 1.5 shows the contribution of each category in the communication technology sector. These exponential growth curves motivate the demand for improved energy efficiency of rack-level power delivery in data centres.

Unplanned outages are another challenge in data centres. The total cost per minute of outage per incident is shown in Figure 1.6. According to data published by the Ponemon Institute, the root cause of unplanned outages in data centres is failures in UPS systems [27]. The contributions of various issues toward unplanned outages are shown in Figure 1.7. Lead-acid batteries are the predominant energy storage devices used in most data centre UPS systems. However, such batteries suffer from critical disadvantages including short lifetimes (3 – 10 years), unexpected failures, difficulties in handling, and toxic components. DC-UPS systems are designed

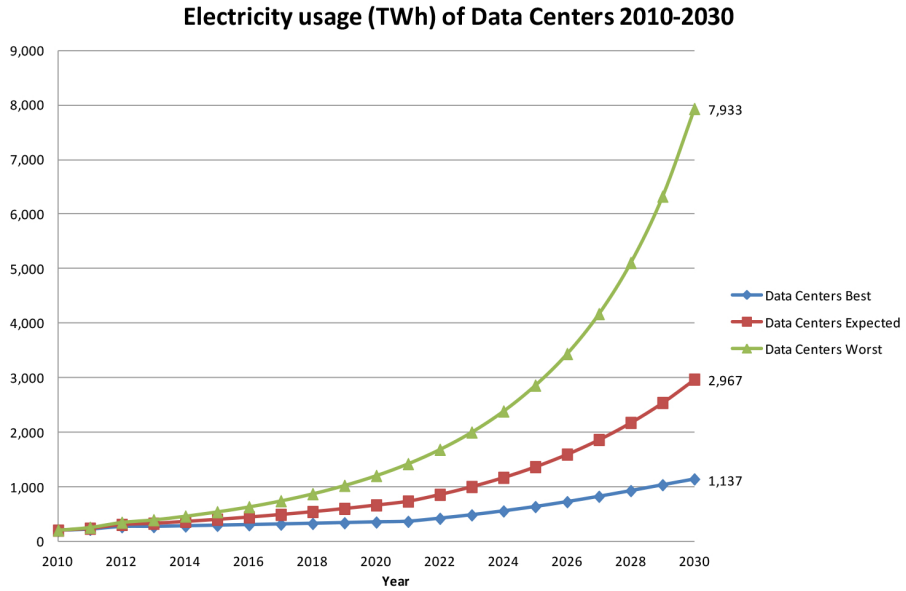


Figure 1.4: Global electricity demand of data centres 2010–2030 [26]

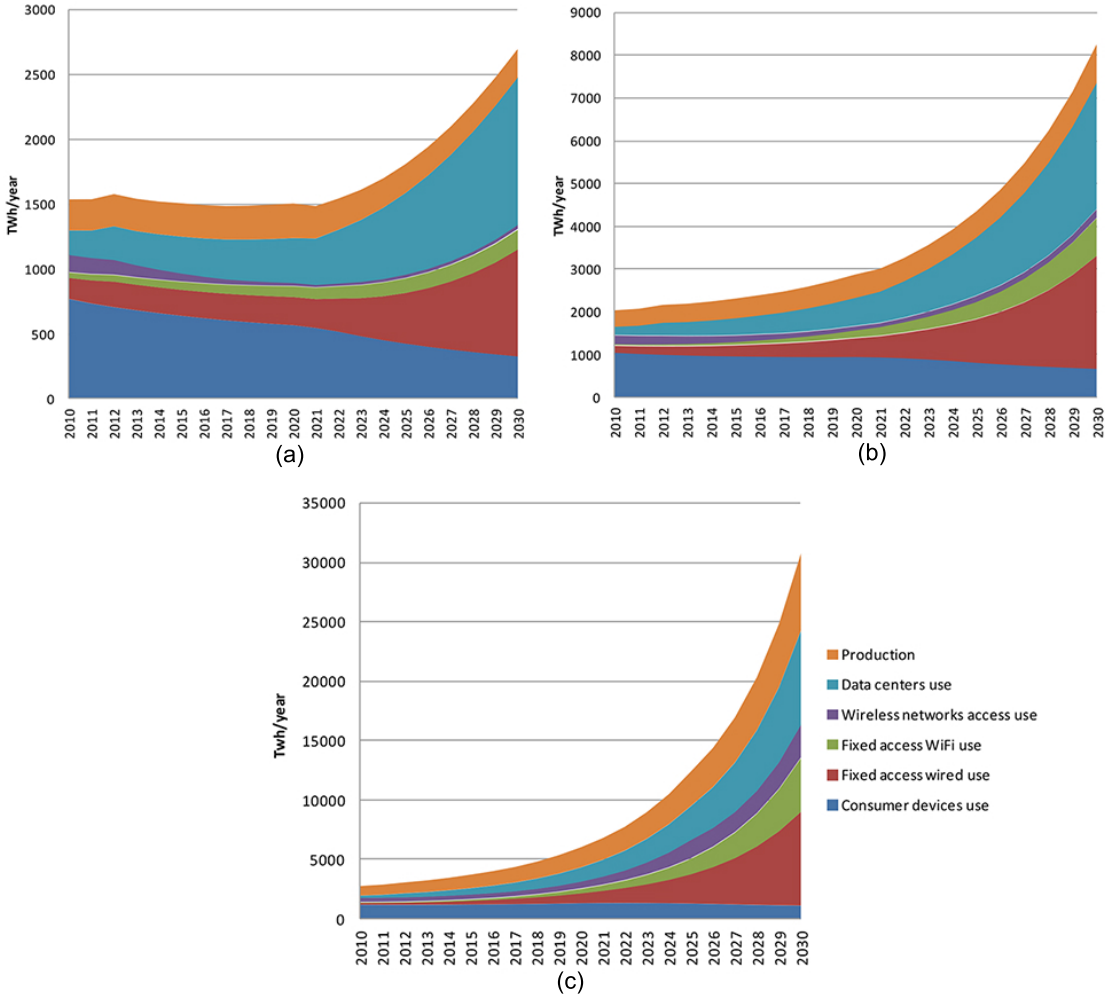


Figure 1.5: Electricity usage 2010–2030 trends per communication technology category for (a) best-case, (b) expected-case, (c) worst-case [26]

to handle power transition to permanent energy backups such as generators and fuel cells. The typical transition time is 15 to 30 s [6]. Battery-based UPS systems can be replaced with super-capacitors in data centres to improve reliability. However, to utilize energy efficiently, suitable power converters need to be developed. Otherwise, a portion of the energy will be lost in the intermediate inverter stage.

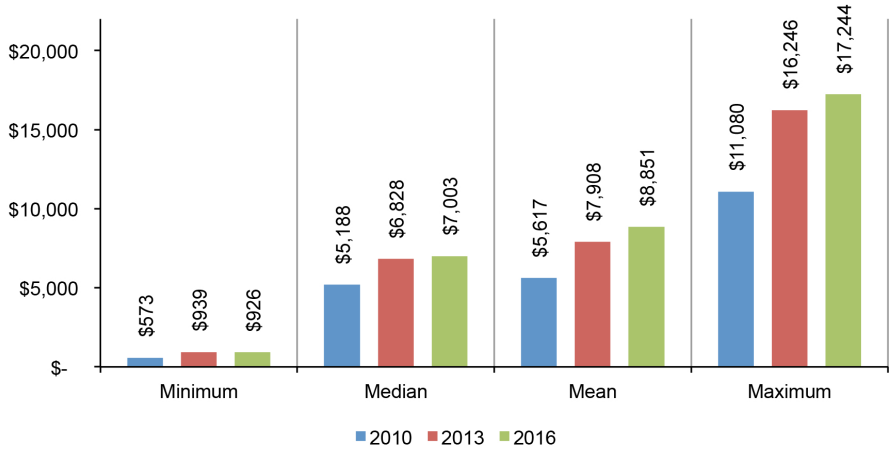


Figure 1.6: Total cost per minute of an unplanned outage [27]

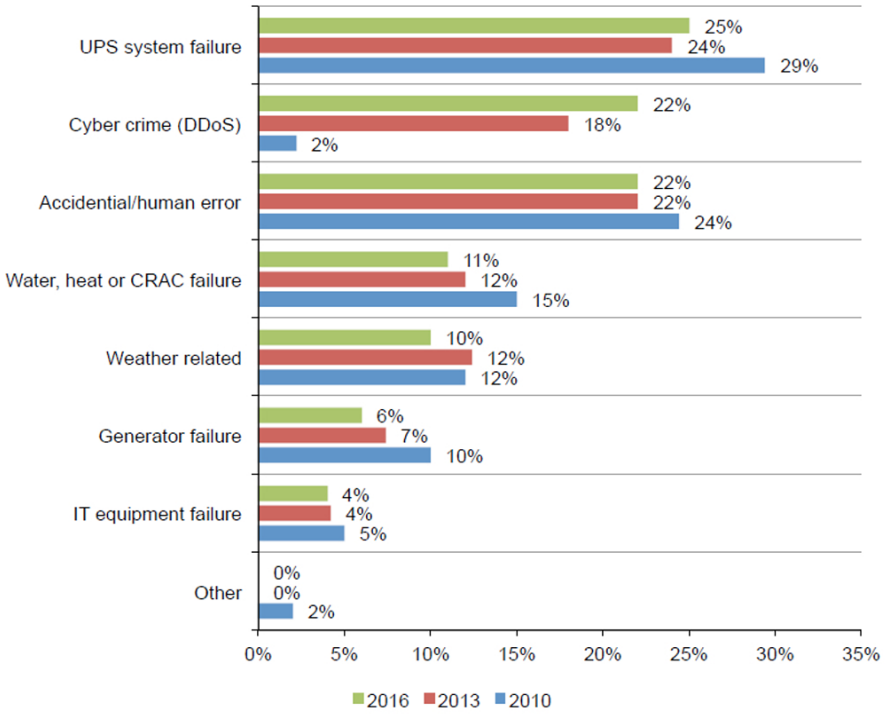


Figure 1.7: Issues causing unplanned outages in data centres [28]

1.3 New Google server rack architecture

More power needs to be pumped to the processor with the increasing processing power at the same voltage. This means increased current circulation in the power cables, which increases the

i^2r loss in power cables reducing the efficiency of the overall system. However, by increasing voltage by 4 times, i^2r loss can be reduced by 16 times. Google has foreseen the problems of 12 V rack-power architecture well in advance. It has been using 48 V rack power architecture in its server racks since 2010. This architecture reduces distribution loss by 16 times and power conversion loss by up to 30% [29]. Google made this architecture public through Open Compute Platform (OCP) by contributing the Open Rack 2.0 specifications to the community, including business competitors like Facebook. These include design specifications and standards for 48 V power shelves, high-efficiency rectifiers, rack management controllers and rack-level battery backup systems. According to the specification of 48 V rack power architecture, peak efficiency between load condition of 30–40% needs to be maintained above 97% while the efficiency at 10–30% load condition need to be maintained above 92% [30]. Also, DC-UPS is distributed, and forms part of the server rack. This arrangement helps to isolate server racks from the central point of failures.

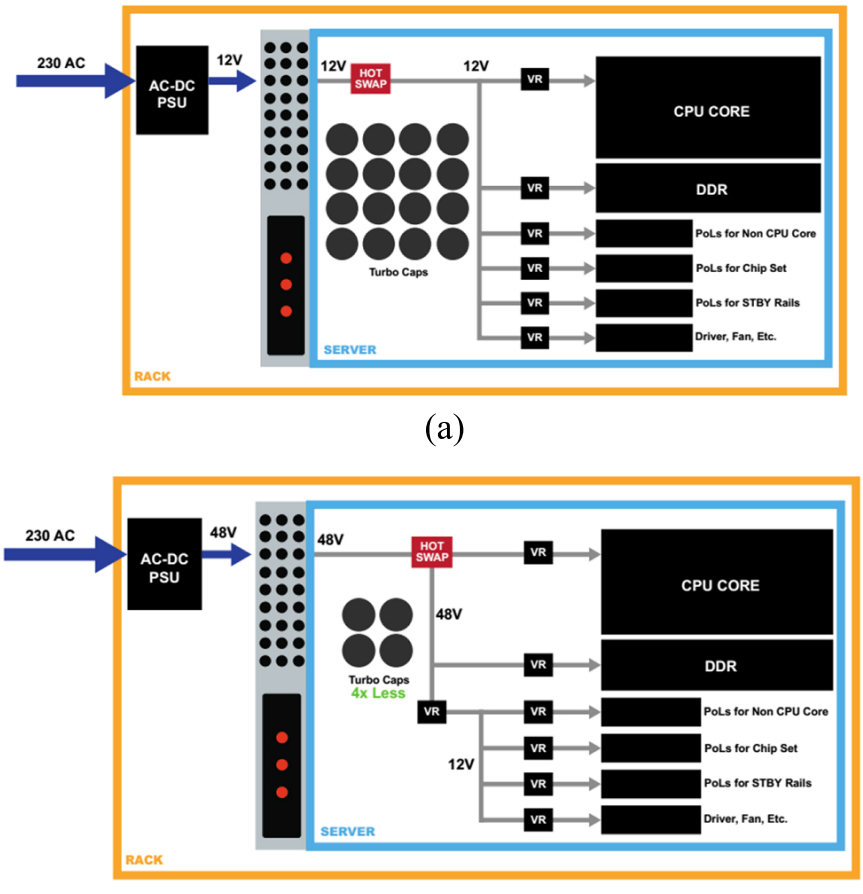


Figure 1.8: Server power delivery architectures: (a) 12 V architecture; (b) 48 V architecture [31]

Figure 1.8 compares the internal power delivery architecture of 48 V with traditional 12 V. Wiwynn is a leading cloud IT infrastructure provider; some of their data help to contrast the performance of these 12 and 48 V power architectures. The number of capacitors required in 48 V architecture is four times less than 12 V architecture due to the low current circulation. Figure 1.9 depicts the efficiency improvements of 48 V architecture with $3, 6, 10$ mΩ distribution

loss (path resistance). Figure 1.10 depicts the total loss reduction of 48 V architecture. The benefits of 48 V rack power architecture can be summarized as:

- Higher conversion efficiency
- Reduced current circulation in cables, with corresponding reductions in distribution loss
- 48 V is still considered as safe voltage, so no additional safety measures are needed

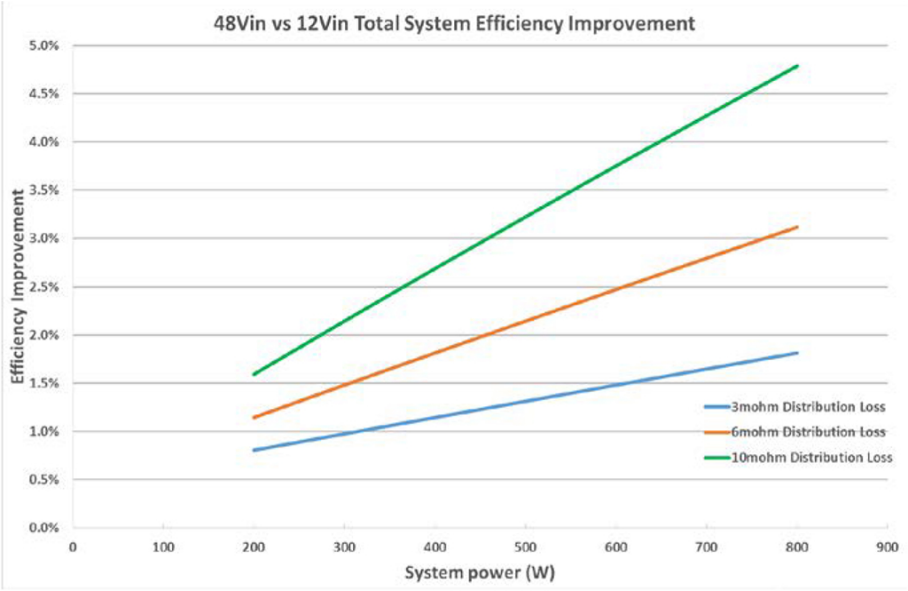


Figure 1.9: Total efficiency improvement 48 V vs 12 V [31]

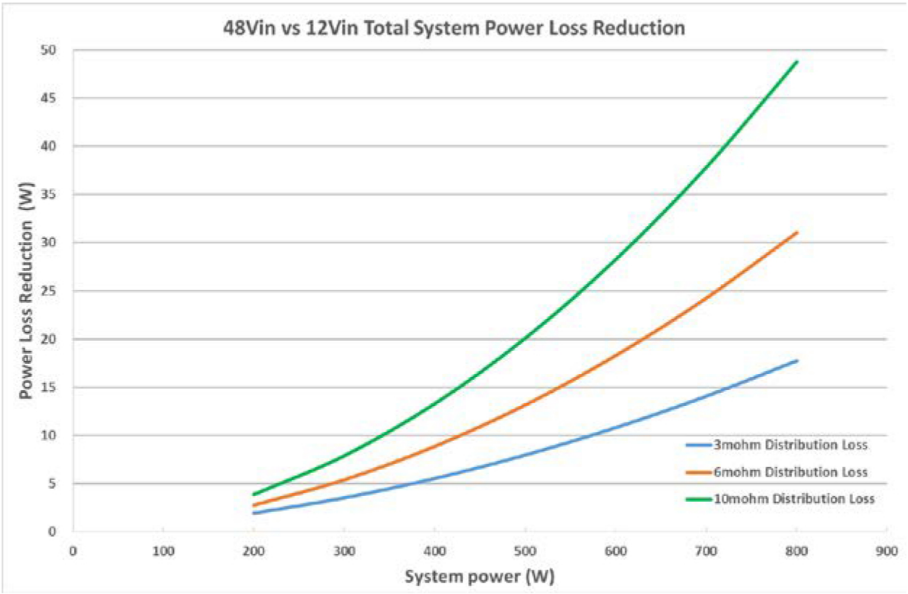


Figure 1.10: Total loss reduction 48 V vs 12 V [31]

The main challenges of the new architecture are developing high efficiency AC-to-DC converters while maintaining similar form factors to fit into existing server racks, not exceeding the cost of the present power converter designs, and not sacrificing transient response performance [31].

Some of the transformer-isolated power converter topologies proposed for the 48 V Google power supply are shown in Figure 1.11. The complexity of transformer design, I^2R loss, implementation of many high-frequency switches and design complexity are the main challenges

of these solutions. Transformer-less topologies proposed are depicted in Figure 1.12. Low reliance on magnetic components, and low drain source voltage (V_{DS}) requirement for MOSFETs (metal–oxide semiconductor field-effect transistor) are the main advantages over transformer-isolated versions. However, these solutions require a large number of high-frequency MOSFETs, increasing design complexity and cost.

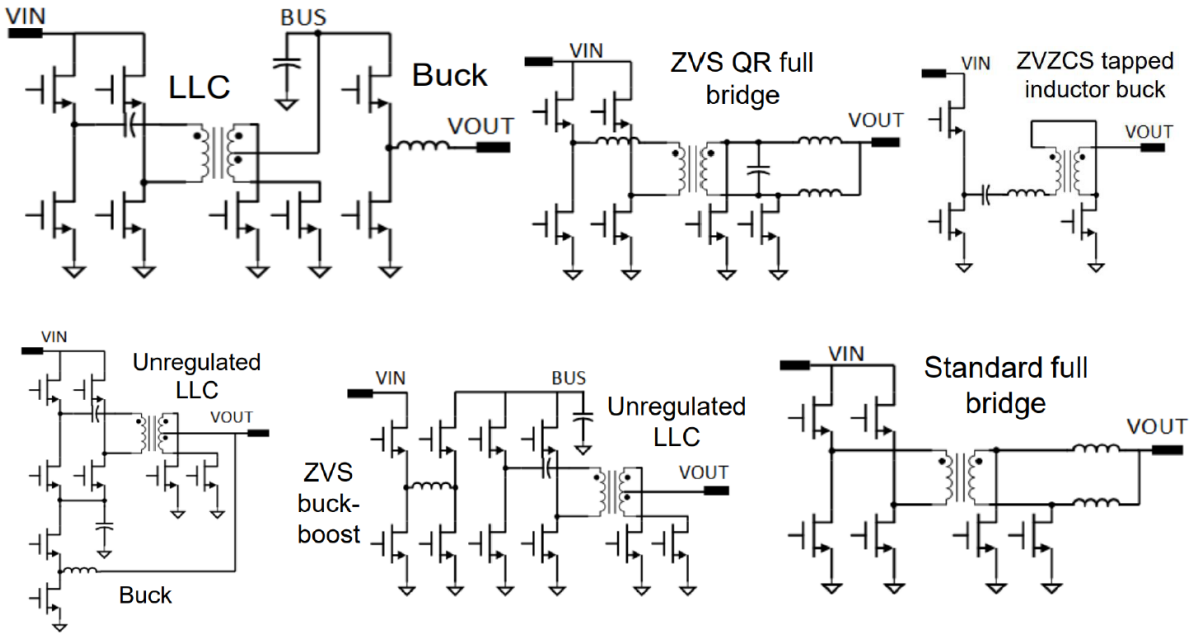


Figure 1.11: Transformer isolated power converter topologies proposed for 48 V Google power supply [24]

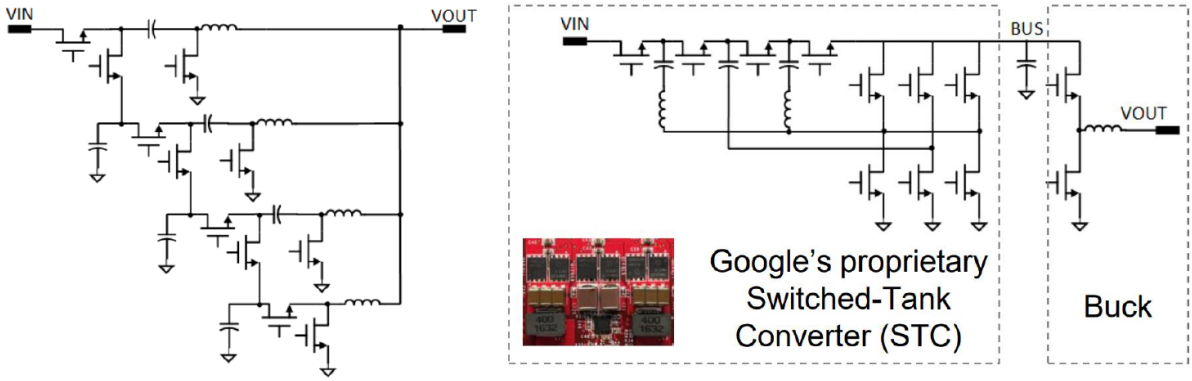


Figure 1.12: Transformer-less power converter topologies proposed for 48 V Google power supply [24]

1.4 Existing power converter techniques and challenges

Rectifier bridges and synchronous rectification are the two common methods to convert voltage from AC to DC in most of the power converters. Electronic systems employ three fundamental techniques to convert DC voltage into different DC voltages: switch-mode power supplies (SMPS), linear power supplies and switched capacitor (charge pump) converters [17].

Linear regulators are ideal to use with applications requiring extremely low noise, such as audio amplifiers and low-power consumer applications such as alarm panels [32]. Figure 1.13 depicts the typical circuit arrangement of a linear power supply. A transformer connected to the AC source reduces the voltage to a usable low level, and a series-pass element (SPE) is introduced to regulate the voltage. This SPE can be a power transistor or MOSFET. In general, linear regulators have low efficiencies (30–60% [33]) and a limited input voltage range, and require bulky components such as transformers. However, these have outstanding output characteristics such as low noise, excellent transient response to load current fluctuations, design simplicity and low-cost design [17].

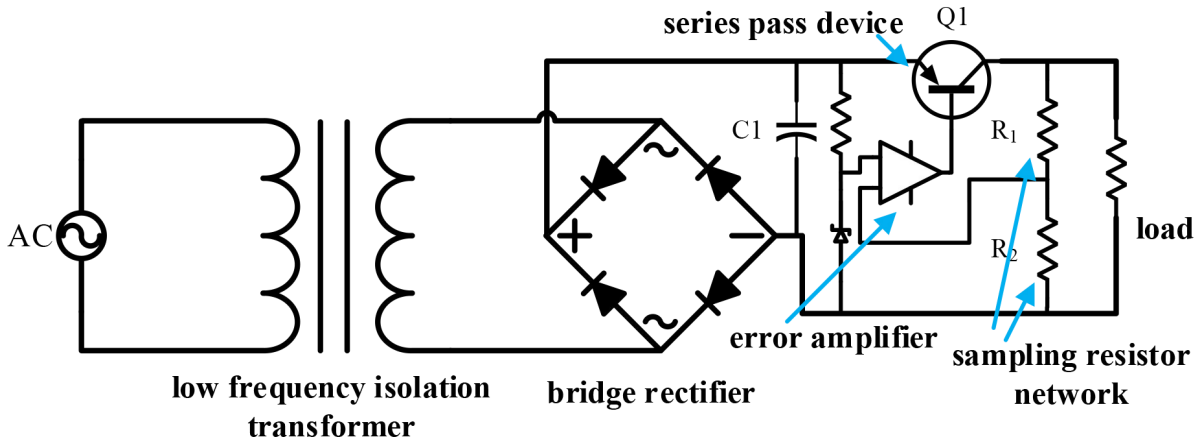


Figure 1.13: Linear power supply topology

Switch-mode power supplies use inductors and capacitors as energy storage devices to step-up or step-down the voltage. The significant advantages of switched-mode power supplies are reduced size (due to high-frequency operation) and significant improvement in efficiency (theoretical efficiency is 100% [33]). High-frequency switches are introduced to regulate voltage using pulse-width modulation. Problems associated with this technique are increased ripple, noise on the output DC supply and the generation of EMI, all of which have to be managed [32]. The three basic topologies used in switching power supplies are buck (step-down), boost (step-up) and buck-boost.

Switch capacitor technique (charge pump) uses a capacitor to store energy instead of an inductor or transformer. Charge pump does not contain inductors that have a significant component size, EMI issues, greater layout sensitivity and higher cost [34]. However, these converters offer best performance at extremely low operating currents, and they are useful in applications such as handheld devices, to enhance battery life [35]. The current capability of the charge pump is limited by the current capacity of the capacitors used, and switching produces a significant ripple [36].

Low dropout (LDO) regulators deliver all the strengths of linear regulators with higher efficiency. LDOs differs from standard linear regulators because of their ability to operate with a minimum voltage difference between the regulated output voltage level and the unregulated input voltage. Normally an LDO can offer a “dropout” (the difference between input and output voltage) of less than 0.3 V while a standard linear voltage regulator has a dropout voltage of 1 V or more. This makes LDOs are an ideal choice for battery-powered portable devices. Figure 1.14

illustrates the significance of linear regulator ICs with switching regulator ICs in the consumer electronics market [37]. LDO regulators have acquired a huge market share. The main problem with LDOs is the limited input voltage range, and their efficiency degrade in situations where the input voltage is high compared to the regulated output voltage.

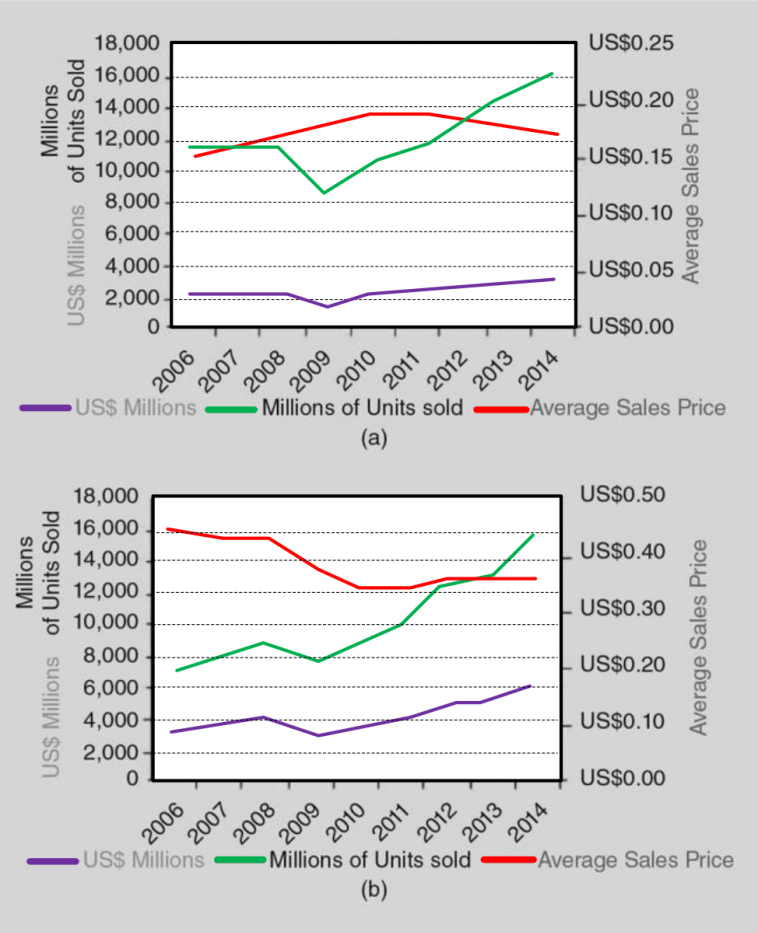


Figure 1.14: The worldwide market forecast for regulator ICs: (a) switching regulators and (b) LDO - type linear regulators [17]

Each technique has its own strengths and weakness. Typically, all three techniques are used to achieve optimal efficiency and transient performance to suit different applications. Table 1.1 compares the features of linear regulators, charge pumps and switch-mode power supplies.

The SCALDO (supercapacitor-assisted low dropout) regulator is a relatively new patented [38] power converter technique developed at the University of Waikato. The supercapacitor assisted low dropout regulator was invented in the year 2008, and a US patent was granted in 2012. Research collaboration was established with the University of Southampton to convert SCALDO into a portable chip. SCALDO is an extra low frequency, highly efficient alternative to linear regulators.

The 5^{th} column of table 1.1 compares SCALDO with existing converter techniques. This technique is based on a completely new loss-circumventing principle in the *RC* charging loop, and a detailed analysis is presented in Chapter 3. In a simple *RC* loop fed by a DC voltage source, if the capacitor has zero initial charge, then when the capacitor reaches its rated voltage the resistive elements in the charging loop will have dissipated the same energy as that stored

Table 1.1: Comparison of existing DC-to-DC converter techniques with SCALDO

Feature	Linear Regulators	Charge Pumps	Switch-Mode Regulators	SCALDO
Design complexity	Low	Moderate	Moderate to high	Low
Cost	Low	Moderate	Moderate	Low
Noise	Lowest	Low	Low to moderate	Lowest
Efficiency	Low to moderate	Moderate to high	High	High
Thermal management	Poor to moderate	Good	Best	Good
Output current capability	Moderate	Low	High	High
Requires magnetic parts	No	No	Yes	No
Limitations	Cannot step up	Vin /Vout ratio	Layout considerations	Switch count cannot step-up

in the capacitor ($\frac{1}{2}CV^2$). However, with the availability of commercial supercapacitors (SC), this loss can be circumvented in two steps: (i) Introducing a useful resistance to the capacitor charging loop such as an LDO (low dropout linear regulator), light bulb, fan or compressor; (ii) replacing the capacitor with a pre-charged supercapacitor to increase the time constant significantly. A detailed discussion of the SCALDO concept is provided in Chapter 2. The benefits of the SCALDO converter can be summarised as:

- Load receives the low-noise and high-current slew-rate capable DC output of a linear regulator
- Switching frequency is extremely low (fractional Hertz to few Hertz)
- RFI/EMI issues are eliminated
- Output currents range from milliampere to over 100 A
- DC-UPS capability

As shown in Table 1.2, SCALDO improves the ETEE (end-to-end efficiency) of a 5-to-3.3-V converter by a factor of 1.33, and for a 12-to-5-V converter by a factor of 2. A linear 5-to-3.3-V converter with nominal 66% ETEE can be theoretically increased to 99%, and a 12-to-5-V linear converter (42% efficiency) can be increased to 84% [39]. The fifth column indicates the efficiency gain applicable to the Google 48 V configuration. When this technique is applied to the case of a rectified 230 V AC to 48 V DC converter for server rack power supplies, the maximum SCALDO efficiency that can be expected is 88.6%. This will be a costly solution due to the large number of SCs and switches required (16 in this case). However, by developing an efficient pre-regulation stage, this efficiency can be enhanced, and the switch count can be reduced. Another limitation of SCALDO is dependency on the availability of LDOs in the market to meet the desired configuration. However, high current LDOs keep higher input to output voltage margin for regulation. In-order to satisfy the current Google server rack specifications, a discrete LDO stage needs to be developed.

1.5 Objective of the research

This study aims to investigate the potential of the SCALDO technique to develop a high-current DC power supply suitable for Google server racks, meeting requirements such as electrical

Table 1.2: Comparison of SCALDO implementations

Converter configurations	5-to-1.5 V	12-to-5 V	5-to-3.3 V	$(230\sqrt{2})$-to-48 V
Ideal efficiency without SCALDO	30%	42%	66%	14.75%
Ideal efficiency with SCALDO	90%	84%	88%	88.6%
Number of SCs used (n)	2	1	3	5
Number of switches required (k) [$k = 3n + 1$]	7	4	10	16
Efficiency improvement factor	3	2	1.33	6
Remarks	high V_{in}/V_{out} ratio	high V_{in}/V_{out} ratio	low V_{in}/V_{out} ratio	Google 48 V architecture

isolation, fast transient response, high efficiency, and DC-UPS.

1.6 The proposed power converter technique

To overcome the limitations of existing converters, a new supercapacitor-assisted power converter is proposed. The new power architecture is shown in Figure 1.15 (b) and compared with the existing architecture (a). In the standard Google 48 V configuration, UPS is implemented at the rack level, with a battery bank being used for energy storage. A separate power supply is connected to the battery bank and a charging circuit needs to be implemented to control the battery charging process as depicted in Figure 1.15(a). In our proposed technique, supercapacitors are used for energy storage, replacing batteries and providing DC-UPS capability as an integral part of the AC-DC converter. With the commercial availability of larger single-cell supercapacitors in three different commercial families (symmetrical EDLC, hybrid and capa-batteries) with single-cell capacitance values up to 70 000 F, SCs are becoming fit-and-forget energy storage devices. This is because SCs have life-cycles of two to three orders of magnitude larger than rechargeable batteries [40]. Since the proposed technique uses capacitor banks operating between two voltage levels just below the bank's rated voltage, this further enhances the life-cycle count [41]. Although the present market price of supercapacitors is relatively high compared to batteries, SCs provide a maintenance-free solution and are not hazardous to the environment, unlike battery-based solutions. Higher power density is another advantage of SC-based UPS solutions. The availability of high voltage rated SC modules in the market is a favourable development for the new architecture. Benefits of the new DC-UPS technique can be summarised as:

- Since the life cycle of capacitors is long, maintenance costs will be very low
- No additional circuits are required to charge the capacitor (as the capacitor bank is part of the power supply)
- Environmentally friendly solution as this is replacing batteries
- High power density storage, means that high current can be easily drawn

In order to overcome the limitations of SCALDO for higher input to output voltage ratios, a new input stage is developed. The overall topology is shown in Figure 1.16. This gives us the flexibility to design any desired SCALDO stage at the output stage while providing transformer

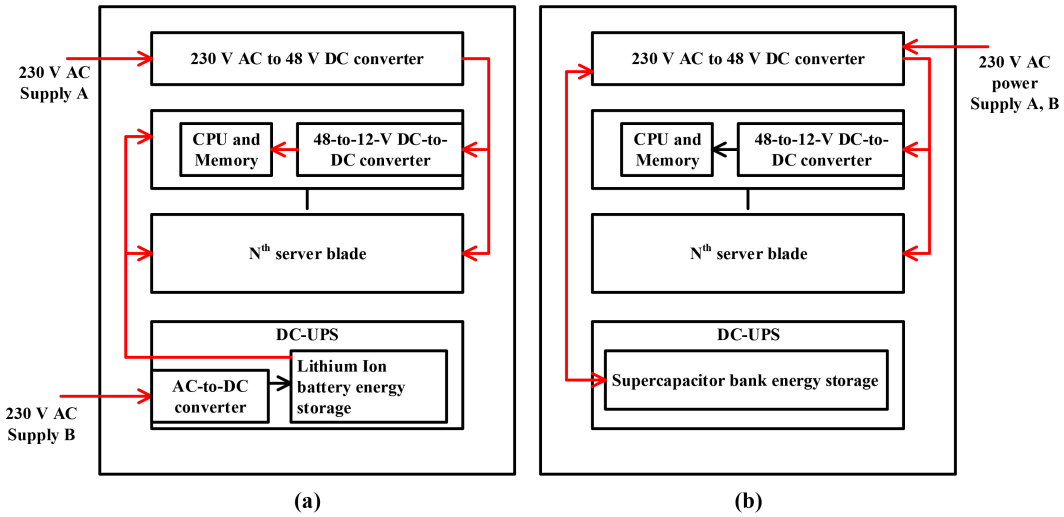


Figure 1.15: Server rack power converter architecture: (a) existing; (b) proposed

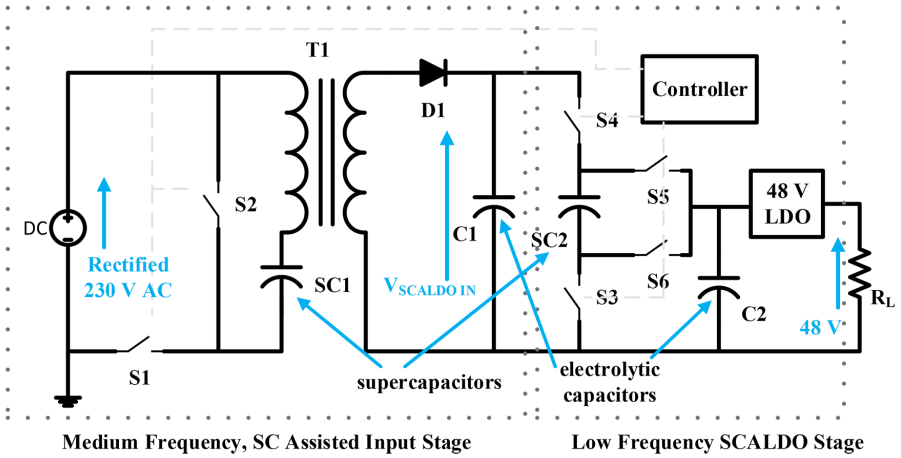


Figure 1.16: Novel power converter solution for modern 48 V Google server racks

isolation. A supercapacitor is placed in series with the transformer primary winding, and the input stage operates at medium frequency to reduce transformer size. A discrete LDO stage is developed to support higher currents. The transformer-isolated input stage provides a voltage step-down from 325 V DC to 100 V DC; the 100−to−48 V high-current SCALDO can then be introduced at the load end of the power supply. Theoretically, this SCALDO configuration is 96% efficient, and the switch count can be reduced to six. The SC bank connected in series with the primary winding of the transformer is the main energy storage of the circuit to embed DC-UPS inside the converter. The watt-hour capability of the UPS depends on the capacity of the capacitor bank and the two voltage margins used. According to the analysis presented in Chapter 3, selecting a higher voltage gap reduces charging efficiency and compromises overall efficiency of the converter. Therefore the capacitor voltage should be constrained to lie within a narrow range close to the rated voltage of the SC bank. The benefits of this converter can be summarised as:

- connected load always sees the DC output of a linear converter based on an LDO
- high current slew-rate capability
- high output load current capability due to low ESR value of commercial SCs

- transformer isolation at the primary side
- SC-assisted two-stage DC-UPS
- wide AC input voltage range
- surge absorbent capability (because of series SC)
- high ETEE (end-to-end efficiency)
- relatively low stress on switches

A number of different topologies were investigated during this PhD in order to identify appropriate power converter techniques and circuit implementations. Chapter 4 describes the design and implementation process of the output SCALDO stage while chapter 5 describes the design and implementation details of the transformer isolated medium-frequency pre-regulator stage.

1.7 Thesis structure

The content of this thesis is organized as follows:

- The present chapter gives a general overview of the research and key motivating factors behind the work.
- Chapter 2 stresses the importance of supercapacitors for energy storage, comparing their engineering specifications with other energy storage devices, then provides an overview of a range of supercapacitor-assisted (SCA) applications.
- Chapter 3 presents a discussion of the loss circumventing principle of the *RC* charging loop, which is the primary operating principle behind supercapacitor assisted converters. A detailed analysis of the supercapacitor assisted loss management technique (SCALoM) is also presented in this chapter.
- Chapter 4: As a part of the new power converter, implementation of SCALDO is extended to handle higher power. A discrete scalable LDO is designed to regulate the voltage at high load current. This chapter details the design and implementation details of this output SCALDO stage.
- Chapter 5 presents the design and implementation details of the transformer-isolated medium frequency input stage of the converter.
- Chapter 6 concludes the thesis with a discussion on opportunities for extending the power converter technique.

1.8 Original contributions

- Analysing the loss circumventing principle in *RC* charging loop, which is the basis of SCALDO
- Identifying a new supercapacitor assisted (SCA) technique feasible for silver box power supplies.
- Identifying novel input stage topology to enhance the efficiency of SCALDO.
- Identifying a novel approach to embed two-stage DC-UPS capability for power supplies.

- Extending SCALDO implementation for higher current and higher voltage configurations at a reduced cost
- Discrete LDO design and implementation
- Developing a mathematical model for the LDO
- Developing simulation models with LTSpice and MATLAB Simulink for the new power converter technique
- Design and implementation of various proof-of-concept prototypes to establish the technical feasibility of the new technique
- Analysis of the DC-UPS capability of the converter

1.9 Chapter summary

This chapter has discussed the motivation for developing new power converter techniques and described challenges in designing power supplies for modern electronics devices with particular emphasis on power challenges in data centres. An overview of the SCALDO converter was also given. The SCALDO converter can be adapted to power Google server racks by introducing a transformer-isolated input stage. Supercapacitor assisted DC-UPS is a reliable alternative to battery-based UPS systems.

The next chapter gives an overview of supercapacitors as an energy storage devices and compares their specifications with other energy storage devices. The Power Electronics research group at the University of Waikato has developed a novel application base of supercapacitors known as SCA (supercapacitor assisted) techniques, and some concepts are described with particular emphasis on SCALDO and SCATMA as they are directly related to the new concept presented in this thesis.

Chapter 2

Energy Storage Systems and Supercapacitor Assisted Techniques

2.1 Introduction

An overview of the supercapacitor assisted low dropout (SCALDO) regulator was provided in the previous chapter. In SCALDO a capacitor rated at farad order is used as a lossless voltage dropper in a linear regulator. Unique among energy storage devices, the supercapacitor has particular importance because of its higher power density, reduced impact on the environment and durability. This chapter gives an overview of supercapacitors, compare them with other energy storage devices and finally discusses traditional and non-traditional applications of supercapacitors.

2.2 Energy storage systems

Superconducting magnetic energy storage (SMES), flywheels, supercapacitors, and Li-ion batteries (the battery type with the highest specific energy) are the leading energy backup systems available today [15]. This section gives an overview of the operating principle of each of devices and compares their strengths.

Batteries store energy in an electrochemical process and are the most popular energy storage system, used in applications ranging from several kilowatt-hour household energy storage systems to megawatt-hour energy storage in power stations. The anode in lithium-ion batteries is made of graphitic carbon while different lithiated metal oxides such as $LiCoO_2$ and $LiMO_2$ can be used as cathodes [15]. Lithium-ion batteries have large energy density, fast response and long cycle lives. They occupy almost 50% of the portable application market. The main disadvantages of lithium-ion batteries are their higher cost due to the need for special packaging and charge monitoring circuits, and limited sources of lithium create a challenge to their wide-spread use.

Flywheels store energy as mechanical energy in spinning disks mounted on two magnetic bearings. The energy stored is a function of the moment of inertia (I) and the angular velocity (ω),

$$E = \frac{1}{2} I \omega^2 \tag{2.1}$$

When the flywheel is considered as a disk of mass M, the equation can be expressed as:

$$E = \frac{1}{4} M r^2 \omega^2 \tag{2.2}$$

where r is the radius of the disk. In order to increase energy storage, the velocity can be increased. However, this is limited by the strength of the disk. Flywheels have very high power density; however, their energy density is relatively limited. They are ideal for frequency regulation in power grid applications. Flywheels are used in aircraft power trains and shipboard power systems to deliver high power for a short time span [15].

Superconducting magnetic energy storage (SMES) is still being researched; it stores energy in an electromagnetic field in a superconducting coil. A basic block diagram of SMES is shown in Figure 2.1, where the superconducting coil, a refrigerator and a power conditioning system are the basic components. Superconducting coils made out of materials such as niobium-titanium (NbTi) are typically used in SMES systems and the temperature is kept very low using a refrigerator unit to reduce the resistance of the coil, which increases current. The superconducting coil stores the energy by the flow of a direct current given by,

$$E = \frac{1}{2} L i^2 \tag{2.3}$$

where L is the inductance of the coil. Depending on the superconducting coil and power conditioning block, SMES units can deal with several megawatts of power demand, and they also have a long cycle life. Today SMESs are used in shipboard power systems, industrial power quality applications, and for supplying short bursts of electricity in power grids [15].

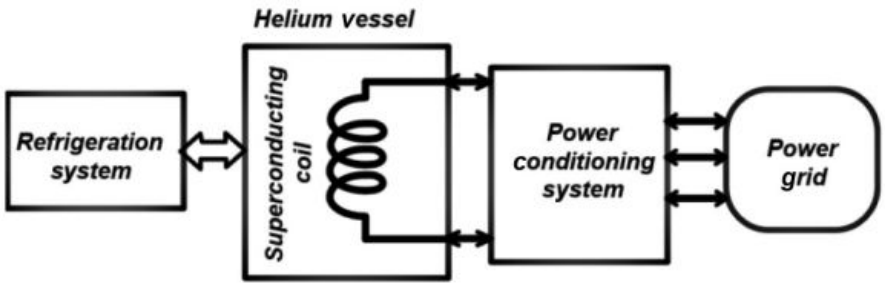


Figure 2.1: Building blocks of superconducting magnetic energy storage (SMES) [15]

Supercapacitors have very high capacitance (rated in farads) compared to typical electrolytic capacitors (rated in micro farads). Banks of supercapacitors can be used for a short term energy storage in various industry applications. A detailed discussion of this device is presented in a later section.

The strengths of these energy storage technologies are compared in Table 2.1 and depicted in a multidimensional graph in Figure 2.2. Supercapacitor-based energy storage is ideal for high power applications as they have highest specific power, and the capital cost per kilowatt ($/kW) is lower and comparable with SMESs and flywheels.

Supercapacitors are an environmentally friendly alternative to battery-based systems, and accessibility is almost the same as batteries due to their wide usage today. Long cycle life means they can be fit-and-forget energy storage solutions. Most of the power converter techniques developed by the power electronics research group (UoW) are based on SCs as temporary energy storage systems. The next section provides an overview of capacitor technology.

Table 2.1: Power, Energy, and cost comparison of the high-power storage technologies (Early developments up to 2015) [15]

Storage technology	Energy density (Wh/kg)	Energy density (kWh/m^3)	Power density (W/kg)	Power density (MW/m^3)	Energy capital cost ($/kWh)	Power capital cost ($/kWh)
Supercapacitor	$0.5-5$	$4-10$	$1000-10,000$	$0.4-10$	$500-15,000$	$100-400$
SMES	$1-10$	$0.2-2.5$	$500-2000$	$1-4$	$1000-10,000$	$200-500$
Flywheel	$10-50$	$20-100$	$500-4000$	$1-2.5$	$2000-5000$	$150-400$
Li-ion	$70-200$	$200-600$	$150-500$	$0.4-2$	$600-2500$	$1200-4000$

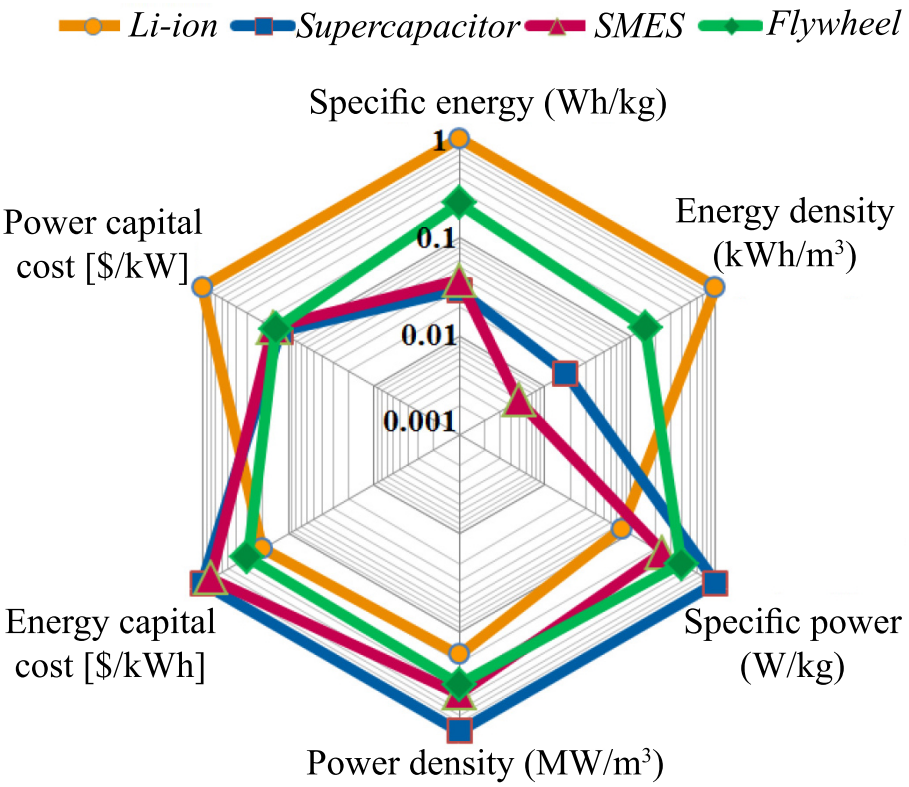


Figure 2.2: Comparing power, energy, and cost of high-power storage technologies [15]

2.3 Overview of capacitors

A capacitor is a device that stores an electrical charge and releases it when the external circuit requires it. Figure 2.3 illustrates the simplest configuration of a capacitor, with two parallel conducting plates separated by a dielectric material (electric insulator) [42]. The parallel plates have an area A and separation d. The capacitance (C) of a capacitor is directly proportional to the area of the conductive plates and inversely proportional to the distance between them,

$$C = \epsilon \frac{A}{d} \tag{2.4}$$

were ϵ is the absolute permittivity of the dielectric material used.

When a capacitor is charged up to voltage (V), the energy stored (E) in the capacitor is given by:

$$E = \frac{1}{2} C V^2 \tag{2.5}$$

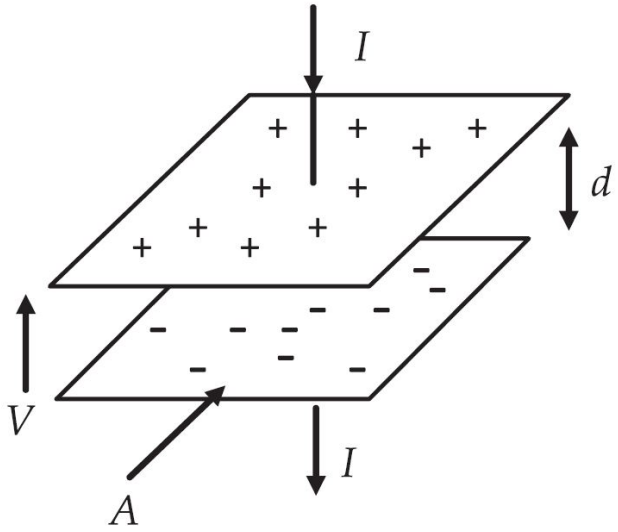


Figure 2.3: Construction of a capacitor [42]

In an electronic circuit, capacitors are used for smoothing, buffering, filtering, bypassing and DC blocking. Based on the capacitor construction and the technology used, the most common types of capacitors are film capacitors, ceramic capacitors and electrolytic capacitors.

Polymeric and mica are the two main film capacitors which are made out of synthetic and natural film-like materials. Film capacitors provide a readily scalable capacitor technology, ranging from nano-joules to hundreds of kilojoules per unit. Film capacitors are polarity independent, general-purpose capacitors that are used in applications requiring tight capacitance tolerances and very low leakage currents [42].

Ceramic capacitors are nonpolarized fixed-value capacitors that are useful for both AC and DC applications. Ceramic capacitor technology provides moderate energy density, high-power density and such capacitors are available in very small (pF) to moderate size (10–100 pF; 5–500 V DC). These capacitors are used in low-voltage DC control circuits, and typical applications include blocking, buffering, bypass, coupling, low-frequency filtering, tuning, and timing for frequencies up to the gigahertz [42].

Electrolytic capacitors are available in several types, including aluminium, tantalum, and niobium. An aluminium electrolytic capacitor's internal structure consists of two aluminium foils, which are separated by a porous material such as paper, which is impregnated with an electrolyte as illustrated in Figure 2.4. Aluminium electrolytic capacitors are available in the range of less than 1 μF to 1 F with working voltages up to several hundred DC volts. These capacitors provide high ripple current capability, which is a key advantage of them.

Properties of these capacitor types are summarised in Figure 2.5. Voltage and capacitance ranges are compared in Figure 2.6. The next section discusses supercapacitor technology development and gives an overview of their traditional applications.

2.4 Supercapcitors

Supercapacitors use active carbon electrodes to increase surface area, and this increases their capacity. The specific energy of supercapacitors is several orders higher than typical electrolytic

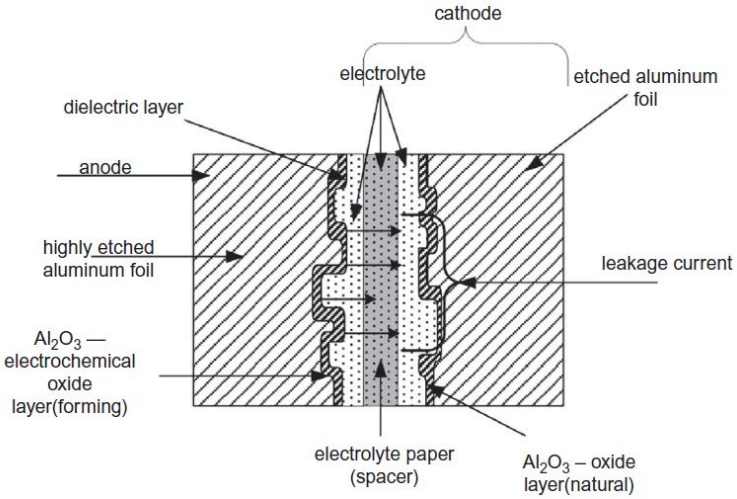


Figure 2.4: Internal structure of an aluminum electrolytic capacitor [42]

	Aluminum	Tantalum	Niobium	Ceramic	Film
Dielectric	Aluminum oxide	Tantalum pentoxide	Niobium pentoxide	Based on barium titanate, etc.	Polyester, polypropylene, etc.
Shape	Screw terminal type, snap-in type, lead terminal type, chip type	Chip type, dip type	Chip type	Chip type, dip type	Dip type, case type for SMD
Advantages	Cheap, small size, and large capacity	Small size and comparatively large capacitance, semipermanent service life	Small size and comparatively large capacitance, semipermanent service life	Small-size, no polarity	Good characteristics, can be made for low- to high-voltage applications, high reliability
Disadv.	Short service life in hot environment, large tolerance, polarized	Can be used with some voltage leeway, polarity	Can be used with some voltage leeway, polarity	Large changes in capacitance due to changes in temperature and DC voltage	Large outside dimensions

Figure 2.5: Characteristics of different capacitor types [42]

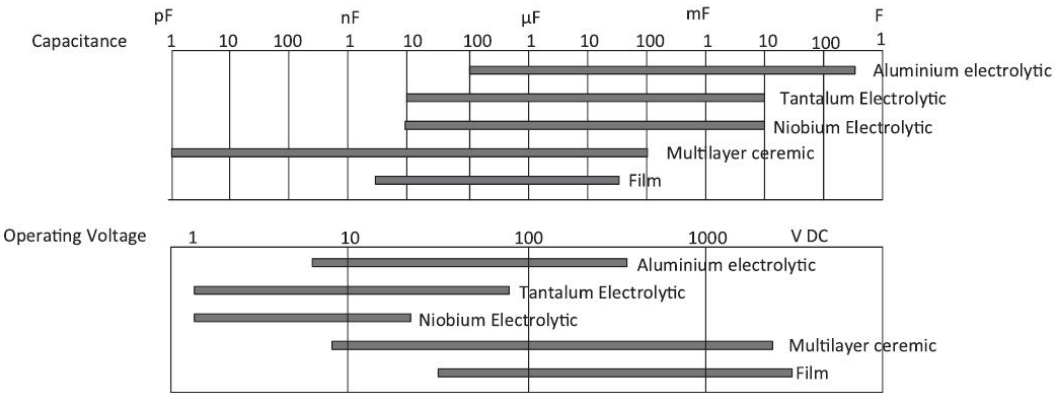


Figure 2.6: Ranges of capacitance and operating voltage of different capacitor types [42]

capacitors. The taxonomy of supercapacitors in Figure 2.7 which shows that electrical double-layer capacitors, hybrid capacitors and pseudocapacitors are the three main varieties of supercapacitors. Figure 2.8 illustrates the internal construction of the three different categories. Electrical double-layer capacitors (EDLCs) use active carbon electrodes whose large surface area result in capacitances of up to 3000 F. Pseudocapacitors store energy with a fast and reversible faradaic reaction (redox reactions) near the electrode surface, and this increases their capacitance compared to EDLCs [44]. Li-ion capacitors are an example of pseudocapacitors. However,

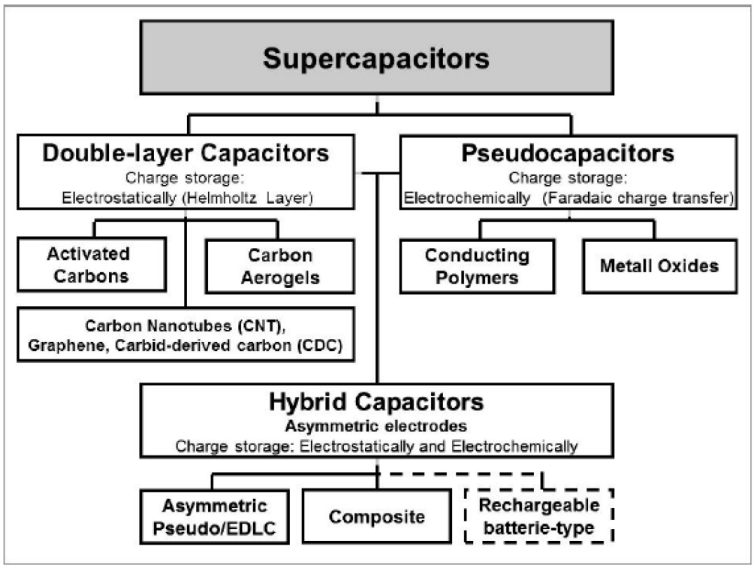


Figure 2.7: Taxonomy of supercapacitors [43]

their power density is not as high as an EDLC, due to the speed of the electrochemical process. Hybrid capacitors use one active carbon electrode and one electrode similar to those in pseudocapacitors, so have intermediate behaviours compared to EDLC and pseudocapacitors (higher power density than pseudocapacitors and higher energy density than EDLCs). Voltage and current discharge curves of EDLCs, hybrid capacitors and capabatteries (pseudocapacitors) under constant resistance are shown in Figure 2.9(a), (b) and (c) respectively. Discharge curves for hybrid SC and capabatteries are shown in Figure2.9 (d), where the x-axis represents percentage depth of discharge.

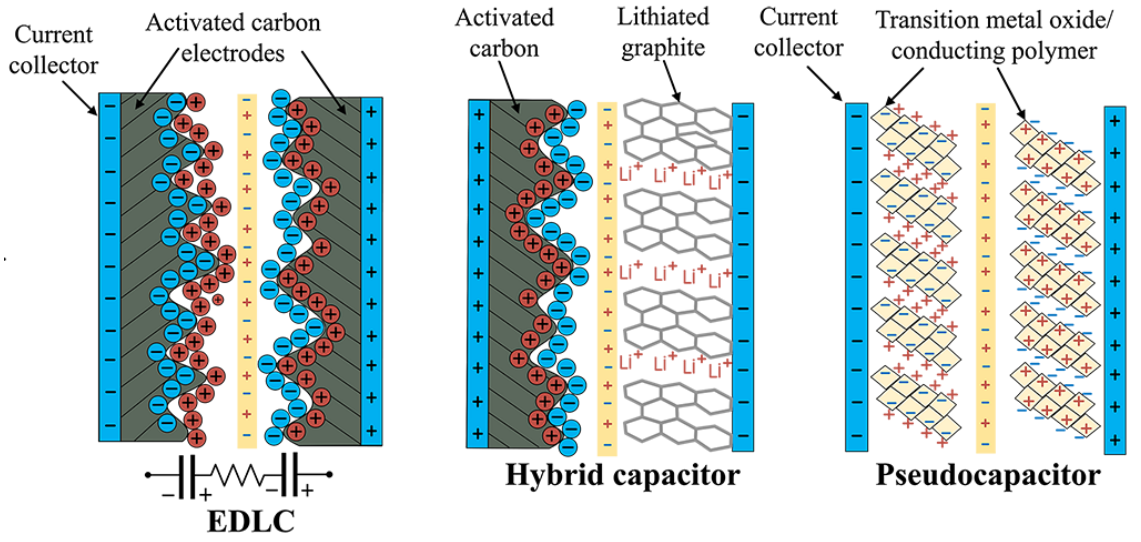


Figure 2.8: Construction of EDLC, hybrid capacitors and pseudocapacitors

While symmetrical supercapacitors are advancing towards rated voltage values of 3.0 V, hybrid versions can reach 3.8 V and higher [16]. With the maximum power delivery condition occurring with equal load resistance and internal resistance, for a supercapacitor, its maximum power capability is given by,

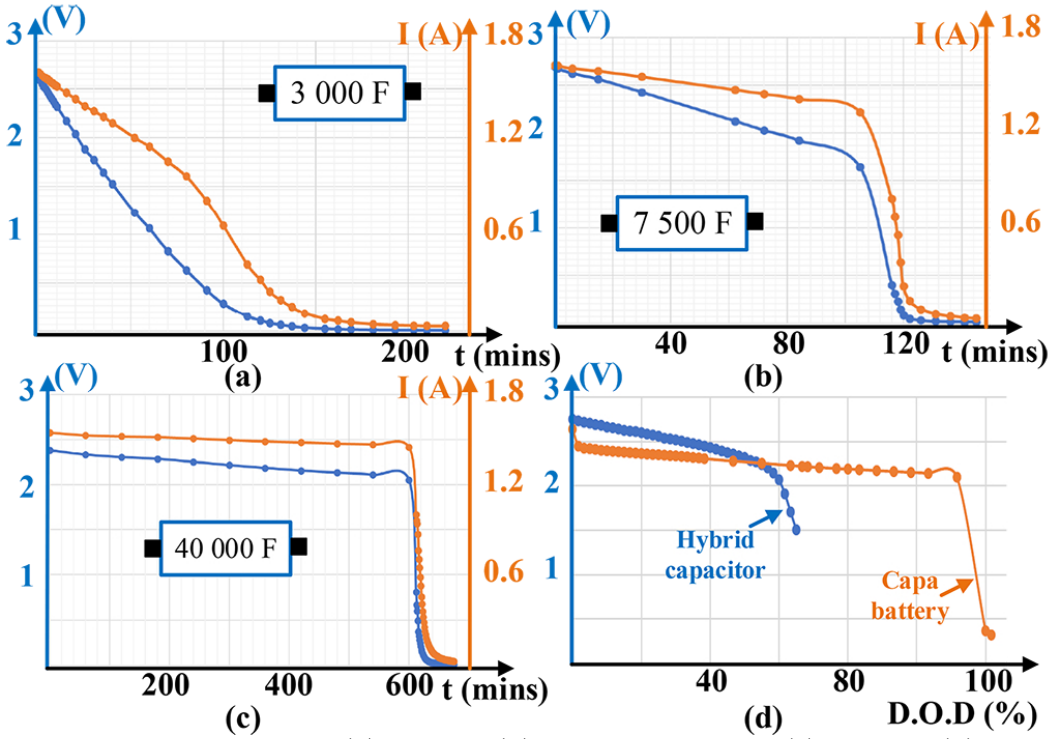


Figure 2.9: Discharge curve of (a) EDLC; (b) hybrid capacitor; (c) CABA; (d) hybrid and CABA, under constant current (voltage against depth of discharge) [1]

$$P = \frac{1}{4r_{\text{int}}}V^2 \tag{2.6}$$

Figure 2.10 depicts the position of supercapacitor families in terms of energy density and power density compared to batteries of different kinds and fuel cells [44]. According to the Ragone plot, the energy density of pseudocapacitors (battery capacitors) almost reaches the energy density of Li-ion batteries. Unlike batteries, the equivalent series resistance of supercapacitors remains constant as they discharge (Figure 2.11).

Table 2.2 compares the essential properties of rechargeable Li-ion and lead-acid batteries with three commercially available families of supercapacitors. The capacitance of a SC remains constant throughout its operating temperature range, as shown in Figure 2.12; however, internal resistance decreases with the increasing temperature. As shown in Figures 2.13 and 2.14, the capacitance of a supercapacitor deteriorates as we use it, while its ESR increases. However, capacitance and resistance performance can be improved by using a supercapacitor below its rated voltage. In both figures, the 2.5 V line verifies this behaviour, and this property is very important when designing supercapacitor-based solutions. The main properties of supercapacitors can be summarised as [41]:

- Low leakage current : less than 5 μA
- High power: very high discharge current
- Low ESR (equivalent series resistance)
- Wide operational temperature :-40 to 85 °C
- Long life: 5 years at 70 °C

- High reliability

Table 2.2: Recent advances in commercial supercapacitor devices [2015–2019], compared with Li-ion and lead-acid batteries [Supercapacitor information courtesy of Samwha Electric, Korea]

Energy storage	Max power (W/kg)	Energy density density (Wh/kg)	Life cycle	Temperature range
Li-ion battery	3 000	200	500 – 1 000	0 to 60
Lead-acid battery	250	100	500 – 1000	0 to 40
Symmetrical supercapacitor	10 000	4 – 10	500 000 – 1 000 000	−40 to 60
Hybrid supercapacitor	5 000	7 – 12	50 000	−20 to 60
Capabattery	4 000	20 – 60	15 000 – 20 000	−20 to 50

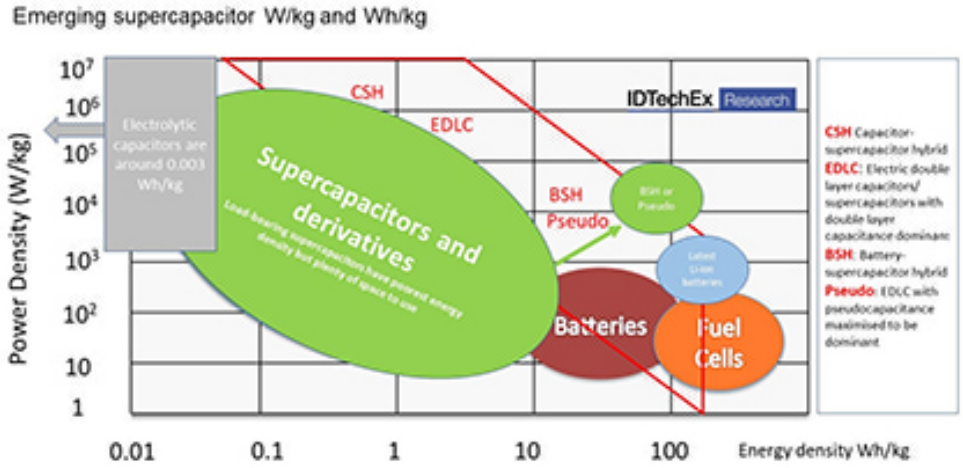


Figure 2.10: Ragone plot of modern supercapacitor [45]

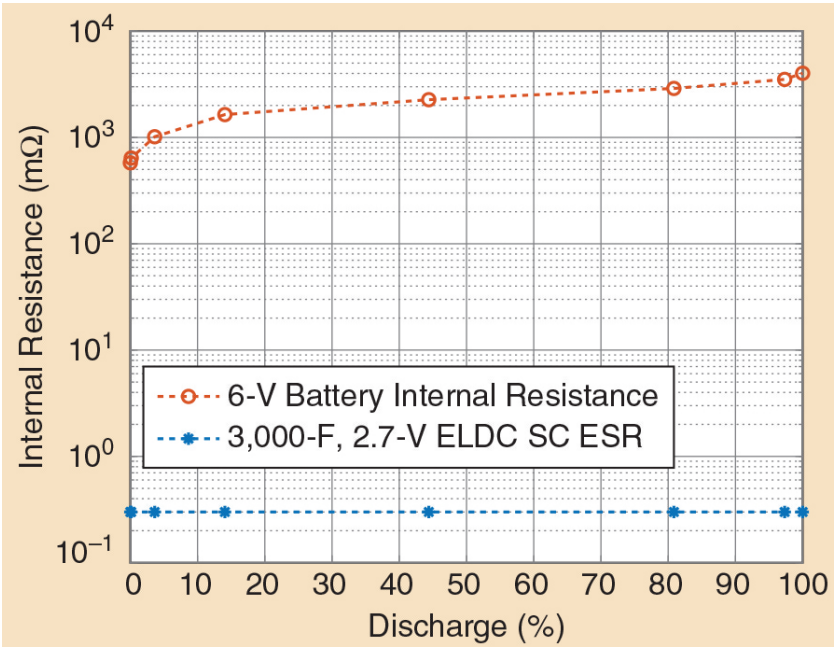


Figure 2.11: A comparison of internal resistance in a supercapacitor vs an energizer 6 V battery [16]

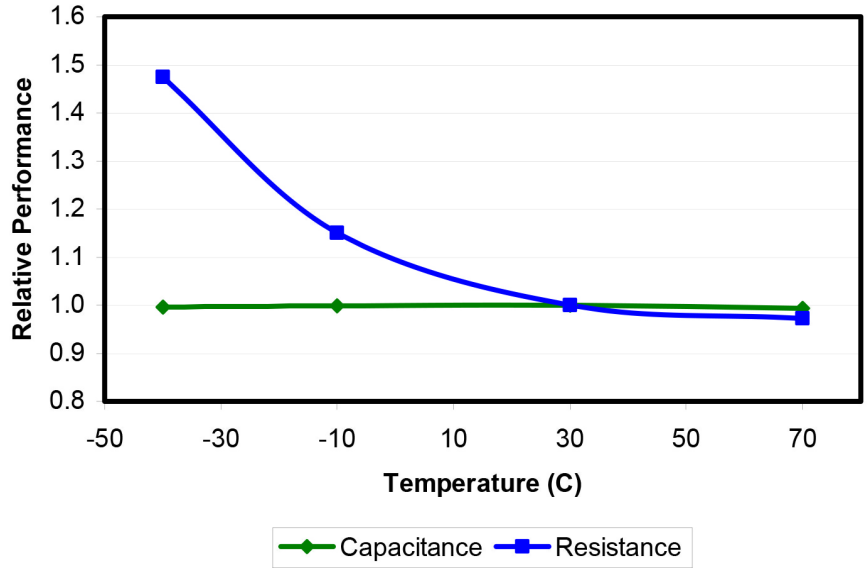


Figure 2.12: Performance of supercapacitor against temperature [46]

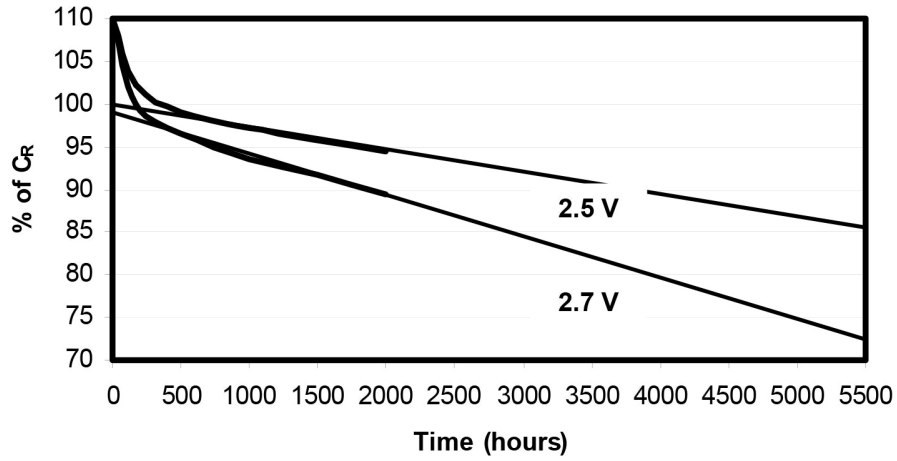


Figure 2.13: Supercapacitor Cell capacitance degradation at 2.7 V and 2.5 V at 65 °C [46]

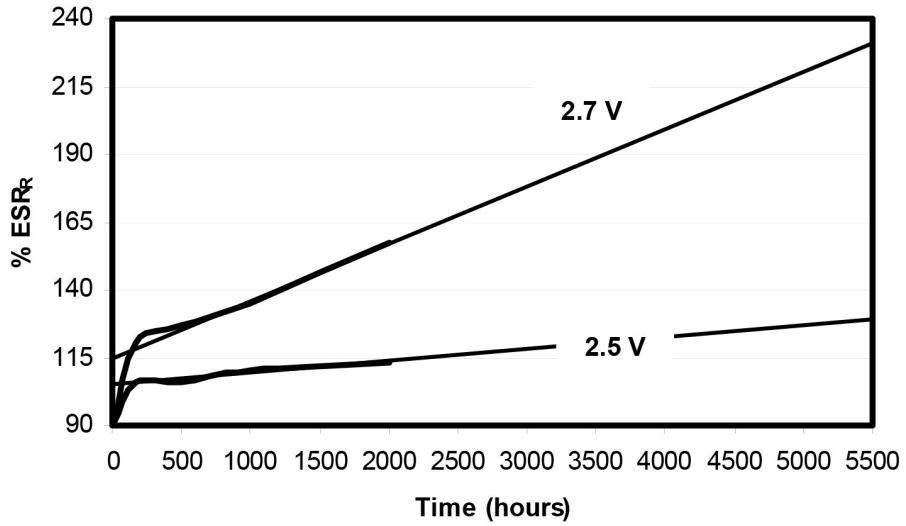


Figure 2.14: Cell resistance degradation at 2.7 V and 2.5 V at 65 ° C [46]

Supercapacitor technology has been developing rapidly over the last decade, with about 80 manufacturers worldwide [47] manufacturing at least three different variations, with single-cell capacitance values from 1 F to over 70 000 F. The geographical distribution of supercapacitor manufacturers is shown in Figure 2.15, which is an indication of the maturity and popularity of supercapacitor technology today [45]. Figure 2.16 lists leading supercapacitor manufacturers, the range of their supercapacitor products and their main applications.

Region	Number
IDTechEx Research	
China	30
USA	19
Japan	10
Europe	9
Korea	4
Other	8
TOTAL	80

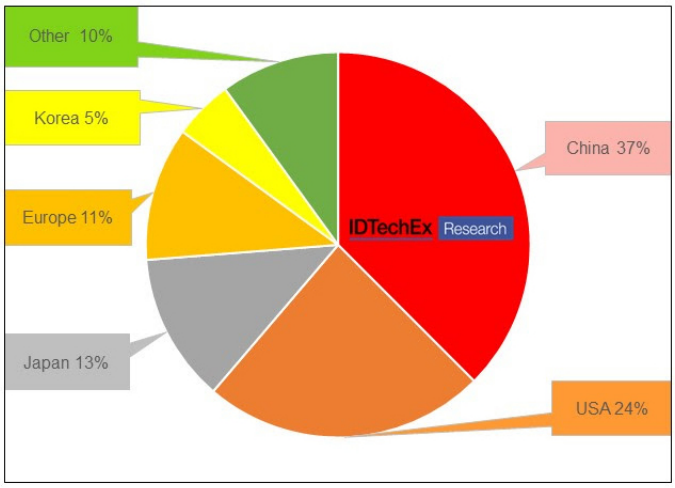


Figure 2.15: Supercapacitor manufacturers by territory 2020 [45]

Examples of the large emerging market for 0.1 kWh to 1MWh supercapacitors

Supplier	kWh	C F	V	Application of large supercapacitor pack	Chemistry
Arvio	7.1	na	na	On- and off-grid inverter battery replacement	LIC
Aowei	60	2200	500	Locomotives	LIC
	9.5	583	500	Tram, marine charger, power compensator.	
	32	605	500	City bus, mining locomotive, tunnel locomotive, port truck	
Shanghai Greentech	0.1	100,000	2.7	Complete battery replacement in mild hybrid car. Peak shave in full hybrid car	LIC
Jianghai	1.1	7500	32	AGV, power grid, EV, train, elevator	LIC
Maxwell	0.235	7.1	1300	UPS, microgrid balancing	EDLC
Maxwell+ partner	8.0	na	na	Photovoltaic smoothing and load shifting	
Maxwell-Freqcon	150	na	na	Microgrid	
LS Ultracapacitor	0.145	62	129.6	Hybrid bus, tram, trolley, heavy duty transport, harbour cranes, ESS electricity purifier.	EDLC
Eaton	900	130 F	62 stack	Hospital UPS and peak shaving.	EDLC
Dongguan Gonghe	7.5	8.5	48	Heavy transport	EDLC
Integrator Oerlikon	0.33	na	na	Large mining excavators	EDLC
Office of Naval Research USA	8.2	na	na	Rail gun	EDLC

Figure 2.16: Emerging market for 0.1 kWh to 1 MWh supercapacitors [45]

As shown in In Table 2.3, the prices of SCs are comparable with traditional electrolytic capacitors of the same size (canister size is given in diameter (d) $\times$ height (h) in mm) [16].

Table 2.3: Price comparison of supercapacitors and electrolytic capacitors of the same canister size [16]

Canister size (d × h mm)	3 V EDLC (F)	Price per 1,000 pieces (USD)	Electrolytic	Price per 1,000 pieces (USD)
8 × 13	1	0.4	100 μ, 25 V	0.18
10 × 20	5	0.53	470 μ, 35 V	0.24
10 × 30	10	0.6	1 000 μ, 25 V	0.4
16 × 25	25	1.6	4 700 μ, 10 V	0.88
18 × 40	50	1.8	470 μ, 50 V	1.7

2.5 Typical applications of supercapacitors

Supercapacitors are used in various industries for power requirements ranging from a few milliwatts to several hundred kilowatts [46]. Unlike batteries, energy storage in supercapacitors does not involve chemical reaction, so supercapacitors can charge/discharge efficiently. Since they have low internal resistance, they can deliver instant high power. This makes them an ideal choice for pulse power applications. By connecting them in parallel with batteries, we can extend battery life as the supercapacitor can buffer peak demand for current. Supercapacitors are used in pulse power applications in digital cameras, hybrid drive systems and regenerative braking systems (to harvest energy) [46]. Supercapacitors are ued for as temporary energy backup in many applications to bridge power supply between power interruptions and to provide backup power. Supercapacitors can be used as the primary power source in applications that require power for a short duration or in situations where they have enough time to replenish the charge. Such applications include toys, emergency flashlights, restaurant paging devices and emergency door power systems. Another application of supercapacitors is using them as an energy reservoir to critical operations during shutdown, memory backup and event notification.

Supercapacitors are widely used in application domains such as automotive, transportation, industrial environments and consumer electronics. Supercapacitors are used in hybrid buses and trains to harvest energy from regenerative braking for subsequent release when the vehicle accelerates. This technique helps to recover energy wasted in the friction-based braking and extends battery life by releasing stored energy during peak demand. Supercapacitors also used to provide cranking power and to stabilise voltage in start-stop systems in automotive applications. They are used in blade pitch systems in windmills to increase the energy grid's reliability and stability. Also, supercapacitors can be used to harvest energy in heavy vehicles such as cranes and to provide burst power in lifting operations. In data centres, supercapacitors can be used to provide short-term DC-UPS following power failures and to bridge with power sources such as diesel generators. In renewable energy installations, supercapacitors can be used as energy storage for stabilising the output. In aircraft, supercapacitors are used to operate doors during power failures [46].

Most supercapacitor manufacturers sell high voltage-capable supercapacitor modules (SCM) which are suitable for cold-weather truck starting, while smaller SC modules of around 15 V DC voltage rating, are used in eco-drives (start-stop systems) in modern automobiles [48]. A few commercially available SC modules from Maxwell Technologies, now owned by Tesla, are shown

in Figure 2.17. The 48 V, 165 F module targets hybrid vehicles, heavy industrial equipment, railway applications, and UPS systems; Its high immunity to shock is a unique advantage. The 75 V, 94 F module (Figure 2.17(b)) is specifically designed for low duty cycle energy storage applications such as wind turbine pitch control and backup power generation. The 125 V, 63 F module targets buses, electric trains and trolleys, heavy-duty transportation, cranes, utility vehicles and mining equipment. The module can operate in temperature from $-40\ ^0$ C to $65\ ^0$ C, and the rated number of duty cycles is 1 000 000. Retrofit modules are shown in Figure 2.17(d) as a drop-in solution that can be used to replace battery systems in 1.5 MW turbines, and one module is equivalent to four batteries, and their charger circuit [49].

(a) (b) (c) (d)

Figure 2.17: Commercially available SC modules from MAXWELL technologies: (a) 48 V module; (b) Technologies' 75 V module; (c) 125 V transportation module; (d) Retrofit solutions for emergency backup systems [49]

2.6 Supercapacitors for AC line filtering

The most common application of capacitors is rectified AC line filtering. It is interesting to see how effective a supercapacitor is for this application. According to the detailed analysis present in [42], supercapacitors have certain disadvantages when used for AC line filtering in utility supplies.

A typical full-wave rectifier circuit and the primary output waveform are shown in Figure 2.18. For the ideal case, after the full-wave rectification and smoothing stage, the approximate DC voltage (V_{DC}) is given by the equation:

$$V_{\mathrm{DC}} \approx V_{\mathrm{peak}} - 2V_{\mathrm{D}} - \frac{I_{\mathrm{L}}}{4fC} \tag{2.7}$$

where V_{peak} represents the peak voltage of rectified DC, V_{D} is the forward voltage drop of the rectifier diode, I_{L} is the average load current, f represents the frequency of the ripple, and C is the capacitance of the smoothing capacitor used.

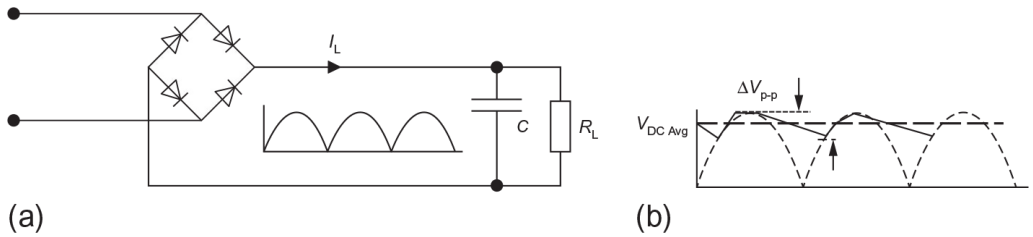


Figure 2.18: AC rectification: (a) full wave rectifier circuit with smoothing capacitor; (b) output waveform [42]

However, in addition to the above basic components, the resistance of the diodes and power source (R_s) appear in series to the circuit, while the equivalent series resistance (ESR) of the capacitor appears in parallel. This case is shown in Figure 2.19. As analysed in [42] the transfer function applied to the output voltage is given by:

$$\frac{V_o(s)}{V_{in}(s)} = \frac{R_L(R_cC_s + 1)}{[(R_L + R_C)R_s + R_LR_C]C_s + (R_L + R_s)} \tag{2.8}$$

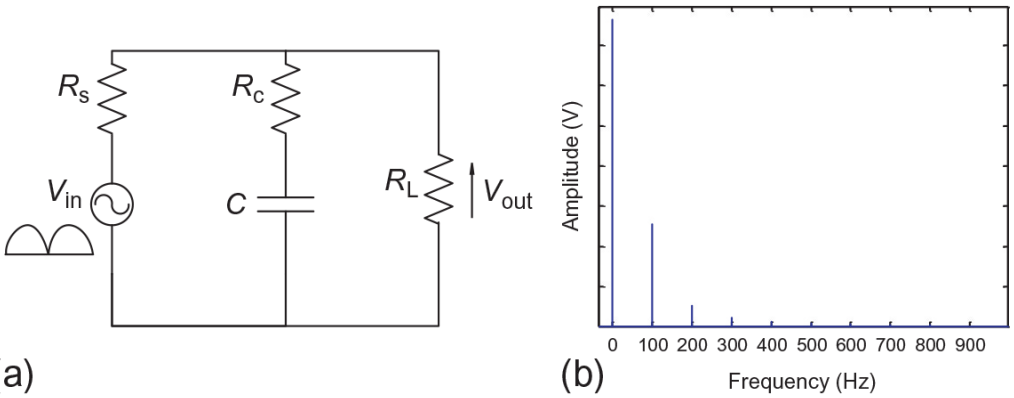


Figure 2.19: Full-wave rectifier circuit: (a) equivalent circuit; (b) spectrum of the full-wave rectified sine waveform [42]

The main purpose of using a capacitor for AC to DC conversion is to increase the DC voltage by minimizing the harmonic components generated by diode rectification. The experiment shown in Figure 2.20 uses a 5 V rms AC rectified waveform with a light load of a 20 Ω. No smoothing capacitor is used for the case shown in Figure 2.20, where (a) depicts the output voltage and input current oscillogram, while (b) depicts the fast Fourier transformed (FFT) waveform. For the second case shown in Figure 2.20(c) and (d) a 3300 μF electrolytic capacitor with 20 mΩ ESR is used as a smoothing capacitor. According to the output waveform shown in Figure 2.20(c), only a small ripple appears, showing effective rectification. According to Figure 2.20(d), most of the higher-order harmonics are suppressed with the capacitor effectively acting as a low-pass filter, increasing the DC component. For the experiment shown in Figure 2.20(e) and (f), two 25 F supercapacitors with 42 mΩ ESR are used as the smoothing capacitor. This arrangement significantly increases the higher-order (100 Hz and above) harmonics and increases the current drawn from the input. The impedance of the capacitor gradually decreases above the frequency of 100 Hz, and this increases the power dissipation in the ESR of the capacitor.

The electrolytic capacitor effectively functions as a smoothing capacitor due to its low time constant compared with the 10 ms half period of the AC waveform. When we carefully study the DC components in FFTs in Figure 2.20(d) and (f), for the supercapacitor the DC component is 2 dB lower than for the electrolytic capacitor. As shown in Figure 2.21 the electrolytic capacitor is effectively working as a low-pass filter with a phase angle of -60^0. However, the supercapacitor phase angle is almost 0 for at around 100 Hz frequency, as shown in Figure 2.21(b).

Another problem with using a supercapacitor for AC line filtering is the initial time needed to stabilise the DC voltage. For example, to rectify 5 V rms AC input, two series 25 F capacitors take 6 s to initialise, while a 3300 μF electrolytic capacitor takes only 550 μs. An oscillogram

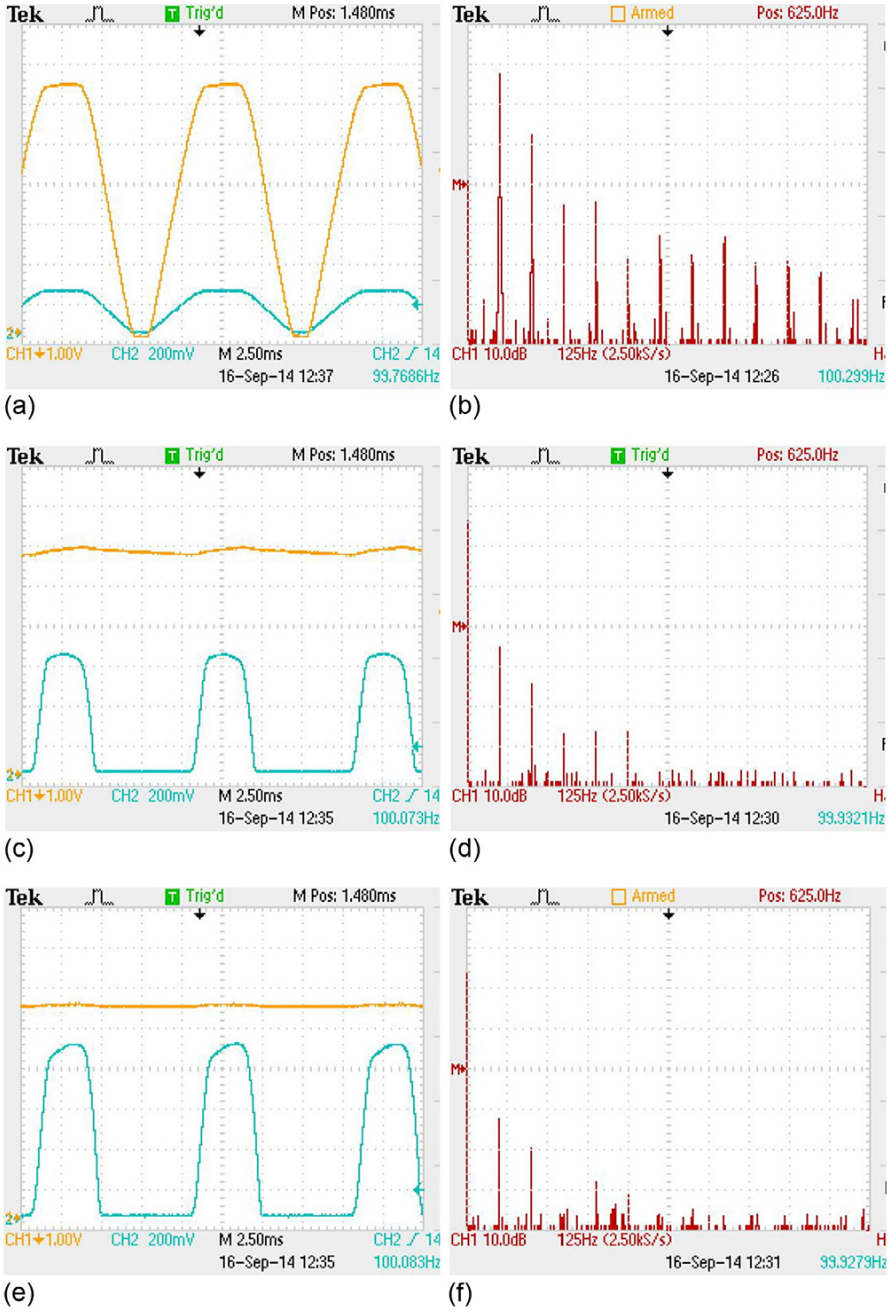


Figure 2.20: Oscillogram and FFT plot for three different cases of rectification: (a)(b) without smoothing capacitor; (c)(d) with a electrolytic capacitor; (e)(f) using supercapacitor as smoothing capacitor [42]

for this scenario is shown in Figure 2.22. Also, due to supercapacitors' low cell voltage, several need to be put in series to obtain the desired voltage capacitor bank.

2.7 Disruptive new applications of supercapacitors

In the previous section, we discussed traditional applications of supercapacitors. The Power electronics research group at the University of Waikato has developed a new range of applications which are now known as supercapacitor assisted (SCA) techniques applicable to high-efficiency

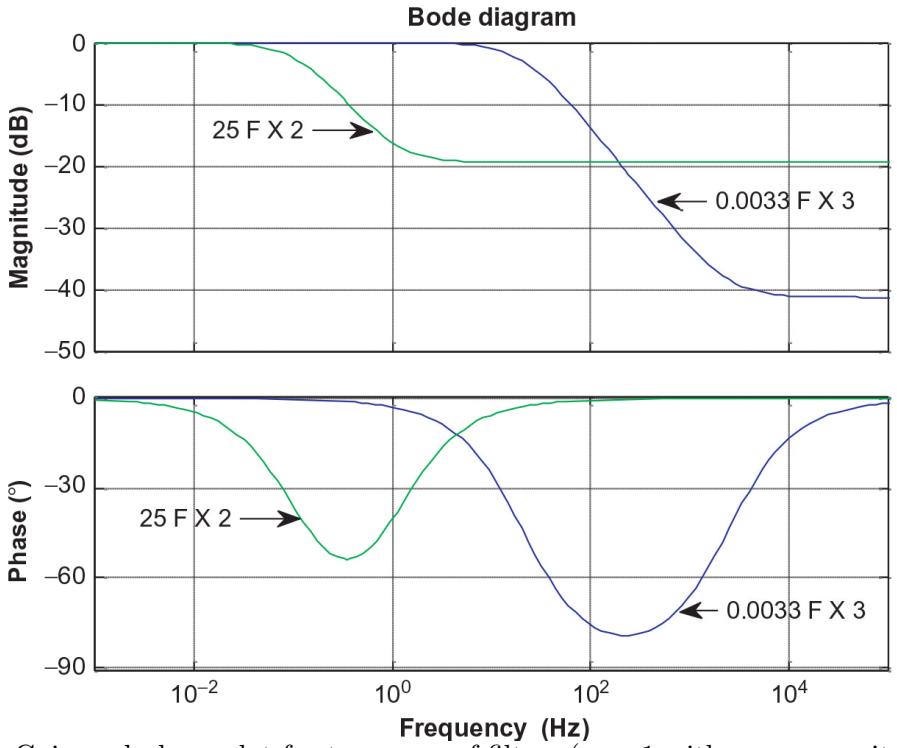


Figure 2.21: Gain and phase plot for two cases of filters (case 1 with supercapacitor and case 2 with electrolytic capacitor [42]

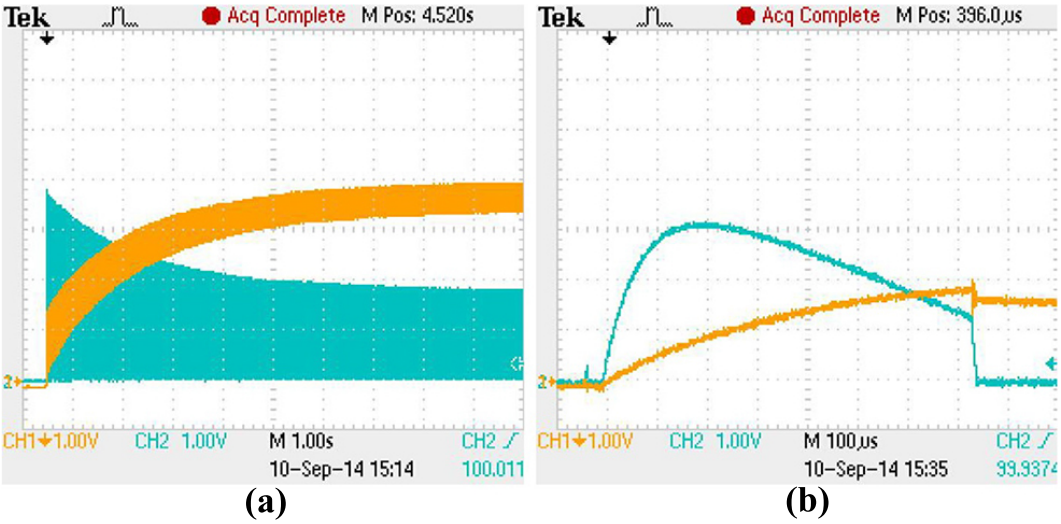


Figure 2.22: Time delays to stabilize the DC output of capacitor filters (a) 25 F supercapacitor and (b) 3300 μF electrolytic capacitor. [42]

DC-DC converters, surge absorbers, rapid heat transfer, white goods and renewable energy-based LED lighting techniques. This section provides an overview of this new range of applications.

SCA techniques such as the SC-assisted low dropout regulator (SCALDO), and SC-assisted LED (SCALED) could be used to achieve significantly higher ETEE (end-to-end efficiency), since they help to remove the converter stages in appliances. These techniques are also useful in eliminating secondary issues such as RFI/EMI typical of high-frequency switching converters. Almost all these SCA techniques are very low-frequency converters, where any switching happens at millihertz to hertz order frequencies.

2.7.1 The SCALDO converter

When designing DC-DC converters, two standard approaches used are (i) linear regulators, where a series pass transistor is fed by a feedback-controlled loop, and (ii) high-frequency switch-mode techniques where a switch, inductor, capacitor and a freewheel diode are combined with a high-frequency PWM controller circuit. A third approach used for very low load requirements is the switch capacitor converter. A switch-mode converter based on ideal components theoretically gives 100% efficiency, but in practice drop to much lower values due to secondary losses in components, particularly the high-frequency switching losses in switching transistors.

In a linear converter the approximate efficiency is governed by the $V_{\text{out}}/V_{\text{in}}$ ratio, indicating that larger voltage differences across series transistors mean lower efficiencies. If $V_{\text{in}} - V_{\text{out}}$ in the worst case situation can be kept very low, a high-efficiency linear converter known as the low dropout (LDO) regulator is produced [50]. Despite the increasing popularity of switch-mode power supplies, linear regulators are still widely used in the industry due to their low noise output and design simplicity [51]. They do not radiate RFI/EMI as switching regulators do, and have fast responses for load and source fluctuations.

SCALDO is an entirely new approach to designing high-efficiency DC-DC converters in which a linear low dropout regulator (LDO) is combined with a low-cost compact SC of a few farads, which acts as a near-lossless voltage dropper (discussed in Chapter 3) and is directly applied as per Figure 2.23(a). Figure 2.23(b) shows how accumulated extra energy in the SC is discharged back to the LDO to maintain the SC charge balance while disconnecting the input energy source during the second half of the low-speed conversion cycle.

The practical operation of the SCALDO technique is implemented using four very low-speed switches to alternate between charging and discharging modes [52]. One fundamental advantage of the SCALDO circuit is that switches operate at very low frequencies in the order of millihertz to fractional hertz, eliminating the RFI/EMI issues typical of high-frequency switching converters. Another important fact is that this technique is not a variation of a switch capacitor converter circuit [53].

SCALDO topology has two design variations: (i) voltage difference between input and output is large with input voltage V_{P} being at least twice the minimum input voltage of the associated LDO ($V_{\text{in}}^{\text{min}}$), and (ii) when V_{P} value is smaller than twice ($V_{\text{in}}^{\text{min}}$).

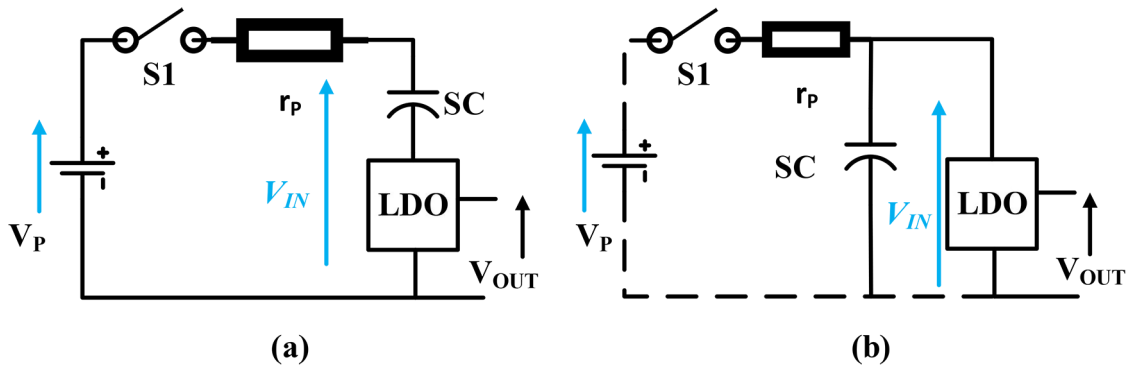


Figure 2.23: The SCALDO concept: (a) supercapacitor accumulating energy; (b) SC discharging to LDO

Design variation where source voltage $V_P > 2V_{min}^{in}$

When the source voltage is more than double the minimum required voltage of the LDO, $V_p - V_{in}$ exceeds the V_{min} voltage and the voltage built in a single capacitor bank is enough to power the LDO. During the charging phase, capacitor banks are connected in series and during the discharging phase, they are connected in parallel. Supercapacitor bank is utilised below its rated voltage in each configuration.

Under this condition, the number of capacitor banks required is given by [17],

$$n < \frac{V_p - V_{min}^{in}}{V_{min}^{in}} \tag{2.9}$$

the SC banks are connected during charging and discharging phases as shown in Figure 2.24.

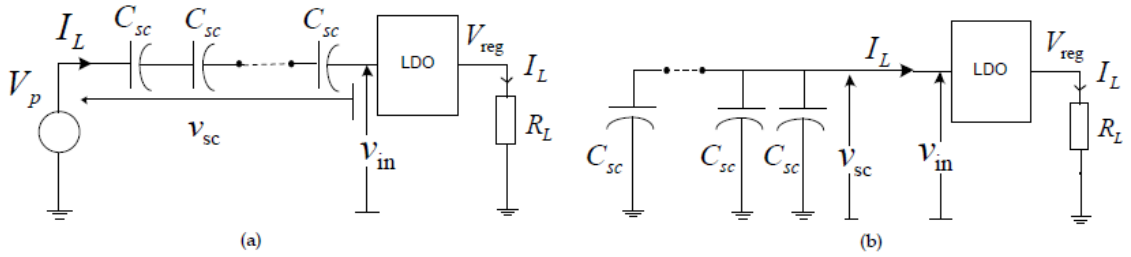


Figure 2.24: The concept of SCALDO regulator for $Vp > 2V_{in}^{min}$: (a) Charging n capacitors in series; (b) discharging n capacitors in parallel releasing stored energy

and the number of switches required is $3n + 1$. Efficiency during this phase is given by,

$$\eta = (n + 1)\,\frac{V_{reg}}{V_p} \tag{2.10}$$

switch arrangement for the general configuration of $V_P > 2V_{in}^{min}$ is shown in Figure 2.25.

Design variation where source voltage $V_P < 2V_{min}^{in}$

When the source voltage is less than double the minimum required voltage of LDO, $V_p - V_{in}$ is less than the minimum required (V_{min}^{in}) voltage and the voltage accumilated in a single capacitor bank is not sufficient to power the LDO. Hence, capacitor banks need to be connected in series to build the required voltage, then connected in parallel, while charging. The number of capacitor banks required is,

$$n > \frac{V_p - V_{min}^{in}}{V_p - V_{min}^{in}} \tag{2.11}$$

the SC banks are connected during charging and discharging phases as shown in Figure 2.26. with $3n + 1$ switches giving efficiency,

$$\eta = \left(1 + \frac{1}{n}\right)\frac{V_{reg}}{V_p} \tag{2.12}$$

switch arrangement for the general configuration of $Vp < 2V_{in}^{min}$ is shown in Figure 2.27.

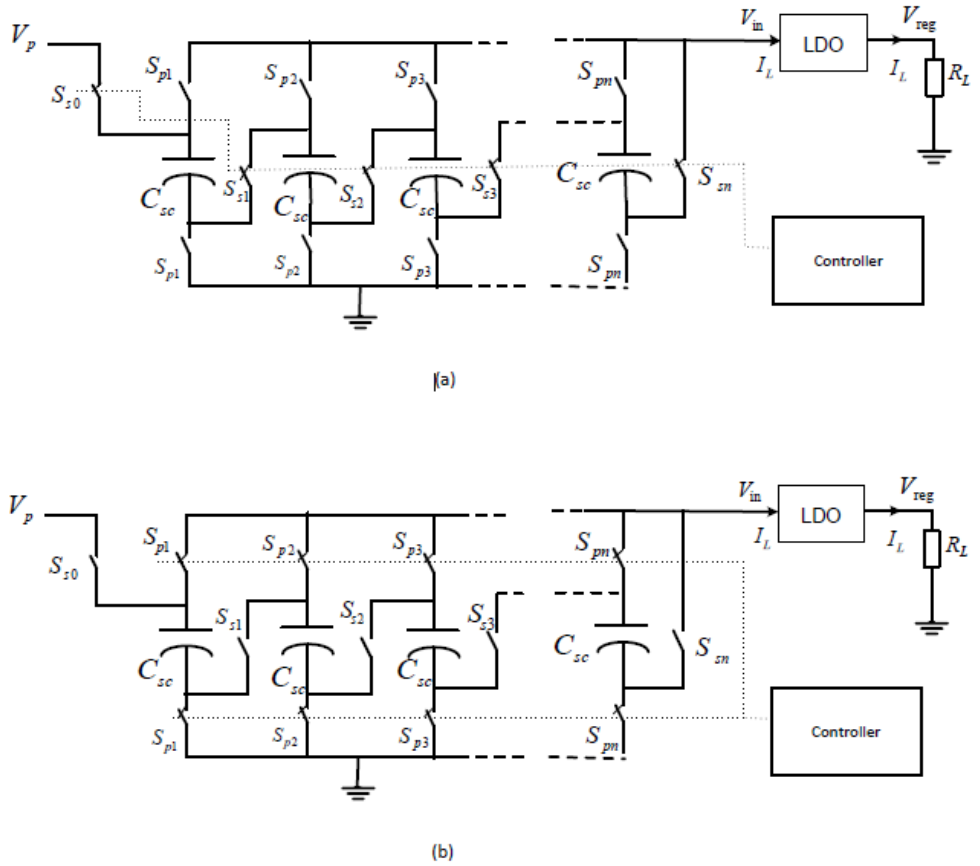


Figure 2.25: Switch arrangement for $Vp > 2V_{\text{in}}^{min}$: (a) charging n capacitors in series; (b) discharging n capacitors in parallel releasing stored energy

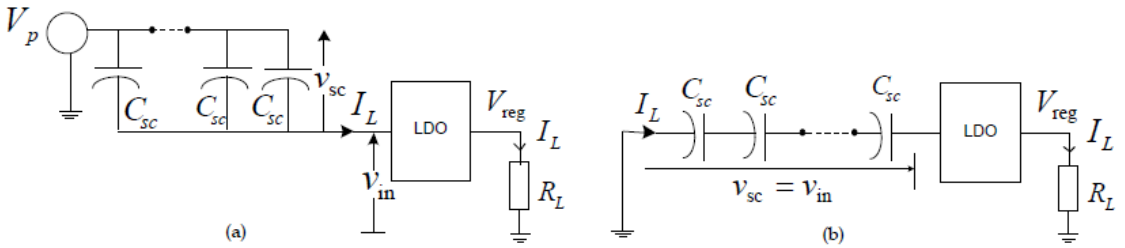


Figure 2.26: The concept of SCALDO regulator for $Vp < 2V_{\text{in}}^{min}$: (a) charging n capacitors in parallel; (b) discharging n capacitors in series releasing stored energy

The switching arrangement for the charging phase of $12 - to - 5 - V$ SCALDO prototyp is shown in Figure 2.28(a), and the switching arrangement for the discharging phase is shown in Figure 2.28(b). Efficiency enhancement for the prototype is depicted in Figure 2.28(c). This design is an example for design variation $V_{\text{P}} > 2\text{V}_{\text{min}}^{\text{in}}$. SCALDO converter is compared with existing power converter techniques in Table 2.4.

SCALDO has been extended to other useful techniques such as the dual-output supercapacitor assisted low dropout regulator (DO-SCALDO), reduced-switch SCALDO (RS-SCALDO) and a SCALDO extension for the Google server rack. Supercapacitor assisted LED lighting (SCALED) and supercapacitor assisted wide input PV inverter (SCAWI-PV inverter) are different branches of SCA techniques described in this chapter.

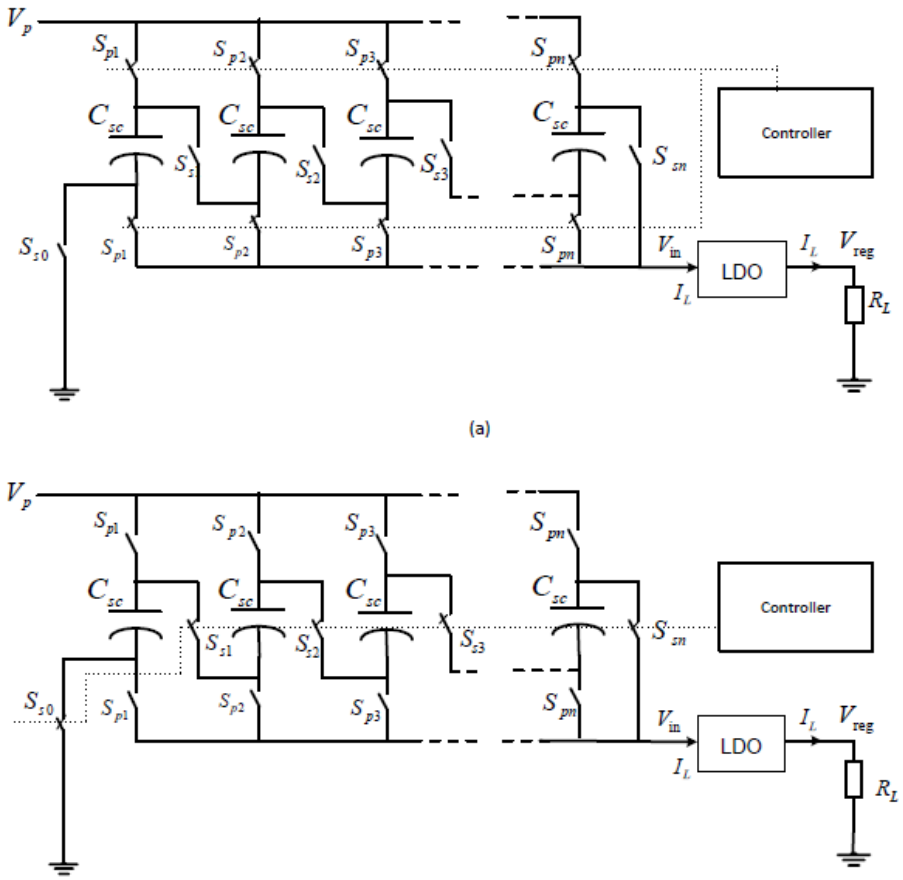


Figure 2.27: Switch arrangement for $Vp < 2V_{\text{in}}^{min}$: (a) charging n capacitors in parallel; (b) discharging n capacitors in series releasing stored energy

2.7.2 Reduced switch SCALDO

Reduced-switch SCALDO (RS-SCALDO [54]) is a topological variation of SCALDO that requires fewer switches. By designing an alternately operated high-current LDO pair, RS-SCALDO can handle high load currents, allowing the development of a linear voltage regulator module (VRM). As shown in Figure 2.29, for the $V_{\text{p}} > 2V_{\text{in}}^{\text{min}}$ criterion, using two identical LDOs the number of switches can be reduced to two in RS-SCALDO instead of the four switches required for SCALDO. More theoretical and experimental details on this new modification can be found in [55].

2.7.3 Dual output SCALDO

Generating dual voltages from a single voltage level is an essential requirement in modern power electronics. The concept of rail-splitting is based on a virtual ground, where the input supply is divided into two halves with respect to this new voltage reference. For example, splitting of a 12 V supply into ±5 V rails from a single battery cell with a virtual ground as the 0 V reference (for the output rails) can be considered as a typical application. In such applications, access to the negative terminal of the battery is not a key requirement for the operation of the downstream devices as they see the dual outputs with respect to the virtual ground.

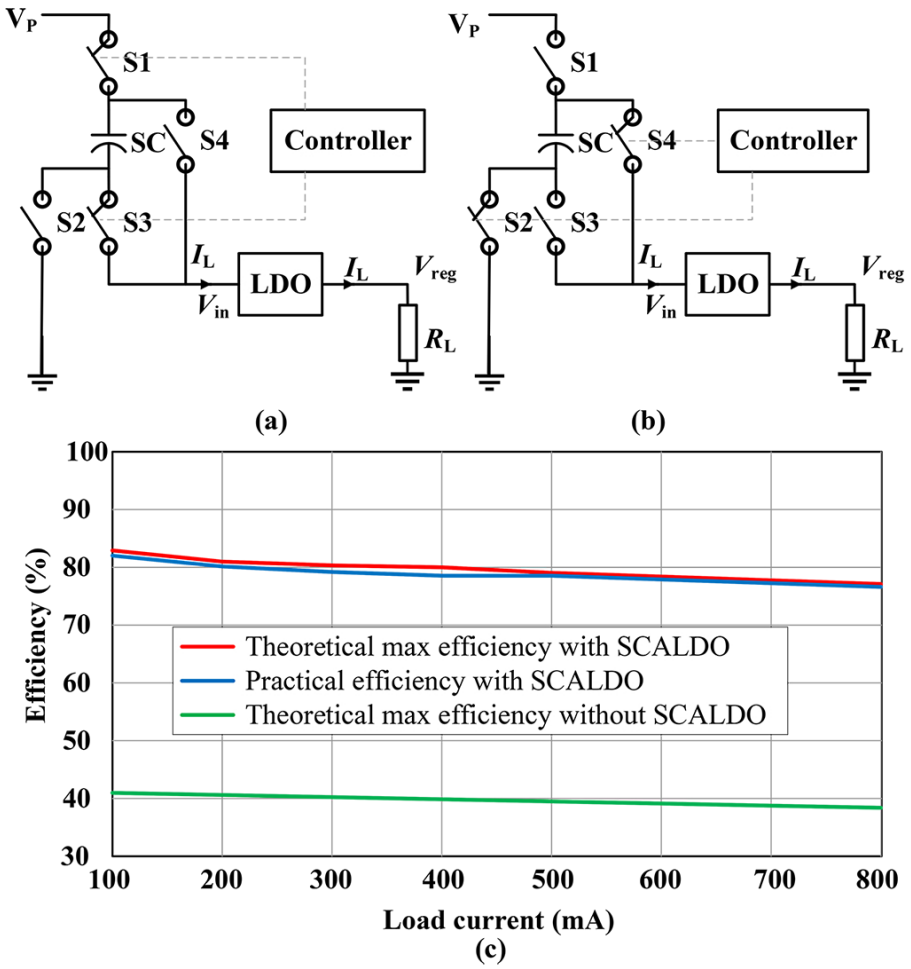


Figure 2.28: SCALDO implementation: (a) switch arrangement for charging phase; (b) switch arrangement for discharging phase; (c) efficiency curve for $12-5$ V prototype [1]

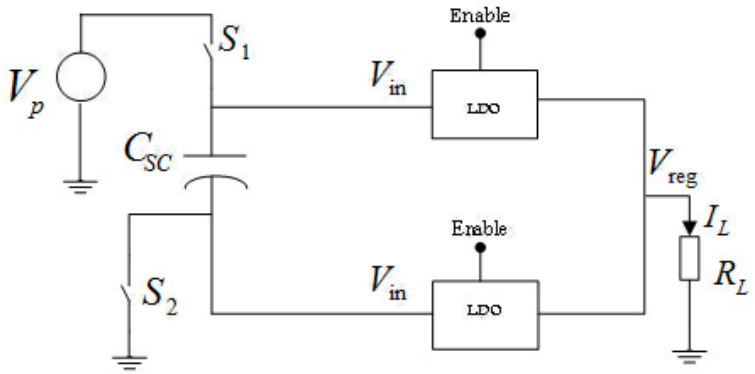


Figure 2.29: Modified RS-SCALDO (reduced switches) configuration with two identical LDOs and two switches

By extending the original SCALDO design a split-rail DC-DC converter with a positive-rail LDO regulator ($\mathrm{LDO_P}$) [56] and a negative-rail LDO regulator ($\mathrm{LDO_N}$) connected in series as illustrated in Figure 2.30 was developed. In this design, the outputs of these two LDO regulators create dual-polarity output voltages with respect to the virtual ground ($\mathrm{GND_V}$). However, in this situation, when there is a mismatch in the load currents of the two LDOs, regulation is not possible. In general, this situation can be overcome by using a voltage-balancing circuit [57, 58],

Table 2.4: Comparison of traditional DC-DC converters with SCA converters

Feature	High-frequency converter	Linear Regulator	SC-based low frequency converter
Cost	high	low	low to moderate
Noise	very high	low	low
Efficiency	high	low to moderate	high
Thermal management	best	good	good
Output current capability	high	high	high
Requirement for magnetic parts	yes	no	no
Design complexity	very high	low	low
Switching losses	very high	low	low
Protection to suppress voltage spikes	required	not necessary	not necessary
Tolerance for surges and power conditioning	no	no	yes
Transient response	slow	fast	fast
DC-UPS	no	no	yes
Form factor	small	small to moderate	depends on SC bank used

but with a loss of efficiency. The DO-SCALDO technique shown in Figure 2.30 brings a novel perspective to solve this fundamental problem using supercapacitor energy circulation to boost higher ETEE. The efficiency gain of DO-SCALDO is shown in Figure 2.31.

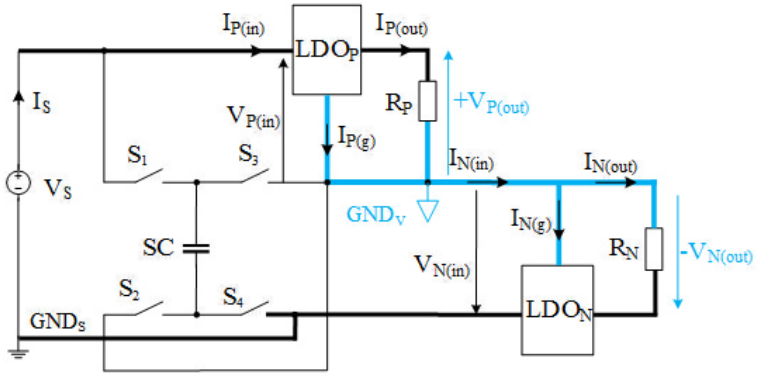


Figure 2.30: Dual output SCALDO topology (GND_V terminal acting as a virtual ground)

2.7.4 Supercapacitor assisted wide input (SCAWI) PV inverter

In developing inverters for solar applications, achieving higher efficiency is a key design requirement. In order to achieve this inverters for renewable energy applications are designed specifically for nominal input voltage values with limited margins [59]. For example, the two 300 W commercial inverters included in Table 2.5 are designed explicitly for 12 or 24 V nominal input voltages, to achieve efficiencies of over 85%. From the same manufacturer, for a 48 V DC input case, you need to select a different model. When inverters are designed for a wider input range, they become more expensive, with a lower ETEE [60]. An example is the 100 VA inverter with a 20 to 60 V input range from Absopulse Electronics [59], which comes with a lower efficiency of around 80% at a higher price.

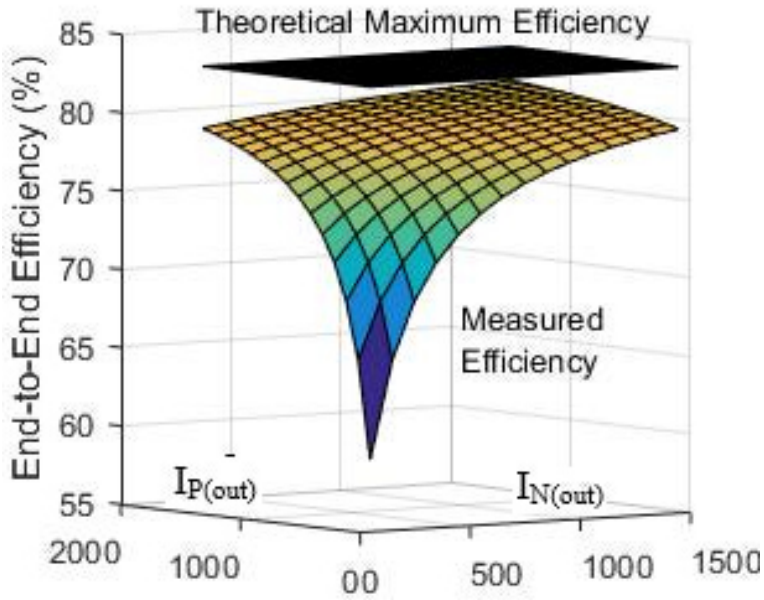


Figure 2.31: End-to-end efficiency of 12 V ±5 V DO-SCALDO (I_{P}-current in positive terminal, I_{N}-current in negative terminal in mA)

The above limitations of commercial inverters suitable for low DC input voltages encouraged the development of the supercapacitor assisted wide input (SCAWI) PV inverter, maintaining the same efficiency range of the original inverter with the added feature of DC-UPS capability.

Here, a single-phase inverter is chosen with its VA rating such that,

$$v_{\mathrm{DC}} i_{\mathrm{DC}} \eta = V_{\mathrm{AC}} I_{\mathrm{AC}} \tag{2.13}$$

where v_{DC} and i_{DC} are the voltage and current on the DC side of the inverter, η represents efficiency of the inverter, and V_{AC} and I_{AC} are the AC output values.

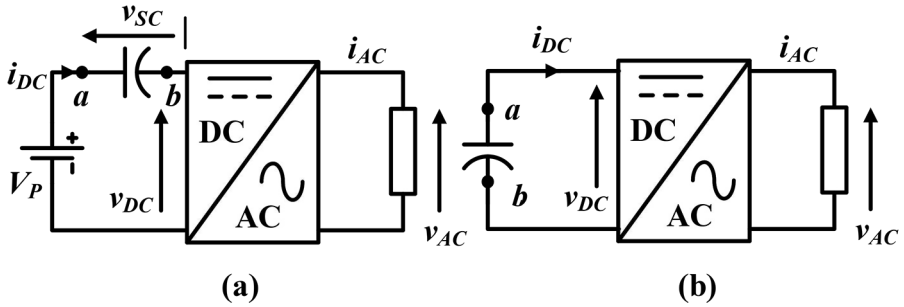


Figure 2.32: SCAWI-PV inverter in (a) SC charging, and (b) discharging phases

In the SCAWI-PV inverter configuration in Figure 2.32(a), an ideal SC is placed in series with the input, which carries a DC voltage of $V_{\mathrm{DC}}^{\mathrm{min}}$ so that the inverter is still operating within its maximum operable DC value ($V_{\mathrm{DC}}^{\mathrm{max}}$). A series-connected SC module will be required here given that the case of single-cell SCs have a low voltage DC voltage rating per cell, in the range of 2.5 to 3.8 V.

With a very large capacitor in series, at the end of the charging phase, V_{DC} will reach a value below its maximum. Then the inverter circuit switches into parallel discharging mode for the

SC, disconnecting the DC input as in Figure 2.32(b). Throughout the charging and discharging cycles of SCAWI PV inverter operation, the commercial inverter is in continuous operation with efficiency:

$$\eta = \frac{V_{\mathrm{AC}} I_{\mathrm{AC}}}{V_{\mathrm{DC}}^{\mathrm{avg}} I_{\mathrm{DC}}^{\mathrm{avg}}} \tag{2.14}$$

showing that the original commercial inverter's efficiency has not been changed due to the modification made by the SC front-end. However, as a result of the SC front-end, the input voltage range of the inverter has been extended to V_{P} (a new value which is twice the nominal DC input).

Figure 2.33 depicts the practical implementation of the concept in Figure 2.32. A model TEP $300-121$ pure sine inverter designed for 12 V nominal input (as in Table 2.5) was used in a SCAWI configuration with an input of 24 V DC and an SC module of 60 F. While achieving a similar efficiency as the 24 V inverter in Table 2.5, a lower-cost 12 V version is used, allowing the price difference to absorb the cost of the SC module. Figure 2.34 shows the measured efficiency at different power outputs, indicating that low-frequency SC front end does not significantly reduce the overall efficiency.

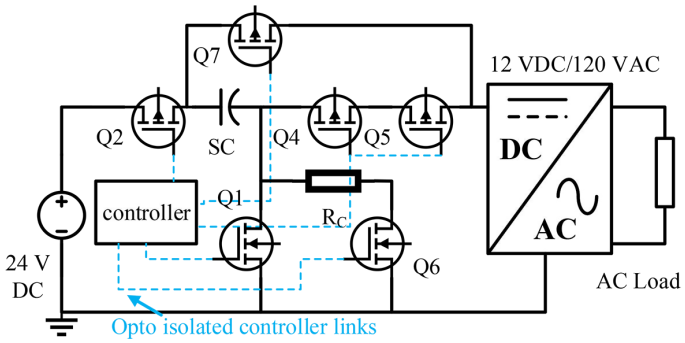


Figure 2.33: SCAWI implementation [1]

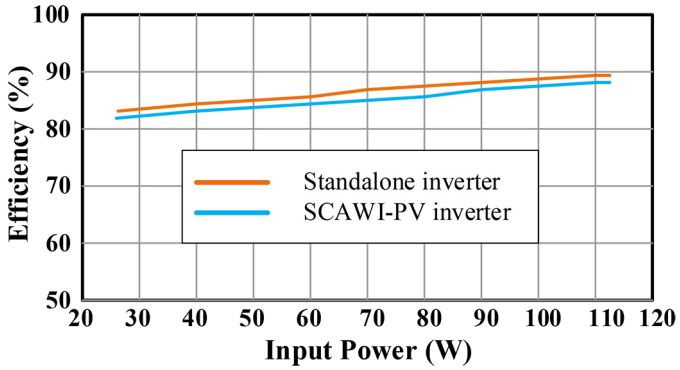


Figure 2.34: Comparison of end-to-end efficiency of the $24-120$ V SCAWI-PV inverter technique and the standalone 12 VDC-120 VAC inverter [1]

Table 2.5: Specifications of commercial PV inverters and SCAWI-PV implementation

Model	Mandaou TEP-300 −121	Mandaou TEP-300 −241	SCAWI 24 VDC-120 VAC
Rated Power	300 W	300 W	300 W
DC input voltage	12 V	24 V	24 V
AC output voltage	120 V	120 V	120 V
No-load current	0.5 A	0.25 A	0.5 A
AC output frequency	50 Hz/60 Hz	50 Hz/60 Hz	50 Hz/60 Hz
AC output waveform	Pure Sine	Pure Sine	Pure Sine
Efficiency	$> 88\%$	$> 86\%$	$> 87\%$
Unit Price (NZD)	150	185	≈ 70

2.7.5 Supercapacitor assisted surge absorber (SCASA)

Supercapacitors can deliver and receive high currents. No harm is done when they are charged with high voltage sources up to their operating voltage. These properties of SCs were used to develop the Supercapacitor-assisted surge absorber (SCASA), another non-traditional application of SCs. This is a patented and commercialised supercapacitor-assisted technique which significantly reduces the component count and the cost of typical surge absorbers. In the capacitor charging circuit, the power dissipated in the loop resistor decreases as the capacitor accumulates energy and reaches a higher voltage since the current across the resistor is lower. A 100 μF capacitor can accumulate 0.5 J energy when it is charged up to 100 V.

Given the above argument about the very high energy storage capability of supercapacitors, when placed in a resistive charging loop, they create a large time constant circuit. If we apply a momentous high DC voltage to the circuit, (such as in lightning-induced voltage on power lines) as in Figure 2.35(b), the capacitor will reach only very small DC value, while most energy in the step DC input will be dissipated in the resistive path of the loop. This simple concept is innovatively extended into the SCASA technique. Figure 2.35 shows the cases of electrolytic capacitor and supercapacitors, indicating why the SCASA technique is feasible, despite the low DC voltage rating of supercapacitors.

The basic SCASA technique is shown in Figure 2.35(c), where typical nonlinear devices (NLDs) such as a metal oxide varistors (MOV) or a bidirectional break-over diodes (BBDs) are combined with a magnetic component and an SC-based sub-circuit. The NLD is placed between the load-side end of a primary coil of a transformer and the return wire, as in Figure 2.35(c). When a surge occurs at the AC input, and the instantaneous voltage due to the surge exceeds the firing voltage of the NLD, a high instantaneous current flows through the primary coil, developing a voltage across the primary turns. This, develops an induced voltage across the secondary coil, and by winding the secondary coil in the opposite direction, the secondary induced voltage can be generated to oppose the surge voltage. The result is the creation of a voltage across the critical load to be protected, which can be less than the instantaneous surge voltage [42].

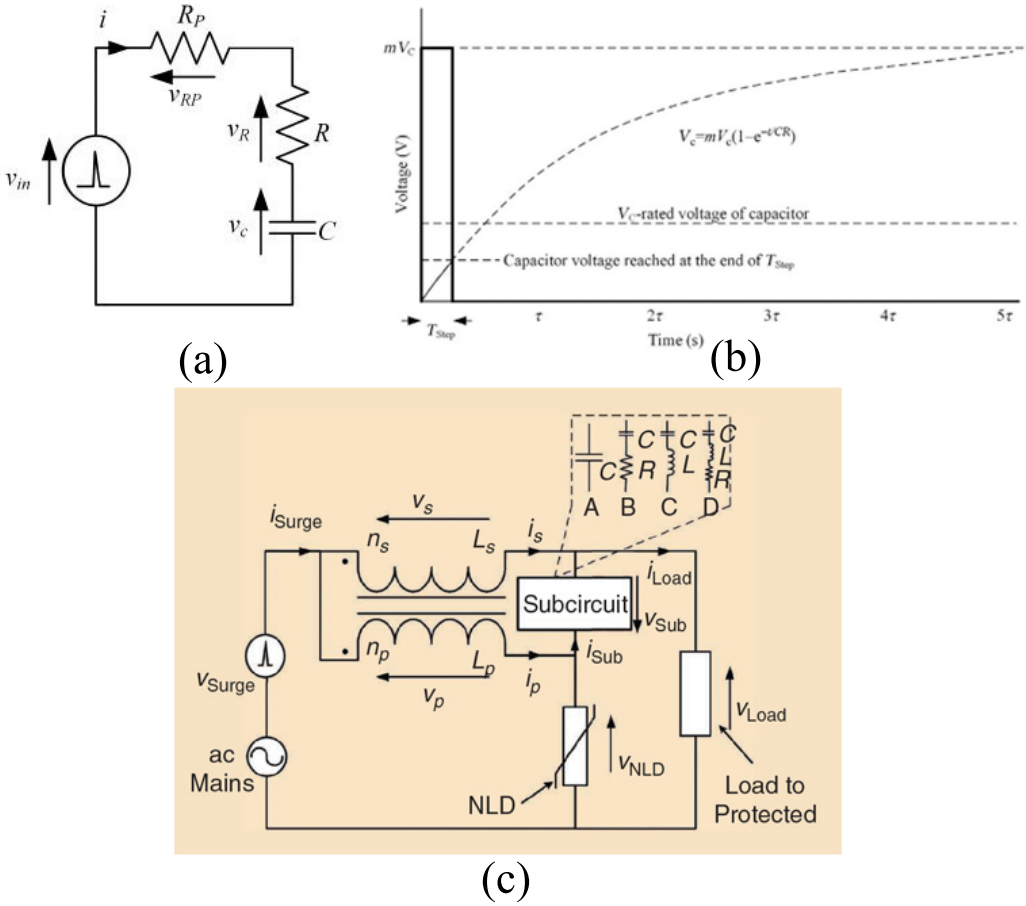


Figure 2.35: Applying short duration pulse on supercapacitor: (a) equivalent *RC* circuit; (b) voltage rise in the capacitor: (c) SCASA concept

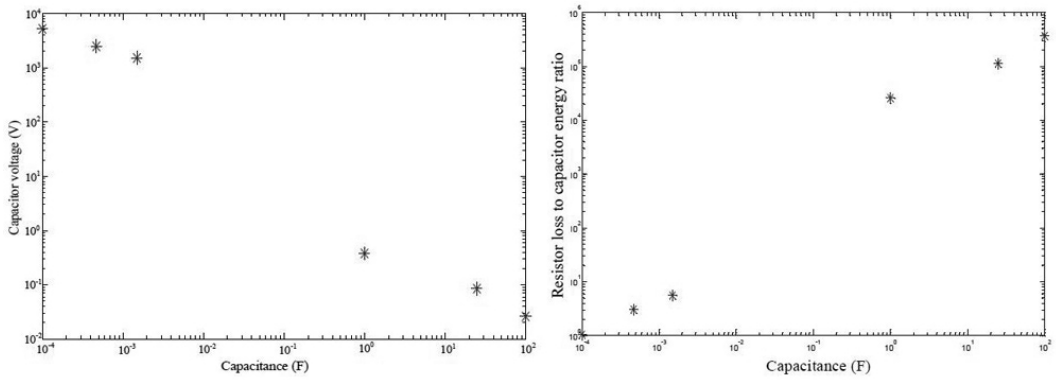


Figure 2.36: Applying short duration pulse on supercapacitor: (a) voltage accumilated for different capacitors for a 6 kV, 50 μs pulse; (b) comparison of energy lost and stored for electrolytic capacitors and SCs subjected to a 6 kV, 50 μs pulse [39]

2.7.6 Supercapacitor assisted temperature modification apparatus (SCATMA)

Given the very low ESR of supercapacitors, they are able to discharge very high current, compared to any rechargeable battery types. This property was used to develop a solution to hot-water delay in domestic water faucets, due to long water pipe lines within a building supplying hot water from a central source. SC-Assisted temperature-modification apparatus (SCATMA) is an "instant" water heating technique based on pre-stored SC energy to overcome the delayed

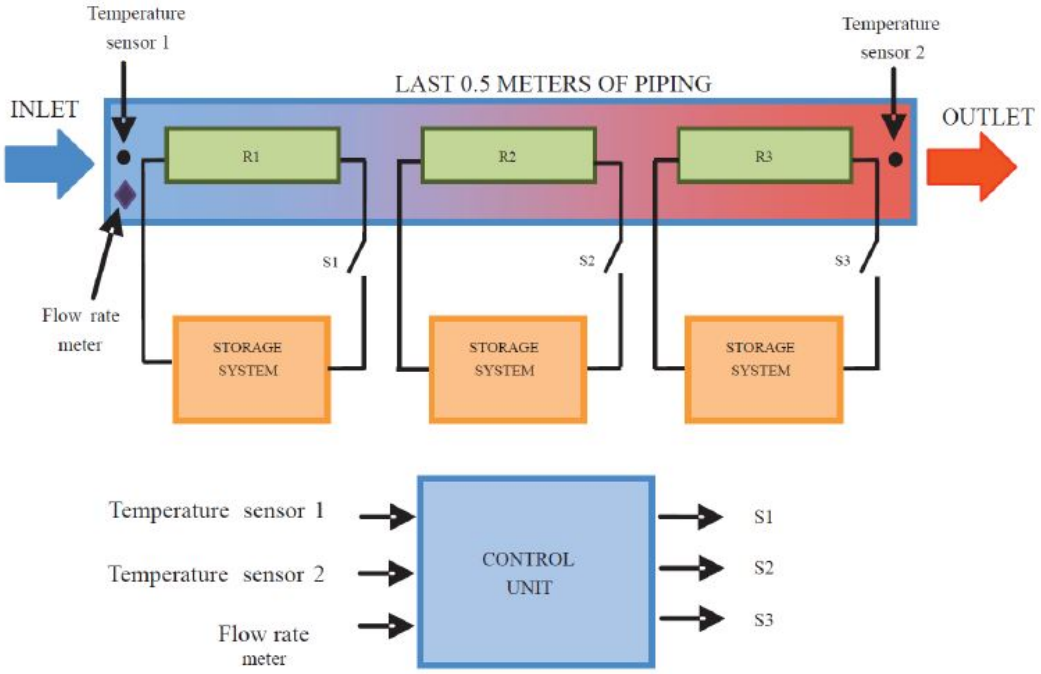


Figure 2.37: SCATMA Bolock Diagram [39]

delivery of hot water in domestic water taps [61]. This technique uses a pre-charged low-voltage SC bank with short-term current delivery capability in the range of 600–2400 A. The system uses SC cells in the range of 1200–5000 F with a storage capability of 0.6–3 Wh [61].

As a part of SCATMA a new fast supercapacitor charging technique, Energy-Limited Transient-Mode Fast Supercapacitor Charger Topology [61, 62] was developed. This topology will be detailed in Chapter 5.

2.7.7 Supercapacitor assisted LED lighting (SCALED)

The SCALED [63] converter inserts an LED lamp as the useful load in a simple *RC* charging loop. LED lamps are the newest and fastest developing energy-efficient lighting technologies. Typically, LED lamps can be considered as constant power loads with brightness proportional to the power and efficacy of the LED elements. LED lamps contain a driver circuit which converts AC to DC as required by the LED bank controller. The brightness of LED lamps remains constant for a wide range of DC voltages around the nominal value of 12 V and they work equally well with negative voltages. Test results are available in [64].

These features were used in the design and development of the SCALED converter. Figure 2.38 shows the basic topology of SCALED where an SC bank and a 12 V LED lamp, or bank of lamps, is used with several low-speed switches. This converter incorporates three modes of operation as depicted in Table 2.6.

The SCALED converter SC bank will series-charge directly from the solar panel powering the 12 V LED lamp. At the start-up phase of the converter, SC banks SC1 and SC2 will charge to 20 V and 9 V by connecting the SC banks directly to the PV module without the two LED lamp banks. Once SC banks 1 and 2 are charged to the required voltage levels, the SCALED converter commences normal operation, in which one SC bank charge to 20 V through one of

the LED lamps while the other SC bank discharges to the remaining LED lamps. When the SC bank reaches the maximum allowable operating voltage of an LED lamp (20 V), it will switch to discharging phase, whereupon it discharges to the minimum operating voltage for an LEDs lamp load (9 V), and the cycle repeats. The SC banks can provide power to the LED lamp loads during low irradiance levels to provide short-term (in the order of minutes) DC-UPS capability. Switches S2 and S4 maintain charge balance of the respective SC banks by alternately switching S1 and S3 as a pair. A controller is required to preserve the switching sequence according to the truth table in Table 2.6.

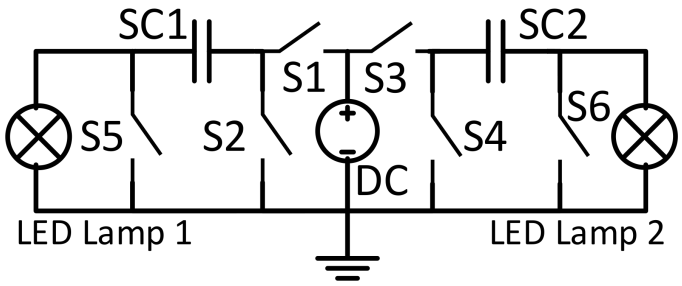


Figure 2.38: SCALED topology [1]

Table 2.6: Switching arrangement for SCALED

Mode	S1	S2	S3	S4	S5	S6
Initial charging	on	off	on	off	on	on
SC2 charging, SC1 discharging	off	on	on	off	off	off
SC2 discharging, SC1 charging	on	off	off	on	off	off

The supercapacitor charging efficiency of the SCALED converter prototype is shown in Figure 2.39. The converter has achieved the target ETEE better than 85%. Theoretically the converter is able to achieve higher ETEE levels in the range of 88.9% to 94% [64]. It is important to highlight here that the above range of efficiencies was achieved without using any MPPT-type DC-DC converter, since the impedance matching required in MPPT is not applicable in this case.

Higher ETEE, low frequency operation eliminating RFI/EMI issues and batteryless short term DC-UPS capability for dealing with irradiance fluctuations are the main features and advantages of this novel converter. More details of this technique are available in [64].

2.7.8 SC-assisted high-density inverter (SCAHDI)

A resistive inverter can be introduced to the capacitor charging loop as a useful resistance, and the SC-assisted high-density inverter (SCAHDI) operates on this principle. The overall inverter is partitioned into smaller inverters. Half of the nominal voltage is supplied by DC sources such as solar panels and the second half is fed by an input DC source in series with the discharged SC banks. Total output is determined by the sum of the series-connected small inverter voltages [39]. A basic block diagram of this technique is shown in Figure 2.40.
The fundamental concepts of this new approach can be summarised as:

- dividing the overall inverter requirement into fractional inverters in terms of output power

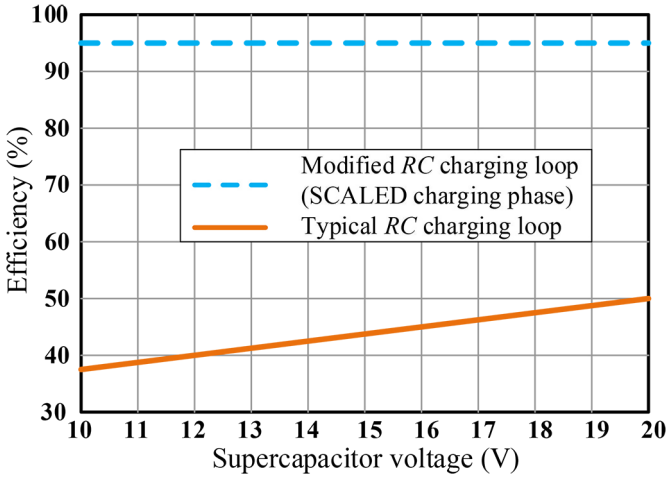


Figure 2.39: Comparison of charging efficiency between direct SC bank replacing battery pack and SCALED converter [64]

- feeding each fractional inverter from half the nominal voltage of the DC source (such as the solar supply)
- using precharged SC banks to power half of the inverters
- feeding the second half of the fractional inverters by an input DC source in series with the discharged SC banks
- ensuring the output voltage of the overall system is based on series-connected outputs of the fractional inverters

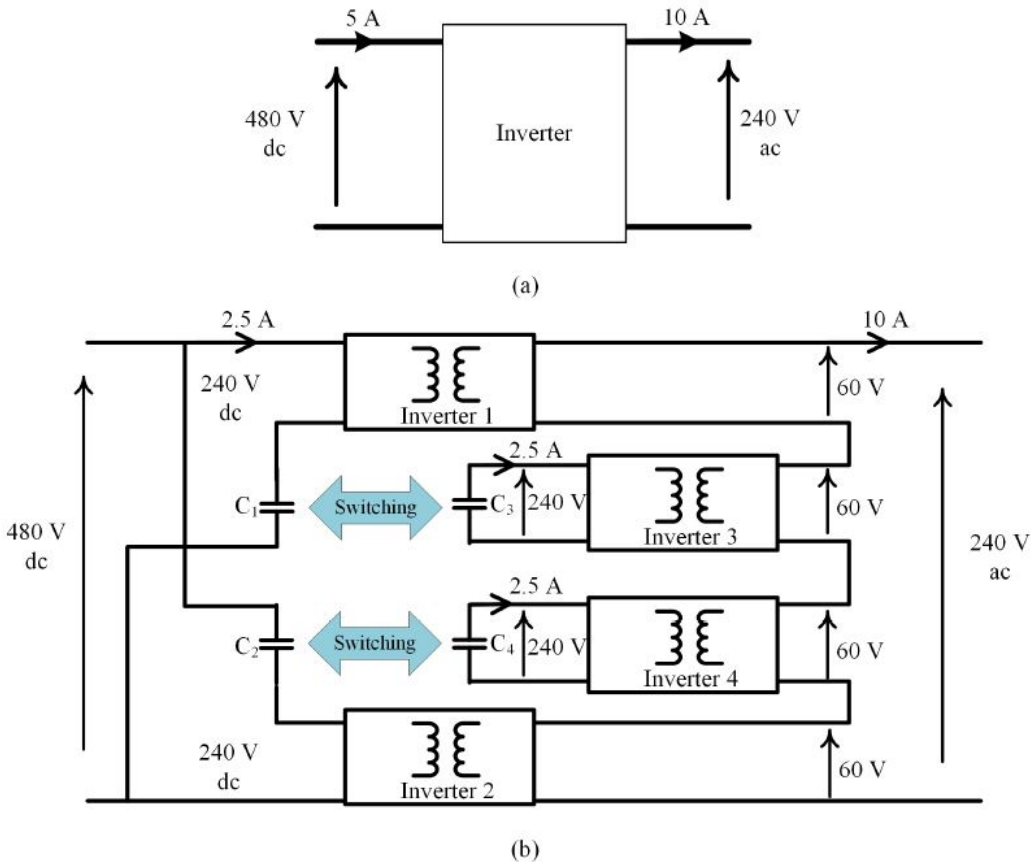


Figure 2.40: The simplified concept of the SCAHDI technique [39]

2.8 Future extensions of SCA techniques

Given the rapid developments of commercial supercapacitor devices, new electrochemistry research and analytical techniques, and modelling of supercapacitors, we expect rapid growth in SC applications [65–67]. This is mostly encouraged by the automotive industry adopting supercapacitors in traditional cars, EVs and sports cars. One good example is the Lamborghini Sian [68], where a supercapacitor module (SCM) is used for rapid acceleration. In traditional cars, the start-stop (eco-drive) systems are today using small supercapacitor module with 15 V DC ratings [69].

SCA techniques can be extended into many more novel techniques. A few examples of early research and ongoing developments in New Zealand are:

- SCA-white goods (SCAWG): an SCM is used with renewable sources of energy to power DC-operable or inverter-driven systems such as refrigerators, washing machines, and heat pumps
- SCA-DC circuit breakers (SCADCB): the high charge-discharge capability of low-cost small supercapacitors can be used in DC circuit breakers
- SCA- brake energy recovery (SCABER): Developing SC-based brake energy recovery using their high charging current capability and rapid energy release

The above is the tip of the iceberg of SC-based power electronic techniques in general. A creative researcher/circuit designer can use the fundamental advantages and properties of the new SCMs for many novel applications.

2.9 Chapter summary

Recent developments in commercial supercapacitors can be summarized as achieving single-cell devices from 1 to over 70 000 F within the same standard canister sizes used for electrolytic and film capacitors. These new devices have allowed the development of a disruptive new application base, branded as supercapacitor assisted (SCA) techniques, based on loss circumventing principle in *RC* loop. Almost all of these SCA techniques use mature power electronic circuits, with added supercapacitor front ends designed to toggle at very low frequencies. The loss circumventing principle in simple *RC* circuits and certain limitation of supercapacitors are discussed in next chapter.

Chapter 3

Loss Circumventing Principle in RC Charging Loop

3.1 Introduction

Until recently, capacitors in electrical circuits were in the range of few pico-farads to about 0.1 mF, leading to RC circuits with time constants of less than 100 ms. Supercapacitors come in similar canister sizes to electrolytic or film capacitors but provide capacitance values $10^5 - 10^7$ times larger generating new circuit design possibilities. In this chapter, we study the supercapacitor-based circuits with one to a few order larger time constants, developing the theoretical basis for a very different and unique set of new power electronics circuit topologies, known as supercapacitor assisted (SCA) techniques. The chapter provides an overview of the loss circumventing principle based on two basic extended design approaches using long time-constant RC circuits: (i) using a useful resistive load as the resistive component; and (ii) slowing down the charging operation significantly by replacing the capacitor with a supercapacitor. The author contributed a chapter to the new edition of Energy Storage Devices for Electronic Systems: Rechargeable Batteries and Supercapacitors (Kularatna, [42]). This chapter is an extract from the book chapter "Loss Circumventing Principle in RC Charging Loop".

3.2 Capacitor charging and discharging

The primary capacitor charging and discharging process can be formulated as below. The special case of starting with a fully discharged capacitor is considered here.

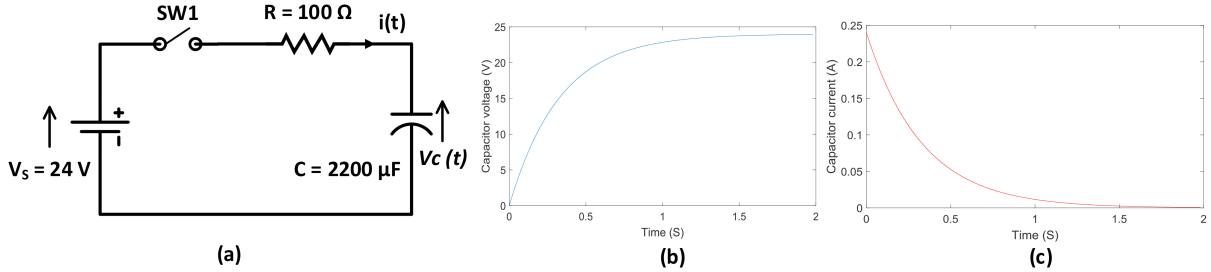


Figure 3.1: RC charging loop: (a) circuit; (b) voltage curve; (c) current curve

Voltage and current versus time curve for the capacitor charging circuit are shown in Figure 3.1. The voltage across the capacitor cannot change instantly; it starts at zero and gradually

reaches the supply voltage. When we turn the switch on, initially, the capacitor acts as a short-circuit, and the current reaches its maximum value. This behaviour is described by Equation (3.1) and (3.2). The capacitor voltage $v(t)$ at time t is given by:

$$v(t) = V_{\mathrm{S}} \left(1 - e^{-t/RC}\right) \tag{3.1}$$

The current through the circuit at time t is given by:

$$i(t) = \frac{V_{\mathrm{S}}}{R} \left(e^{-t/RC}\right) \tag{3.2}$$

where R is the total loop resistance, the capacitance of the capacitor is given by C, and V_{S} represents the supply voltage. Based on the circuit time constant given by $\tau = RC$ the capacitor takes approximately five time constants (5τ) to reach its final voltage. Table 3.1 compares the time constant for several different capacitors with and without a 10 Ω load resistance. A general capacitor discharging circuit with and without load resistance is shown in Figure 3.2. Ideal short circuit is placed across its terminals in Figure 3.2(a) and an external resistor of 10 Ω is connected in Figure 3.2(b). The effect of the time constant τ on the capacitor charging curve is shown in Figure 3.3.

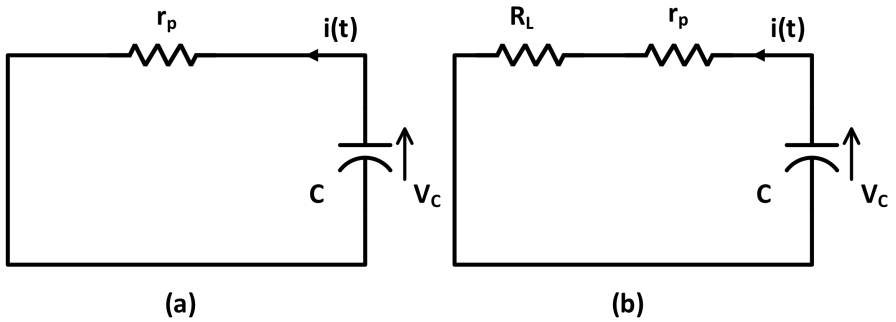


Figure 3.2: Discharging a capacitor: (a) into its own ESR (short-circuited); (b) into 10 Ω load resistance

Table 3.1: Approximate time constant τ for different capacitor resistor combinations

Capacitor	ESR Ω	τ with ESR	Approximate τ with external $R = 10$ Ω
1 μF 50 V	4.5	4.5 μS	14.5 μS
10 μF 50 V	1.6	16 μS	116 μS
100 μF 50 V	0.1	10 μS	1 mS
AVX 1 F	0.24	240 mS	10 S
AVX 10 F	0.025	250 mS	100 S
AVX 120 F	0.008	960 mS	1200 S

Now consider the capacitor discharge circuit as shown in Figure 3.4. If the initial voltage of the capacitor is considered as V_{I} then the voltage at time t, $V(t)$ is given by:

$$v(t) = V_{\mathrm{I}} \left(e^{-t/RC}\right) \tag{3.3}$$

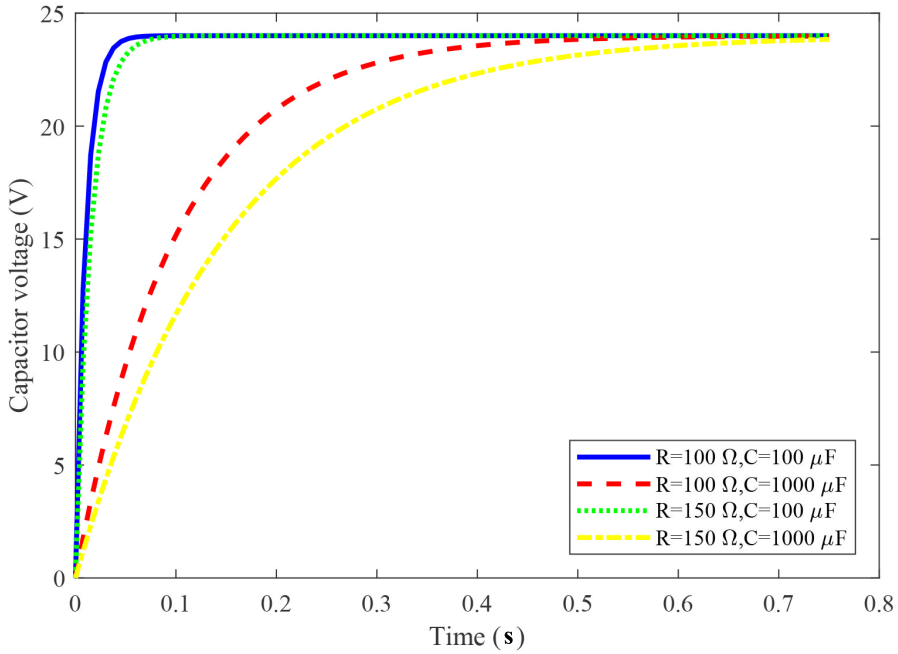


Figure 3.3: Effect of τ on charging curve of a capacitor

The current flow in the circuit $i(t)$ at time t is given by:

$$i(t) = -\frac{V_{\mathrm{I}}}{R}\left(e^{-t/RC}\right) \tag{3.4}$$

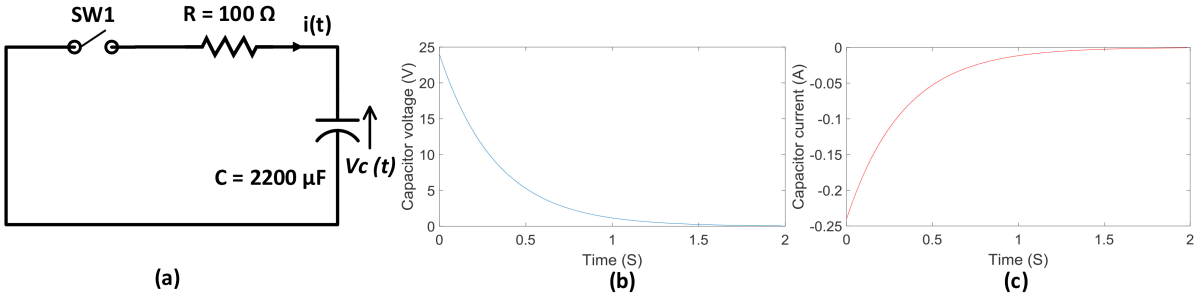


Figure 3.4: *RC* discharging: (a) circuit; (b) voltage curve; (c) current curve

When a capacitor is charged from an initial value of V_1 to a final value of V_2 the energy accumulated by the capacitor during the period is given by:

$$E = \frac{1}{2}C\left(V_2^2 - V_1^2\right) \tag{3.5}$$

3.3 Generalized case of the RC circuit; impact of initial charge and DC source voltage

This section discusses the charging and discharging efficiency of a precharged capacitor. When a capacitor is precharged, charging efficiency can be higher since the voltage drop across the loop resistance is lower. The effect of two different power supplies on the charging curve is depicted

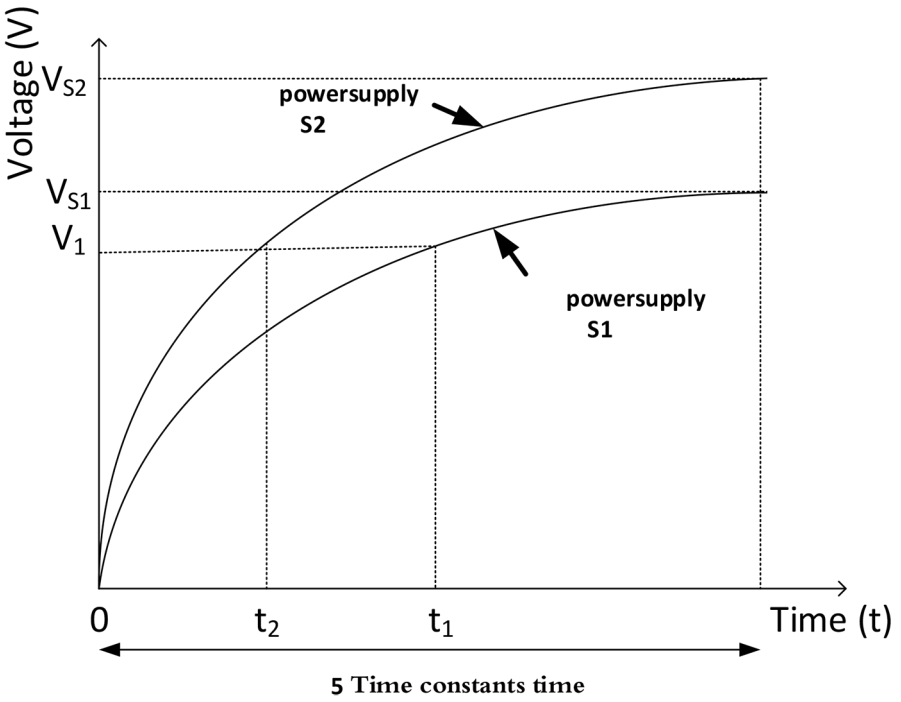


Figure 3.5: Charging a capacitor under different power supplies S1 and S2

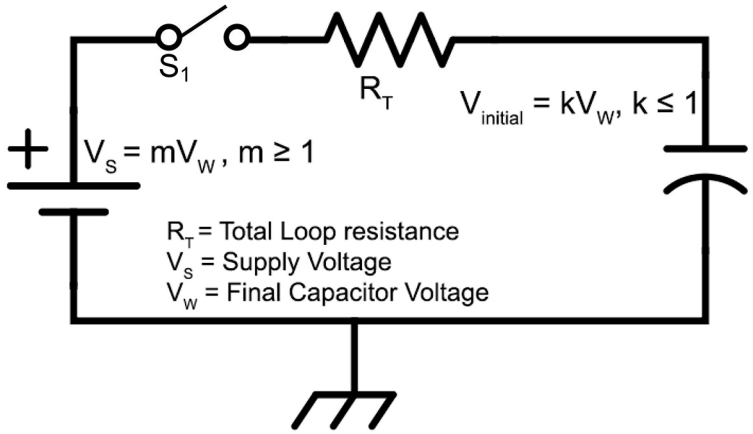
in Figure 3.5. Here $t_2 < t_1$, which means a capacitor reaches a given voltage (V_1) earlier under a higher voltage power supply. In a practical situation, no capacitor should be charged beyond its rated DC voltage. In general for the safety of the component, we charge a capacitor to a lower value than its maximum DC voltage rating. (We later indicate this design maximum as the working voltage of the capacitor). Given this case, V_1 should be within the DC rating of the capacitor. This case is of particular relevance to supercapacitor-based RC circuit since the circuit time constant is significantly increased, allowing the use of a low-speed switch to stop capacitor overcharging.

However, when we charge the capacitor with a higher voltage, charging efficiency is reduced due to the higher voltage drop across the loop resistance. In order to analyse this general case, specifically applicable to a loop with a supercapacitor, we consider the case of a source voltage of m times the rated DC voltage of the supercapacitor V_{W} ($m \geq 1$), where the capacitor is pre-charged to a voltage of k times V_W.

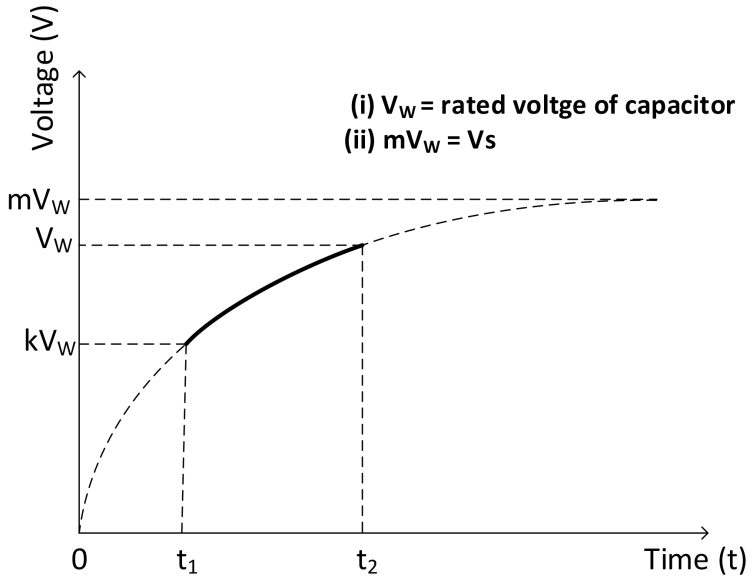
When a fully-discharged capacitor bank charges from 0 to V_{W} from a DC supply of mV_{W}, the capacitor voltage at time t is:

$$v(t) = mV_{\mathrm{W}}\left(1 - e^{-t/RC}\right) \tag{3.6}$$

Following the curve in Figure 3.6(b), let t_1 and t_2 be the times required for $v(t)$ to reach kV_{W} ($0 < k \leq 1$) and V_{W} respectively. We analyse how capacitor charging responds when the power supply voltage (V_S) is higher than the rated voltage (V_{W}) of the capacitor which carries a precharge voltage kV_{W}. We aim to determine how the efficiency of the charging process varies as a function of k (the initial voltage fraction) and m (the power supply over-voltage factor). In



(a)



(b)

Figure 3.6: Charging capacitor with a initial voltage: (a) circuit; (b) voltage curve

a practical circuit with a large time constant due to a supercapacitor, a switch should be used to open the loop when the capacitor reaches its rated DC value to avoid overcharging.
Rearranging Equation (3.6), charging an empty capacitor from a supply of voltage mV_{W} ($m \geq 1$), the times taken to reach target voltages kV_{W} and V_{W} are given respectively by the expressions:

$$e^{-t_1/RC} = \frac{m-k}{m} \text{ and } e^{-t_2/RC} = \frac{m-1}{m} \tag{3.7}$$

The instantaneous voltage across resistor at time t is given by

$$\begin{aligned} mV_{\mathrm{W}} - V_{\mathrm{C}} &= mV_{\mathrm{W}} - mV_{\mathrm{W}}(1 - e^{-t/RC}) \\ &= mV_{\mathrm{W}} e^{-t/RC} \end{aligned}$$

where V_{C} represents instantaneous voltage of the capacitor. The increment in stored energy between time t_1 and t_2 is given by

$$E_{\mathrm{C}}(t_2, t_1) = \frac{1}{2}CV_{\mathrm{W}}^2 - \frac{1}{2}C(kV_{\mathrm{W}})^2 = \frac{1}{2}CV_{\mathrm{W}}^2(1-k^2) \tag{3.8}$$

while the energy loss in the resistor over this time interval is given by the integral

$$E_{\mathrm{R}}(t_2, t_1) = \int_{t_1}^{t_2} i^2 R dt \tag{3.9}$$

with

$$i^2(t)R = (mV_{\mathrm{W}} - v(t))^2/R = \frac{m^2V_{\mathrm{W}}^2}{R}e^{-2t/RC}$$

Integrating (3.9), and substituting end-point expressions (3.7), leads to

$$E_{\mathrm{R}}(t_2, t_1) = \frac{1}{2}CV_{\mathrm{W}}^2(k^2 - 2mk + 2m - 1)$$

giving an energy efficiency ratio of

$$\eta = \frac{E_{\mathrm{C}}}{E_{\mathrm{C}} + E_{\mathrm{R}}} = \frac{1-k^2}{2m(1+k)} = \frac{1+k}{2m} \tag{3.10}$$

In the limit $k \to 0$ (no capacitor precharge) with $m \to 1$ (no power supply overvoltage factor), efficiency $\eta \to \frac{1}{2}$, giving us the textbook standard case of capacitor charging. Equation (3.10) indicates that charging efficiency is higher when the capacitor is not fully discharged.

If our goal is to minimize charging time, then we would set an over-voltage factor $m > 1$, but this implies higher current and *reduced* efficiency since $\eta \sim \frac{1}{m}$ (when k approaches 1). The general case for variable k and m values are depicted in Figure 3.7, showing that optimal efficiency is reached when k and m are close to unity.

3.3.1 Applying the generalized theory in an AC-DC converter

The analysis above can be used to explain the case of an AC-DC converter based on a bridge rectifier and a capacitor, with a load of R_{L} connected as in Figure 3.8(a). Figure 3.8(b) depicts the capacitor charging phase, where $2R_{\mathrm{d}}$ represents the two diodes in the bridge rectifier, in series with the loop parasitic resistances represented by r_p. The smoothing capacitor is represented by C, with its equivalent series resistance (ESR) represented by r_{ESR}.

Given the case of load R_L connected to the circuit, for the Thevenin's equivalent circuit across the capacitor terminals, R_{T} can be derived as:

$$R_{\mathrm{T}} = ((2R_{\mathrm{d}} + r_{\mathrm{P}})//R_{\mathrm{L}}) + r_{\mathrm{ESR}}$$

where // represents parallel resistance. However, since in many practical rectifier circuits $(2R_{\mathrm{d}} + r_{\mathrm{p}}) \ll R_{\mathrm{L}}$, the Thevenin equivalent resistance can be reduced to:

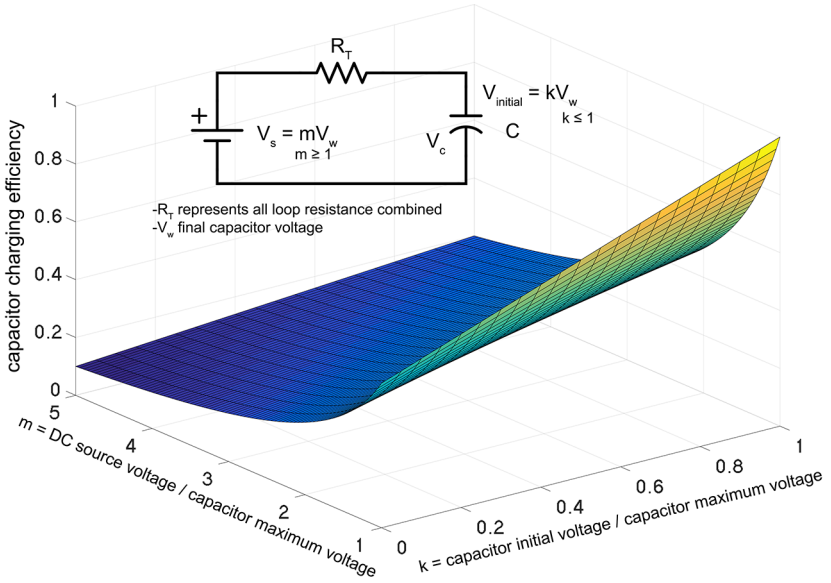


Figure 3.7: Graphical representation of the circuit behaviour in terms of efficiency versus m and k

$$R_{\text{total}} = (2R_{\text{d}} + r_{\text{P}}) + r_{\text{ESR}}$$

This outcome is shown in Figure and 3.9.

If the DC source voltage is less than the rated value of the smoothing capacitor (in the case of $m = 1$), the capacitor voltage will fluctuate from V_{P} to kV_{P} as shown in Figure 3.8(e), with the assumption that the diode voltage drop is negligible. Equation (3.10) now reduces to:

$$\eta = \frac{1+k}{2} \tag{3.11}$$

In this case capacitor operate between tiny voltage margin (impact of sine wave is minimal) which is equal to the ripple voltage. For the simplicity of analysis DC behavior is assumed.

This outcome is visualised in Figure 3.10. According to the graph, efficiency improves as k gets closer to the unity. The precharge factor k can be related to ripple voltage $V_{\text{r(p-p)}}$ and input peak voltage V_{P} as below:

$$k = \frac{V_{\text{P}} - V_{\text{r(p-p)}}}{V_{\text{P}}} = 1 - \frac{V_{\text{r(p-p)}}}{V_{\text{P}}} \tag{3.12}$$

If this analysis is applied to a typical rectifier charging circuit with a peak voltage of 12 V (after rectification) and a peak-to-peak ripple of 2 V, 91.65% theoretical efficiency can be achieved.

When a higher current is drawn from the circuit, $V_{\text{r(p-p)}}$ increases, and k deviates from unity. This lowers the efficiency of the overall system. This energy will be dissipated as heat in the series resistance of the capacitor, the on-resistance of the diode and the path resistance of the circuit.

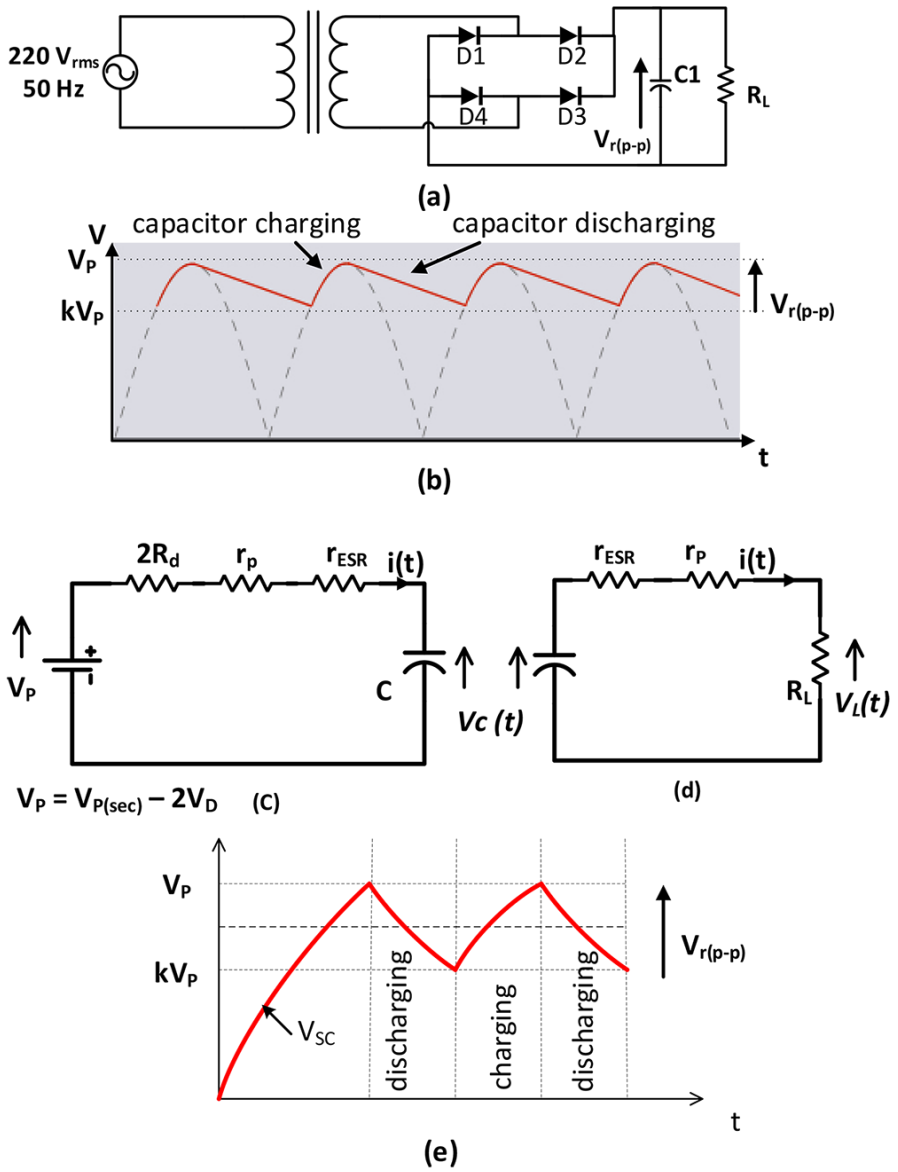


Figure 3.8: Rectifier circuit: (a) basic schematic; (b) ripple waveform; (c) equivalent capacitor charging circuit; (d) equivalent capacitor discharging circuit; (e) capacitor charge-discharge waveform

3.4 Analysis of discharging efficiency

Figure 3.8(d) depicts the equivalent circuit for capacitor discharging to the load. The ESR of the capacitor(R_{ESR}), path resistance (r_P) and the load (r_L) appear in series to the capacitor. The total resistance (R_{T}) of the discharge circuit is given by:

$$R_{\mathrm{T}} = r_{\mathrm{ESR}} + r_{\mathrm{P}} + R_{\mathrm{L}}$$

The initial current at the discharging phase is given by (capacitor is charged up to V_{P}):

$$I_{\mathrm{I}} = \frac{V_{\mathrm{P}}}{R_{\mathrm{T}}}$$

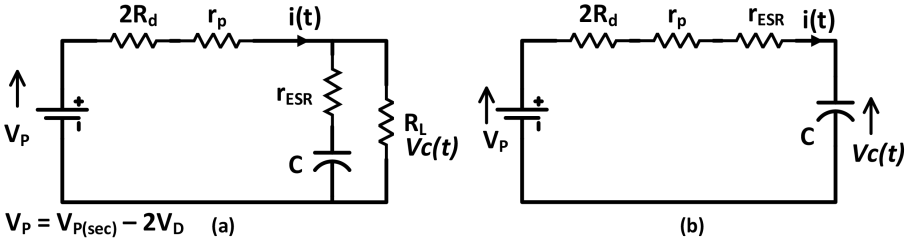


Figure 3.9: Rectifier circuit: (a) capacitor charging circuit; (b) Thevenin equivalent circuit

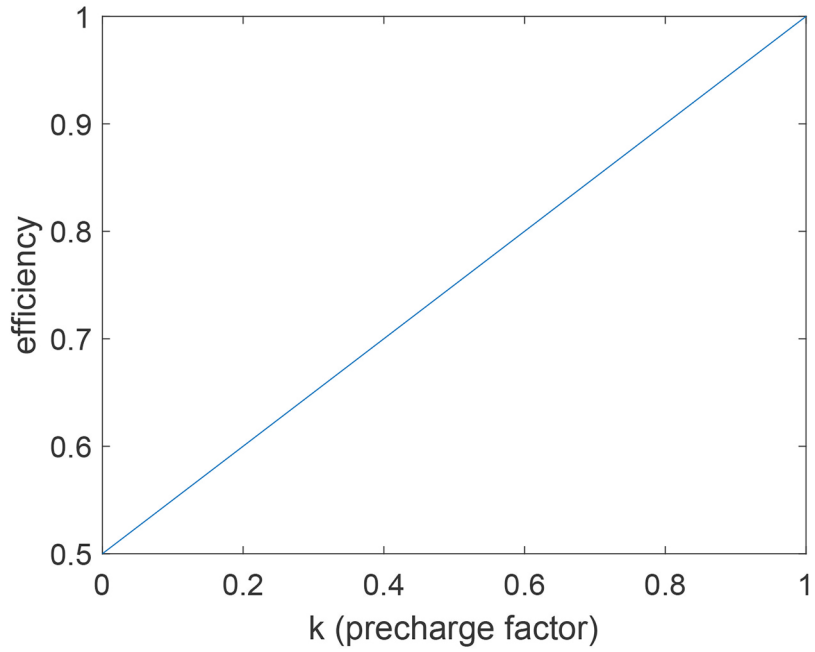


Figure 3.10: Charging efficiency of a smoothing capacitor in a bridge rectifier circuit

Current at time t, $i(t)$ is given by,

$$i(t) = I_{\mathrm{I}} \left(e^{-t/R_{\mathrm{T}}C} \right)$$

However, as this is a series circuit where the same current appears across each component, average current and voltage can be used for the calculations. Here the term $I_{\mathrm{L(avg)}}$ represents average load current and $V_{\mathrm{L(avg)}}$ represents average voltage across the load over the discharging time.

The efficiency η of the discharge circuit can be calculated as:

$$\eta = \frac{E_{\mathrm{R_L}}}{E_{\mathrm{R_L}} + E_{\mathrm{r_{ESR}}} + E_{\mathrm{r_P}}} = \frac{R_{\mathrm{L}}}{R_{\mathrm{L}} + r_{\mathrm{P}} + r_{\mathrm{ESR}}}$$

where $E_{\mathrm{R_L}}$ represents energy consumed by the load, $E_{\mathrm{r_{ESR}}}$ represents energy dissipated in series resistance of the capacitor and $E_{\mathrm{r_P}}$ represents energy dissipated in the path resistance.

Sometimes load is not linear; in this case the average resistance $R_{\mathrm{L(avg)}}$ can be calculated as:

$$R_{\mathrm{L(avg)}} = V_{\mathrm{L(avg)}}/I_{\mathrm{L(avg)}}$$

Generally, the capacitor discharging phase is more efficient than the charging phase. Using capacitors with low ESR and maintaining load resistance at a higher value compared to ESR and the path resistance can enhance the efficiency of the discharge circuit. In other words, at low current, the capacitor discharging process is more efficient.

In the equivalent circuits for capacitor charging and discharging, load resistance has little effect on the charging phase, but it has a higher impact on the discharging phase. For this reason, the time constant of the discharge circuit is larger than that of the charging circuit, and the shape of the ripple waveform can be easily explained.

The efficiency of the *RC* charging loop can be enhanced by introducing a useful resistance, depending on the ratio between the parasitic resistance and the useful resistance. This efficiency enhancement is depicted in Figure 3.11.

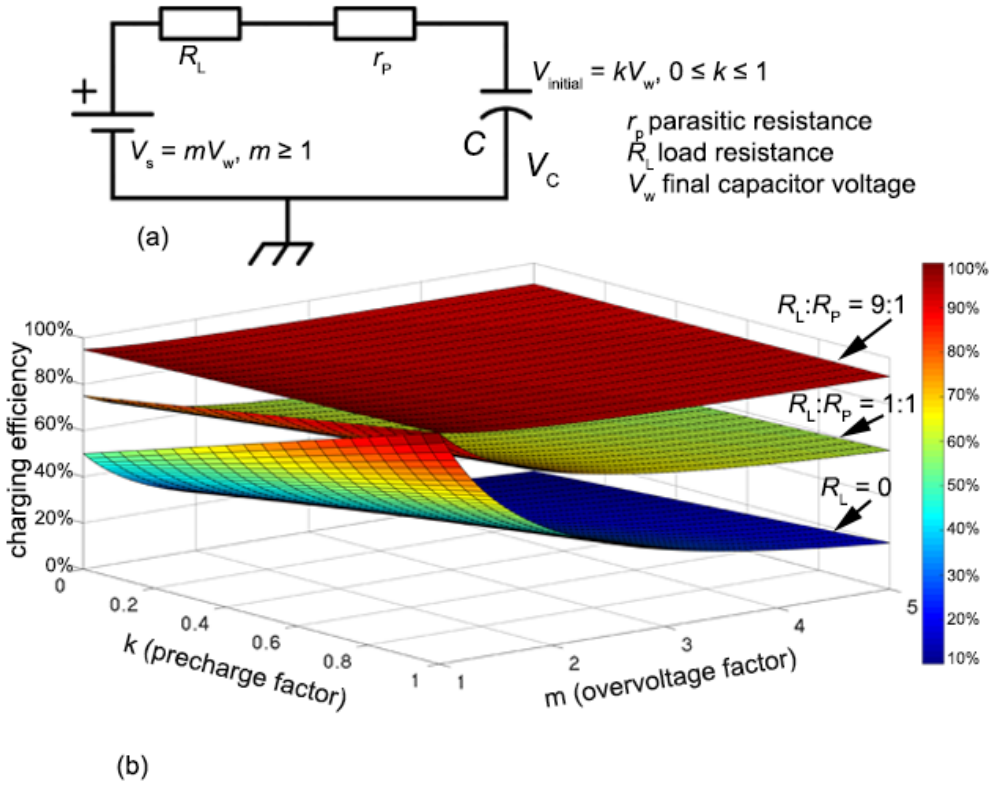


Figure 3.11: Insertion of a useful resistance into the RC charging loop: (a) modified circuit with useful resistance R_{L} inserted; (b) charging efficiency versus m and k

3.5 Supercapacitor as a lossless voltage dropper

When capacitors and inductors are compared, capacitors have a clear volumetric advantage as an energy storage device. To store 100 J of energy, a 50 H inductor is required when it is carrying a 2 A current, as given by $\frac{1}{2}Li^2$, and this is an extremely large inductor. However, a supercapacitor rated at 100 F and 2.7 V with a volume of only 17.1 mL can store 364 J of energy when it is fully charged. Due to the low ESR of supercapacitors, instant high currents can be drawn, which makes SCs less dissipative than batteries. The time constant of commercial SCs can be very large, and current can be considered to be constant over a short time span.

A series-connected SC can be considered as a lossless voltage dropper as shown in [13]. The supercapacitor assisted (SCA) techniques discussed in the earlier chapter, and the new power converter technique, are based on the above properties of SCs.
The voltage range ΔV of a capacitor over a time interval Δt can be estimated as,

$$(I_{\mathrm{C}} = C\frac{dv}{dt}) \implies \Delta V \approx \frac{I_{\mathrm{C}}\Delta t}{C} \tag{3.13}$$

where I_{C} represents the capacitor current. The above simple relationship indicates that when the capacitor becomes larger, the voltage change occurring at the capacitor terminals becomes smaller. In a practical case of a 100 F supercapacitor, which could be of the same physical can size as a 100 uF electrolytic capacitor, the voltage change will be almost one million times smaller for the same charging current.

This provides the practical base to develop the SCALDO technique discussed in the previous chapter, justifying our treatment of an ideal supercapacitor as a lossless voltage dropper.

3.6 Chapter summary

In this chapter, the *RC* charging loop has been analysed with the goal of optimising capacitors' charging efficiency while inserting a useful resistive load in the loop to recover a substantial fraction of the wasted energy. The application of this loss circumvention principle in the *RC* charging circuit has allowed the Power Electronics Research Team at the University of Waikato to develop several non-traditional supercapacitor-based circuit topologies such as SCALDO, SCASA, SCATMA, SCADHI and SCALED. The next chapter details the high current capable SCALDO stage designed for the new power converter.

Chapter 4

High Current SCALDO Stage Design and Implementation

4.1 Introduction

Current SCALDO converters are designed for output voltages less than 12 V, and the maximum current capability is limited to a few amperes. Most of the initial prototypes were implemented with solid-state relays and commercially available LDOs. However, commercially available high current LDOs have a higher input to output voltage margin for regulation, and this factor limits the practical efficiency that a SCALDO converter can achieve at a higher current. Also, solid-state relays are costly for high current configurations. Since the body diode creates a discharge path for LDO, directly replacing solid-state-relays with MOSFETs reduces the efficiency.

This study aimed to develop a high-current (10 A) SCALDO stage suitable for a Google server rack with the efficiency above 90%.

4.2 Requirements of the output stage

The main requirement of the output stage was to develop a high-current SCALDO with a minimum number of switches while maintaining efficiency. As detailed in Chapter 2, SCALDO have two implementations, depending on the input and output voltage, as $V_{\mathrm{P}} > 2V_{\mathrm{min}}^{in}$ and $V_{\mathrm{P}} < 2V_{\mathrm{min}}^{in}$. For the high-current SCALDO implementation developed in this study we considered the operating condition $V_{\mathrm{P}} > 2V_{\mathrm{min}}^{in}$ (V_{P} = SCALDO input voltage, V_{min}^{in}=minimum required voltage for LDO). For this configuration the number of supercapaciors required is [70],

$$n < \frac{V_{\mathrm{p}} - V_{\mathrm{min}}^{\mathrm{in}}}{V_{\mathrm{min}}^{\mathrm{in}}} \tag{4.1}$$

The number of switches to be used is given by $3n + 1$. However, because of the pre-regulator stage, the SCALDO input voltage can be chosen to have one supercapacitor bank, so the SCALDO stage can be implemented with four low frequency switches. To keep this minimum switch count, from inequality (4.1), we can derive the following inequality:

$$1 < \frac{V_{\mathrm{p}} - V_{\mathrm{min}}^{\mathrm{in}}}{V_{\mathrm{min}}^{\mathrm{in}}}$$
$$2V_{\mathrm{min}}^{\mathrm{in}} < V_{\mathrm{p}}$$

For the proof-of-concept prototype, we developed an 80 to 12 V power converter which is the output voltage is one-fourth of the Google 230 V AC-to-48 V power supply. In order to achieve higher efficiency, dropout in the LDO should be minimal, and we aimed developing discrete LDO stage with 0-0.5 input to output voltage margin. For the calculation, we have have assumed that the dropout voltage was 0.5. Then the next important decision was the operating voltage margin of the supercapacitor. According to the analysis detailed in Chapter 3, operating an SC within a narrow voltage margin increases the charging efficiency of the *RC* loop. Considering all these factors, we decided to operate the SC within a 1 V margin. During SCALDO discharge phase, the load is powered by the SC. The minimum voltage of the SC ($V_{\mathrm{SC(min)}} = 12.5$). With a 1 V margin, SC can be charged up to 13.5 V. During the charging phase of the SCALDO, the minimum required voltage of the LDO should be maintained at the LDO input. This means for this configuration the minimum source voltage should be $V_{\mathrm{P}} = 13.5 + 12.5 = 26$
The efficiency of the SCALDO is,

$$\eta = (n+1)\,\frac{V_{\mathrm{reg}}}{V_{\mathrm{p}}}$$

which for a single supercapacitor bank, (i.e., n=1) , reduces to,

$$\eta \quad = \quad = \frac{2V_{\mathrm{reg}}}{V_{\mathrm{p}}} = \frac{2 \times 12}{26} = 92.3\%$$

When the same design parameters are applied to a 48 V output power supply, the voltage of the supercapacitor should be maintained between $48.5 - 49.5$ V, and the minimum source voltage should be $V_{\mathrm{P}} = 49.5 + 48.5 = 98$ V, leading to a correspondingly higher efficiency,

$$\eta \quad = \quad \frac{2 \times 48}{98} = 97.9\%$$

Table 4.1: Design parameters for 12 V SCALDO stage and 48 V SCALDO stages

Parameter	12 V prototype	48 V design
Voltage drop of LDO	0.5 V	0.5 V
Minimum input for LDO	12.5 V	48.5 V
Supercapacitor voltage margin	$12.5 - 13.5$ V	$48.5 - 49.5$ V
Source voltage for SCALDO	26 V	98 V
Theoretical efficiency	92.3%	97.9%

The main specifications of this input stage can be summarised as:

- Design and implement a discrete 12 V LDO stage with a maximum of 0.5 V voltage drop at 10 A load current.
- Design and implement a 12 V SCALDO stage with 26 V input voltage with a theoretical efficiency of 92.3%.
- Set the operating frequency of the converter at fractional hertz by choosing an appropriate supercapacitor bank.

4.3 Justification of an LDO-based output for the Google architecture

All electronic devices are vulnerable to radio frequency interference (RFI) also known as electromagnetic interference (EMI). Most and almost all high frequency switching converters generate significant amounts RFI/EMI [71]. However, LDO being a linear regulator without any switching elements, is free of RFI/EMI issues. In addition, the LDO regulator has high output current slew-rate capability [16]. Embedding the LDO within a SCALDO controller means the SCALDO regulator inherits all of the LDO advantages.

4.4 High current discrete LDO design and implementation

This section discusses the process of designing an LDO with the efficiency above 90%. Different application contexts of LDOs are shown in Figure 4.1. Figure 4.1(a) depicts a traditional AC-DC regulator in which the LDO performs ripple rejection, eliminating AC hum and regulating the output voltage. In Figure 4.1(b), an LDO is used in a battery-powered application to regulate voltage by maintaining a constant voltage as the battery discharges, thereby extending the usable life of the battery. In Figure 4.1(c) an LDO is used as post-regulation stage for switch-mode power supplies. Switching regulators are well known for their efficiency, although there are concerns with electromagnetic interferences. Ripple in the source degrades the performance of analogue circuits. In this context, an LDO provides active filtering and improves the power supply's overall regulation. In Figure 4.1(d) LDOs are used in a multi-rail battery-powered application. This arrangement is useful when different blocks of the application require different voltages [72].

In this thesis, the overall power supply combines a medium frequency switch-mode front end with a SCALDO output stage as depicted in Figure 4.2. The LDO is part of the SCALDO stage, and as discussed in Chapter 3, acts as a useful load in the supercapacitor charging path, minimizing losses. The LDO makes sure that the output sees smooth constant voltage. Due to the very low voltage dropout requirement and unavailability of high-current, high-voltage LDO regulators, a custom-built LDO stage was designed. The next section discusses how we addressed this design challenge.

4.4.1 Basic LDO design

A basic linear regulator is shown in Figure 4.3. A series pass device, error amplifier, voltage reference and a sampling resistor network are the basic components of a linear regulator. The error amplifier compares the output voltage with the reference and adjusts the resistance of the series pass element to maintain the output voltage at a constant value. An LDO is a special linear regulator in which the series pass semiconductor's input-to-output voltage difference is maintained at very low value. This small voltage drop combined within a low-power controller gives a higher efficiency in general. The basic requirements of the specific LDO design in the project can be summarised as:

- precise output voltage

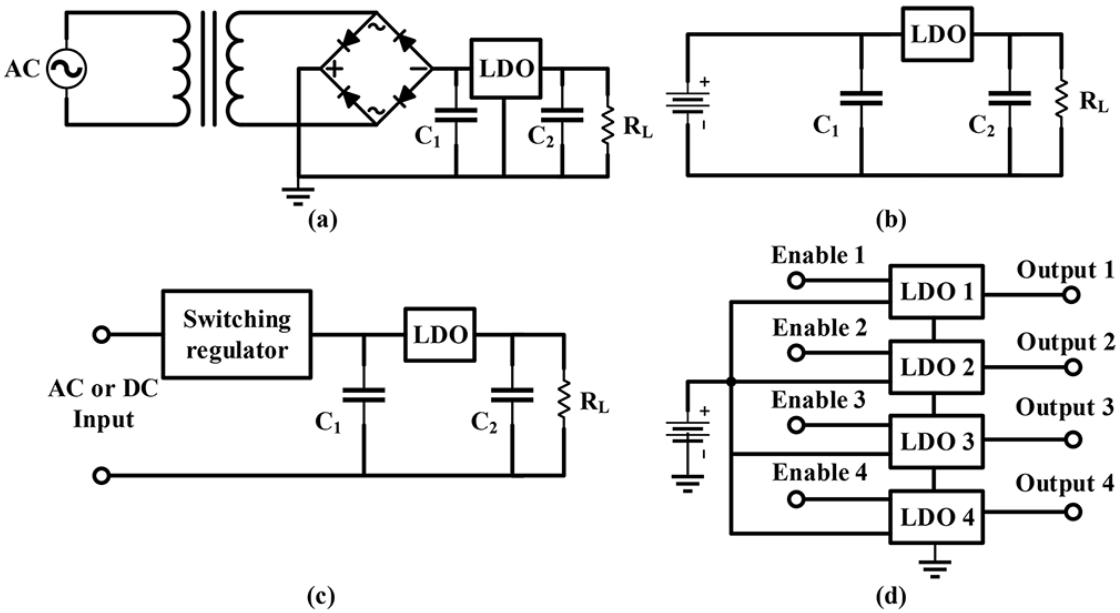


Figure 4.1: Typical applications of LDOs in DC power management systems [72]

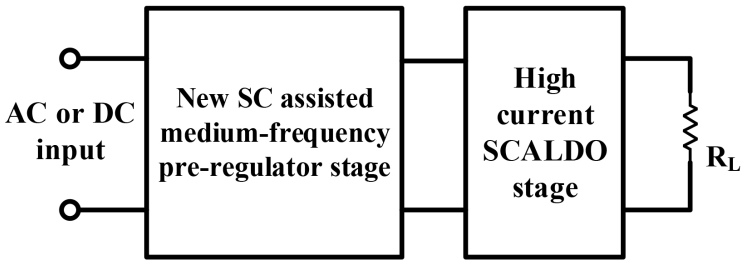


Figure 4.2: Proposed high-current power converter technique

- very low dropout voltage in the range of 0.1 to 0.5
- low power controller circuit

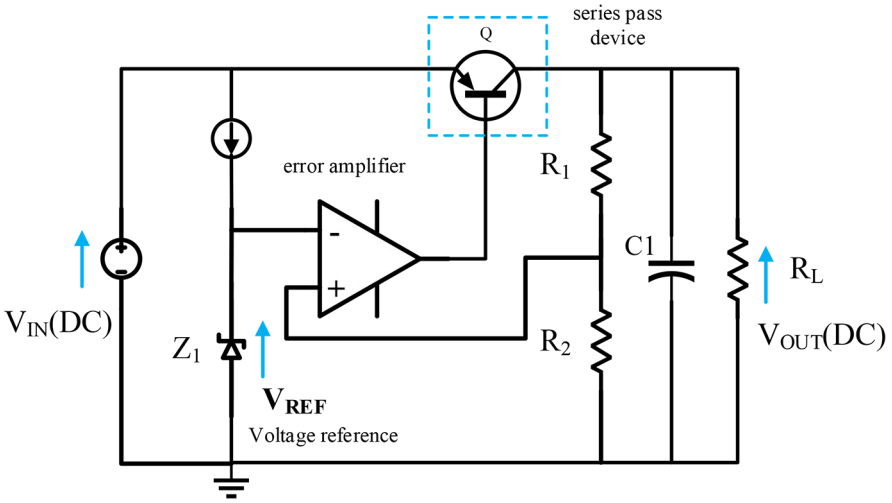


Figure 4.3: Component arrangement of a basic linear regulator [72]

Different LDO designs illustrated in the literature are shown in Figure 4.4 [72]. Figure 4.4(a) shows an NPN-transistor-based linear regulator which requires a minimum $2.5 - 3.0$ V voltage

margin (input to output voltage difference) to operate. In Figure 4.4(b), an NPN-transistor-based linear regulator is shown with a PNP transistor driver. This arrangement can reduce the dropout voltage to $1.2 - 1.5$ V. A PNP-transistor based linear regulator is shown in Figure 4.4(c), and this configuration further reduces the dropout voltage to $0.3 - 0.6$ V. Figure 4.4(d) depicts a linear regulator based on a P-channel MOSFET. Regulators with a very low voltage dropout can be achieved with these MOSFETs. However, MOSFETs are costly compared to BJT devices. The regulator shown in Figure 4.4(e) is an N-channel MOSFET-based design with a separate chip for the controller function. These optimise the die area of the chip and cost for higher current regulators. However, this is a multiple package solution. By considering design flexibility, complexity, pros and cons of each design, we chose a discrete P-MOSFET-based design to achieve our LDO configuration.

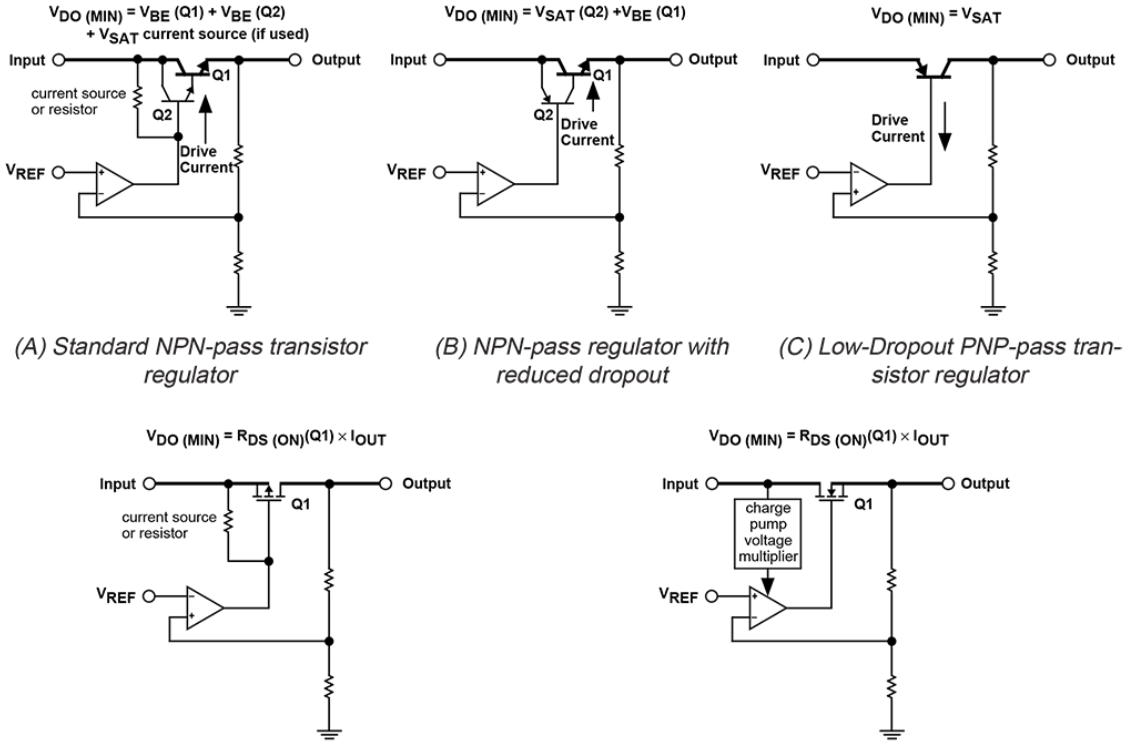


Figure 4.4: Main types of linear regulators: (a) standard NPN-pass transistor regulator; (b) NPN-pass regulator with reduced dropout; (c) low-dropout PNP-pass transistor regulator; (d) P-channel MOSFET-pass transistor regulator; (e) N-channel MOSFET-pass transistor regulator [72]

The initial version of the LDO we designed is shown in Figure 4.5, which is the textbook version of the MOSFET-based regulator described earlier. The possibility of directly applying this schematic was tested by implementing a prototype to regulate at 12 V. We loaded this regulator up to 10 A load current and a cooling fan was used as the MOSFET generated a great deal of heat. In this regulator design, we had to maintain over 1 V voltage difference between the input voltage and the output to achieve stable regulation. An LM741 op-amp was used as the error amplifier and an SUP70101EL-GE3 Vishay P-MOSFET as the series pass device. This MOSFET had 0.01 Ω of resistance at a 10 V gate voltage.

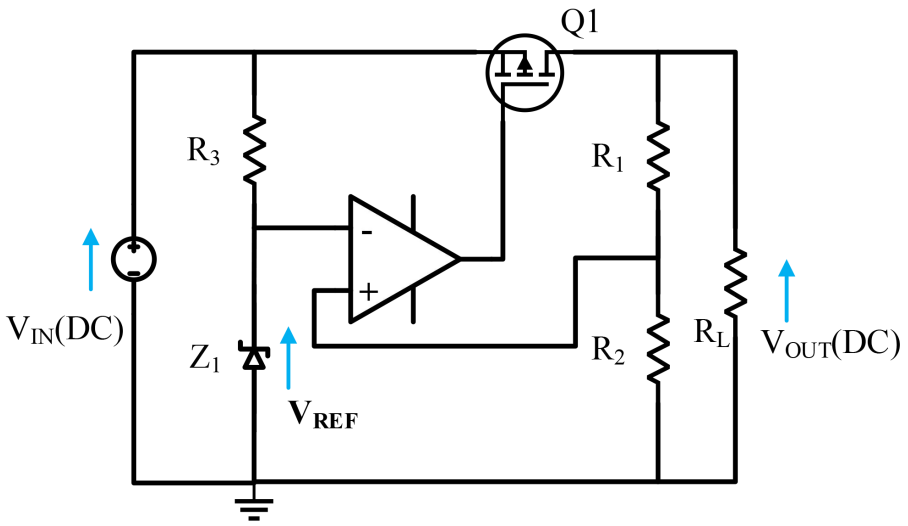


Figure 4.5: Linear regulator with a MOSFET as series pass device

In order to refine our LDO to meet the design objectives, we studied the behaviour of the MOSFET and analysed the linear regulator in detail. A primary requirement is to have a very low drop-out voltage, in the order of 0.1 to 0.5 V. A summary of our analysis is provided in the following section.

4.4.2 Analysis of the LDO

A linear regulator is a constant voltage source, which adjusts its internal resistance (R_{IN}) according to the changes in load resistance (R_{L}) to ensure constant voltage is maintained at the output (Figure 4.6(a)).

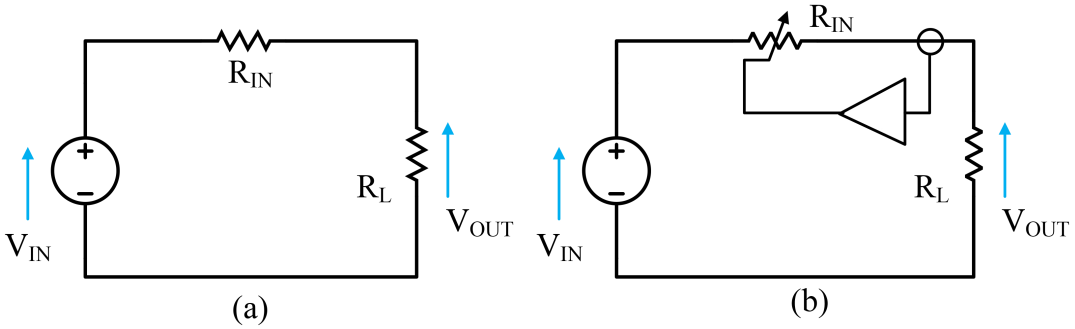


Figure 4.6: Voltage source: (a) with internal resistance R_{IN}; (b) with error correction

The output voltage for Figure 4.6(a),

$$V_{\mathrm{OUT}} = V_{\mathrm{IN}} \times \frac{R_{\mathrm{L}}}{R_{\mathrm{IN}} + R_{\mathrm{L}}} \tag{4.2}$$

Therefore for good regulation, the internal resistance must be significantly smaller than the load resistance ($R_{\mathrm{IN}} \ll R_{\mathrm{L}}$) (otherwise voltage variation through internal resistance can be dominating, specially with the increasing load current).
To minimize error in output voltage, load variation should be monitored and internal resistance should be compensated according to these variations as shown in Figure 4.6(b).

In another words, the ratio between R_{IN} and R_{L} should be kept constant,

$$R_{\mathrm{IN}} = R_{\mathrm{L}} \times k \tag{4.3}$$

In the LDO implementation shown in Figure 4.5, a P-MOSFET is used as the variable resistor with an opamp-based feedback loop controlling the gate voltage of the P-MOSFET. A representative regulation sequence is shown in Figure 4.7. During a sudden drop in load resistance R_{L} (increase in I_{L}), V_{OUT} drops and the voltage drop across the series pass device (V_{DS} of MOSFET) increases. At the same time the feedback voltage drops below the reference voltage, increasing the error signal to compensate the gate voltage and shift to higher gate voltage (V_{GS3}), thereby increasing the load current to maintain V_{OUT} constant. Eventually the, error becomes zero and gate voltage stabilizes in the new value. The output characteristic shown in Figure 4.8 confirms the regulation sequence discussed above. When R_L drops, the P-MOSFET's operating point jumps from P1 to P2 and then $P3$.

For given quiescent point P^*, where output voltage has stabilized (V_{OUT} and V_{DS} are constant):

$$R^*_{\mathrm{IN}} = \frac{V_{\mathrm{DS}}}{I^*_{\mathrm{OUT}}} \tag{4.4}$$

$$R^*_{\mathrm{L}} = \frac{V^*_{\mathrm{OUT}}}{I^*_{\mathrm{OUT}}} \tag{4.5}$$

where R^*_{IN} represents internal resistance, R^*_{L} is load resistance, V^*_{OUT} represents output voltage and I^*_{OUT} represents output current at quiescent point P^*.
From these equations we can derive the linear relationship required for linear MOSFET regulator.

$$I^*_{\mathrm{OUT}} = R^*_{\mathrm{LOAD}} \times \frac{V_{\mathrm{DS}}}{V_{\mathrm{OUT}}} \tag{4.6}$$

For the optimum operating condition where dropout voltage is at its minimum point, P-MOSFET operates at its linear region as shown in Figure 4.9. For this region relationship between input and output voltage is given by [74],

$$V_{\mathrm{IN(min)}} = V_{\mathrm{OUT}} + V_{\mathrm{DROP(min)}} = V_{\mathrm{OUT}} + R_{\mathrm{DS(ON)}} \times I_{\mathrm{OUT}} \tag{4.7}$$

This behaviour is elaborated in Figure 4.10 and 4.11.

For the MOSFET we selected for the implementation (SUP70101EL), behaviour of $R_{\mathrm{DS(ON)}}$ aginst load current and temperature is shown in Figure 4.12(c) and 4.12(d) respectively. It is important to note that $R_{\mathrm{DS(ON)}}$, heavily depend on the junction temperature.

MOSFET output resistance ($R_{\mathrm{DS(ON)}}$) can be reduced by connecting an array of P-MOSFETs in parallel. By considering a P-MOSFET for n identical parallel MOSFETs, the output on resistance becomes $R_{\mathrm{DS(ON)}}/n$ and the total current is $n(V_{\mathrm{IN}} - V_{\mathrm{OUT}})/R_{\mathrm{DS(ON)}}$ at the best operating point (dropout voltage is minimum). In other words, the load current is divided into n MOSFET branches, resulting in low current circulation in individual branches. Since P-MOSFETs

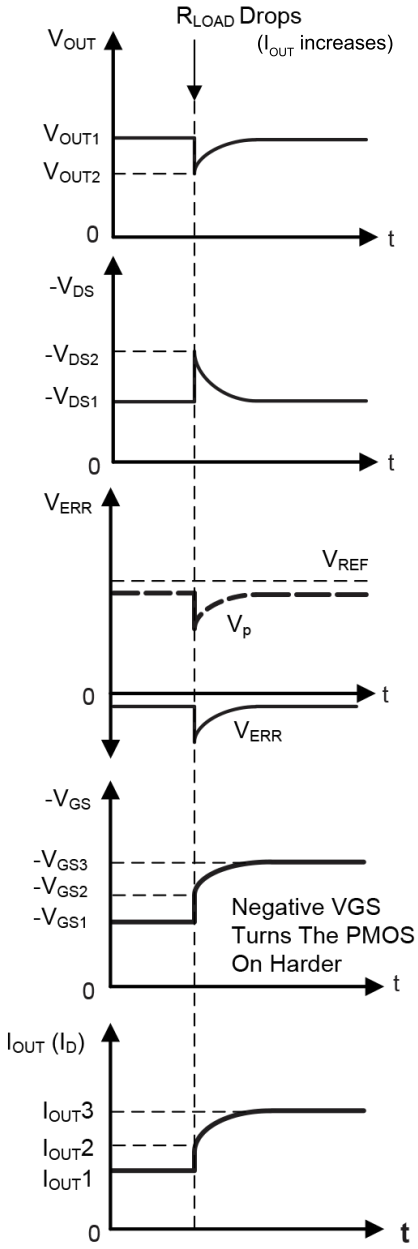


Figure 4.7: Regulation sequence sequence of an LDO with drop in load resistance [73]

generally have a positive temperature coefficient for output resistance and the temperature has a significant impact on the on-resistance, low current circulation helps to maintain the junction temperature at a low value and the on resistance will stay close to the rated datasheet value. Also by referring to the characteristic curve shown in Figure 4.8, at low drain current V_{DS} can be pushed more toward 0, which means low dropout voltage for LDO. Parallel MOSFETs help us to reduce current flown in individual MOSFETs and eventually reduce the dropout voltage.

When the voltage drop is larger than, minimum drop, in order to establish bias points large signal model of MOSFETS can be applied. P-MOSFET. The basic pin layout of the P-MOSFET is shown in Figure 4.13(a) and the large signal model is shown in Figure 4.13(b) [75]. Here V_{SG} $(= -V_{\mathrm{GS}})$ represents source gate voltage, V_{SD} represents source drain voltage, C_{ox} represents capacitance per unit gate area, μ_{p} is mobility of electrons in the channel. k'_{p} combine the effect

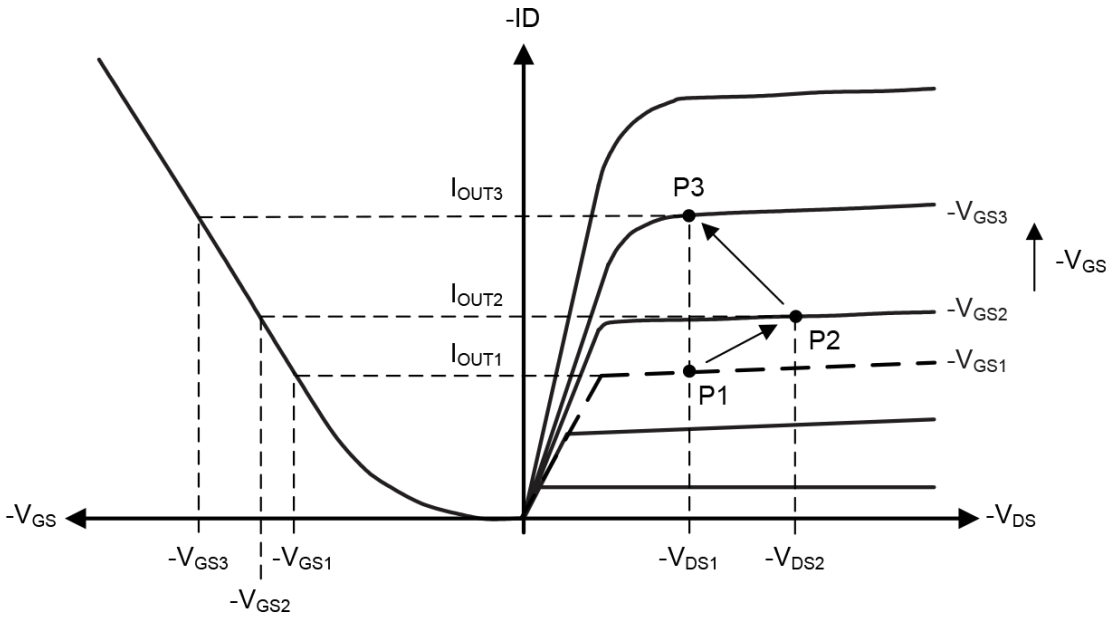


Figure 4.8: P-MOSFET input output characteristic curve [73]

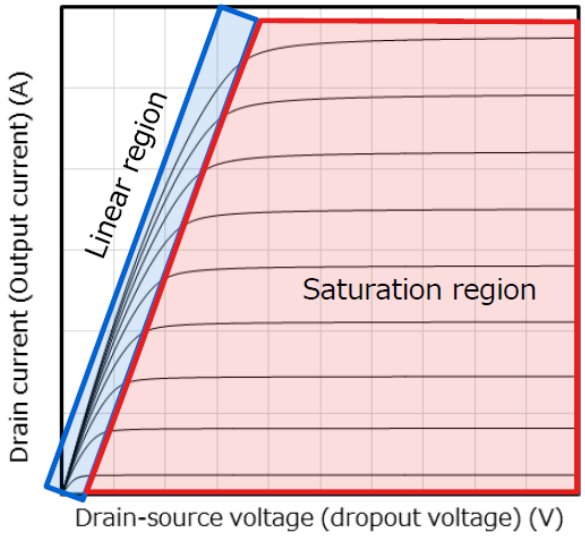


Figure 4.9: Regions of P-MOSFET operation [74]

of C_{ox} and μ_p, is the process transconductance parameter which has dimensions A/V^2. Ratio of the channel width (W) to channel length (L), known as aspect ratio of the MOSFET and drain current is propositional to W/L ratio of a MOSFET [75]. V_t is the gate threshold voltage of the MOSFET. The saturation-region drain current will increase slightly as the drain-to-source voltage increases, this effect is known as channel-length modulation and output resistance r_O is introduced to incorporate this effect to the MOSFET model [75]. r_o is typically in the range of $10 - 1000$ kΩ.

By applying Figure 4.13 equivalent circuit to P-MOSFET based linear regulator, equivalent circuit shown in Figure 4.14 can be derived. Channel-length modulation effect r_o is neglected for simplicity of the analysis.

Considering Figure 4.14 output voltage of LDO is given by,

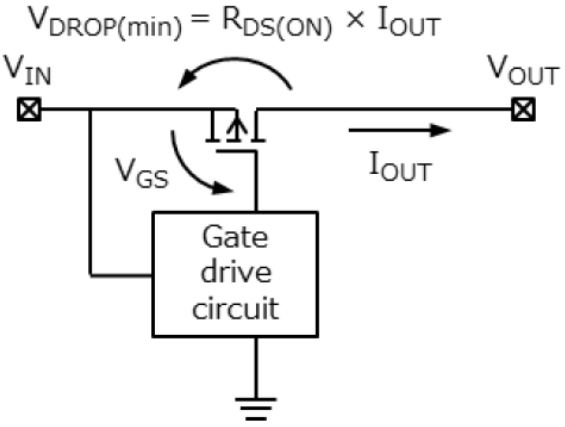


Figure 4.10: Dropout voltage of an LDO with a P-MOSFET pass device [74]

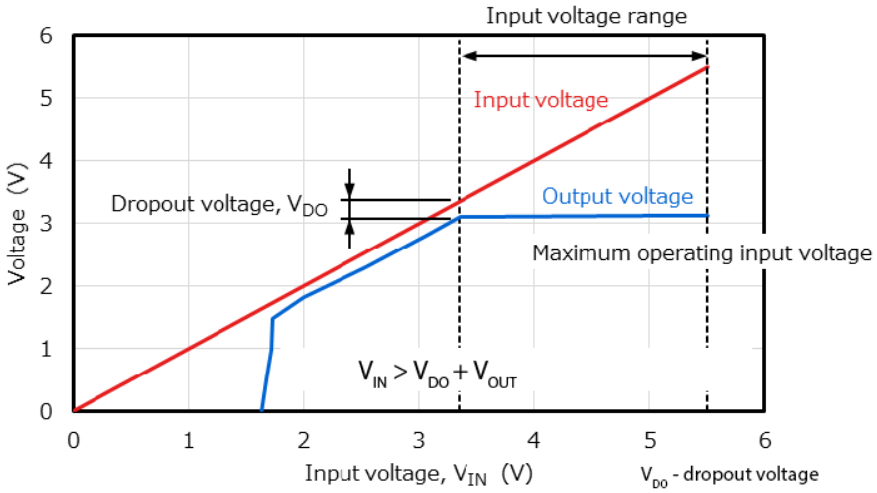


Figure 4.11: Input voltage range and dropout voltage of linear regulators [74]

$$V_{\mathrm{OUT}} = \frac{V_{\mathrm{REF}}}{R_2}(R_1 + R_2) \tag{4.8}$$

Then the MOSFET drain current I_{D} is given by (here we assume current toward opamp non inverting terminal is 0),

$$I_{\mathrm{D}} = \frac{V_{\mathrm{OUT}}}{R_{\mathrm{L}}//(R_1 + R_2)} \tag{4.9}$$

$$= \frac{V_{\mathrm{REF}}(R_1 + R_2)}{R_2\,(R_{\mathrm{L}}//(R_1 + R_2))} \tag{4.10}$$

$$I_{\mathrm{D}} = \frac{V_{\mathrm{REF}}(R_1 + R_2)}{R_2\,(R_{\mathrm{L}}//(R_1 + R_2))} \tag{4.11}$$

However, from the P-MOSFET large signal model, I_{D} in saturation region is given by,

$$I_{\mathrm{D}} = \frac{1}{2}\mu_{\mathrm{P}} C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{SG}} - |V_{\mathrm{t}}|)^2 \tag{4.12}$$

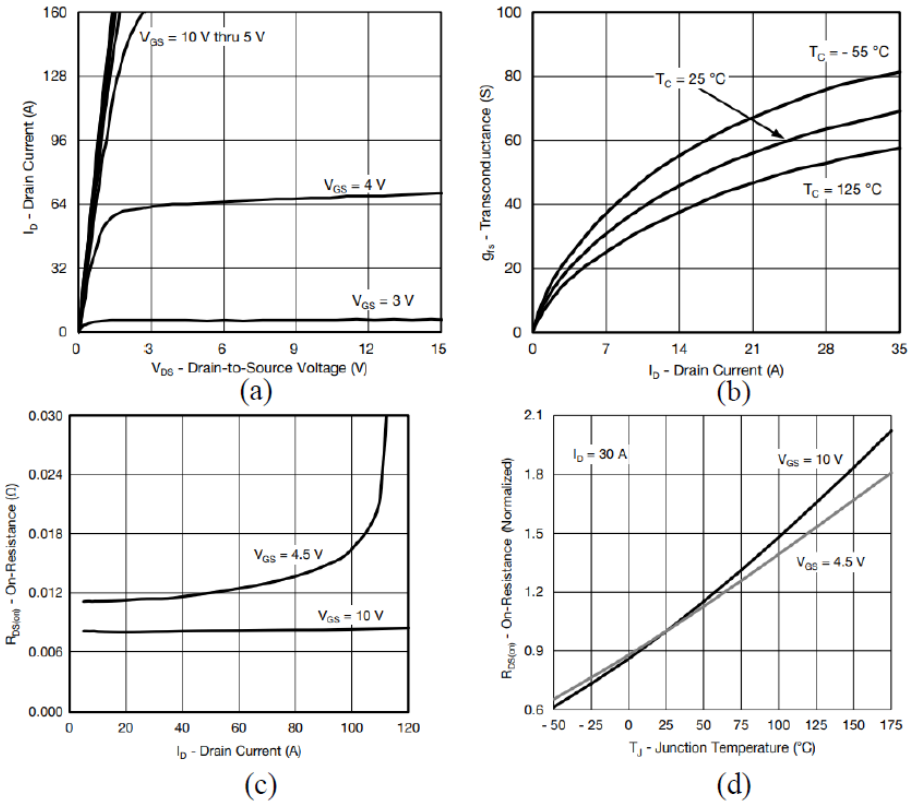


Figure 4.12: Typical characteristics curves of P-type MOSFET (SUP70101EL from Vishay): (a) Output characteristics curve; (b) transconductance with drain current; (c) on resistance vs drain current; (d) on-resistance vs junction temperature

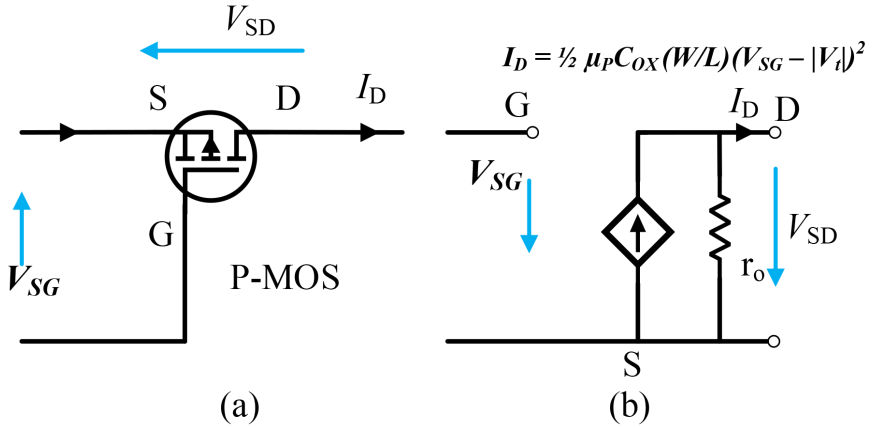


Figure 4.13: P-MOSFET: (a) large signal parameters; (b) simplified large signal equivalent circuit [75]

By combining Equation 4.11 and 4.12, bias point can be established as,

$$V_{\mathrm{SG}} = \sqrt{\frac{2LV_{\mathrm{REF}}(R_1+R_2)}{\mu_{\mathrm{P}}C_{\mathrm{ox}}WR_2\left(R_{\mathrm{L}}//(R_1+R_2)\right)}} + |V_{\mathrm{t}}| \tag{4.13}$$

However for the boundary between saturation region and the triode region,

$$V_{\mathrm{SD}} = V_{\mathrm{SG}} - V_{\mathrm{t}} \tag{4.14}$$

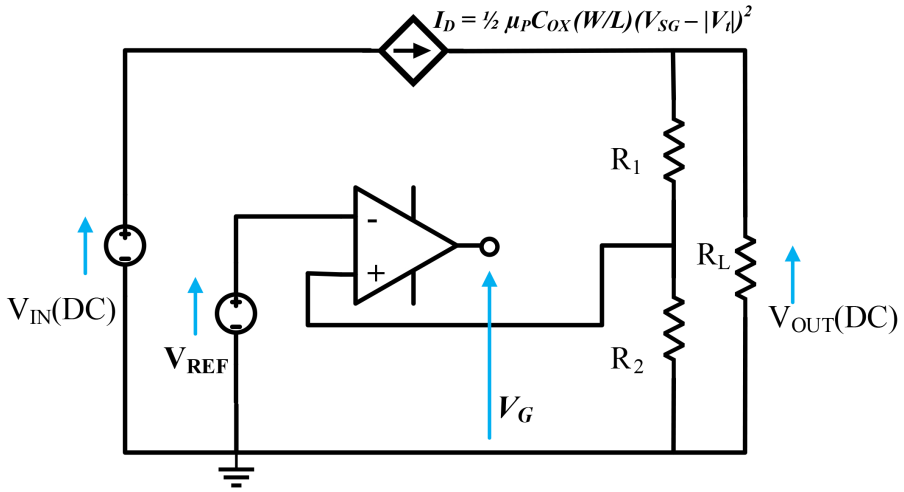


Figure 4.14: Large signal equivalent circuit of the P-MOSFET based regulator

Where V_{SD} is the dropout voltage of P-MOSFET. Substituting Equation 4.14 to Equation 4.13, dropout voltage can be obtained,

$$V_{SG} - |V_t| = V_{SD} = \sqrt{\frac{2LV_{REF}(R_1 + R_2)}{\mu_P C_{ox} W R_2 \left(R_L // (R_1 + R_2)\right)}} \tag{4.15}$$

The analysis can be extended considering small signal parameters of the P-MOSFET for step response around the bias point. The basic pin layout of the P-MOSFET is shown in Figure 4.15(a) and the small signal model is shown in Figure 4.15(b) [76]. Here v_{sg} $(= -v_{gs})$ represents source gate voltage, V_{SD} represents source drain voltage, g_m represents the transconductance (slope of I_D verses V_G at a given bias point), and r_o represents the output resistance of the MOSFET for a given V_{SD} $(= -V_{DS})$.

Transconductance g_m depends on the given operating point and, by differentiating Equation 4.12 respect to V_{SG}, can find the equation for g_m,

$$g_m = \mu_P C_{ox} \frac{W}{L} (V_{SG} - |V_t|) \tag{4.16}$$

by substituting bias point value of V_{SG} from Equation 4.13, exact value of g_m can be calculated. This behaviour of g_m around given V_{SG} is shown in Figure 4.16. v_{sg} is the step response of the gate voltage around given bias point voltage of V_{SG}.
For the boundary between saturation region and the triode region ($V_{SG} - |V_t| = V_{SD}$), Equation 4.16 reduces to,

$$g_m = \mu_P C_{ox} \frac{W}{L} V_{SD} \tag{4.17}$$

As shown in Figure 4.16, the transconductance can be obtained considering the gradient of the drain current (i_D) vs the gate voltage v_{sg} curve for given bias point.

By applying Figure 4.15 equivalent circuit to P-MOSFET based linear regulator, equivalent circuit shown in Figure 4.17 can be derived.

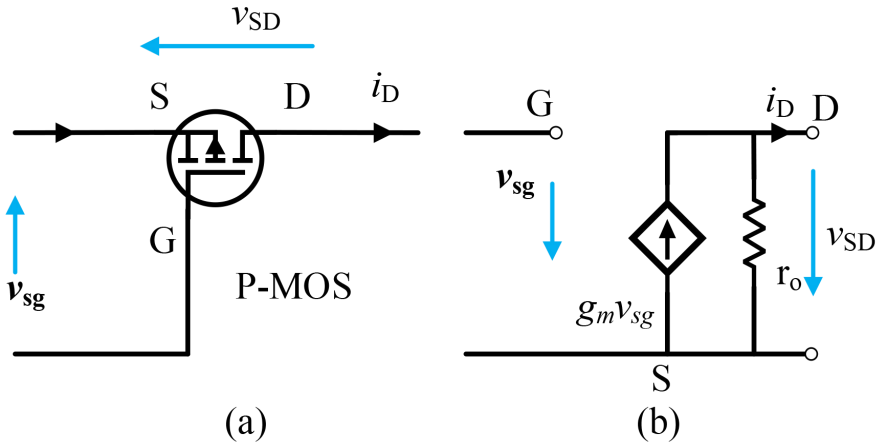


Figure 4.15: P-MOSFET: (a) small signal parameters; (b) simplified small signal equivalent circuit [76]

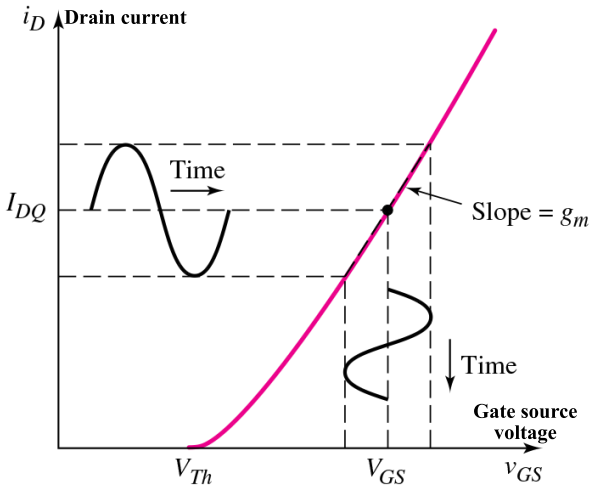


Figure 4.16: MOSFET drain current against gate voltage [76]

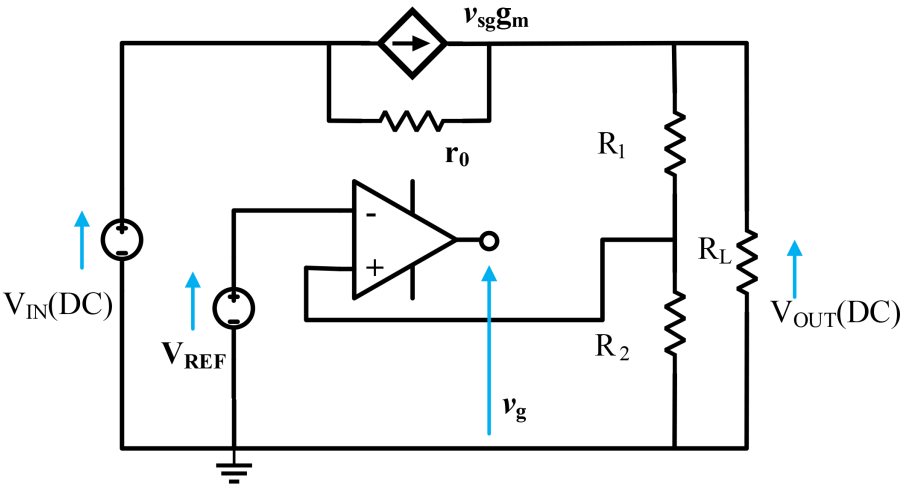


Figure 4.17: Equivalent circuit of the MOSFET based regulator

The output voltage of the opamp v_g is given by:

$$v_g = \left[\frac{(V_{OUT}R_2)}{(R_1 + R_2)} - V_{REF}\right] A_V \tag{4.18}$$

Then the gate voltage of the P-MOSFET v_{sg} is given by:

$$v_{\mathrm{sg}} = V_{\mathrm{IN}} - \left[\frac{(V_{\mathrm{OUT}}R_2)}{(R_1+R_2)} - V_{\mathrm{REF}}\right] A_{\mathrm{V}} \tag{4.19}$$

This equation can be simplified substituting $K_1 = \frac{(R_2)}{R_1+R_2}$, giving

$$v_{\mathrm{sg}} = V_{\mathrm{IN}} - K_1 V_{\mathrm{OUT}} A_{\mathrm{V}} + V_{\mathrm{REF}} A_{\mathrm{V}} \tag{4.20}$$

As shown in Figure 4.17, R_1 and R_2 are the sampling resistors and A_{V} represents the differential voltage gain of the operational amplifier. Here we have assumed that the current entering the noninverting terminal of the opamp is negligible.
The output voltage of the LDO, V_{OUT} is given by:

$$V_{\mathrm{OUT}} = \left[v_{\mathrm{sg}} g_{\mathrm{m}} + \frac{(V_{\mathrm{IN}} - V_{\mathrm{OUT}})}{r_{\mathrm{o}}}\right] ((R_1+R_2)//R_{\mathrm{L}}) \tag{4.21}$$

However r_{o} is a very large value, and assuming its effect (channel length modulation effect) is negligible, Equation 4.21 can be rewritten to,

$$V_{\mathrm{OUT}} = (v_{\mathrm{sg}} g_{\mathrm{m}})\,(R_1+R_2) \tag{4.22}$$

Substituting v_{sg} from Equation (4.20),

$$V_{\mathrm{OUT}} = [V_{\mathrm{IN}} g_{\mathrm{m}} - K_1 V_{\mathrm{OUT}} A_{\mathrm{V}} g_{\mathrm{m}} + V_{\mathrm{REF}} A_{\mathrm{V}}]\,((R_1+R_2)//R_{\mathrm{L}})$$

The above equation can be expan to:

$$V_{\mathrm{OUT}} = \left[V_{\mathrm{IN}} g_{\mathrm{m}} + V_{\mathrm{REF}} A_{\mathrm{V}} g_{\mathrm{m}} - \frac{R_2}{R_1+R_2} V_{\mathrm{OUT}} A_{\mathrm{V}} g_{\mathrm{m}}\right] ((R_1+R_2)//R_{\mathrm{L}})$$

$$V_{\mathrm{OUT}} = \left[V_{\mathrm{IN}} g_{\mathrm{m}} + V_{\mathrm{REF}} A_{\mathrm{V}} g_{\mathrm{m}} - \frac{R_2}{R_1+R_2} V_{\mathrm{OUT}} A_{\mathrm{V}} g_{\mathrm{m}}\right] \frac{(R_1+R_2)R_{\mathrm{L}}}{R_{\mathrm{L}}+(R_1+R_2)}$$

$$V_{\mathrm{OUT}} = \frac{V_{\mathrm{IN}} g_{\mathrm{m}}(R_1+R_2)R_{\mathrm{L}} + V_{\mathrm{REF}} A_{\mathrm{V}} g_{\mathrm{m}}(R_1+R_2)R_{\mathrm{L}}}{R_{\mathrm{L}}+(R_1+R_2)+R_2 R_{\mathrm{L}} A_{\mathrm{V}} g_{\mathrm{m}}} \tag{4.23}$$

For the boundary condition $g_{\mathrm{m}} = \mu_{\mathrm{P}} C_{\mathrm{ox}} \frac{W}{L} V_{\mathrm{SD}}$.

Dividing both numerator and denominator by A_{V} in Equation 4.23:

$$V_{\mathrm{OUT}} = \frac{\frac{V_{\mathrm{IN}} g_{\mathrm{m}}(R_1+R_2)R_{\mathrm{L}}}{A_{\mathrm{V}}} + V_{\mathrm{REF}} g_{\mathrm{m}}(R_1+R_2)R_{\mathrm{L}}}{\frac{R_{\mathrm{L}}+(R_1+R_2}{A_{\mathrm{V}}}) + R_2 R_{\mathrm{L}} g_{\mathrm{m}}} \tag{4.24}$$

and assuming very large A_V ($A_V \to \infty$) the equation reduces to,

$$V_{OUT} = \frac{V_{REF}}{K_1} = V_{REF}\frac{R_1 + R_2}{R_2} \tag{4.25}$$

Which is the familiar Equation for output voltage of P-MOSFET based linear voltage regulator. Selecting opamp with higher input impedance and very high open loop gain, we can achieve higher accuracy of output voltage.

4.5 LDO implementation

The LDO stage was implemented according to the schematic shown in Figure 4.18 with two parallel MOSFETs; it produced outstanding performance. This circuit can regulate at 12 V output voltage for 12.5 V input voltage maintaining only a 0.5 V voltage margin at a 10 A load current. It was important to use a MOSFET with very low on-resistance as we were particular about the dropout voltage. For this implementation, we used an SUP70101EL P-channel MOSFET, which has an on-resistance of 0.0101 mΩ (from data sheet) and a drain to source maximum voltage of 100 V, well above the required value. Typical characteristics curves of this MOSFET are shown in Figure 4.12. Behaviour of I_D for different gate voltages plotted in Figure 4.12(a). The behaviour of transconductance vs drain current is shown in Figure 4.12(b). At gate voltage $V_{GS} = 10$ V, we can expect constant on-resistance below 12 mΩ. Junction temperature has a huge impact on the on-resistance, and the V_{DS} voltage drop is decided by this factor. This behaviour is shown in Figure 4.12(d). MOSFET does not generate significant heat, even at 10 A load current. However, we used a cooling fan and heat sink to keep the MOSFET at room temperature as on-resistance is a function of the temperature.

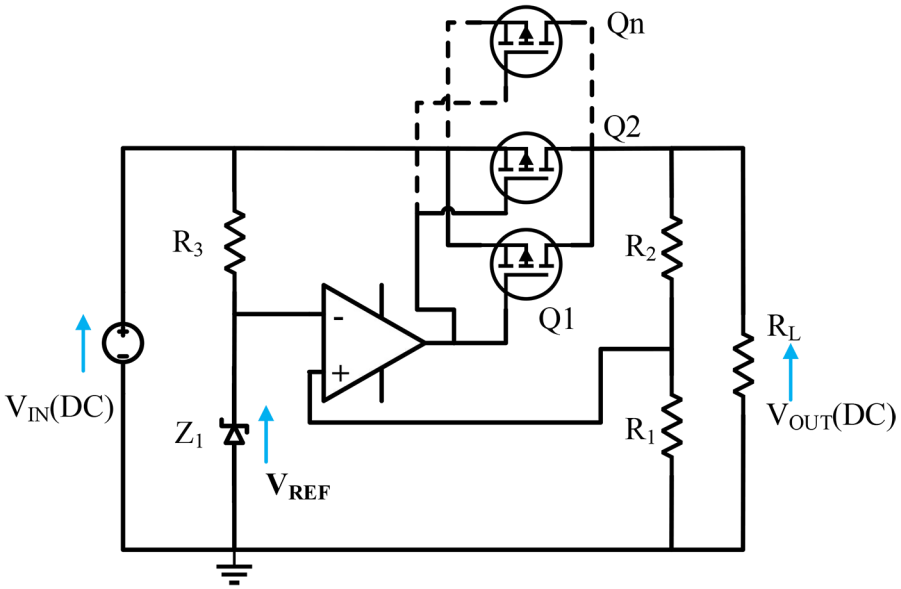


Figure 4.18: Implementation of the LDO-stage: schematic with n parallel P-MOSFETs

Zener-based shunt references and band gaps were considered as the reference voltage for the error amplifier. Shunt references have some advantage including simple design, small package, low cost and stability over a large range of voltage and current. However, they lack flexibility in

voltage values. Bandgap references can produce a wide range of voltages, increasing the design flexibility. They can also work with small headroom voltage such as 100 mV, can produce precise voltage and have low-temperature drift. After considering stability over a range of voltage and current, cost and design complexity, we chose a zener-based shunt voltage reference as shown in the schematic Figure 4.18.

4.5.1 Experimental validation

The LDO stage was tested using an electronic load, TEXIO PXL-151A, which is shown in Figure 4.19. The load can handle up to 300 W power, and the current rating is 150 A. This load can be configured to act as constant current (CC), constant resistance (CR), constant power (CP), and constant voltage (CV) loads. The slew rate performance of a power supply can be measured by enabling the switching mode of the electronic load.

Figure 4.19: TEXIO Kenwood PXL-151A-DC electronic load

The line and load regulation performance of the LDO prototype are shown in Figures 4.20 and 4.21 respectively. Output and input voltage waveform for 1, 4, 6 and 10.8 A load current conditions are depicted in oscillogram format in Figure 4.22.

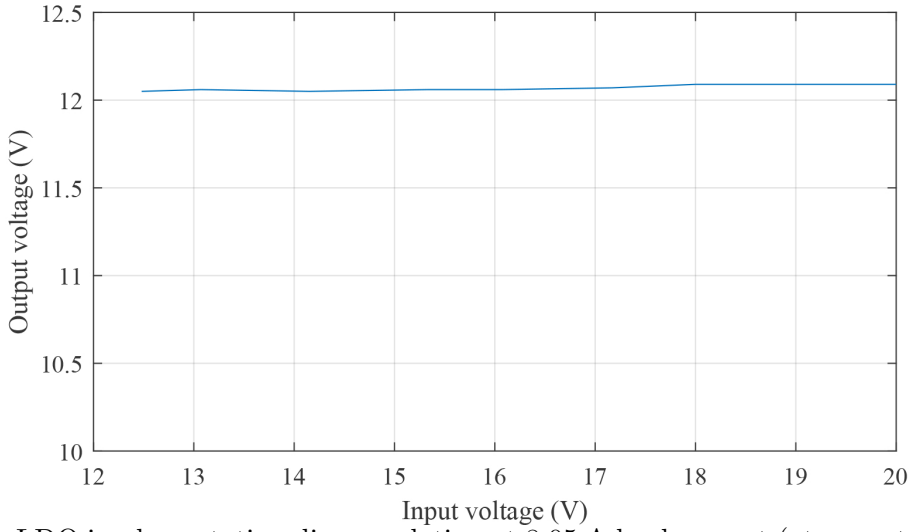


Figure 4.20: LDO implementation, line regulation at 8.05 A load current (at room temperature)

Theoretical efficiency and practical efficiency are compared in Figure 4.23. The experimental setup is shown in Figure 4.24.

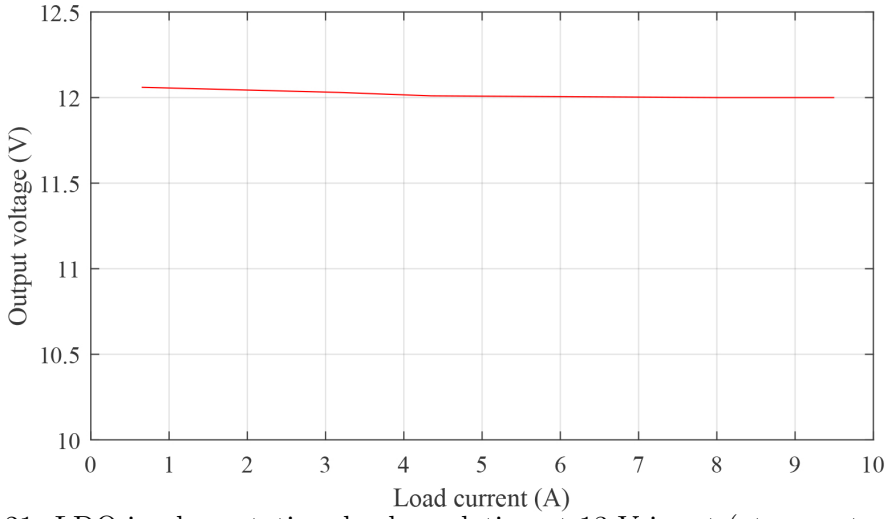


Figure 4.21: LDO implementation, load regulation at 13 V input (at room temperature)

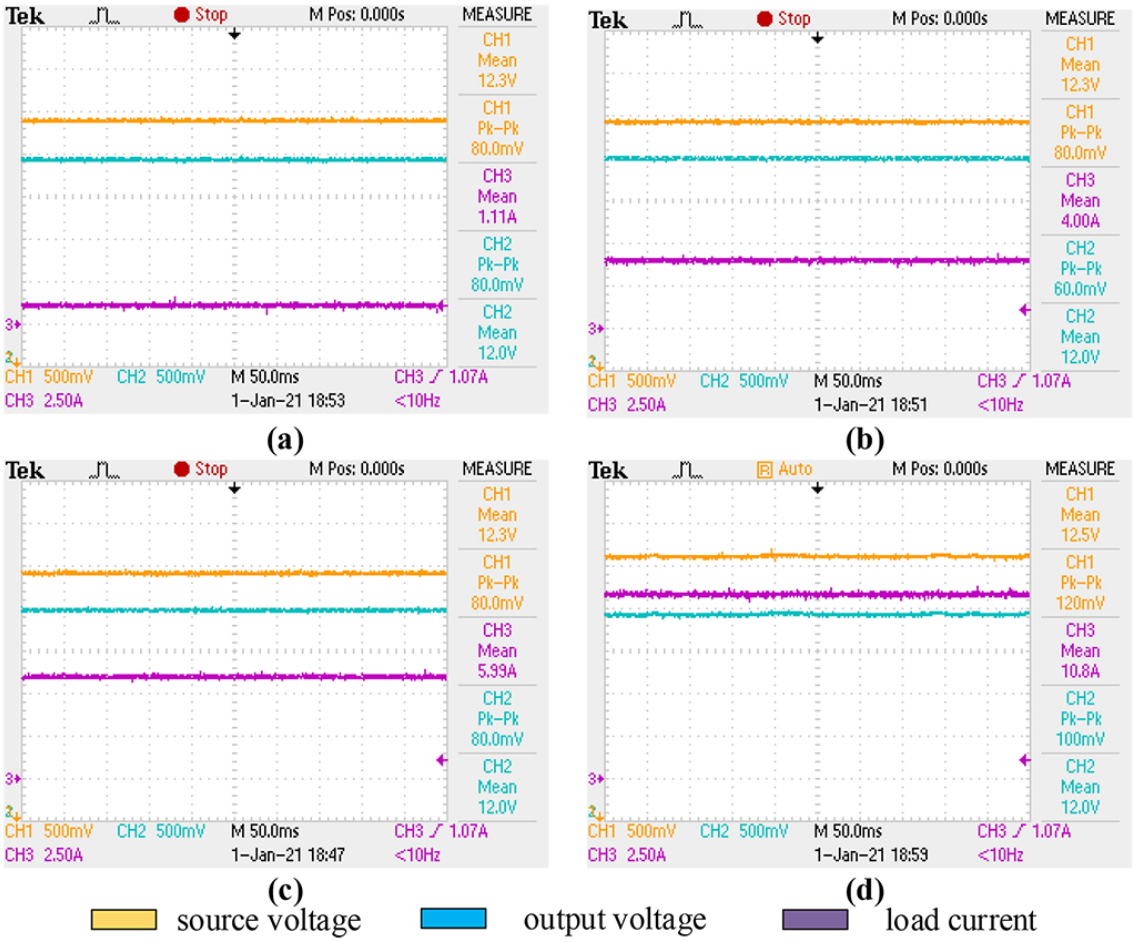


Figure 4.22: Input and output voltage waveform of the LDO circuit for a range of load current: (a) 1.11 A; (b) 4 A; (c) 6 A; (d) 10.8 A

4.5.2 Load transient response of LDO

Transient response is a useful property of a power supply that determines its performance during sudden variations in load. A transient response is defined as the maximum allowable output voltage variation for a step-change in load current [17]. The value of the output capacitor C_0,

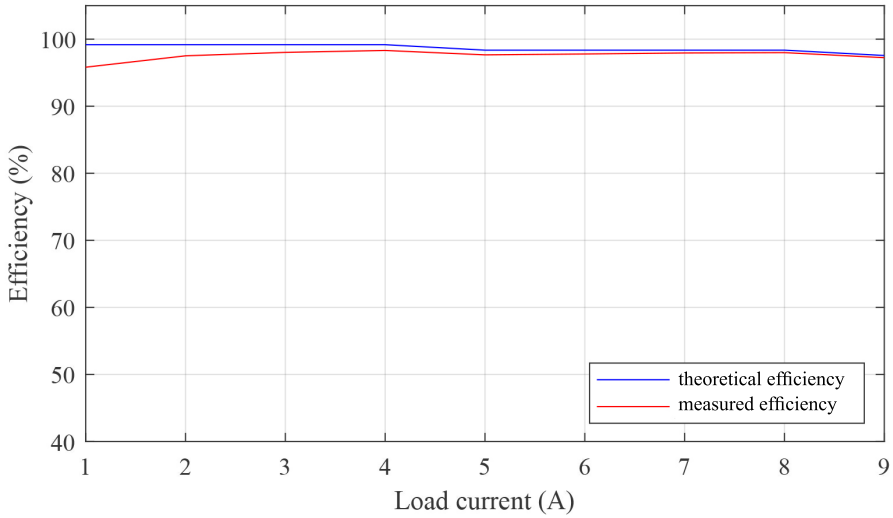


Figure 4.23: LDO efficiency data

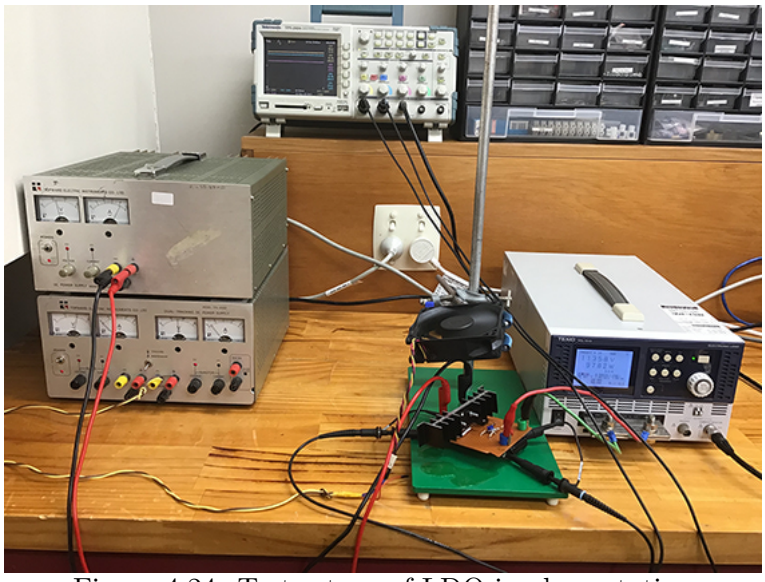


Figure 4.24: Test set-up of LDO implementation

the equivalent series resistance (ESR) of the output capacitor, and the maximum load current ($I_{\mathrm{L,max}}$) are the main contributors to the maximum transient response [17].

DC electronic load can be used to measure the transient response of the power converter. Preset A and B were load current in Ampere that could be set in advance using the menu. The load switching function allowed us to toggle these load conditions alternatively. The slope of the rising edge, slope of the falling edge, and the frequency of operation can be configured using menus in the electronic load. Figure 4.25 shows a sample oscillogram for the data we obtained for various slew rate conditions.

4.6 High current SCALDO stage design and implementation

This section discusses the design and implementation details of this SCALDO stage. The output voltage of the SCALDO is the same as the output voltage of the LDO, and for the prototype, this was 12 V. Since we had the flexibility over the input voltage due to the pre-regulation

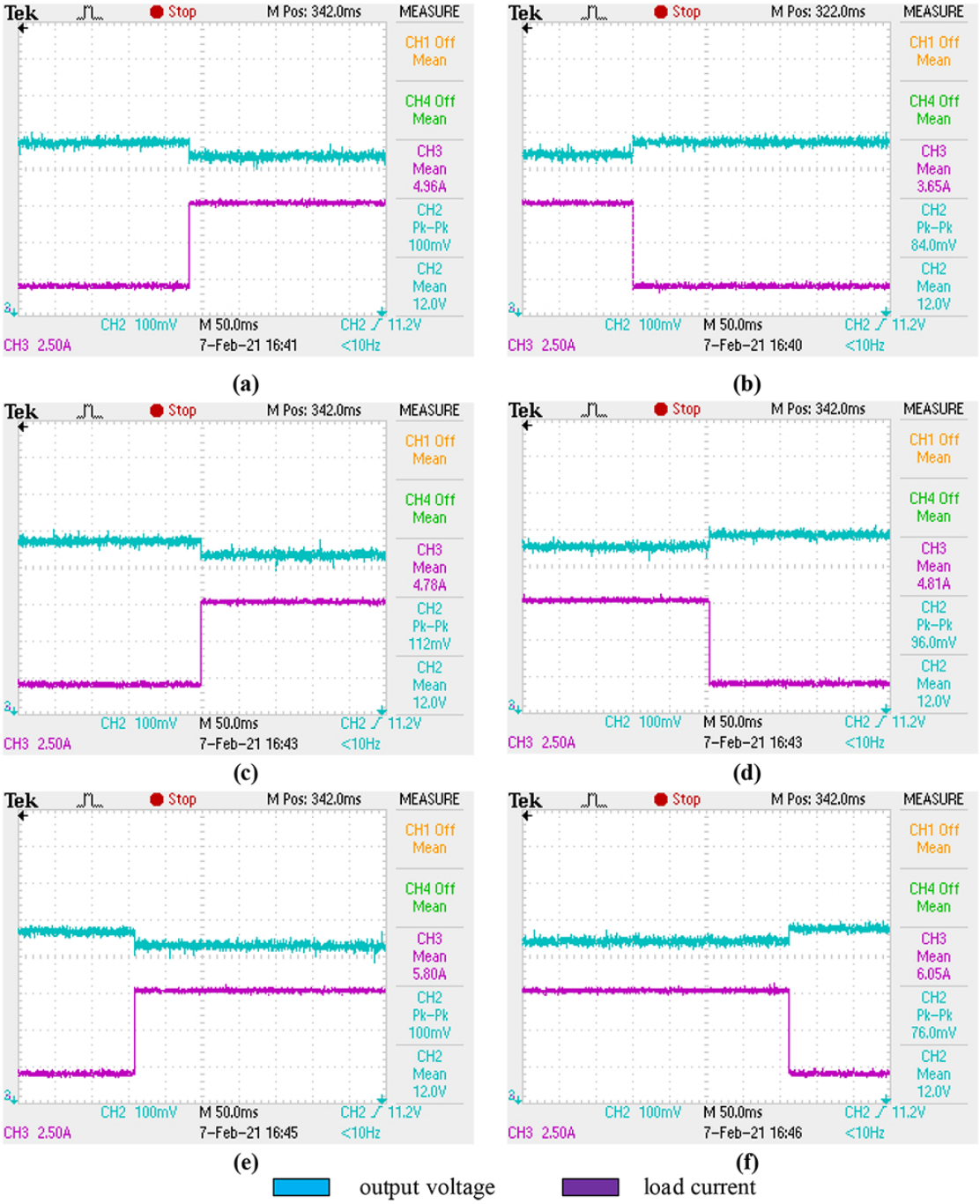


Figure 4.25: Transient response oscillogram of LDO prototype for various test setups: (a) current rising from 2 to 8 A at 1 A/μs; (b) current falling from 8 to 2 A at 1 A/μs; (c) current rising from 2 to 8 A at 10 A/μs; (d) current falling from 8 to 2 A at 10 A/μs; (e) current rising from 2 to 8 A at 20 A/μs; (f) current falling from 8 to 2 A at 20 A/μs

stage we chose the configuration $V_{\mathrm{P}} > 2V_{\mathrm{in}}^{\mathrm{min}}$. The design parameters of this SCALDO stage are shown in Table 4.2. In the basic SCALDO configuration of column-1 of the table, a single capacitor bank is used and the input voltage is chosen to satisfy $V_{\mathrm{p}} > 2V_{\mathrm{in}}^{\mathrm{min}}$. Four switches are required as shown in Figure 4.26. Taking the internal resistance of the supercapacitor as r_{sc} and the on-resistance of a switch as r, the maximum voltage that the supercapacitor can charge up to is given by $V_{\mathrm{p}} - V_{\mathrm{in}}^{\mathrm{min}} - I_{\mathrm{L}}(2r + r_{\mathrm{sc}})$, for load current I_{L} discharge time is given by:

$$t_{\mathrm{dch}} = \frac{C}{I_{\mathrm{L}}}[V_{\mathrm{in}}^{\mathrm{max}} - V_{\mathrm{in}}^{\mathrm{min}}] \tag{4.26}$$

where C is the capacitance of supercapacitor used. By considering the voltage ESR of the capacitor (r_{sc}) and the resistance of the MOSFETs (r), the above equation can be rewritten as:

$$t_{\mathrm{dch}} = C\left[\frac{V_{\mathrm{p}} - 2V_{\mathrm{in}}^{\mathrm{min}}}{I_{\mathrm{L}}} - (4r + 2r_{\mathrm{sc}})\right] = T_1 \tag{4.27}$$

Details of the calculations are available in [17].

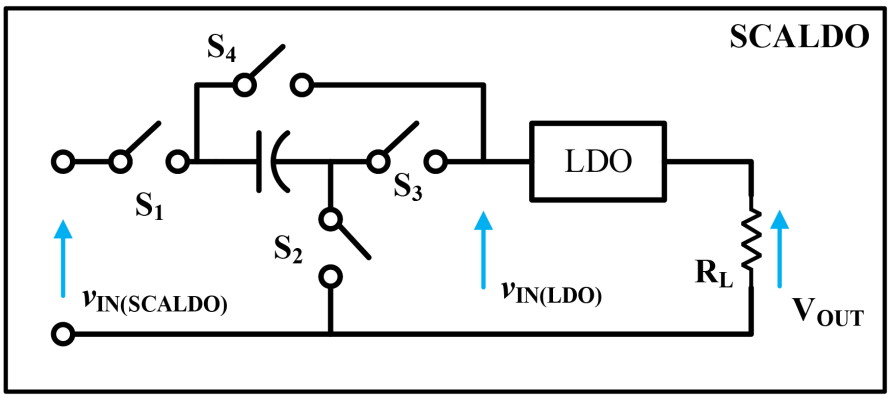


Figure 4.26: The basic SCALDO concept

It is invaluable to have a simulation model of a SCALDO to observe behaviours in different configurations. An LTspice simulation model of SCALDO was developed as a part of the study prier to full implementation. The next section describes this simulation model and output waveforms.

Table 4.2: SCALDO parameters: n=number of supercapacitor banks, k=number of switches, $V_{\mathrm{sc}}^{\mathrm{max}}$=maximum voltage across the supercapacitor, t_{ch}=supercapacitor charge time, t_{dch}=supercapacitor discharge time; η=efficency for three different cases of SCALDO configurations [17]

Parameters	$V_{\mathrm{p}} > 2V_{\mathrm{in}}^{\mathrm{min}}$ basic config.	$V_{\mathrm{p}} > 2V_{\mathrm{in}}^{\mathrm{min}}$ general case	$V_{\mathrm{p}} < 2V_{\mathrm{in}}^{\mathrm{min}}$ general case
n	1	$n < \frac{V_{\mathrm{P}} - V_{\mathrm{in}}^{\mathrm{min}}}{V_{\mathrm{in}}^{\mathrm{min}}}$	$n < \frac{V_{\mathrm{in}}^{\mathrm{min}}}{V_{\mathrm{P}} - V_{\mathrm{in}}^{\mathrm{min}}}$
k	4	$3n + 1$	$3n + 1$
$V_{\mathrm{sc}}^{\mathrm{max}}$	$V_{\mathrm{p}} - V_{\mathrm{in}}^{\mathrm{min}} - I_{\mathrm{L}}(2r + r_{\mathrm{sc}})$	$\frac{1}{n}\left[V_{\mathrm{p}} - V_{\mathrm{in}}^{\mathrm{min}} - I_{\mathrm{L}}\left[(n+1)r + nr_{\mathrm{sc}}\right]\right]$	$V_{\mathrm{p}} - V_{\mathrm{in}}^{\mathrm{min}} - \frac{I_{\mathrm{L}}}{n}(2r + r_{\mathrm{sc}})$
t_{ch}	T_1	$\frac{T_{\mathrm{n}}}{n}$	T_{n}
t_{dch}	T_1	T_{n}	$\frac{T_{\mathrm{n}}}{n}$
η	2	$1 + n$	$1 + \frac{1}{n}$

4.6.1 LTspice Simulation of SCALDO

The main operating states of SCALDO are shown in Figure 4.27. When we turn on the converter, the circuit needs to operate in the initial charging state until the supercapacitor voltage reaches

$V_{\mathrm{P}} - V_{\mathrm{LDO(min)}}$ This means for input voltage $V_{\mathrm{P}} = 26$ V and $V_{\mathrm{LDO(min)}} = 12.5$ V, the converter stays in the initial charging state until the SC voltage reaches 13.5. Then the converter switches to the SC discharging state, and the SC discharges down to $V_{\mathrm{LDO(min)}}$. Then the converter toggles between charging and discharging states as long as it operates.

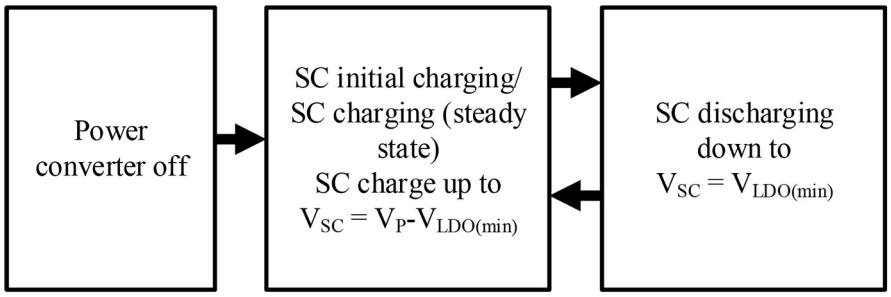


Figure 4.27: State chart for SCALDO operation

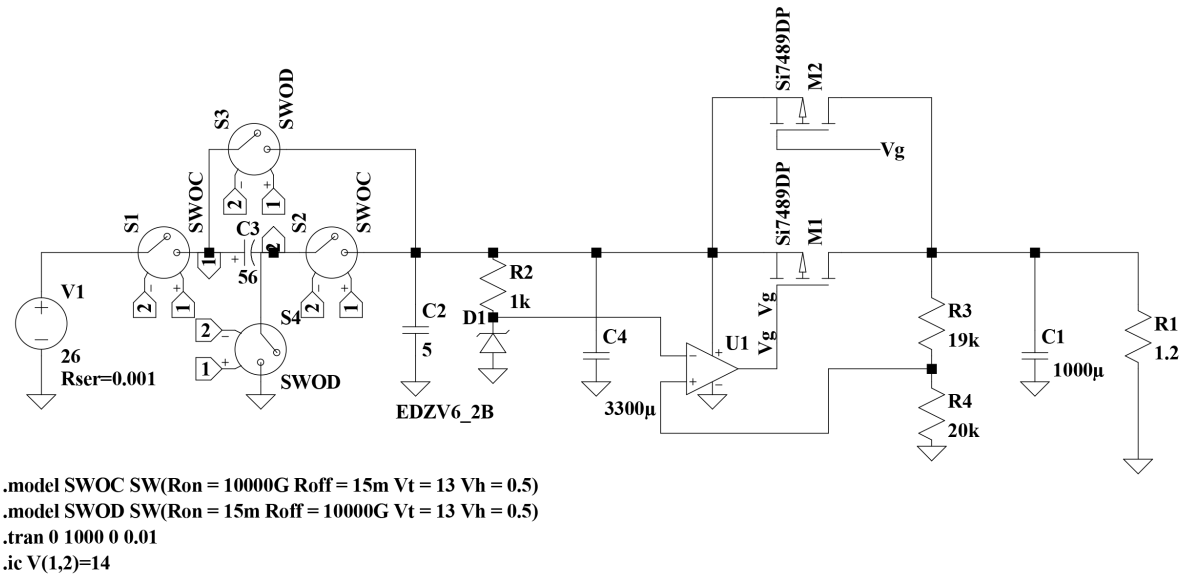


Figure 4.28: Schematic for the LTspice simulation of SCALDO

The LTSpice simulation model of the SCALDO is shown in Figure 4.28. Realising the switching network of the design was an important design challenge. This was accomplished with voltage control switches in LTSpice as detailed in Appendix B of [63]. The basic model of the operation is given by:

```
.model MYSW SW(Ron=1 Roff=1Meg Vt=5 Vh=0.4)
```
(4.28)

Here MYSW represents the model name, Ron and $Roff$ represent the on and off resistance of the switch. To reduce the voltage drop, Ron should be kept at a small value in the range of milliohms (mΩ). However this should be a feasible value for practical implementation (depending on the on-resistance of MOSFET switches used). Vt and Vh are the trip and hysteresis voltages: the switch trips at $(Vt - Vh)$ and $(Vt + Vh)$. According to the SCALDO design discussed in this study, the supercapacitor voltage should be maintained between 12.5 and 13.5 V. This meansthat,

$$Vt + Vh \;=\; 13.5\ V \quad and \quad Vt - Vh = 12.5\ V$$

implying that $Vt = 13, Vh = 0.5$. SCALDO switches S1 and S2 should turn on at the same time while switches S3 and S4 also operate together. In order to model this behaviour, the on and off resistances of S1 and S2, were swapped for switch S3 and S4. These two switch models are shown below.

```
.model SWOC SW(Ron=100000G Roff=15m Vt=13 Vh=0.5)        (4.29)
.model SWOD SW(Ron=15m Roff=100000G Vt=13 Vh=0.5)        (4.30)
```

The output voltage, output current, supercapacitor voltage, supercapacitor current, and LDO input voltage waveforms obtained from the LTspice simulation are shown in Figure 4.29. Further details of the simulation are available in Appendix A. A 15 mΩ on-resistance was applied to the voltage control switches in order to model practical MOSFET behaviour. In order to minimise the voltage drop across switches, a MOSFET with the lowest on-resistance was chosen. For the LDO simulation a Si7489DP MOSFET switch was used, which had 41 mΩ on-resistance. The voltage drop in the path directly impacts the converter's final efficiency as this voltage drop determines the minimum required input voltage for the converter.

4.6.2 SCALDO implementation

As shown in Figure 4.30, early versions of SCALDO prototypes were developed using solid-state relays. Current paths can be easily controlled using solid-state relays as they create no ground isolation problems and reduce the design complexity. However, scaling SCALDO to handle higher current was challenging as solid-state relays (SSD) are very expensive for higher current configurations. The Crydom GNA5 series 10 A SSD costs $\$NZD70$ according to the pricing in Mouser; four such switches were required for basic SCALDO configuration. As detailed in [77], some of the important losses identified in early SCALDO implementations can be listed as:

- ESR and leakage current losses in supercapacitors
- losses due to on-resistance of the switches
- power dissipated in the path resistance of the circuit
- power consumption of the controller circuit
- loss in buffer capacitors

Most of these losses are unavoidable. However, another critical problem identified in the implementation is the visibility of parasitic discharge paths for supercapacitors due to the body diode of the MOSFET as depicted in Figure 4.31(a). A few strategies that can be used to block current paths are:

- Adding a diode to the output path
- Adding a MOSFET to the output path
- Using a load switch IC with reverse current blocking

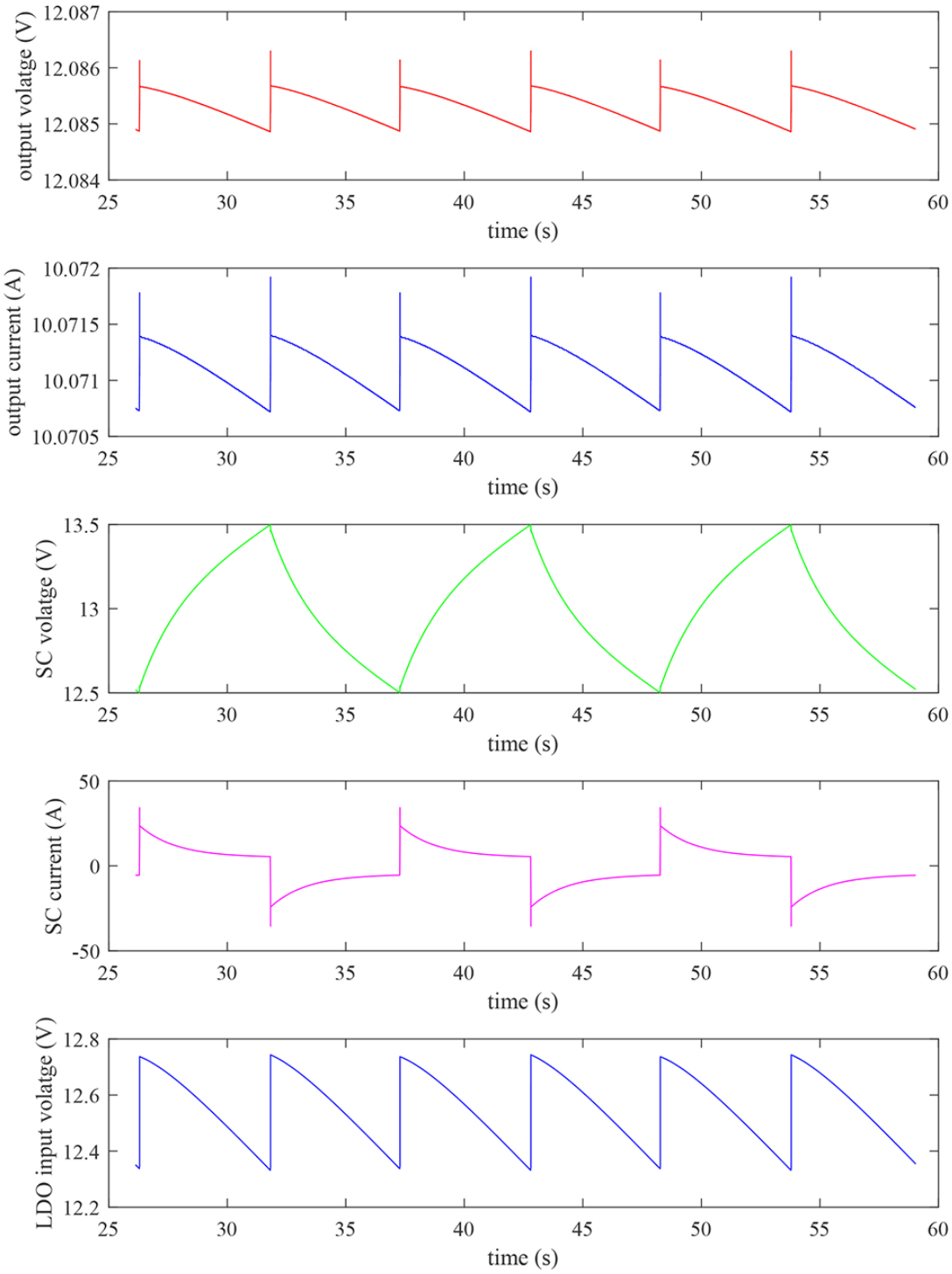


Figure 4.29: Waveform of the SCALDO simulation

Using a diode as shown in Figure 4.31(b), is not an viable solution as the additional voltage drop reduces the SCALDO stage's efficiency. Using a load switch IC with reverse current blocking increases the circuit's design complexity as we would then have four switches to control. Insering a MOSFET as in Figure 4.31(b) ads 15 mΩ extra resistance to the path, and costs $NZD 3. However, for low current implementation, MOSFETs can be costly as the transistor count increases to six. After considering considering these advantages and drawbacks we

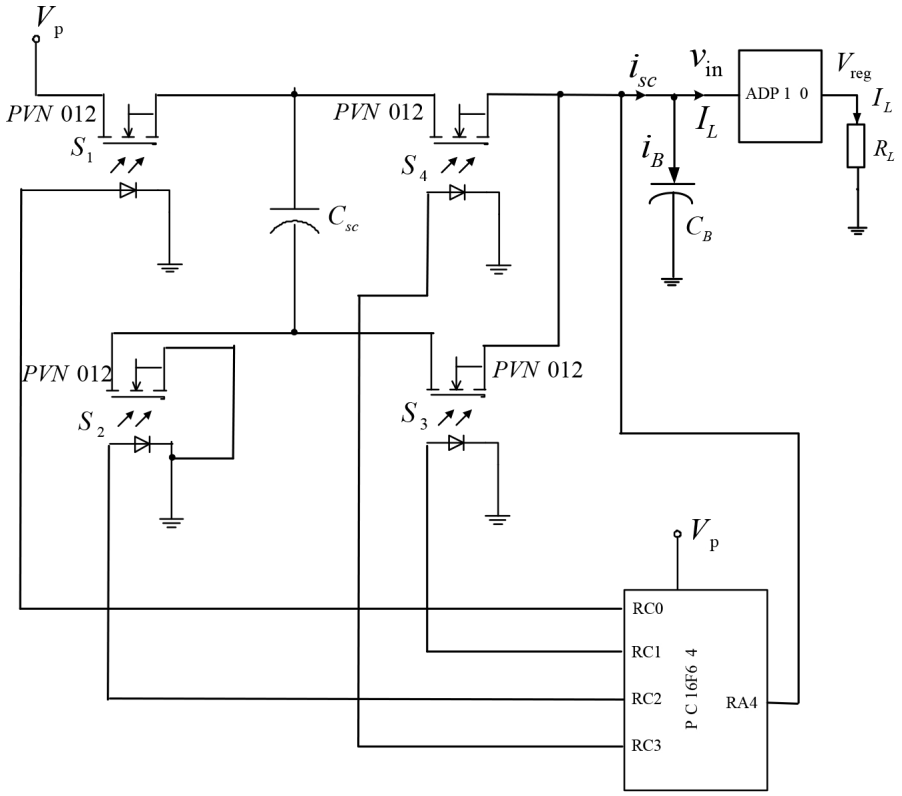


Figure 4.30: Solid state relay based SCALDO implementation [17]

chose to implement our switch network with back-to-back MOSFETs. High current MOSFETs are cost-effective compared to solid-state relays. A 30% Loss reduction can be obtained in a MOSFET-based solution as shown in Figure 4.32. A schematic of the high current SCALDO implementation is shown in Figure 4.33.

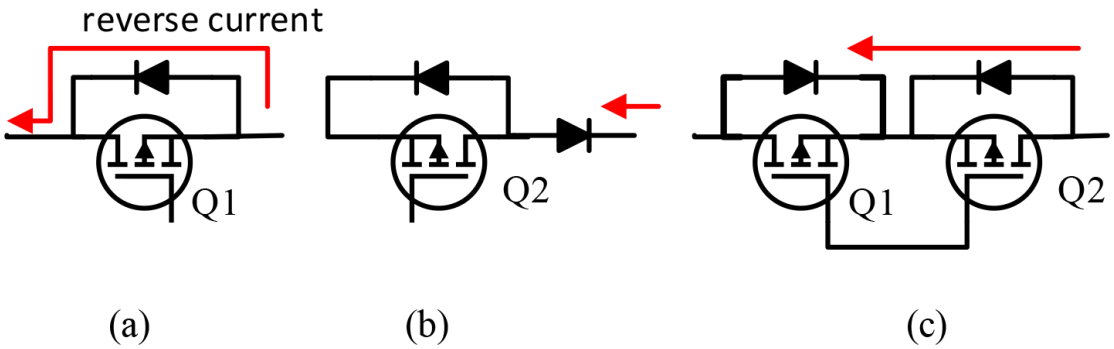


Figure 4.31: Reverse current blocking strategies: (a) basic issue; (b) using diode in series; (d) using back-to-back MOSFETs

The two main operating phases of SCALDO and the corresponding current paths are shown in Figure 4.34. Figure 4.34(a) depicts the series supercapacitor charging stage, where three p-MOSFETs occur in series. In Figure 4.34(b), the load is powered by the supercapacitor bank and two n-MOSFETs, and one p-MOSFET appear in series. For the implementation of the basic SCALDO configuration, the voltage drop for the SC charging phase is then given by $3r_{\text{pmos}} + r_{\text{ESR(sc)}}$, where r_{pmos} is the on-resistance of the P-channel MOSFET. For the SC

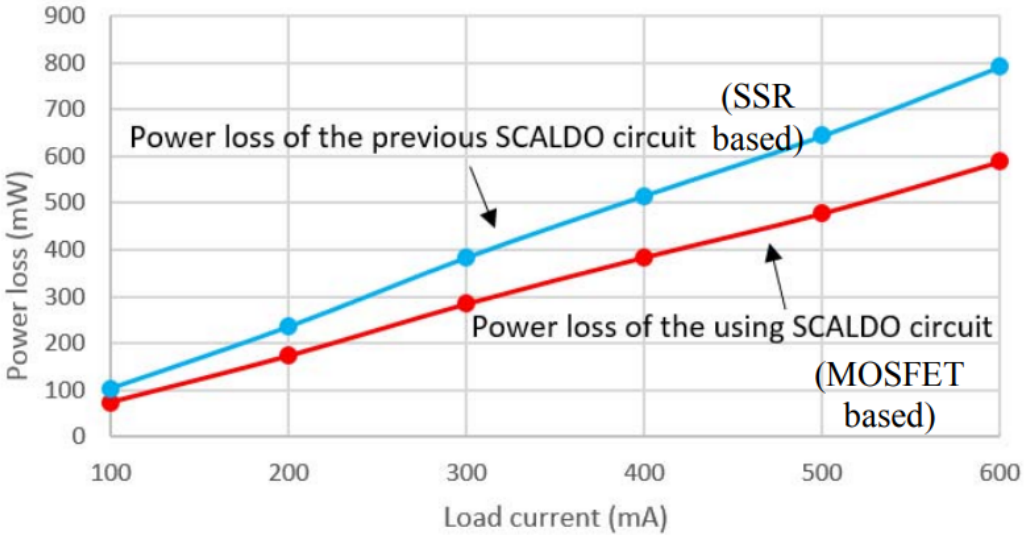


Figure 4.32: Power loss comparison of MOSFET-based SCALDO and solid state relay-based (SSR) SCALDO implementations [77]

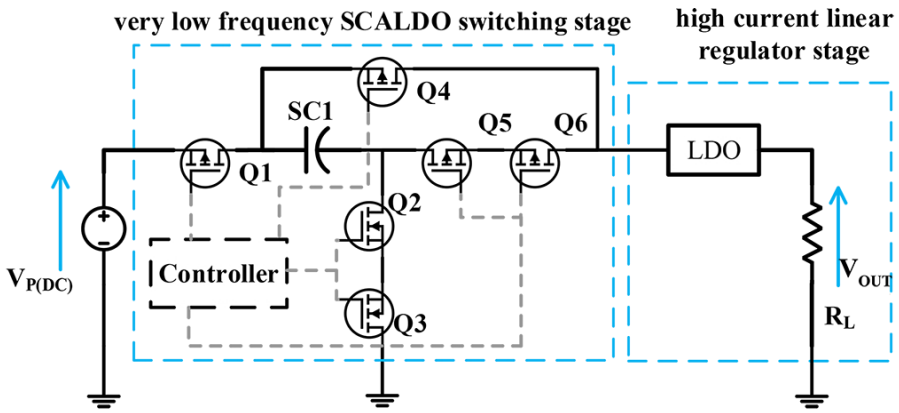


Figure 4.33: High-current SCALDO schematic

discharging phase this voltage drop is given by $2r_{\text{nmos}} + r_{\text{pmos}} + r_{\text{ESR}}$, where r_{nmos} is the on-resistance of N-channel MOSFET.

Ignoring the voltage drop in ESR and path MOSFETs, the maximum power dissipated in the LDO p-MOSFET is given by:

$$\begin{aligned} P_{\text{max}} &= (V_{\text{P}} - V_{\text{OUT}})\, I_{\text{L}} \\ &= (26 - 12)10 = 140\ W \end{aligned}$$

The LDO MOSFET should be capable of handling this peak power dissipation during initial SC charging state. However, during the steady-state phase of the operation, power dissipation in the MOSFET is minimal.

A PIC16F690 microcontroller was used to implement the controller circuit. MOSFETs were driven using BC547 NPN transistors as shown in Figure 4.35(a)(b). By default the gate voltage of the N-MOSFET was set to 15 V. When the controller pin was set to 5 V, the transistor moved to the forward bias region and started conducting; this arrangement was the same for SCALDO 48 V design as the gate set to 15 V. As a result of this, the N-MOSFET gate was voltage set

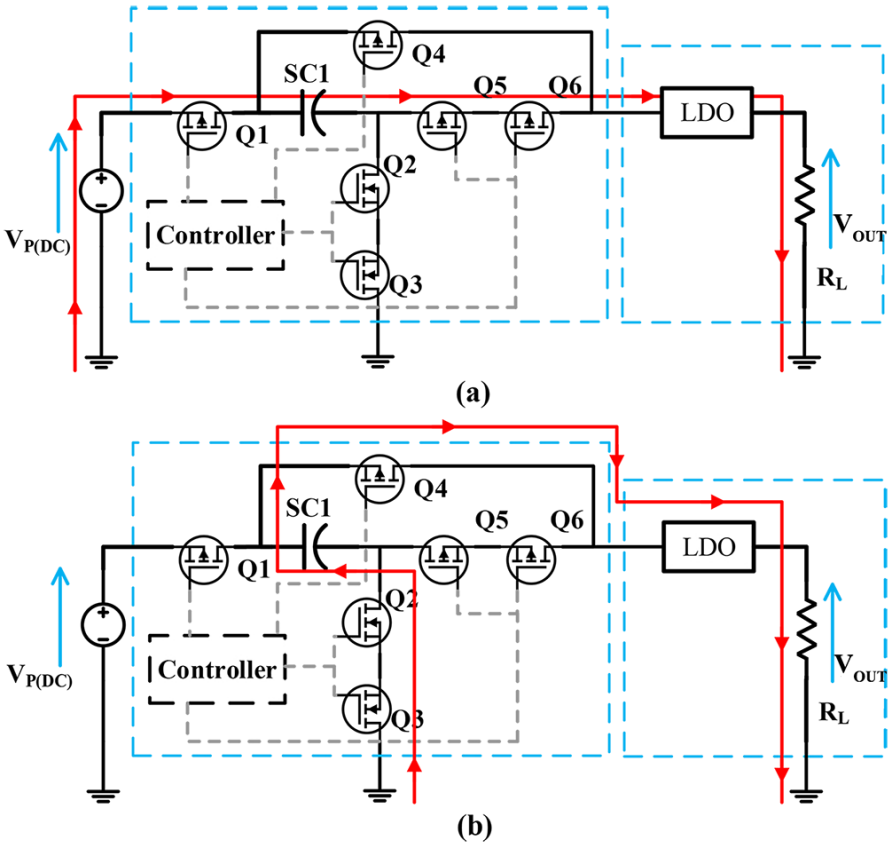


Figure 4.34: SCALDO current circulation: (a) during SC charging; (b) SC discharging

to 0 V. By default, the P-MOSFETS were at an off state as the gate was connected with the source, as shown in Figure 4.35(b). When the transistor was conducting, R1 and R3 acted as a voltage divider and set the gate voltage to −15 V relative to the source, and P-MOSFET started conducting. It is important to turn on MOSFETs with the proper gate voltage as output resistance depends on the gate voltage. Two characteristics curves of MOSFETs extracted from the data sheets are shown in Figure 4.36. When choosing values for R1 and R3 in Figure 4.35, the following condition should be satisfied in order to keep the voltage drop of the switch at a minimum value:

$$V_{\mathrm{G}} = V_{\mathrm{S}} \times \frac{R1}{R1 + R3} \quad and \quad V_{\min} \leq V_{\mathrm{G}} \leq V_{\max} \tag{4.31}$$

where V_{G} represents the gate voltage and V_{S} represents the voltage at the MOSFET source pin. The $V_{\min}$ value was selected from the datasheet to turn on the P-MOSFET with the specified low on-resistance and $V_{\max}$ gate voltage.

For the implementation, SUP70101EL-GE3 P-chanel MOSFET and IRF100B202 N-MOSFET were used. The main parameters of the switches are provided in Table 4.3. At the maximum load current ($I_{\mathrm{L}} = 10$ A) the power dissipated in the N-MOSFET is $I^2R = 10^2 \times 0.007 = 0.7$ W. During on-time the voltage drop in each N-MOSFET is as low as 0.07 V. The power dissipation in P-MOSFET is $I^2R = 10^2 \times 0.0101 = 1$ W and the per switch voltage drop is 0.1 V. For the MOSFET switches used, it is not required to have heat sinks as power dissipation is not significant.

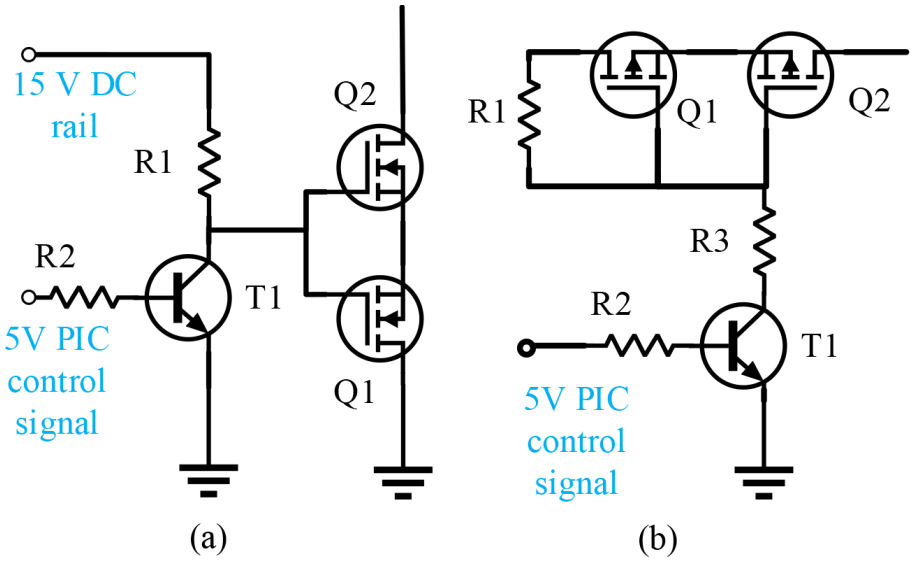


Figure 4.35: Driving MOSFET switches: (a) n-MOSFET driver circuit (b) p-MOSFET driver circuit

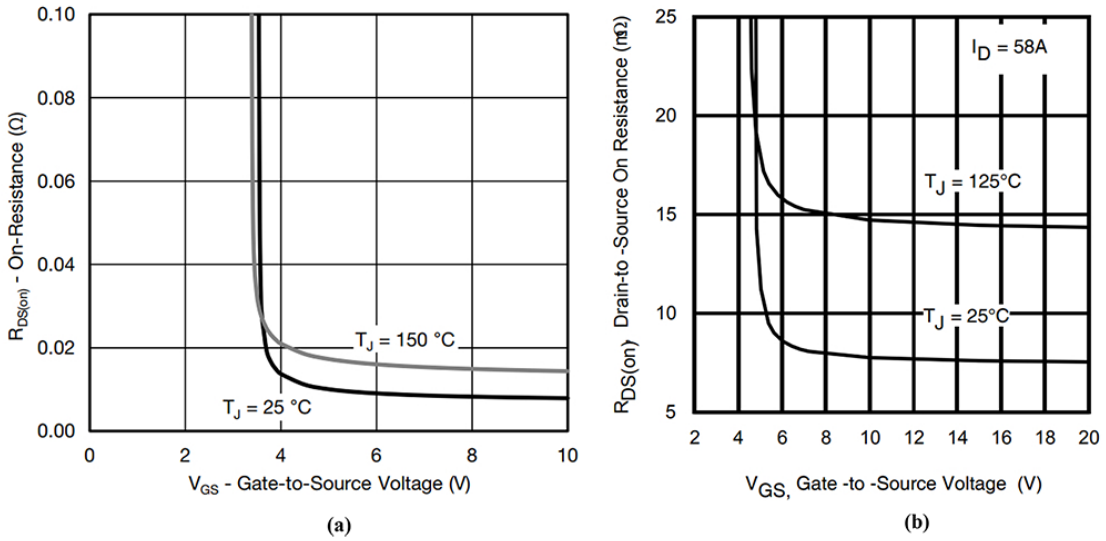


Figure 4.36: On-resistance of (a) $SUP70101EL-GE3$ P-MOSFET and (b) $IRF100B202$ N-MOSFET as a function of gate voltage

As discussed earlier, the same P-MOSFET is used for LDO implementation. The worst case scenario, arises when the supercapacitor bank is at the initial 0 V charging state leading to $26-12 = 14$ V drop appearing across the switch, ignoring the voltage drop in switches in between. Then the power dissipation is $14 \times 10 = 140$ W (70 W for eac of the two MOSFETs in parallel), and we must use a heatsink to avoid damaging the MOSFET. Also, since the on-resistance of the MOSFET increases with junction temperature, it is important to maintain the device at room temperature. It is advisable to choose a power MOSFET with well above normal power ratings for the maximum power dissipation calculated here. Details of the supercapacitor bank used for this implementation are listed in Table 4.4 and the datasheet is attached in Appendix A.

Detailed schematics, PCB design and data sheets for the main components are attached in Appendix A. The circuit requires two DC rails to power a PIC microcontroller (5 V) and 15 V to

Table 4.3: Specifications of MOSFETS used for SCALDO implementation

Component	Usage	Max drain source voltage V_{DS} (V)	On resistance $R_{DS(on)}$ Ω	Gate voltage V_{GS} (V)	Drain current I_D (A)	Power P_d (W)
SUP7010EL	p-channel	−100	0.0101	±20	−120	375
IRF100B202	n-channel	100	0.0072	±20	97	221

Table 4.4: LSUM 016R8L 0058F EA supercapacitor module specification

Property	Value
Rated voltage	16.8 V
Max. voltage	18.0 V
Capacitance	58 F
Maximum ESR	22 mΩ
Maximum current	210 A
Specific energy	3.2 Wh/kg
Max stored energy	2.3 Wh
Cycle life	500 000

power an N-MOSFET. Two linear regulators were designed using commercially available chips, as shown in Figure 4.37. For higher currents, this arrangement causes losses and lower the overall efficiency. The controller circuit draws less than 100 mA so does not have a significant impact on overall efficiency. The same DC rails could be used to power the 48 V output SCALDO stage. However, current-limiting resistors would need to be scaled to suit voltage differences. For the 12 V configuration the R1 resistor can be selected as:

$$R1 = (V_P - 15)/0.1 \approx 100\ \Omega \tag{4.32}$$

and the power rating should be higher than $P = VI = 11 \times 0.1 = 1.1$ W, so a 100 Ω, 5 W resistor can be chosen as R1.

The value of the R2 resistor can be calculated as:

$$R2 = (15 - 5)/0.1 = 100\ \Omega \tag{4.33}$$

where the power rating is given by $(P = VI = 10 \times 0.1 = 1\ W)$. A 100 $\Omega, 5\ W$ resistor is a good choice for this resistor also.

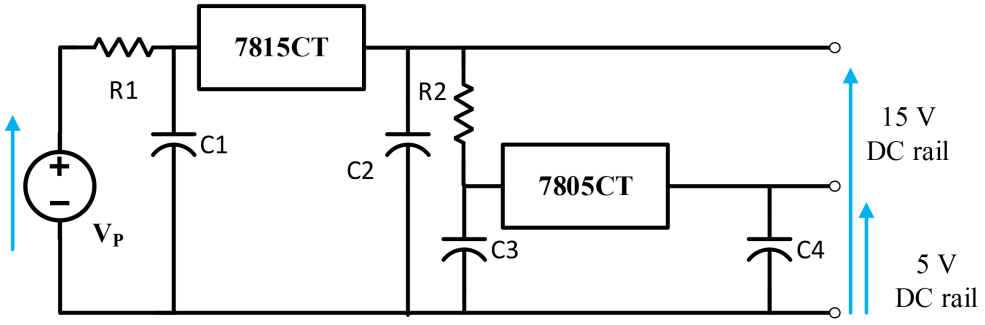


Figure 4.37: Power controller circuit in SCALDO

The 12 V SCALDO prototype implementation is shown in Figure 4.38 and the SCALDO test set-up is shown in Figure 4.39.

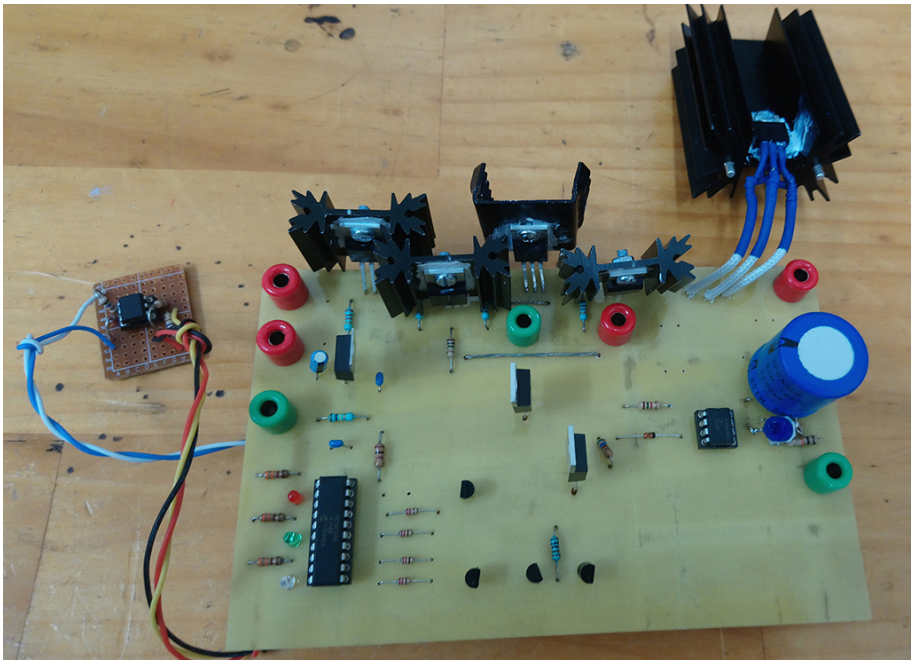


Figure 4.38: SCALDO implementation circuit

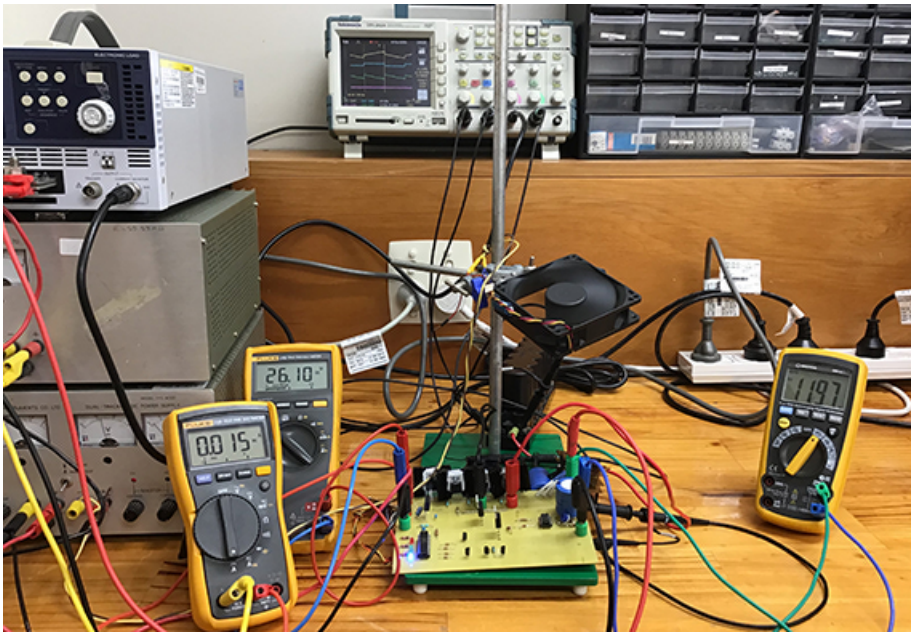


Figure 4.39: Test set-up for the SCALDO prototype

Oscillograms obtained from the SCALDO prototype at various load currents are shown in Figure 4.40; oscillograms of output voltage profile, supercapacitor voltage, load current and LDO input voltage profile are shown in the figure. These readings were used to calculate the efficiency at each load condition, as depicted in Figure 4.41.

Transient performance data obtained from the SCALDO prototype are shown in Figure 4.42. In each case, the load current was changed from 2 to 8 A at various slew rates such as 1, 10

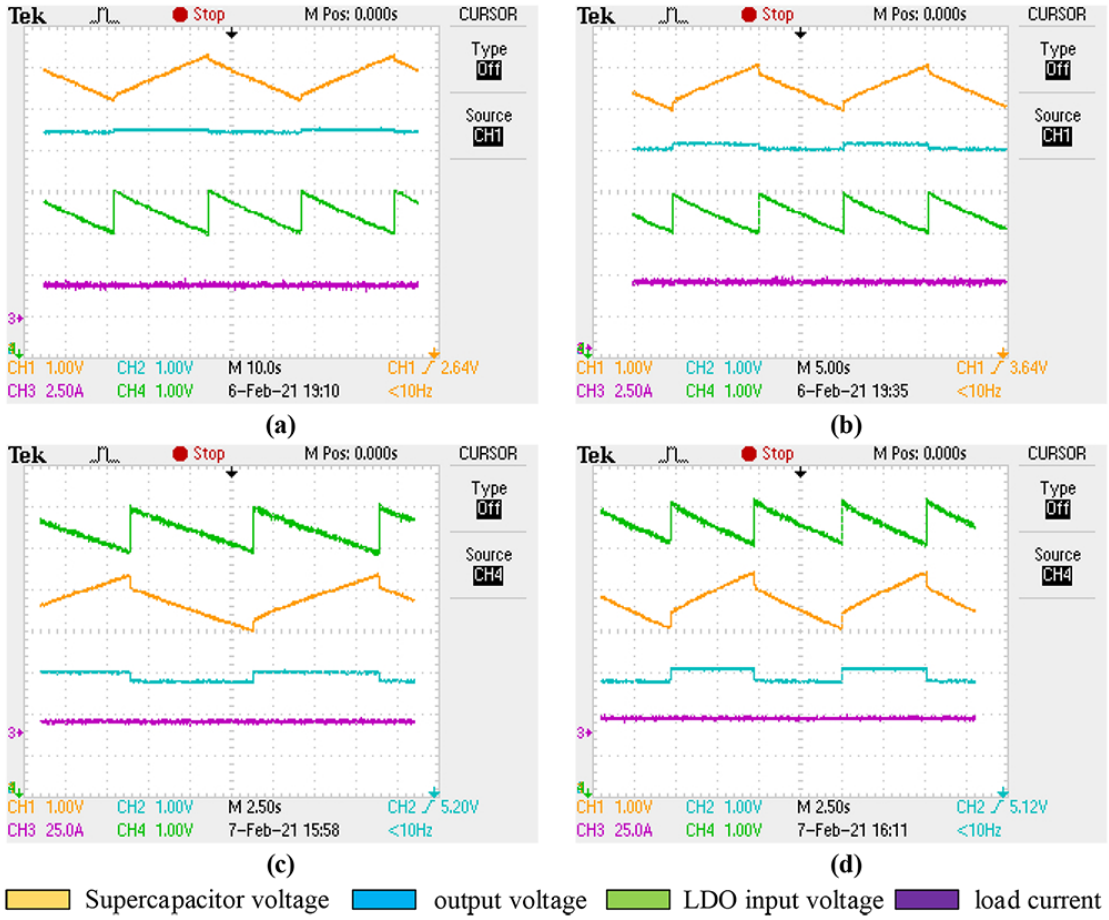


Figure 4.40: Oscilloscope waveform of 26-to-12 V SCALDO regulator for load currents of (a) 2 A (b) 4 A (c) 6 A (d) 8 A at an input voltage of 26 V

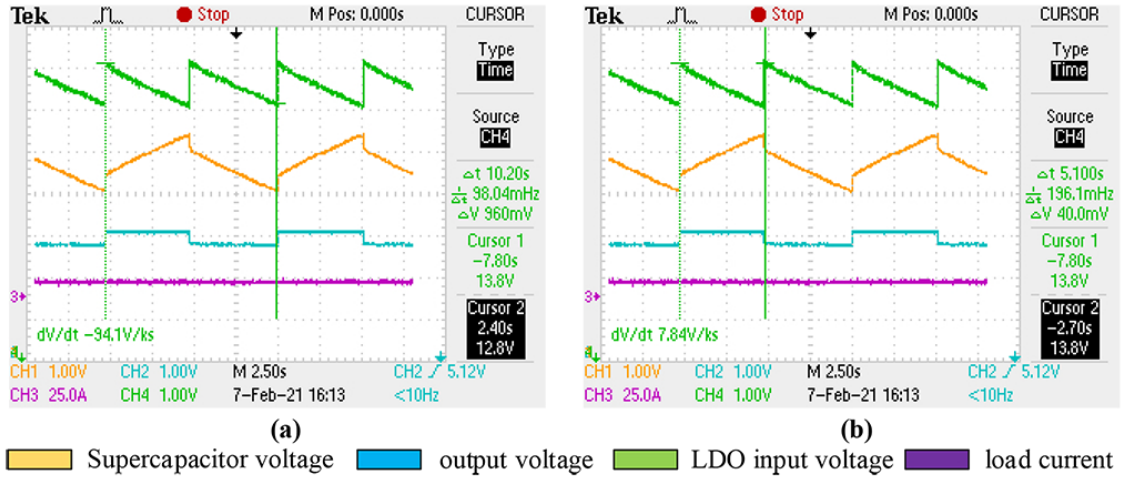


Figure 4.41: Oscilloscope waveform of 26-to-12 V SCALDO regulator for load currents of 6 A: (a) obtaining period; (b) Obtaining charging time

and 20 A/μs. Waveforms showing both rising and the falling edges were captured. Load voltage fluctuation at each test condition did not exceed 40 mV.

Calculating end-to-end efficiency is not straightforward in SCALDO as the converter toggles between two phases of operation. During the offline state, the converter consumes no current.

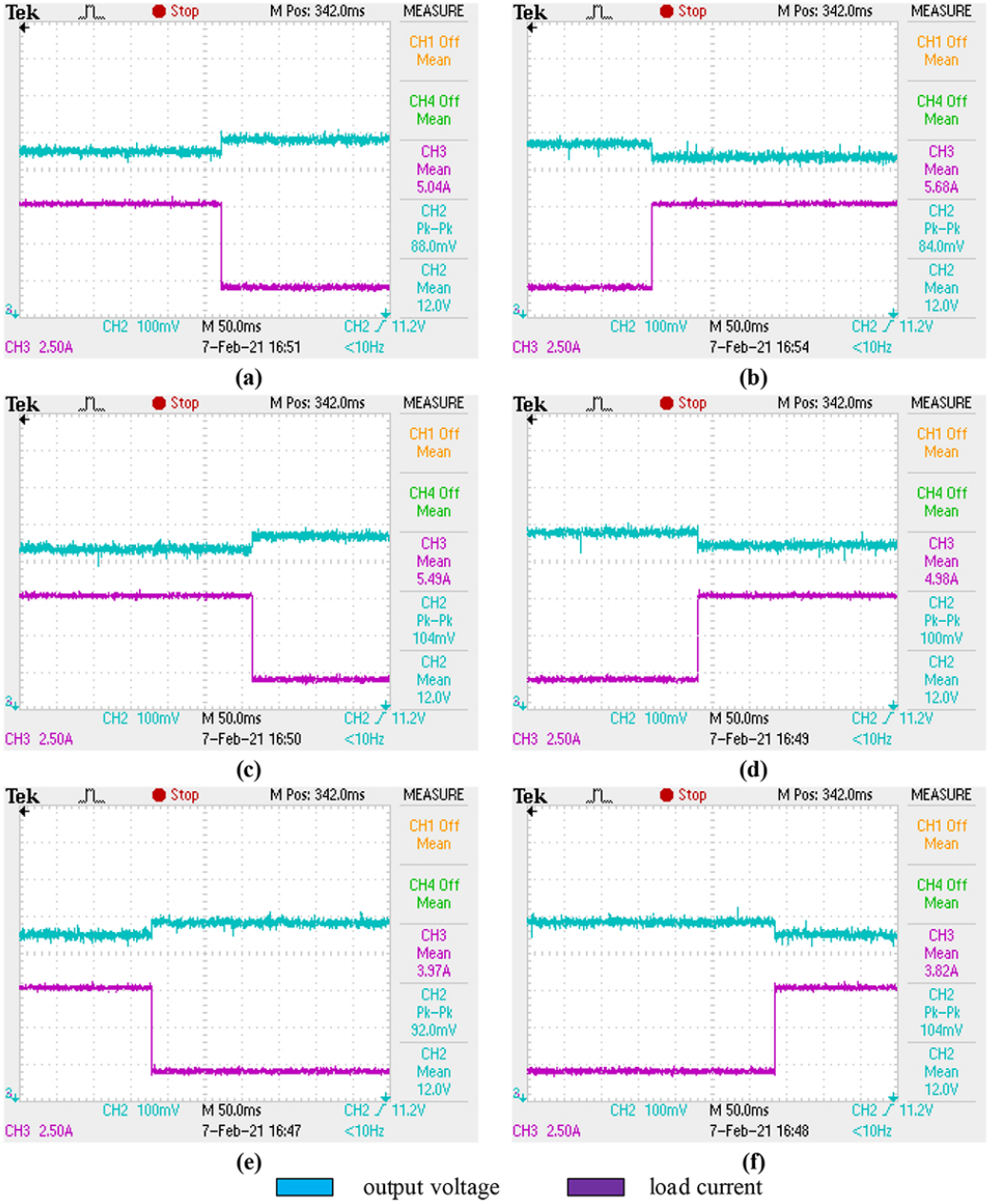


Figure 4.42: Transient response oscillogram of SCALDO fo various load conditions: (a) current falling from 2 A to 8 A at 1 A/μs; (b) current rising from 8 A to 2 A at 1 A/μs; (c) current falling from 2 A to 8 A at 10 A/μs; (d) current rising from 8 A to 2 A at 10 A/μs; (e) current falling from 2 A to 8 A at 20 A/μs; (f) current rising from 8 A to 2 A at 20 A/μs

In order to calculate the efficiency, we used the average current as detailed in [17], where V_{P} represents input voltage, I_{in} is input current, V_{reg} is regulated output voltage, I_{L} is load current and I_{c} is the current drawn by the controller circuit.The average current of the SCALDO is given by:

$$I_{\mathrm{avg}} = \frac{[I_{\mathrm{in}} - I_{\mathrm{c}}]t_{\mathrm{ch}}}{t_{\mathrm{ch}} + t_{\mathrm{dch}}} \tag{4.34}$$

Here t_{ch} and t_{dch} are the charging and discharging times of SCALDO supercapacitor bank respectively. Then the overall end-to-end efficiency of the SCALDO stage is given by:

$$\eta = \frac{V_{\text{reg}} I_{\text{L}}}{V_{\text{P}} I_{\text{avg}}} \times 100\% \tag{4.35}$$

The load performance of SCALDO is primarily determined by the LDO stage. Load regulation data obtained from the prototype are depicted in Figure 4.43. The theoretical and the practical efficiencies of the prototype are compared in Figure 4.44.

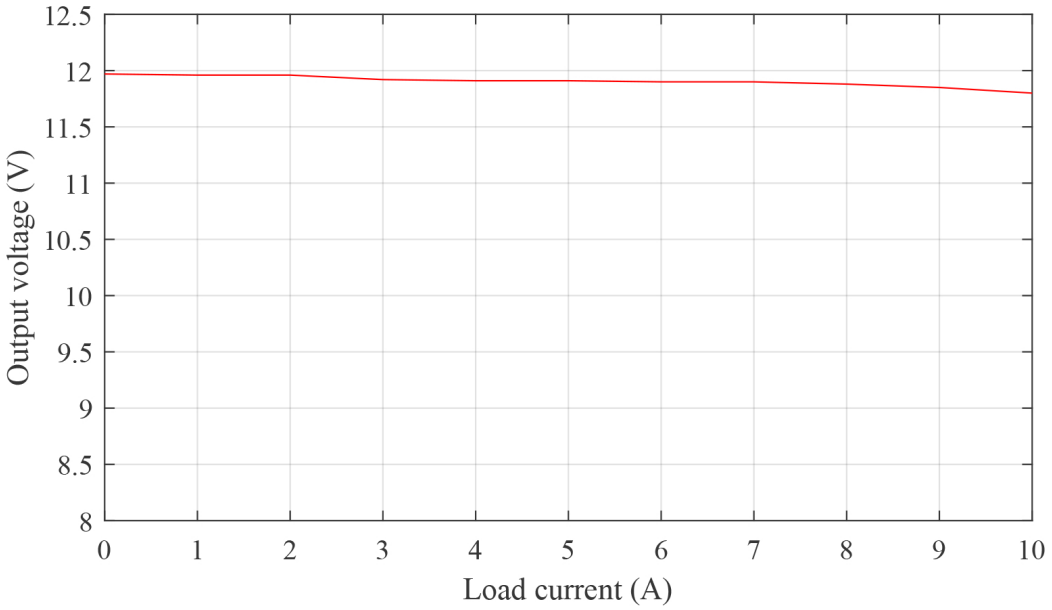


Figure 4.43: SCALDO load regulation at 26 V input

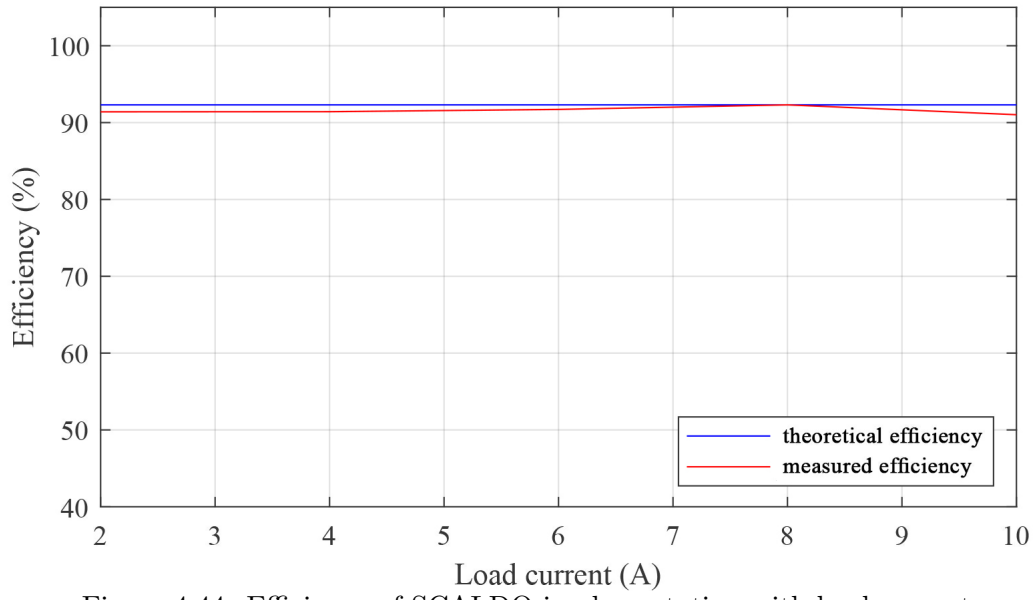


Figure 4.44: Efficiency of SCALDO implementation with load current

This prototype was not optimised for cost. However, in order to give a general idea we have indicated prototype costing in Table 4.5.

Table 4.5: Cost estimation for 26-to-12 V SCALDO implementation

Component	Unit cost (NZD)	Quantity	Cost (NZD)
SUP70101EL-GE3	3.93	6	23.58
IRF100B202	2.23	2	4.46
PIC16F690	3.69	1	3.69
LM741	1.45	1	1.45
BC547	0.43	4	1.72
7805TC	1.07	1	1.07
7815TC	0.92	1	0.92
TDK2200 μF	3.83	1	3.83
10 kΩ pot	1.34	1	1.34
Heat sink for TO-220AB	1.07	6	5.56
Rest of the resistors and filter Capacitors	2.00	1	2.00
PCB printing	10.00	1	10.00
Total			59.67

4.7 Scaling SCALDO output from 12 V to the 48 V required for a Google power supply

Technical aspects associated with scaling this SCALDO to 48 V are discussed in this section. The LDO stage should be able to regulate at 48 V with LDO minimum input voltage of 48.5 V. Assuming the SC bank charges up to 49.5 V to provide keeping a 1 V margin between charge and discharge cycles, the minimum required input voltage is,

$$V_{\text{in(min)}} = V_{\text{SC(max)}} + V_{\text{LDO(min)}} = 49.5 + 48.5 = 98 \text{ V} \tag{4.36}$$

The V_{DS} voltage of the selected MOSFETs should be well above this value, and the power rail and MOSFET driver resistor should be chosen according to minimum and maximum voltages. For better design flexibility, MOSFETs with $V_{\text{G}} = \pm 30$ can be chosen (easier to calculate resistor values when gate can tolerate higher voltage). For LDOs the minimum power rating is given by:

$$P = VI = [V_{\text{P}} - V_{\text{OUT}}]\, I_{\text{L(max)}} = (98 - 48) \times 10 = 500\ W \tag{4.37}$$

Since we are using two MOSFETs in parallel, and assuming identical characteristics, each MOSFET should have a power rating well above 250 W.

Another aspect is improving the accuracy of the LDO. Instead of using a simple zener-based voltage reference, a bandgap voltage reference could be selected to improve the voltage accuracy of the LDO.

4.8 Chapter summary

This chapter discussed how we extended SCALDO to handle higher voltage and current conditions, keeping the efficiency at the higher level required by the overall converter. The new LDO stage could regulate with minimum voltage drop, and the converter was tested up to 10 A load

current. Detailed test results were presented in the chapter. Further implementation details are available in Appendix A. The next chapter discusses the design and implementation details of the medium frequency preregulation stage of the power converter.

Chapter 5

Transformer Isolated Preregulator Stage for SCALDO

5.1 Introduction

The design and implementation details of a high-current scalable SCALDO was discussed in the previous chapter. For some power converter configurations, SCALDO is not practical due to the large number of switches and capacitors required, and the cost. This problem can be overcome by introducing a switched-mode preregulation stage. The new topology introduced in this chapter is a unique supercapacitor-assisted medium-frequency power converter with galvanic isolation and DC-UPS capability. A significant amount of time was spent refining the new topology and implementing prototypes to determine practicality. This chapter details the background of this preregulator topology, theoretical insights and prototypes.

5.2 SCATMA: fast supercapacitor charger topology

Design of the new preregulator stage was inspired by the fast supercapacitor charger developed by the power electronics research group at the University of Waikato for the supercapacitor assisted temperature modification apparatus (SCATMA) [61, 62]. This section presents a summary of fast supercapacitor charger topology.

As depicted in Figure 5.1, the supercapacitors are partitioned into two identical banks with labels C1 and C2. The circuit is driven by rectified AC without smoothing. The first phase of the operation is depicted in Figure 5.2, where MOSFET sw is at the "on" conducting state. Since diode D is not conducting, the primary winding of the flyback converter accumulates energy, acting as an inductive voltage dropper in the supercapacitor C1 charging loop. Overcharging of the capacitor bank is avoided by monitoring the capacitor bank voltages. Then the during "off" state of sw, stored energy in the primary winding of the transformers transfers to capacitor bank C2 as diode D starts conducting similar to the operation of a flyback converter. This stage is depicted in Figure 5.3.

This design is a useful, practical instance of loss-minimisation similar to that discussed in Chapter 3, except that here the transformer coupled with a second SC bank provides the useful load. The converter was designed to operate at 20 kHz. This converter is ideal for high-power applications that use supercapacitor energy storage. This design can either reduce the time taken to charge the supercapacitor bank or it improve charging efficiency. The major achievement of the SCATMA fast charger is to reduce the charging time of the supercapacitor

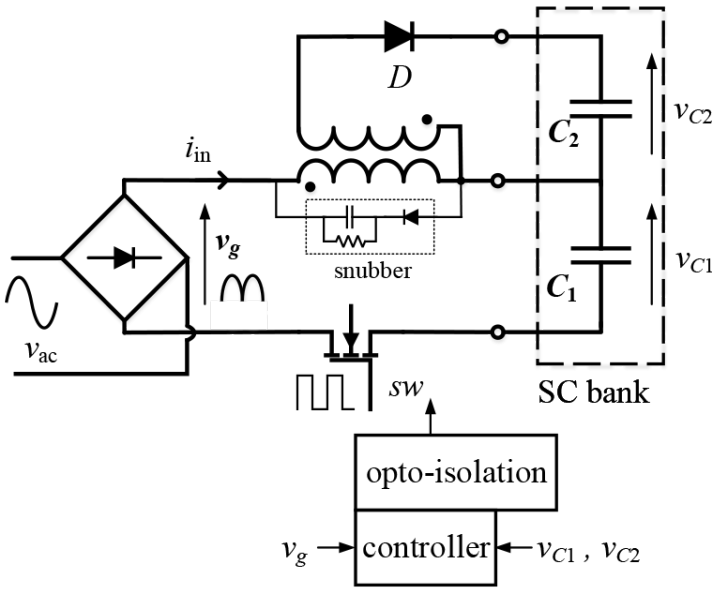


Figure 5.1: SCATMA: Energy-limited transient-mode fast supercapacitor charger topology [61]

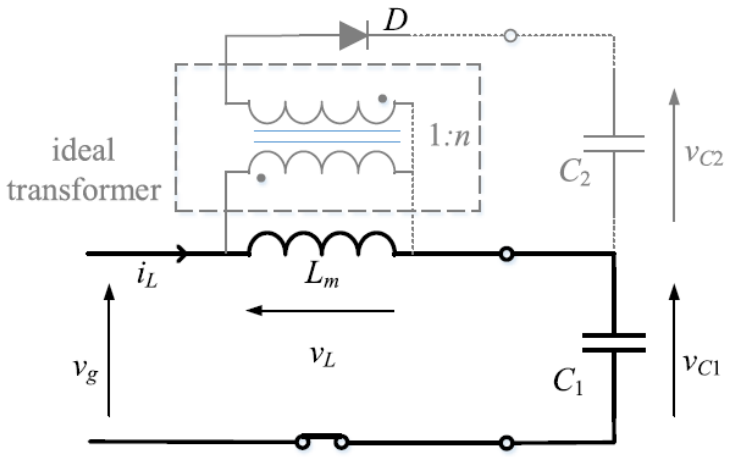


Figure 5.2: SCATMA fast charger: On state of the MOSFET [61]

bank by a significant factor. The converter does not require a bulky smoothing capacitor at the rectification stage [61, 62, 78, 79]. Potential applications include portable nail guns, hot water dispensers, high-efficiency water dispensers, sink-waste crushers and cargo-tow tractors.

The medium frequency preregulation stage for high power SCALDO was inspired by the SCATMA approach. Detailed theoretical arguments and some simulation work helped us identify the new power converter design at an early stages. However, we had to overcome several technical challenges to implement the topology and to scale up to a 10 A load current.

5.3 The topology of preregulator stage for SCALDO

The overall power converter solution is depicted in Figure 5.4. Details of the high current SCALDO were presented in the previous chapter. In developing a pre-regulation stage, the *RC* loop (power source side) can be further modified by inserting an ideal inductor as a lossless voltage dropper and energy storage element. In actual implementation, a fly-back transformer

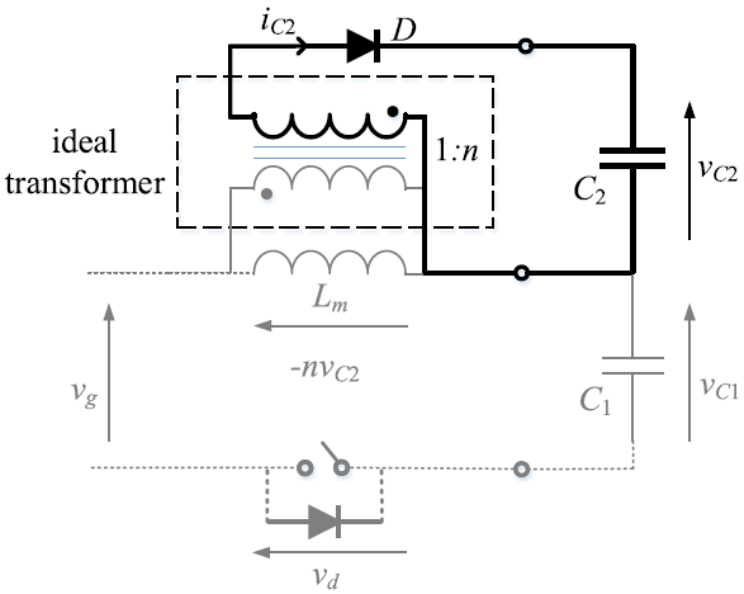


Figure 5.3: SCATMA fast charger: Off state of the MOSFET [61]

can be used instead of a simple inductor to isolate the output of the power converter from the input supply. When the design is applied to Google 48 V power supply, the pre-regulation stage is fed by 230 V rectified AC mains and produces 98 V DC at the output side, a suitable voltage for 48 V SCALDO as discussed in the previous chapter.

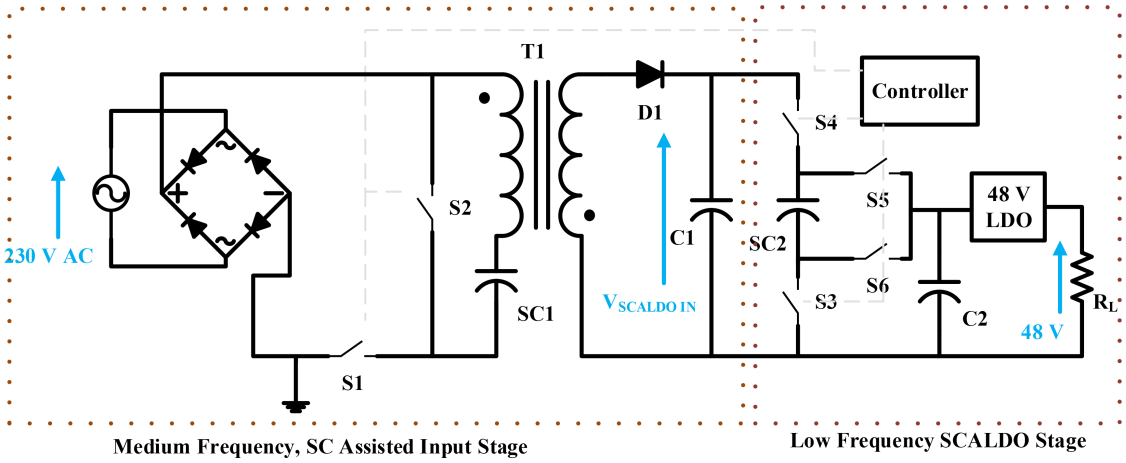


Figure 5.4: Overall power converter solution for 48 V Google server rack

As depicted in Figure 5.5 our new approach uses an enhanced version of SCATMA fast supercapacitor charger [61] to achieve 98 V at the secondary side with galvanic isolation. The output SCALDO stage is indicated as load resistance (R_L) here. In the **first phase** of operation, switch Q2 is kept open while switch Q1 switches at 20 kHz frequency. During the "on" period of Q1, the SC supercapacitor bank accumulates energy; this voltage must be monitored to avoid overcharging. As switch Q1 changes to its off state, energy stored in the primary winding is transferred to the secondary winding in fly-back mode. When SC voltage reaches its maximum value, the circuit is switched to its **second phase**, leaving Q1 open and switching Q2 at 20 kHz frequency. During the on time of switch Q2, energy stored in supercapacitor SC is transferred

to the secondary side in forward mode. During "off" time of switch Q2, energy stored in C1 electrolytic capacitor is transferred to load. When the voltage of SC drops below the threshold value, the circuit returns to its initial phase. These operating stages are summarised in Table 5.1. In the prototype, these switches are implemented with N-MOSFETs and pattern of operating MOSFET gates are shown in Figure 5.6. During each cycle of the operation, net $\int vdt$ of inductor and net $\int idt$ of the capacitors will be maintained at zero.

The benefits of the new power supply can be summarised as:

- the connected load always sees the DC output of a linear converter based on an LDO; this provides low-noise and higher current slew rate capability
- there is a high output load current capability due to the low ESR value of commercial SCs, which allows high charge/discharge current
- transformer isolation at the primary side
- short term DC-UPS capability [80]
- surge absorbent capability
- high ETEE
- low stress on switches
- simplicity compared with existing solutions

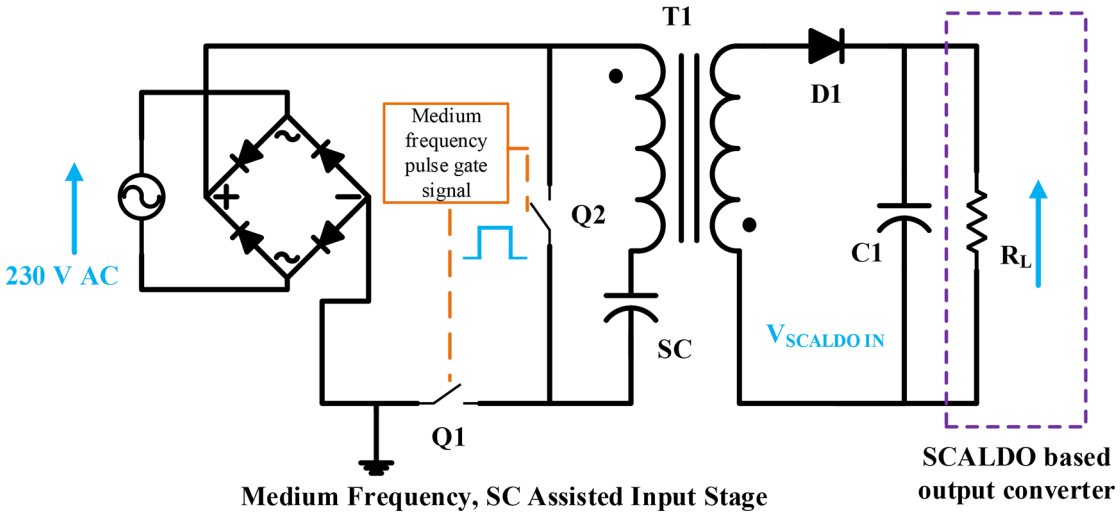


Figure 5.5: Preregulator stage: Topology

Table 5.1: Pre-regulation stage, summary of the operation

Phase	Q1	Q2	Description
Phase 1(flyback)	on (20 kHz)	off	SC charges via primary winding
	off (20 kHz)	off	transfer energy in flyback mode to secondary
Phase 2(forward)	off	on (20 kHz)	SC discharges to secondary in forward mode
	off	off (20 kHz)	C1 capacitor discharges to the load

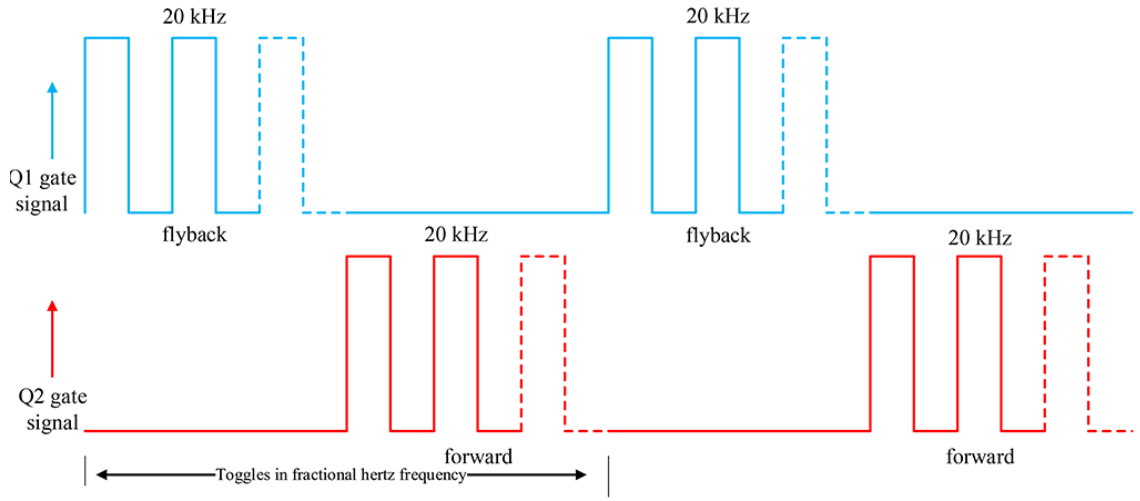


Figure 5.6: Pattern of operating Q1 and Q2 switches in new power converter topology

5.3.1 Analysis of phase 1: charging of SC via primary winding

Figure 5.7 depicts parasitic components in a non-ideal transformer such as leakage inductance l_{p}, winding resistance r_{p}, and core loss (R_{C}). These parasitic components are excluded from the analysis for simplicity. Figure 5.8(a) depicts the basic current flow of the converter during the on state of MOSFET Q1 and Figure 5.8(b) depicts the current flow during its off state. The Q1 switching waveform, voltage change across L_{m} (V_{LM}) and inductor current (I_{LM}) during the fly-back energy transmission stage are depicted in Figure 5.9. Magnetizing inductance is indicated as L_{m}. The turns ratio of the transformer is given by $n = \frac{N_{\mathrm{P}}}{N_{\mathrm{S}}}$ and V_{D} represents the forward voltage drop of the output diode. Supercapacitor voltage is assumed constant for one cycle.

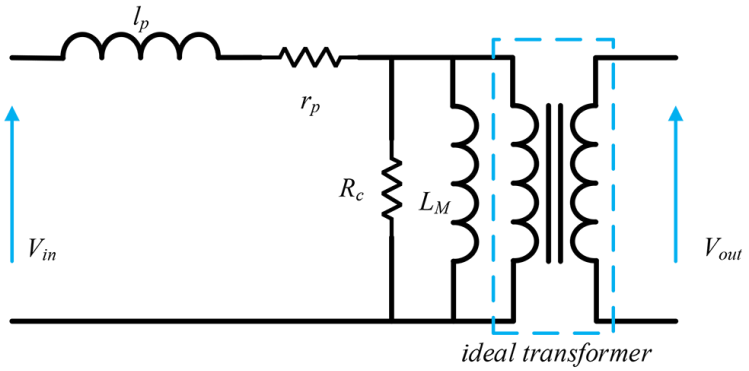


Figure 5.7: Simplified transformer model for flyback mode energy transmission

During the first sub-interval (0–t_{on}) where Figure 5.8(a) applies, the voltage across the inductor L_{m} is,

$$V_{\mathrm{LM}}(t) = V_{\mathrm{IN}}(t) - V_{\mathrm{SC}}(t) \tag{5.1}$$

During the second sub-interval (t_{on}–T_{S}) where Figure 5.8(b) applies, voltage across the inductor L_{M} is

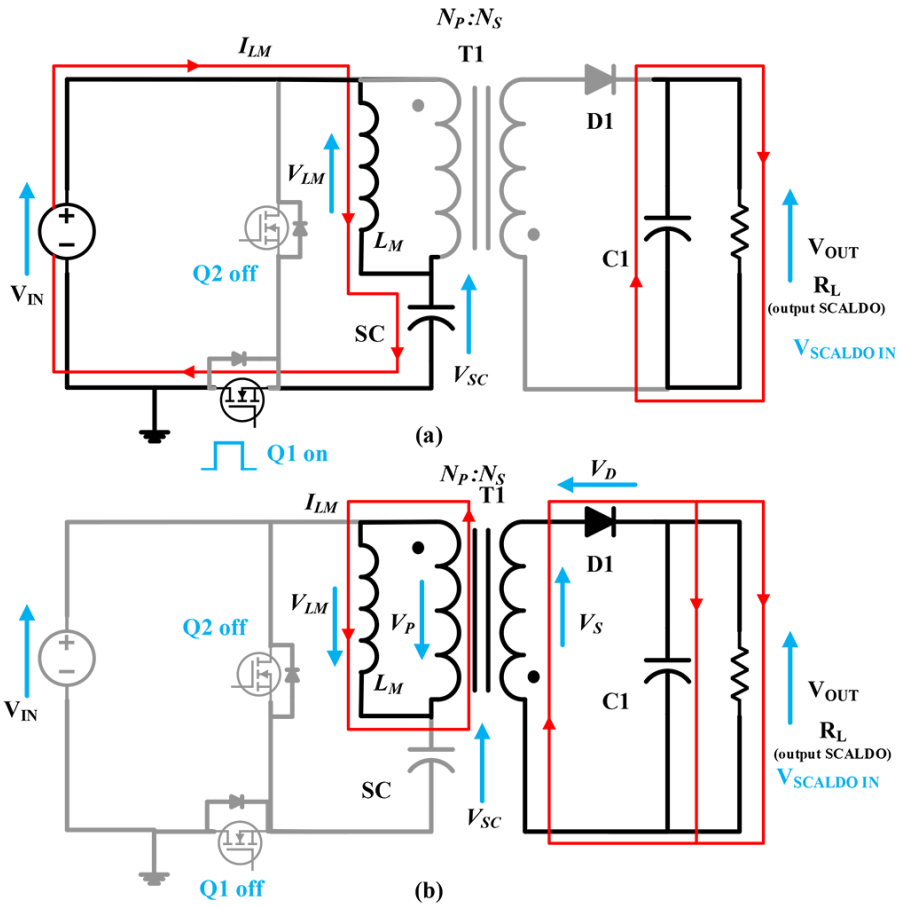


Figure 5.8: Phase 1: operation similar to a flyback converter (Q2 open, Q1 operates in medium frequency pulse): (a) Q1 on state; (b) Q1 off state

$$V_{\mathrm{LM}} = -n(V_{\mathrm{OUT}}(t) + V_{\mathrm{D}}) \tag{5.2}$$

From the definition of the inductor voltage,

$$V_{\mathrm{L}}(t) = L_{\mathrm{M}} \frac{di_{\mathrm{L}}(t)}{dt} \tag{5.3}$$

Figure 5.9 depicts the relevant waveform applicable to Figure 5.8.
Integrating this over one cycle $(0 - T_{\mathrm{S}})$

$$I_{\mathrm{LM}}(T_{\mathrm{S}}) - I_{\mathrm{LM}}(0) = \frac{1}{L_{\mathrm{M}}} \int_0^{T_{\mathrm{S}}} V_{\mathrm{LM}}(t)dt = 0$$

By applying the principle of volt-second balance to the inductor L_{M},

$$\big(V_{\mathrm{IN}}(t) - V_{\mathrm{SC}}(t)\big)t_{\mathrm{on}} + \big(-n\left(V_{\mathrm{out}}(t) + V_{\mathrm{D}}\right)\big)t_{\mathrm{off}} \quad = \quad 0$$

and substituting $t_{\mathrm{on}} = DT_{\mathrm{s}}$ and $t_{\mathrm{off}} = (1 - D)T_{\mathrm{s}}$, the duty cycle D can be derived as

$$D = \frac{t_{\mathrm{on}}}{t_{\mathrm{on}} + t_{\mathrm{off}}} = \frac{nV_{\mathrm{out}}(t) + nV_{\mathrm{D}}}{V_{\mathrm{in}}(t) - V_{\mathrm{SC}}(t) + nV_{\mathrm{out}}(t) + nV_{\mathrm{D}}} \tag{5.4}$$

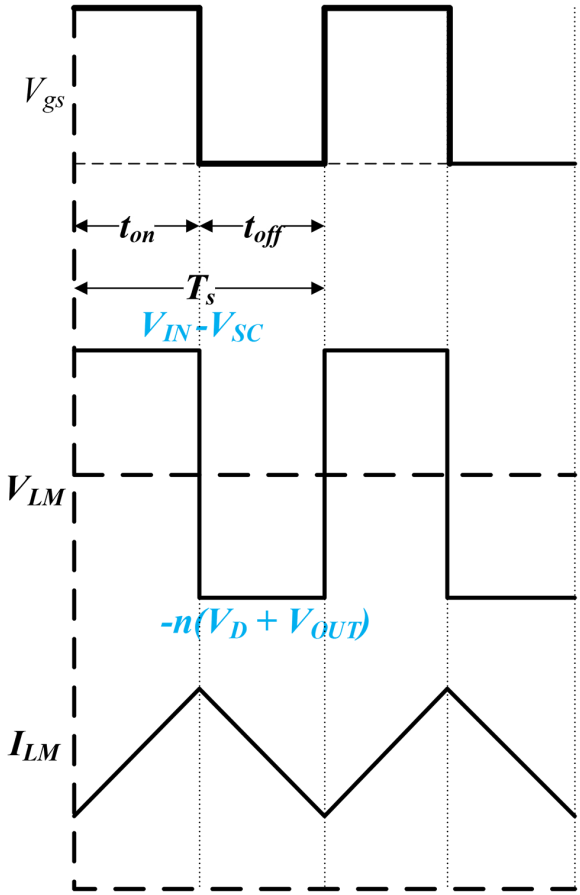


Figure 5.9: New power converter, waveform of the flyback mode operation

5.3.2 Analysis of phase 2: discharging of SC to secondary winding

The second phase of operation is depicted in Figure 5.10, where energy is transferred to the secondary side in forward mode. The transformer primary, secondary and output waveforms are shown in Figure 5.11. An equivalent circuit for the "on" and "off" states of MOSFETs are Q22 is depicted in Figure 5.12(a), and (b) respectively.

During the "on" state of MOSFET Q2, energy stored in the supercapacitor transfers to the load and to the buffer capacitor as depicted in Figure 5.12(a). Buffer capacitor (C1) voltage quickly reaches $\frac{V_{\mathrm{SC}}}{n} - V_{\mathrm{D}}$, since the capacitor charges under the parasitic resistance of the path including diode on resistance and the equivalent series resistance (ESR) of the capacitor (the time constant is very short as this resistance is in the order of milliohms).

During the "off" state of Q2, energy stored in the buffer capacitor pumps to the load as depicted in 5.12(b). However, this circuit's time constant is dominated by the load resistance which is very large compared to the charging phase. This explains the asymmetric shape of the output ripple voltage waveform depicted in Figure 5.11.

The load current I_{OUT} during the discharging phase is given by:

$$I_{\mathrm{OUT}}(t) = \frac{\left(\frac{V_{\mathrm{SC}}}{n} - V_{\mathrm{D}}\right) e^{-t/R_{\mathrm{L}}C1}}{R_{\mathrm{L}}} \tag{5.5}$$

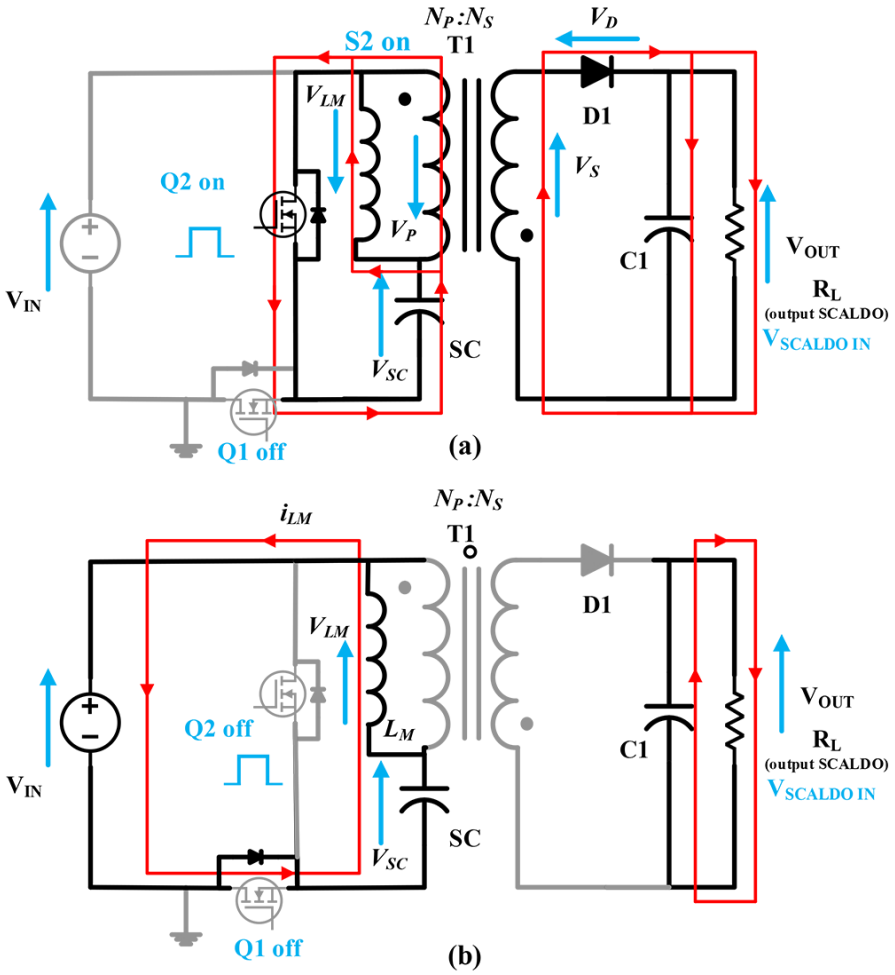


Figure 5.10: New topology, operation similar to forward-mode converter (Q1 open, Q2 operates in medium frequency pulse)

The integral of the current gives the charge in the capacitor (considering time interval t_{on} to T_{s}, which is equals to t_{off}):

$$\Delta Q = C1\Delta V_{\text{OUT}} = \int_0^{t_{\text{off}}} I_{\text{OUT}}(t)\,dt = \int_0^{t_{\text{off}}} \frac{1}{R_{\text{L}}}\left(\frac{V_{\text{SC}}}{n} - V_{\text{D}}\right) e^{-t/R_{\text{L}}C}\,dt \tag{5.6}$$

$$\Delta V_{\text{OUT}} = \left(\frac{V_{\text{SC}}}{n} - V_{\text{D}}\right)\left(1 - e^{\frac{-t_{\text{off}}}{R_{\text{L}}C1}}\right) \tag{5.7}$$

Substituting $t_{\text{off}} = \frac{1-D}{f_{\text{sw}}}$ in Equation (5.7), where D is the duty cycle and f_{sw} is the switching frequency of the converter,

$$\Delta V_{\text{OUT}} = \left(\frac{V_{\text{SC}}}{n} - V_{\text{D}}\right)\left(1 - e^{\frac{-(1-D)}{f_{\text{sw}}R_{\text{L}}C}}\right) \tag{5.8}$$

reverse voltage built in magnetising inductance (L_{M}) collapse due to the current flow through the body diode of Q1 as shown in Figure 5.10. By applying Kirchhoff's voltage law to the loop,

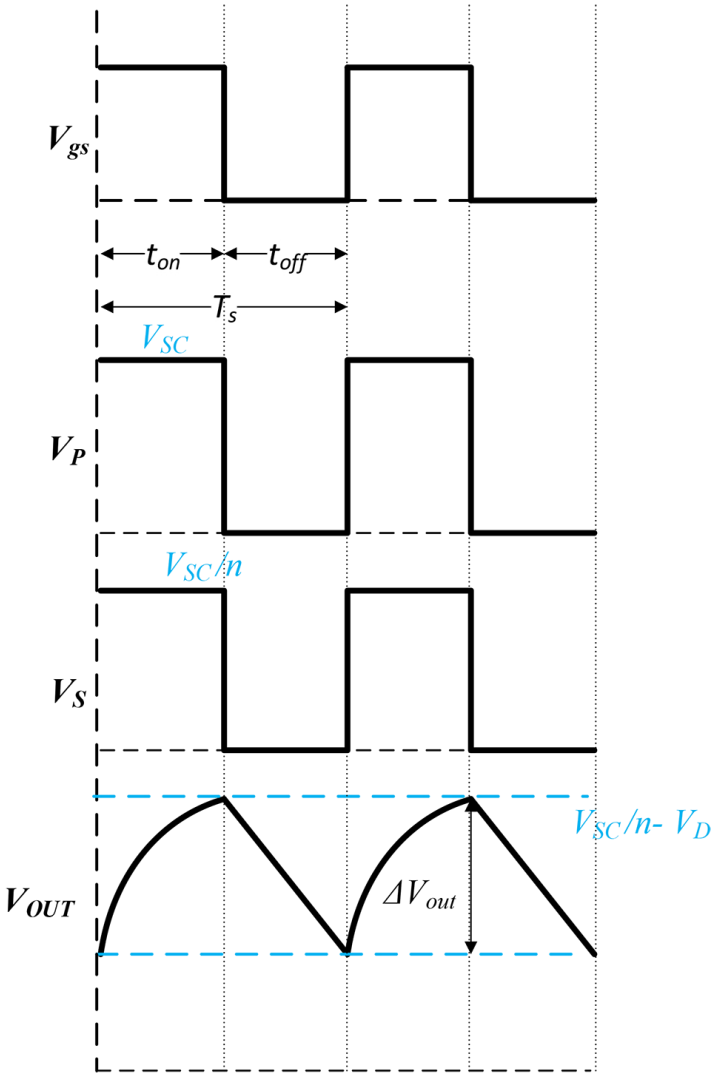


Figure 5.11: New topology, waveform of the forward-mode operation

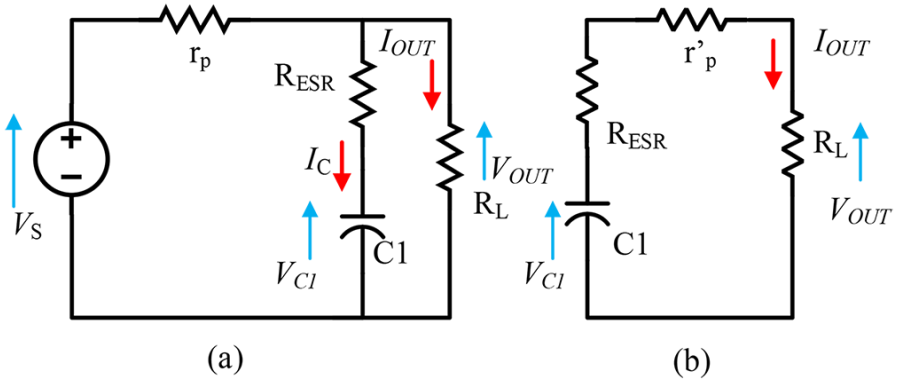


Figure 5.12: Equivalent circuits for forward-mode operation: (a) "on" state of Q2; (b) "of" state of Q2

$$
\begin{aligned}
V_{\mathrm{LM}} &= V_{\mathrm{IN}} - V_{\mathrm{SC}} \\
L_{\mathrm{M}} \frac{di_{\mathrm{LM}}}{dt} &= V_{\mathrm{IN}} - V_{\mathrm{SC}}
\end{aligned}
$$

Equation (5.8) is helpful to understand the impact of the output current, duty cycle, operating frequency, and capacitance of the output buffer capacitor on the ripple voltage, as shown in Figure 5.13 (output current is not shown here as output current is a function of the connected load).

In order to understand the behaviour of the buffer capacitor, standard values of electrolytic capacitors were considered, for the range C1 = 1000 μF to 10 000 μF, with 1000 μF being taken as the default value. With increasing capacity, electrolytic capacitors become bulkier and more expensive. We take 0.5 as the default value for the duty cycle, and in order to observe its effect, changed its value from 0 to 0.5. During each cycle, the transformer core should get enough time to demagnetise, and this provides a constraint for the duty cycle. 20 kHz is considered as the default value for the switching frequency considering the design parameters of the transformer, with frequency changes from 10 to 100 kHz were conducted to see the effect on the ripple voltage. Higher frequency operation creates electromagnetic interference issues in the converter, so a moderate frequency (20 kHz) was chosen for simulation and implementation. Further details of this issue are presented in the transformer design section.

By weighing all of these factors, the selected design parameters are listed in Table 5.2. The next section describes the LTspice and Simulink simulation models developed to verify this topology.

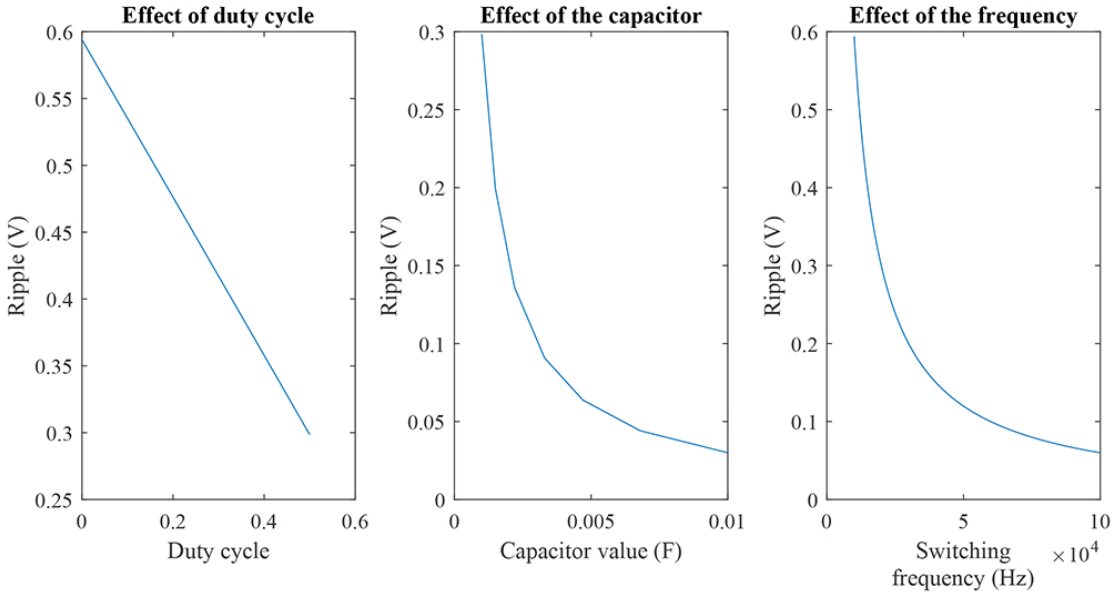


Figure 5.13: Forward mode operation: output ripple based on duty cycle, buffer capacitor and operating frequency

Table 5.2: Design parameters for pre-regulation stage

Parameter	Value
Duty cycle, D	0.5
Operating frequency, f_{sw}	20 kHz
Buffer capacitor, C1	2200 μF

5.4 Simulating the pre-regulator stage with MATLAB Simulink

Matlab Simulink is a powerful tool for electronics circuit simulations. To identify the converter's conceptual accuracy, Simulink based model was built at the early stage of the research, as shown in Figure 5.14. The controller circuit is depicted in Figure 5.15. Flexibility over model parameters and the ability to implement controller logic are some of the reasons that encouraged us to choose Simulink among other simulation software. The output voltage, output current, supercapacitor voltage, supercapacitor current and V_{DS} waveform for forward and flyback MOSFETs are shown in Figure 5.16, and zoomed flyback mode waveforms are shown in Figure 5.17 while zoomed forward mode waveforms are shown in Figure 5.18. Detailed model parameters are presented in Appendix B. Since the model is not related to the existing converter technique, this model is also a creative output of the research and significant effort put into developing the model. When the model parameters are substitute to Equation 5.8,

$$\begin{aligned}\Delta V_{\mathrm{OUT}} &= \left(\frac{V_{\mathrm{SC}}}{n} - V_{\mathrm{D}}\right)\left(1 - e^{\frac{-(1-D)}{f_{\mathrm{sw}} R_{\mathrm{L}} C}}\right) \\ &= \left(\frac{40}{0.81} - 0.25\right)\left(1 - e^{\frac{-(1-0.5)}{20000\times 2.6\times 4400\times 10^{-6}}}\right) \\ &= 0.106\end{aligned}$$

For the model turns ratio of the transformer = 0.81, forward voltage drop of the diode = 0.25 V, operating frequency = 20 kHz, capacitor connected 4400 μF and load resistance is 2.6 Ω. Here we have assumed SC voltage is fixed and equals to 40 V; the duty cycle is fixed to 0.5%. Then from the equation we get ripple voltage of 0.107 V, which is comparable with ripple appeared in forward mode voltage waveform in Figure 5.18.

The next section details the transformer design process for the power converter.

5.5 Transformer design

Transformer design was one of the fundamental challenges of the new power converter topology. The new topology was not conventional as the current circulates in both directions in the primary winding. Flyback mode operation is mainly considered for the transformer design, as a low current prototype implementation helped to verify the feasibility of using the same transformer for forward operation. This section discusses the important considerations of the transformer design process and presents design details of transformers suitable for the low-power prototype and for a second design scaled for 1 kW, 48 V Google power supply.

5.5.1 Frequency of operation

This circuit topology is based on a medium to high-frequency (20 kHz) isolation transformer. The size of the transformer can be decoupled from the power rating requirement since the core size and number of turns required per volt is inversely proportional to the frequency of operation. Depending on the volume restrictions within a rack-power supply, the input conversion stage's switching frequency can be adjusted. The general impact of frequency is shown in Figure

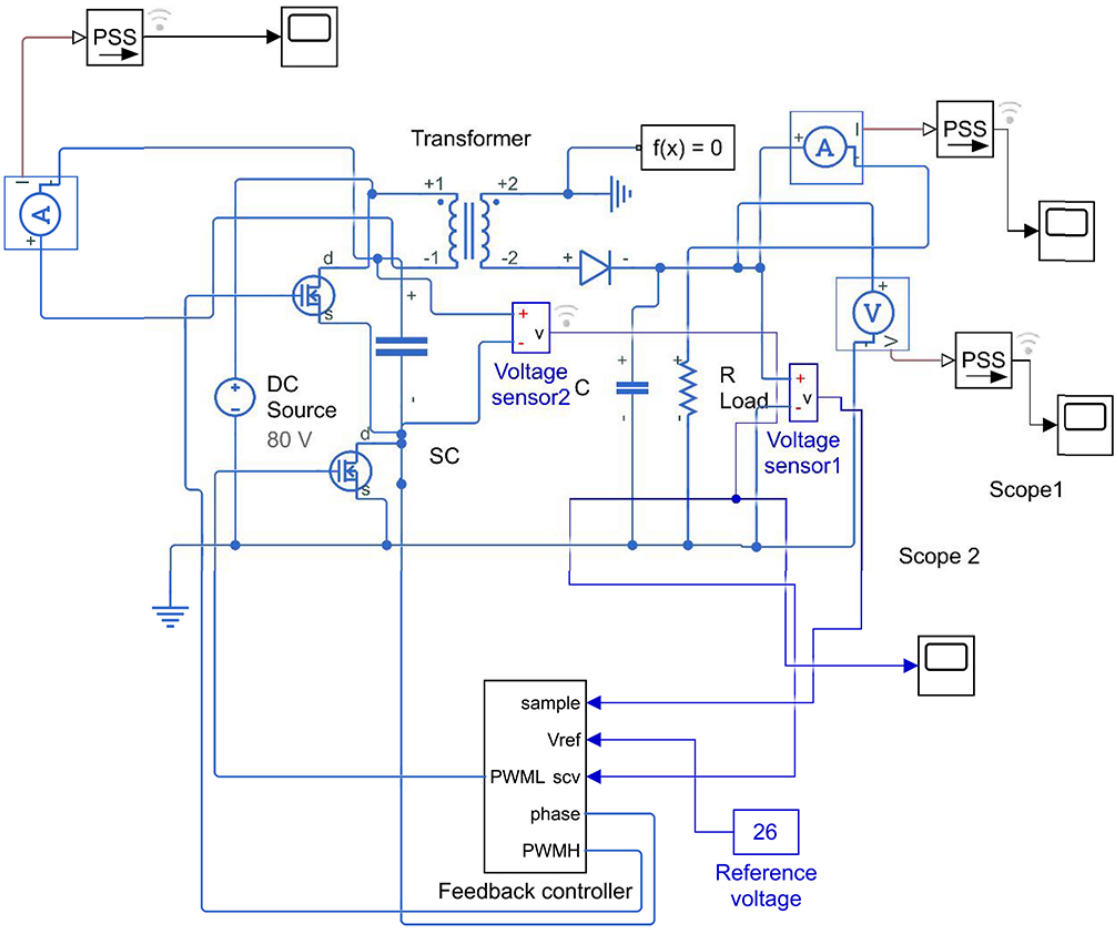


Figure 5.14: MATLAB Simulink model of pre-regulation stage

5.19: winding loss is higher at lower frequencies, while core loss is higher at higher frequencies. The output ripple of the power supply can be reduced by increasing the converter's operating frequency according to the analysis conducted in the previous section, and enabling reduction of the size of the output capacitor. Small capacitors and inductors mean a reduction in the total cost of the design. However, the electromagnetic interference (EMI) of a switching regulator is proportional to the square of the switching frequency so moving to a higher frequency significantly increases EMI issues.

Figure 5.20 shows the maximum flux density of ferrite K, F, P, and R materials against frequency at room temperature, where higher flux density is recorded at frequencies close to 20 kHz.

In addition to the operating frequency, there were several other parameters to be considered in the transformer design, including core material, geometry and size, maximum peak power density, primary and secondary winding ratios, number of turns, wire gauge and air gap necessary to prevent core saturation [81]. Magnetics product catalogues and transformer design guides and SCATMA: fast charger flyback transformer design materials were used for transformer design.

5.5.2 Core material and core geometry selection

Ferrite is an ideal core material for transformers, inverters, and inductors in the frequency range of 20 kHz to 3 MHz due to low core cost and low core losses. Ferrite cores can also be used

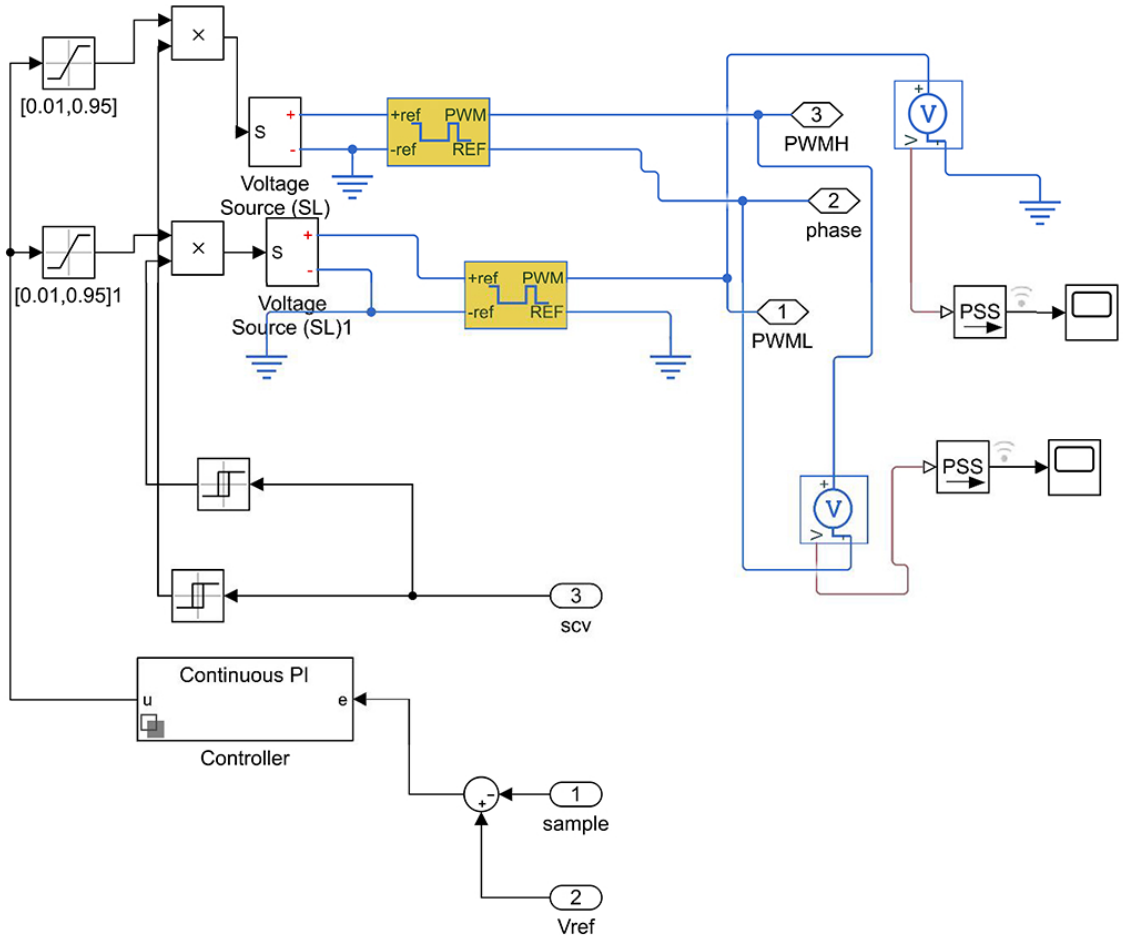


Figure 5.15: MATLAB Simulink controller circuit

in flyback transformer, providing high voltage capability. Powder cores (MPP, High Flux, Kool Mμ and XFLUX) offer soft saturation, higher magnetic flux density, and better temperature stability [84].

Different ferrite materials have optimum core loss performance in over particular ranges of temperatures as shown in Figure 5.21. P materials have better core loss performance from 25 to 120 °C. Also, P material provides the lowest core loss for frequencies up to 500 kHz, and is readily available in many sizes [84]. For these reasons, a ferrite P material core was selected for the two transformer designs discussed in this thesis.

Different transformer core geometries are illustrated in Figure 5.22. Pot cores are ideal in a location where shielding winding from EMI noise is a primary concern. round slab (RS), double slab (DS), and RM cores are a version of the pot core with an additional opening for larger wires to be accommodated and assist in removing heat from the assembly. These cores require 40% less space for mounting compared to pot cores. PQ cores are specifically designed for switched-mode power supplies. Power output, inductance and winding area are maximised while minimising core weight, volume and PCB footprint. Compared to other core geometries, PQ cores tend to operate with fewer hots spots because of their uniform cross-sectional area. EC, ETD and EER cores combine the advantages of E cores and pot cores. The wide openings on each side of the core provide ample space for the large wires used in low voltage switch-mode power supplies while improving air circulation around the core. The round shape of the core

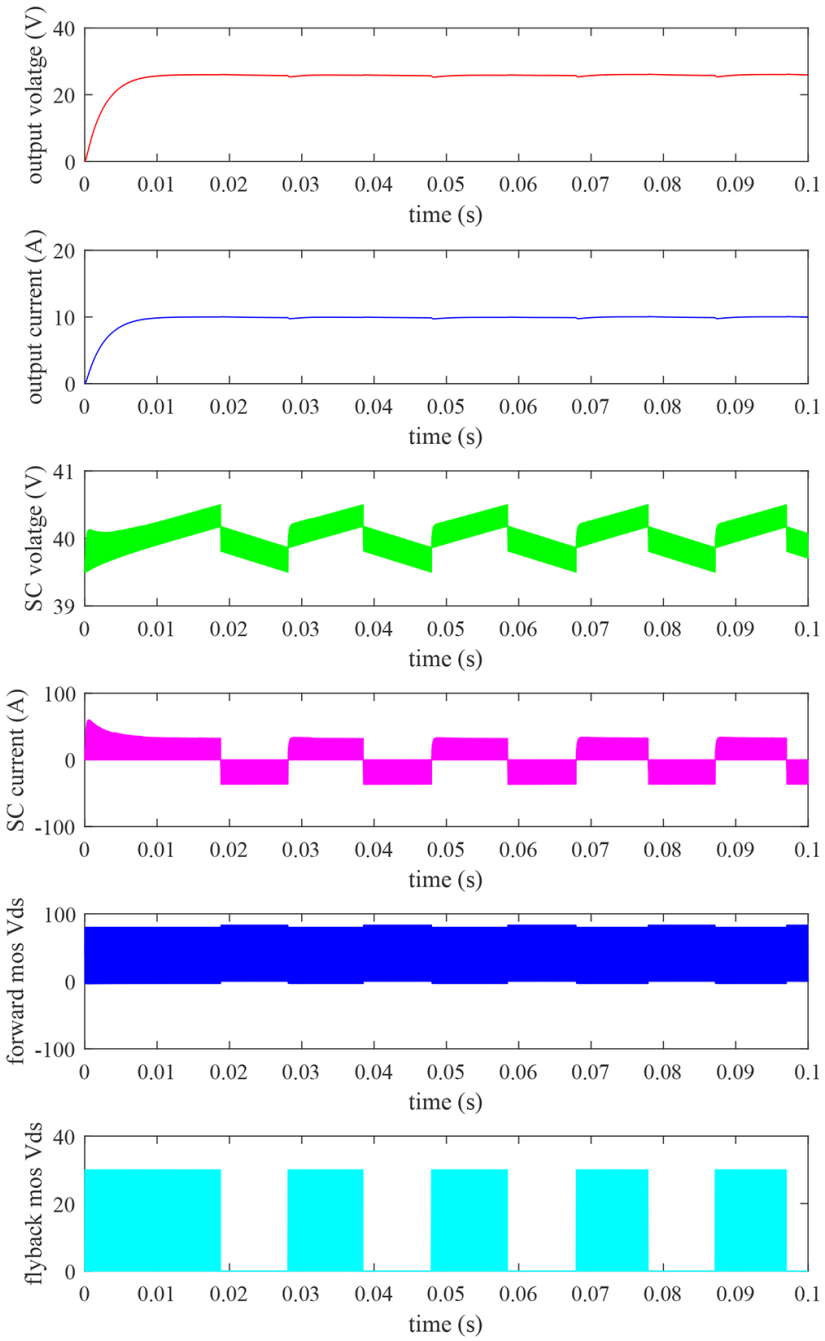


Figure 5.16: Data obtained from MATLAB simulink model (pre-regulation stage)

reduces the path length of the coils and reduces winding costs by 11%, thus reducing winding loss by 11%. A round centre post also eliminates the sharp bending in the wires that occurs with windings on a square centre post. EP cores are round centre-post cubical shaped with excellent shielding from EMI. This core design uses its volume effectively and saves space. The main advantages of E, and ER cores are simple bobbin winding, ease of assembly, availability of sizes and low cost making them an excellent choice for applications that do not require RMI shielding. planer E cores provide excellent thermal characteristics, economical assembly, low leakage inductance, and higher consistency. Toroid cores are the least expensive cores and are available in a variety of sizes. They also have good self-shielding properties. These cores are

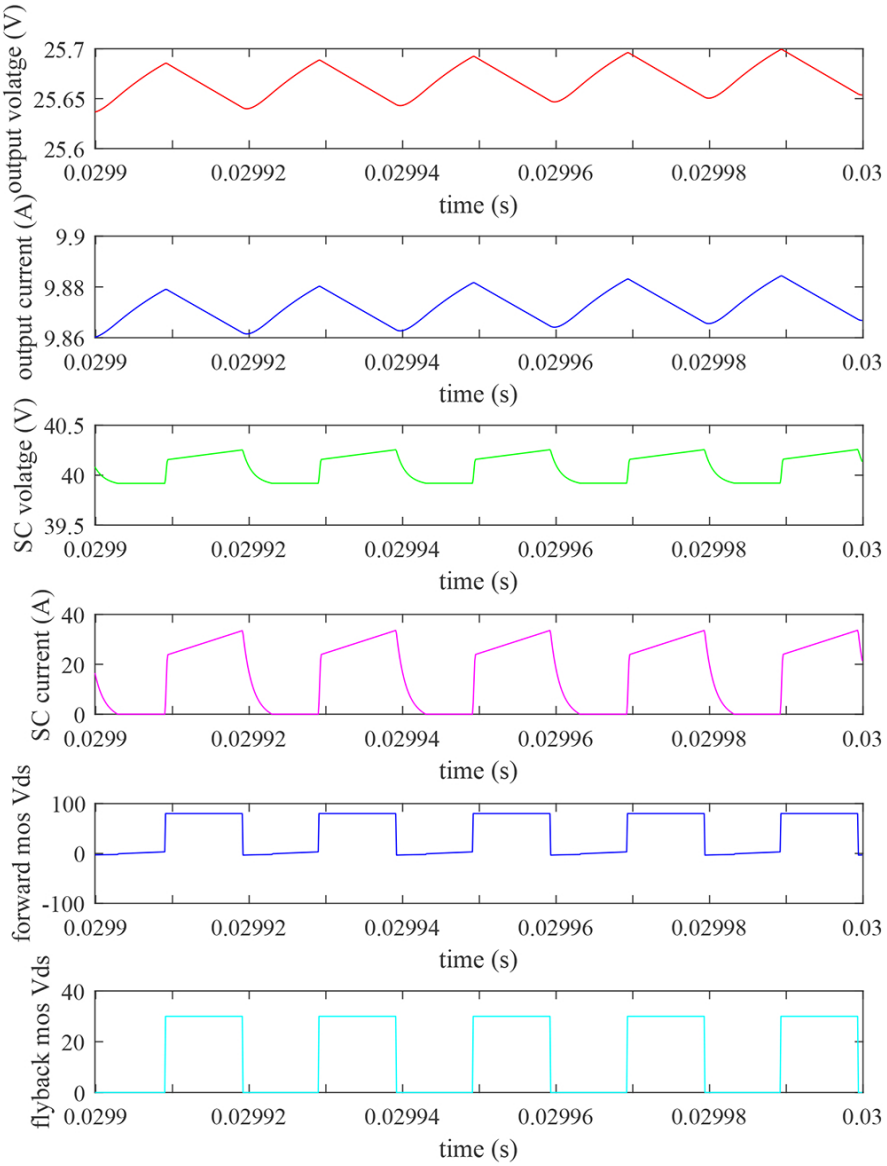


Figure 5.17: Data obtained from Simulink model: flyback mode operation

ideal for high vibration-environments [84].

An ETD core is used for the prototype developed in this study as they are an ideal choice for SMPS, have good thermal characteristics, are low-cost and easily assembled. ETD cores are an economical choice for power transformer design due to their round centre post, which minimises the length of copper cable required. The transformer can be designed with minimum winding resistance and copper loss. Considering the strengths of each of the core geometries, an ETD core was used for the pre-regulator prototype and for the 1 kW transformer design.

Transformer design specifications

This section describes the design process for the two transformers discussed in this thesis. Magnetics transformer design materials and references [85] were used for the transformer design. Design specifications of the two transformers are shown in Table 5.3. Above 20 kHz, core loss increases for ferrite core, and the flux level should be kept within ±2 kG [84]. 20 kHz was

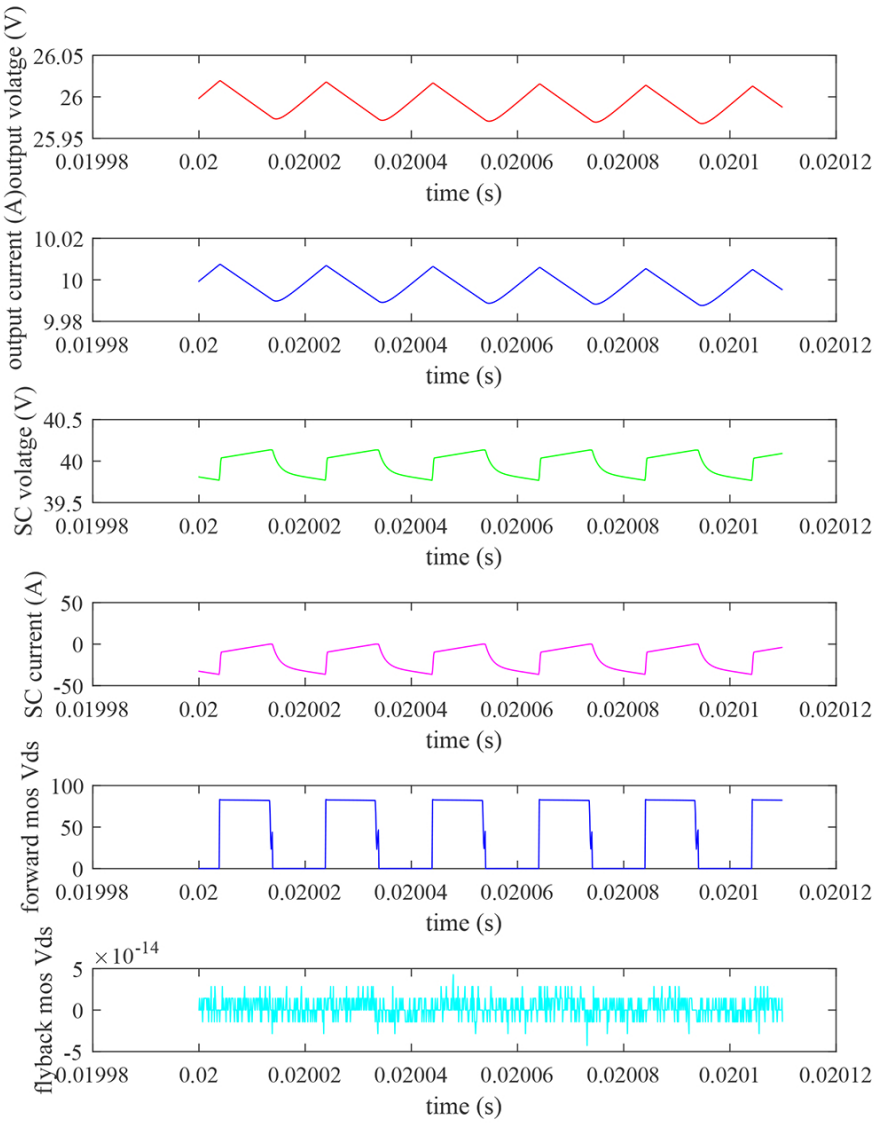


Figure 5.18: Data obtained from Simulink model: forward mode operation

Table 5.3: Pre-regulator stage: transformer specifications

Property	Transformer 1	Transformer 2
Output Power	1kW	260 W
Maximum input voltage	325 V DC	80 V DC
Average voltage across primary winding	162.5 V DC	40 V DC
Output voltage	100 V DC	26 V DC

chosen as the minimum frequency to minimize core loss and maximize flux density. According to [84] the maximum usable flux density in this frequency is 2000 G, and as the transformer is operated at the first half of the B-H curve, the maximum flux density is considered as 1000 G. The magnetic core can be selected based on power handling capability or the $W_a A_c$ product where W_a is the winding area of the core,

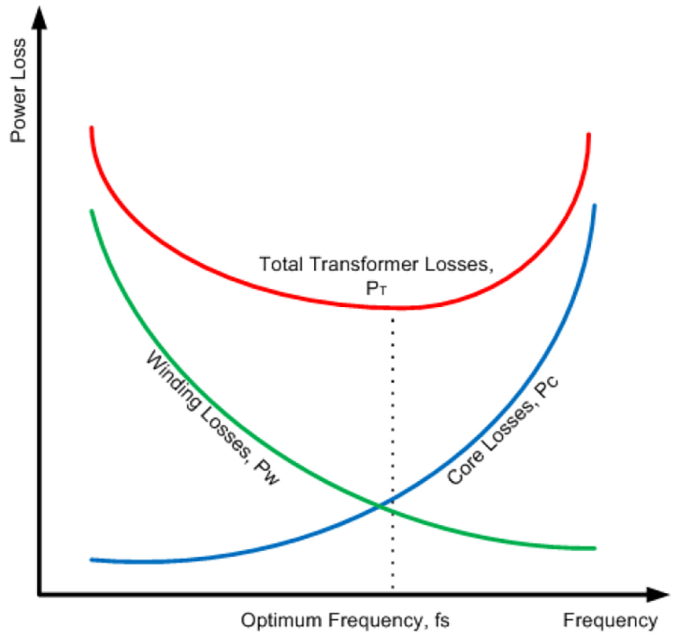


Figure 5.19: Principle for determining the optimum frequency of a transformer at a given flux density [82]

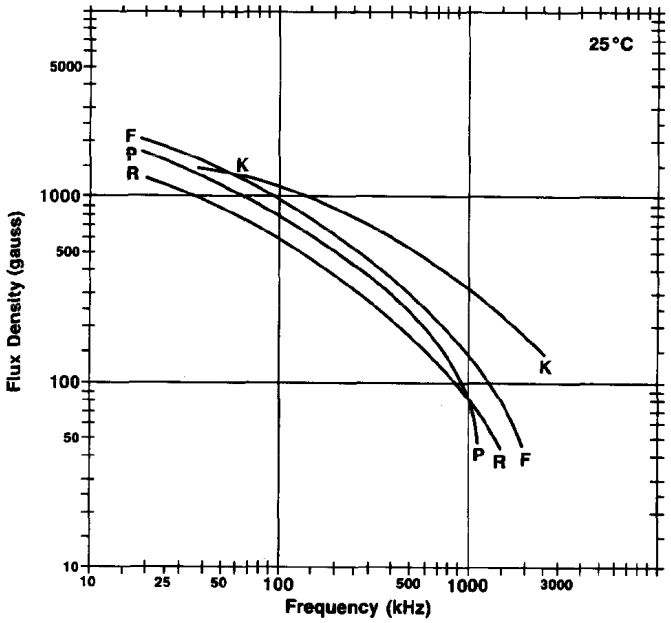


Figure 5.20: Flux density vs. frequency curve for ferrite material cores [83]

$$W_{\mathrm{a}}A_{\mathrm{c}} = \frac{P_{\mathrm{in}}C_{\mathrm{w}} \times 10^{8}}{4BfK} \tag{5.9}$$

Where f represents operating frequncy, B is the maximum flux density, P_{in} is the input power of the transformer and C_{W} is the current capacity of the wires. For square wave excitation and E cores this constant is $C_{\mathrm{W}} = 5.07 \times 10^{-}3$ cm^2/A and for the core the winding factor is $K = 0.7$ [85]. For a 1 kW transformer, the W_aA_c product can be calculated as 10.178 cm^4. The transformer core $45959ETD$ was selected from the Magnetics® Ferrite core material catalogue. For the core, the inductance per turn $A_{\mathrm{L}} = 6240$ nH/T, the $W_{\mathrm{a}}A_{\mathrm{c}}$ product is 14 cm^4, the area

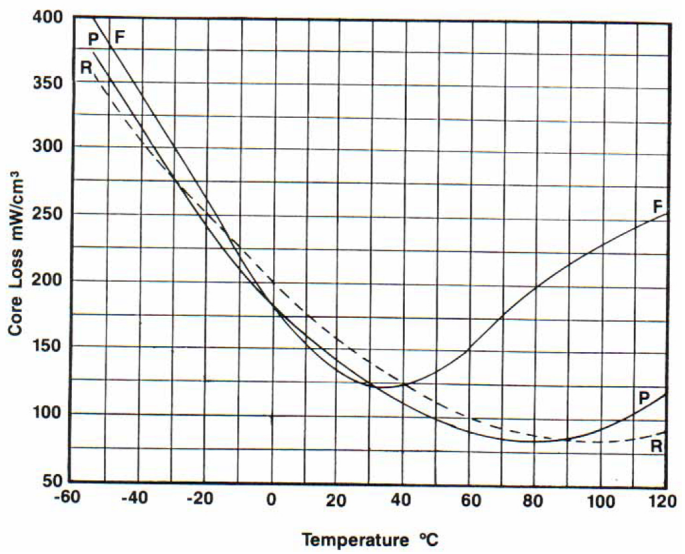


Figure 5.21: Flux density vs. temperature curve for ferrite material cores [83]

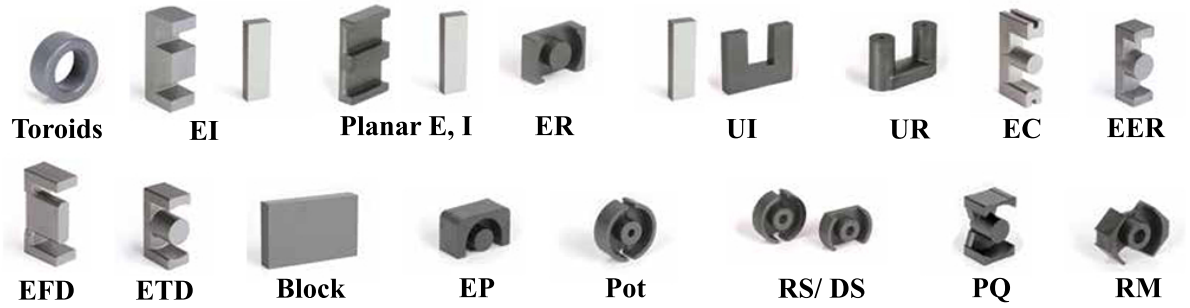


Figure 5.22: Ferrite core geometries from Magnetics ferrite core catalogue 2017

of the core $A_c = 3.68$ cm^2 and path length $L_e = 13.9$ cm. Same oversized core is chosen for 260 W prototype considering the design flexibility and higher power handling capability.

These parameters can be used to calculate number of turns in the primary winding as shown in Equation 5.10.

$$N_p = \frac{V \times 10^8}{4BA_c f} \tag{5.10}$$

Where V represents the primary winding voltage. A maximum DC voltage of 325 V (230 V_{rms}) was considered for the calculation. After substituting these values the number of turns in the primary winding N_P was calculated as 78 turns. For the 260 W prototype the value $N_P = 27$.

In order to decide the number of turns in the secondary winding, the average voltage of primary winding (V_P) is equal to 162 V. The expected voltage at the secondary winding (V_S) is 100 V. Based on these values the number of turns in secondary winding N_s can be calculated using transformer equation,

$$\frac{N_P}{N_S} = \frac{V_P}{V_S} \tag{5.11}$$

giving $N_{\mathrm{S}} = 48$ turns. For the 260 W prototype terns ratio is kept at 1 to have a range of input voltage ($60 - 80$ V). When the supercapacitor is charged up to (30) half of the minimum input voltage (60 V) the flyback mode operation reduces to $30 - 26$ V converter.

Then the thickness of the wire can be obtained,

$$KW_{\mathrm{a}} = N_{\mathrm{p}} A_{\mathrm{wp}} + N_{\mathrm{s}} A_{\mathrm{ws}} \tag{5.12}$$

where K is the winding factor, A_{wp} is the cross-sectional area of wire used in the primary winding and A_{ws} is the cross-sectional area of wire used for the secondary winding. Here $W_{\mathrm{a}} = W_{\mathrm{a}} A_{\mathrm{c}}/A_{\mathrm{c}} = 380$ mm^2. The same copper wire thickness can be used for both windings, and this thickness can be calculated as 2.1 mm^2. By referring to the wire gauge charts, 14 AWG wire with cross-sectional area 2.08 mm^2 and diameter 1.63 mm can be used for both primary and secondary windings for the 1 kW design. For the 260 W prototype, wire thickness is 11 AWG where cross-sectional area 4.17 mm^2 and diameter 2.31 mm.

When a conductor carries alternating current, the current density towards the surface of the conductor tends to increase, and this reduces the effective cross-section area for current flow. This is called skin-effect, and is a secondary cause for power loss in a transformer. This can be minimised by introducing multiple strings of copper wire in the transformer winding. According to [85], the skin depth of copper at 20 kHz frequency is 0.46 mm, and the minimum diameter of wire that should be maintained is 1 mm. Therefore multiple strings of 18 AWG (1.02 mm diameter) wires should be used for winding. Then for the 1 kW transformer design number of strings can be selected as 2 ($A_{\omega} = mA'_{\omega}$, where m represents the number of strings, A_{ω}, A_{ω} represents cross-section area of the wire old and new). For the 260 W transformer, four 18 AWG wires can be used, and this will be an aggressive choice. However, four strings will give ample time for the transformer to cool in between cycles.

The converter transformer is used for both normal transformer action and energy storage, but this dual-use requires that the transformer not be saturated. The core reluctance can be increased by introducing an air gap, and the current can be controlled. Air gap L_{g} can be calculated from,

$$L_{\mathrm{g}} = \frac{0.4\pi N_{\mathrm{P}}^2 A_{\mathrm{c}}}{100 L_{\mathrm{m}}} - \frac{L_{\mathrm{e}}}{\mu_{\mathrm{r}}} \tag{5.13}$$

Where the μ_{r} is the relative permeability of the ferrite core,

$$\mu_{\mathrm{r}} = \frac{A_{\mathrm{L}} L_{\mathrm{e}}}{0.4\pi A_{\mathrm{c}} \times 10} \tag{5.14}$$

For the core chosen calculated $\mu_{\mathrm{r}} = 1875.6$. In order to decide maximum ratings of the transformer peak current $I_{\mathrm{P}}^{\max}$ and voltage across primary winding $V_P^{\max}$, forward and flyback modes are considered separately. Maximum primary inductance ($L_{\mathrm{m}}^{\max}$) of the converter can be calculated using Equation (5.16), is derived from (5.15).

$$L_{\mathrm{m}} = v_p \frac{D}{f_{\mathrm{s}} \Delta i_{\mathrm{P}}} \tag{5.15}$$

$$L_{\mathrm{m}}^{\max} = V_{\mathrm{P}}^{\max} \frac{D}{f_{\mathrm{s}}^{\min} I_{\mathrm{P}}^{\max}} \tag{5.16}$$

where $f_{\mathrm{s}}^{\min}$ is the minimum frequency of the transformer. Consider duty cycle $D = 0.5$ as general point for calculation. By applying the definition of root mean square value for flyback current waveform (triangular waveform), the maximum value $I_{\mathrm{P}}^{\max}$ can be calculated,

$$I_{\mathrm{P}}^{\mathrm{rms}} = \sqrt{\frac{1}{T_{\mathrm{s}}} \int_0^{T_{\mathrm{s}}} i_{\mathrm{P}}(t) dt} = \frac{1}{\sqrt{6}} I_{\mathrm{P}}^{\max} \tag{5.17}$$

giving $I_{\mathrm{P}}^{\max} = \sqrt{6} I_{\mathrm{P}}^{\mathrm{rms}} = \sqrt{6} \times 1 \text{ kW}/ 230 \text{ V} = 10.6 \text{ A}$.

For forward mode operation, maximum voltage of the transformer will not exceed 170 V and maximum current will be high compared to flyback converter considering flyback energy transmission is sufficient to decide maximum inductance of the transformer. For maximum $V_P^{\max} = 325V$, $\Delta i_{\mathrm{P}} = i_{\mathrm{P}}^{\max} = 10.65\text{A}$. Then $L_{\mathrm{m}}^{\max}$ will be 331.9 μH. Hence the air gap is calculated as $L_{\mathrm{g}} = 0.84$ mm. This air gap can be achieved introducing insulating material to the centre of transformer. For 260 W transformer $L_{\mathrm{m}}^{\max}$ will be 200 μH, and the air gap is calculated as $L_{\mathrm{g}} = 0.16$ mm. Design details of the 1 kW and 260 W transformers are shown in Table 5.4; and picture of the prototype transformer design is shown in Figure 5.23.

5.5.3 Transformer measurements

Uncoupled inductance in the transformer cause for voltage spikes in the primary side switching. Parameters shown in Figure 5.24 were obtained to measure leakage inductance (l_p), mutual inductance M, and coupling coefficient k of the transformer as indicated in the text. In Figure 5.24(a) represents primary inductance ($L1$), Figure 5.24(b) is the secondary inductance ($L2$),

Table 5.4: Pre-regulator stage: transformer design parameters

Property	T1 (1 kW)	T2 (250 W)
Frequency range	$20 - 200$ kHz	$20 - 200$ kHz
Magnetic Inc. part number	ETD 59	ETD 59
Magnetic material Type	P	P
Core shape	ETD	ETD
Maximum primary inductance	331.9 μH	200 μH
Area product ($A_{\mathrm{c}}W_{\mathrm{a}}$)	3.68 cm^4	3.68 cm^4
Inductance factor (A_{L})	6240 nH/T	6240 nH/T
Effective path length (L_{e})	13.9 cm	13.9 cm
Effective cross sectional Area (A_{c})	3.68 cm^2	3.68 cm^2
Primary turns (N_{P})	78	27
Secondary turns (N_{S})	48	27
Wire gauge	18 AWG	18 AWG
Airgap length at centre	0.84 mm	0.16 mm

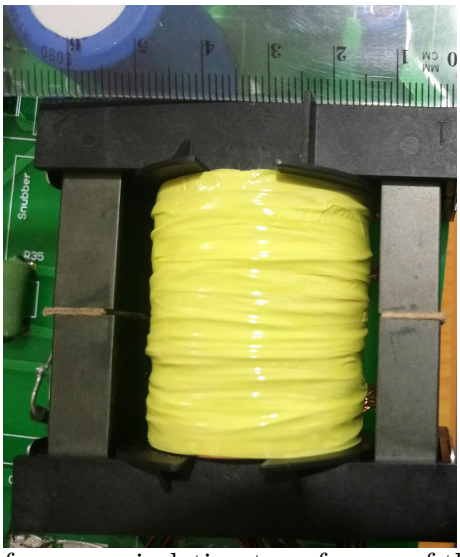


Figure 5.23: Medium-frequency isolation transformer of the pre-regulator stage

Figure 5.24(c) gives the leakage inductance (l_{p}) and Figure 5.24 (d) and (e) represents series connection inductance (L_{a}) and inverse series inductance (L_{b}) in order. The measurements were obtained using *RLC* meter at the operating frequency 20 kHz.

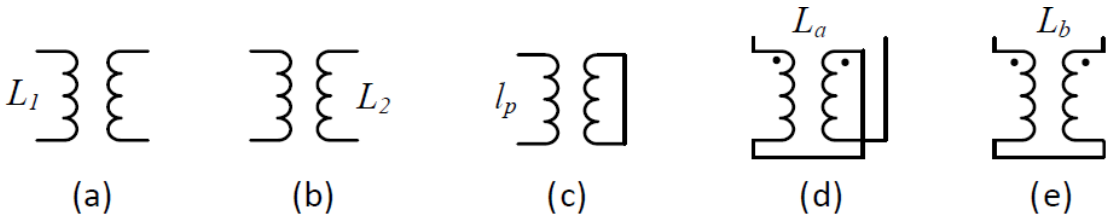


Figure 5.24: Transformer parameters of pre-regulator stage: (a) primary inductance; (b) secondary inductance; (c) leakage inductance; (d) series connection inductance; (e) inverse series connection inductance [85]

The series connection inductances $L_{\mathrm{a}}, L_{\mathrm{b}}$ can be written as [85],

$$L_{\mathrm{a}} = L_1 + L_2 + 2M \tag{5.18}$$

$$L_{\mathrm{b}} = L_1 + L_2 - 2M \tag{5.19}$$

$$\tag{5.20}$$

solving these two equations, for summed and mutual inductances,

$$L_1 + L_2 = \frac{L_{\mathrm{a}} + L_{\mathrm{b}}}{2} \tag{5.21}$$

$$M = \frac{L_{\mathrm{a}} - L_{\mathrm{b}}}{4} \tag{5.22}$$

The RLC meter readings are listed in Table 5.5.
mutual inductance M can be calculated as:

$$M = \frac{990.51 - 5.51}{4} = 246.25\ \mu\mathrm{H} \tag{5.23}$$

Table 5.5: pre-regulator stage, transformer measurements

Parameter	Value μH
Primary inductance (L_1)	220.68
Secondary inductance (L_2)	276
Leakage inductance (l_p)	2.06
Series inductance (L_a)	990.51
Inverse series inductance (L_b)	5.51

coupling coefficient k can be calculated as:

$$k = \sqrt{\frac{M^2}{L_1 L_2}} = \sqrt{\frac{246.25^2}{220.68 \times 276}} = 0.998 \tag{5.24}$$

$$\tag{5.25}$$

Implementation details of the converter prototype are presented in next section.

5.6 Circuit implementation

5.6.1 Driving MOSFETSs

At the initial stage of the prototype implementation, an IR2183 driver IC is used to drive floating ground MOSFET. Schematic of the implementation is shown in Figure 5.25 and the circuit board is shown in Figure 5.26. Standard half-bridge driver circuit turns on and off high side MOSFET and low side MOSFET in individual cycles, replenishing the bootstrap capacitor during each cycle. Gate pulse for the high-side of the MOSFET generated from the voltage of bootstrap capacitor. However, in the proposed design, the converter operated high-side MOSFET after a few low-side MOSFET operation cycles. The typical electrolytic capacitor could not sustain voltage for long to operate high-side MOSFET in this configuration. As a solution to this problem, a small supercapacitor is introduced as a bootstrap capacitor for the driver IR2183. This implementation could handle a load current up to about 2 A. Although a supercapacitor can hold power for longer, it takes longer to replenish the capacitor. This issue reduces the flexibility of forward and flyback mode phase transitions. As a solution to this transformer-isolated gate driver technique also investigated.

Transformer isolated gate drivers are ideal for high-frequency high voltage applications. This approach is shown in Figure 5.27. However, fast and accurate signal timing is required. DC voltages developed in the winding can cause the transformer to saturate, and high current circulation can damage the controller circuit. The main advantage of the circuit is the ability to generate a higher voltage gate signal from a low voltage controller signal. This can be achieved by adjusting the turns ratio of the gate driver transformer. This approach was tested on the new power converter but was not successful, as unwanted oscillations were introduced into the circuit. These noises created significant issues at higher loads, generating heat in the main isolation transformer and creating voltage spikes in the gate signal.

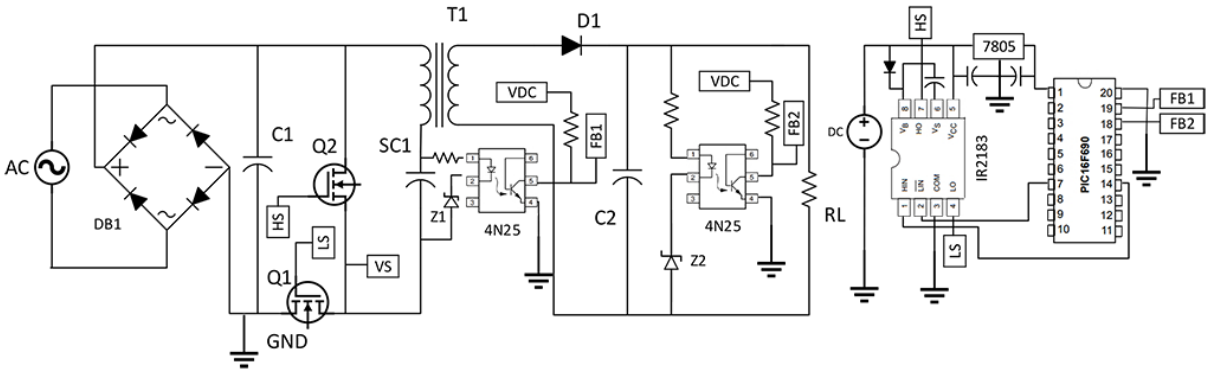


Figure 5.25: Pre-regulator stage, half bridge driver based implementation

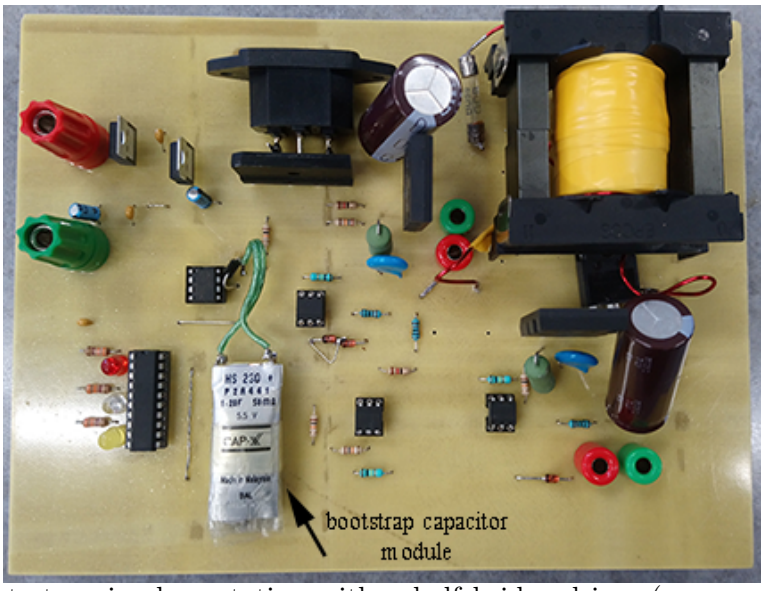


Figure 5.26: Input stage implementation with a half bridge driver (supercapacitor is used as bootstrap capacitor)

In our next design, floating MOSFET was driven with an isolated DC rail, and IXDD614PI high current MOSFET drivers were introduced to drive both MOSFETs, as shown in Figure 5.28. This design improved the current capability of the power converter stage up to 10 A. The high-side gate driver power-rail can be powered by a 15 V linear regulator connected to the supercapacitor bank as the high-side MOSFET and SC bank share the same ground. The controller circuit consumes current in the range 50 to 100 mA. And alternative solution to power the controller is using a 50 Hz transformer with two 12 V isolated output terminals which can be rectified regulate with 15 V commercially available linear regulator. It is important to have a smooth power delivery for the controller circuit.

5.6.2 Controller algorithm of the power converter

The controller algorithm of the power converter is shown in Figure 5.29. The converter is set to flyback mode for the initial charging stage of the capacitor bank. As seen in the simulation and the implementation supercapacitor voltage has a huge ripple. The output voltage of the power converter is continuously monitored, and the pulse width of the gate signal is adjusted to maintain the regulation. As the supercapacitor module accumulates, charge, the voltage across

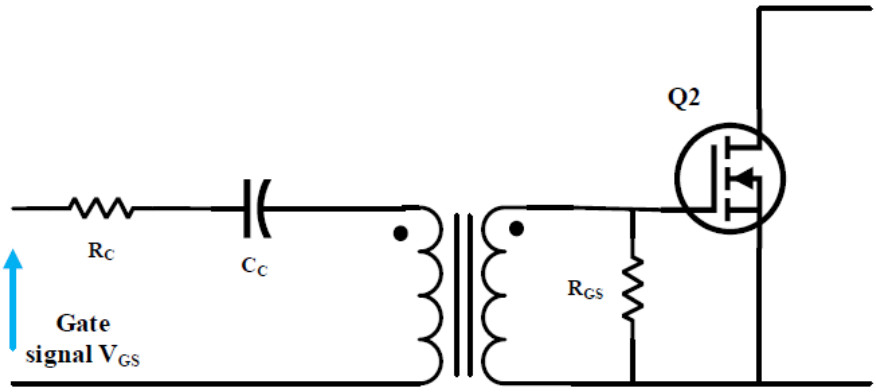


Figure 5.27: Transformer isolated gate driver circuit

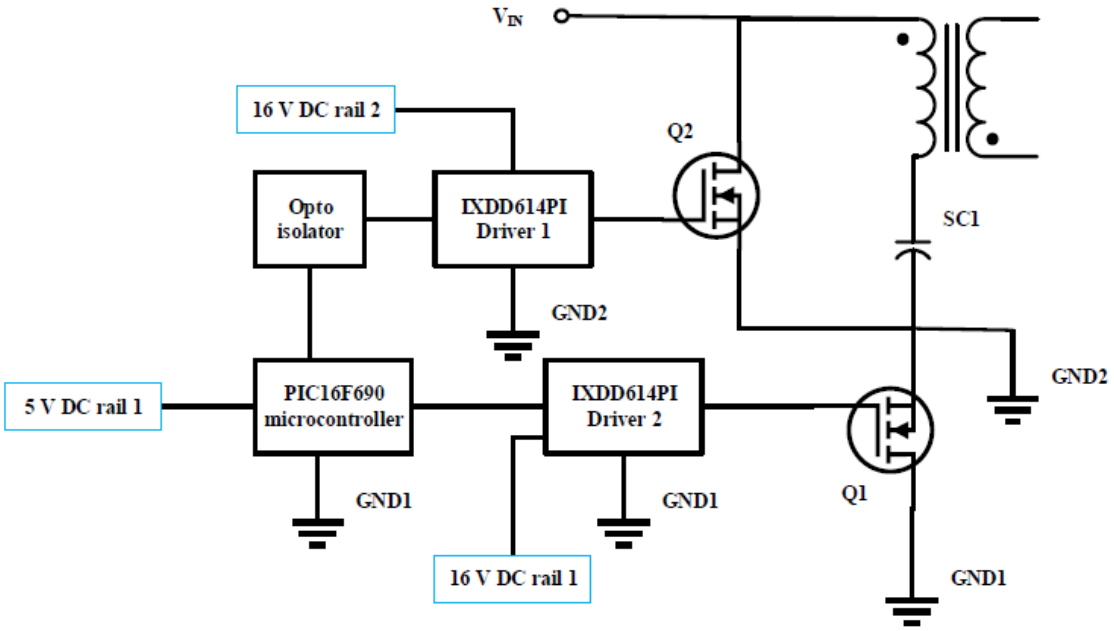


Figure 5.28: MOSFET driver circuit of the pre-regulator stage (Q2 is with floating ground))

primary winding drops below the minimum required voltage for regulation. At this point, the power converter toggles to its forward mode and the supercapacitor bank discharges to the load as long as output voltage can be regulated. Similar to flyback mode, the output voltage is measured throughout to maintain regulation. When the output voltage drop below the regulated voltage the converter returns to flyback mode. This cycling continues as long as we power the controller.

Certain advantages of the algorithm discussed can be summarised as below:

- No extra logic is required to implement DC-UPS capability and no need to monitor input voltage to detect power interruptions
- Only need to measure the output voltage, can minimize ADC register reading delays in controller loop

- Can skip monitoring supercapacitor voltage, to avoid large voltage ripple due to switching, can monitor output voltage instead

However, since the maximum supercapacitor voltage is not fixed and can be varied with the input voltage, a higher voltage rated supercapacitor should be used. Implementation of this controller logic is presented in Appendix B.

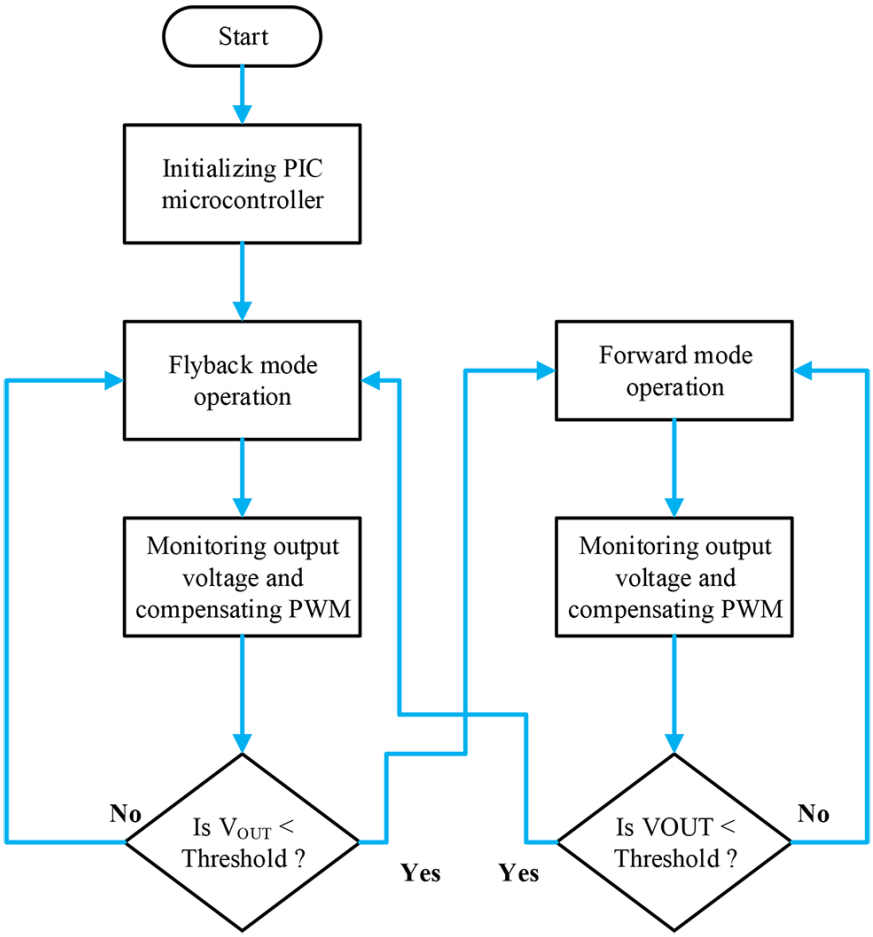


Figure 5.29: Controller algorithm of the pre-regulator stage

5.6.3 Prototype details and results

The 80−to−26 V prototype is shown in Figure 5.30. Two $SIHG47N60E-GE3$ MOSFETs were used to drive the transformer in both forward and flyback modes. The MOSFETs has on resistance around 64 mΩ and suitable for high-frequency switching (Datasheet in Appendix B). The controller is designed with PIC16F690 microcontroller, and switches were operated at the operating frequency 20 kHz. As detailed in the previous section, MOSFETs were driven with a IXDD614PI high current gate driver. large heat-sinks were attached to two MOSFETs in later versions, and a cooling fan was also used. The schematic of the prototype implementation is shown in Figure 5.31. Detailed schematics and PCB layouts are presented in Appendix B.

The test setup for input stage implementation is shown in Figure 5.32. The converter is powered with 80 V, 1500 W bench power supply. Supercapacitor bank used for prototype

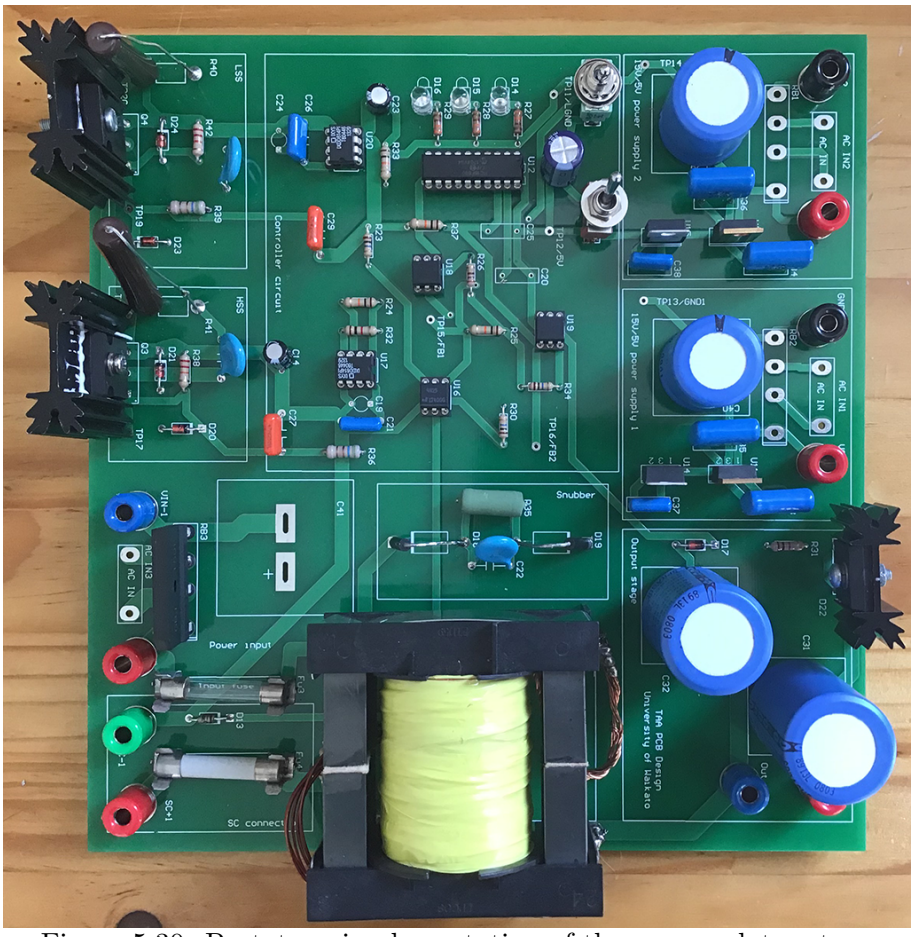


Figure 5.30: Prototype implementation of the pre-regulator stage

implementation is shown in Figure 5.33, where three series LSum 016R8L 0058F SC banks from Ls Mtron are connected in series to form 19.3 F, 50.4 V capacitor bank with 66 mΩ ESR.

Oscillograms of output voltage, output current, V_{DS} of flyback MOSFET switch and, V_{DS} of forward MOSFET switch voltage shown in Figure 5.35 for 2, 6 and 10 A load currents. In Figure (a) and (b) operates in flyback mode while (b) and (d) are instances where the converter works in forward mode. Phase transitions of the converter and the supercapacitor bank voltage are shown in Figure 5.34, which was obtained at 4 A load current.

Transient performance data obtained from the input stage for various test conditions are shown in Figure 5.36. In each case, the load current was changed from 2 to 8 A at various slew rates such as (a,b)1 A/μs, (c,d)10 A/μs, and (e,f) 20 A/μs. The waveforms of both the rising (left column) edge and the falling (right column) edge were recorded. Load variations have no significant impact on the output voltage profile. Input and output filter stages should be designed to reduce RFI/EMI issues and will be addressed in a future prototype.

Load and line regulation data obtained from the prototype are shown in Figures 5.37 and 5.38 respectively.

Calculating end-to-end efficiency is not straightforward for the pre-regulator stage, as the converter toggles between forward and flyback phases. During the offline state, the converter consumes no current. To calculate the efficiency in one cycle, we consider E_{IN}, the input energy consumption in one cycle,

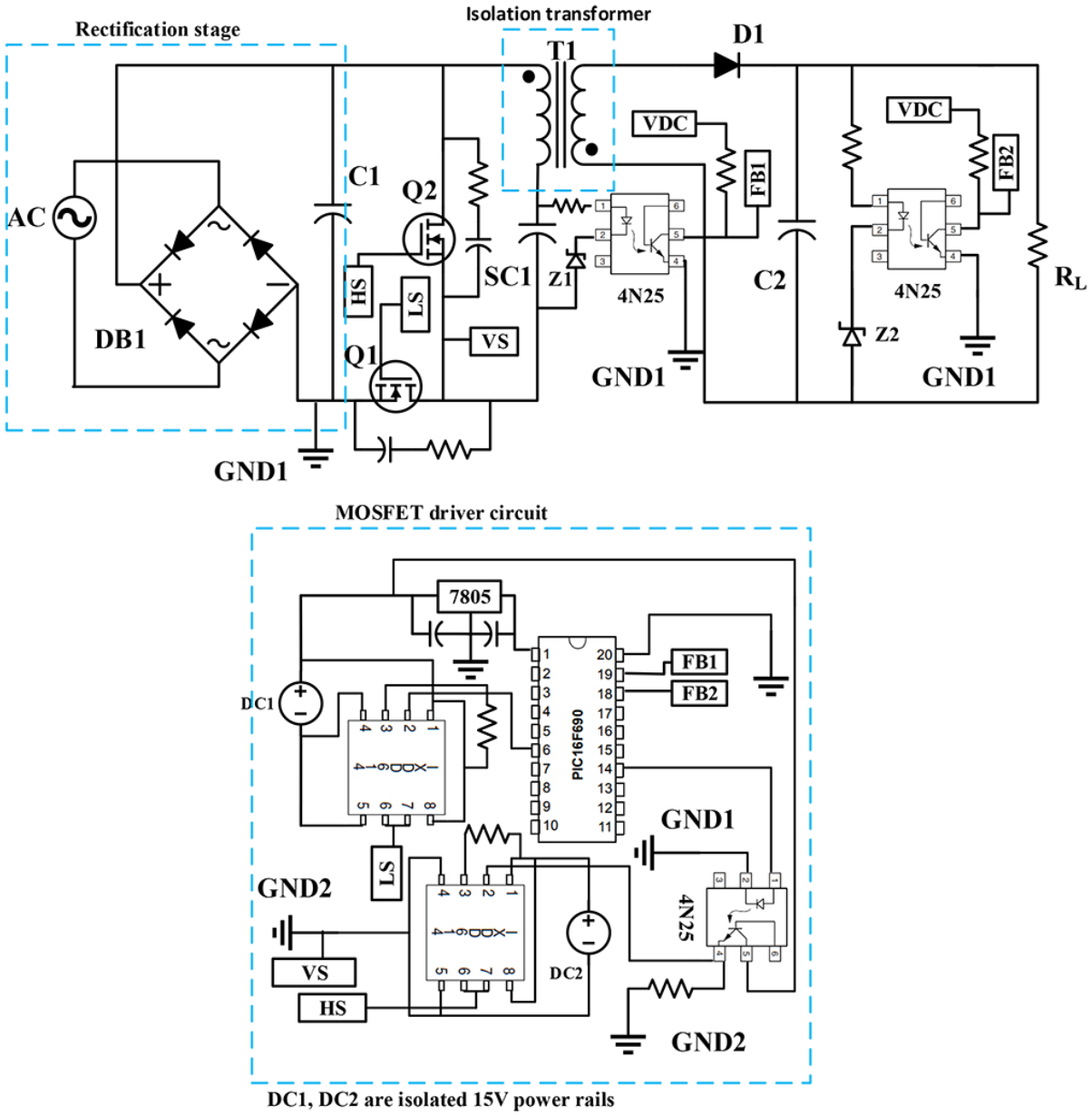


Figure 5.31: Circuit schematic of the medium-frequency pre-regulator stage

$$E_{\mathrm{IN}} = I_{\mathrm{IN(RMS)}} \times V_{\mathrm{IN(RMS)}} \times t_{\mathrm{ch}} \tag{5.26}$$

where $I_{\mathrm{IN\ (RMS)}}$ represents input RMS current, $V_{\mathrm{IN\ (RMS)}}$ represents input RMS voltage and t_{ch} is the charging time of the capacitor. The output energy in one cycle is given by:

$$E_{\mathrm{OUT}} = I_{\mathrm{OUT(RMS)}} \times V_{\mathrm{OUT\ (RMS)}} \times (t_{\mathrm{ch}} + t_{\mathrm{disch}}) \tag{5.27}$$

where t_{dis} is the discharge time of the supercapacitor and total cycle time T $(t_{\mathrm{ch}} + t_{\mathrm{ch}})$. Then the efficiency η can be estimated as:

$$\eta = \frac{E_{\mathrm{OUT}}}{E_{\mathrm{IN}}} \times 100\% \tag{5.28}$$

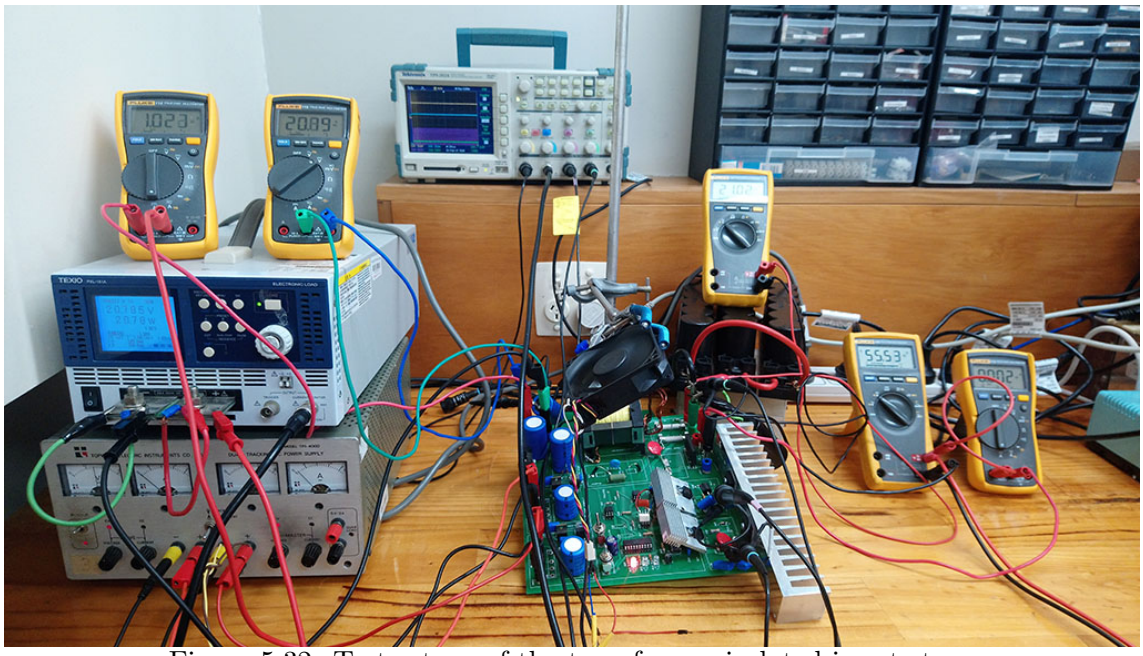


Figure 5.32: Test set-up of the transformer isolated input stage

Figure 5.33: Supercapacitor bank used for the pre-regulator prototype (three LSUM 016R8L capacitor banks from LS Mtron are connected in series to form 19.3 F 50.4 V SC bank with 66 mΩ ESR

The efficiency curve of the prototype is depicted in Figure 5.39. The converter efficiency is close to 80% at 1 A load current and drops to 66% at 10 A load conditions. This is due to the various secondary losses in the power converter at high current. This study mainly focuses on technically solving the power transfer stage of the converter (power transfer stage), and opportunities to improve its efficiency will be explored in a future study. Various issues contributing to power losses in the converter can be summarised as :

- core losses and winding resistance in the isolation transformer
- losses in the power MOSFETs used for switching
- losses in snubber circuits
- conduction losses in the circuit

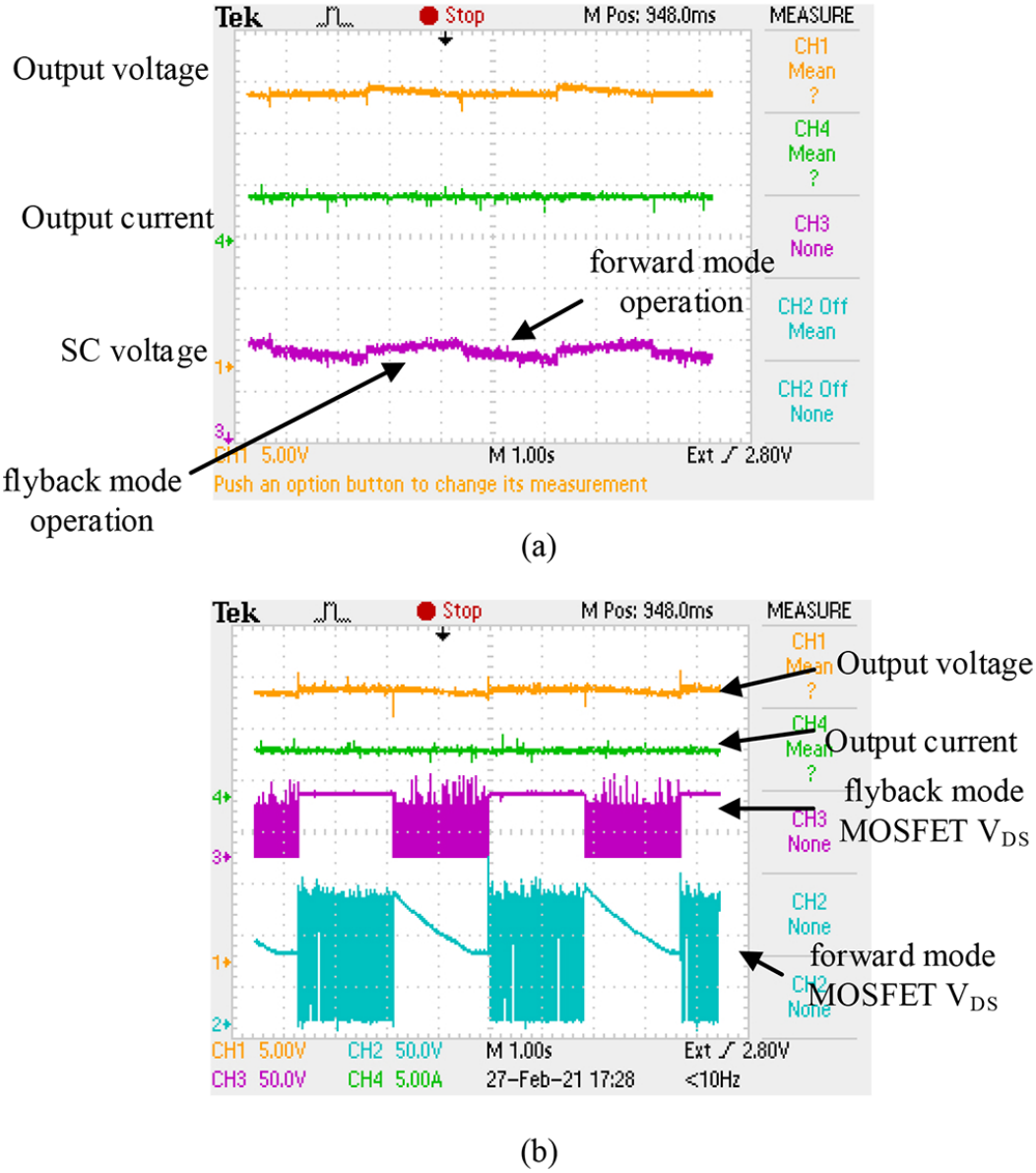


Figure 5.34: Waveform of 80-to-26 V prototype: (a) output voltage and current waveform with supercapacitor voltage; (b) output voltage and current waveform with drain source voltage of MOSFETs

5.7 Overall circuit

Test setup of the overall circuit is shown in Figure 5.40. Oscillogram obtained at 2 A and 10 A load current are shown in Figure 5.40. Output characteristics of the power converter is dominated by the output SCALDO stage. Voltage and current profile of overall converter at 1.7 A and 10.4 A load current are shown in Figure 5.41.

Discussion on DC-UPS capability of the new power converter is presented in following section.

5.8 Scaling converter for 48 V configuration

The converter can be scaled to 48 V Google power supply by upgrading the input stage to rectified 230 V AC main to 98 V converter. In order to meet these specifications the transformer

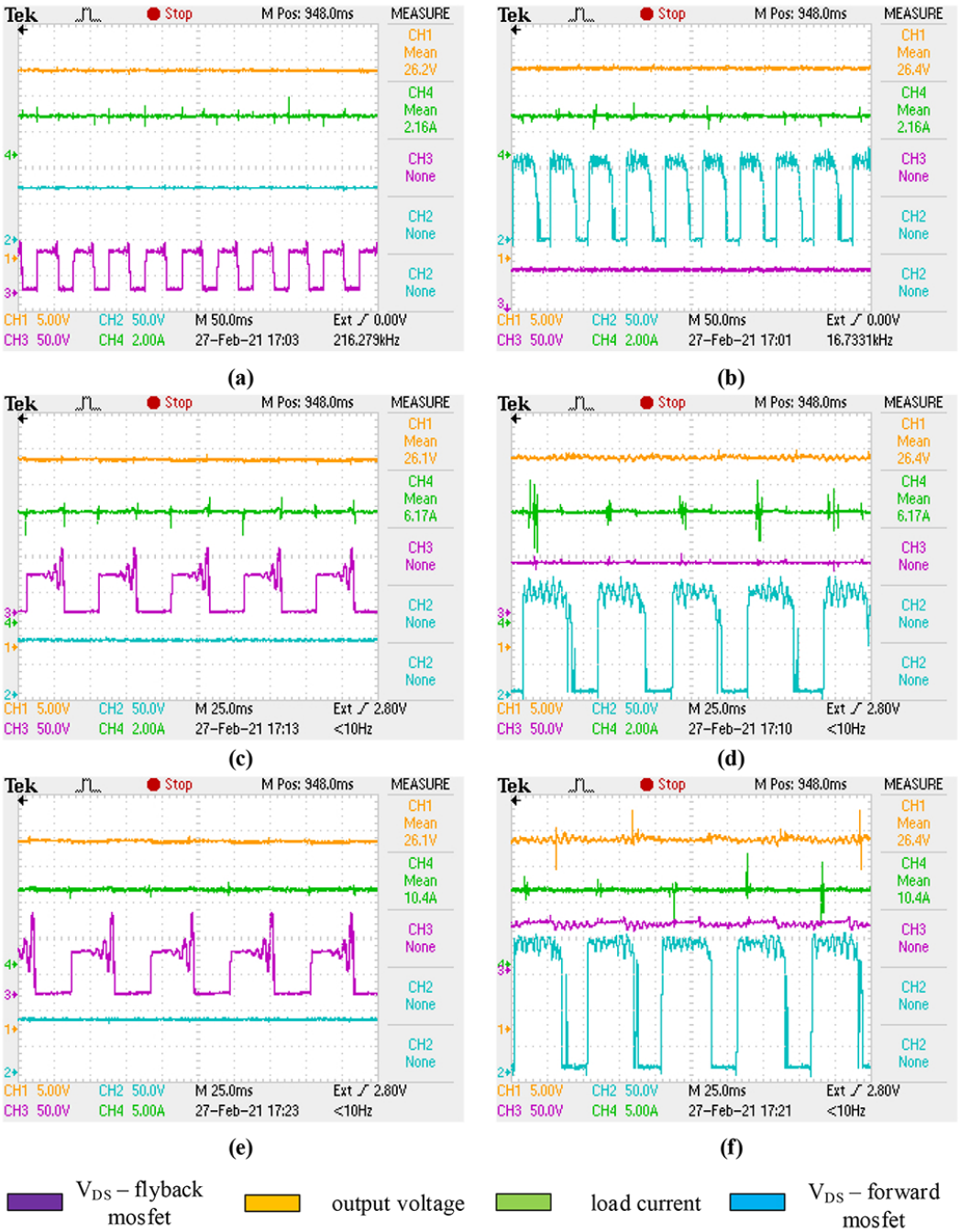


Figure 5.35: Oscilloscope waveform for output voltage, load current, V_{DS} of 80-to-26 V input stage for load currents of (a)(b) 2 A; (b)(c) 6 A; (d)(e) 10 A load currents for flyback and forward operations

should be scaled to meet the power delivery requirement of the Google server rack. Power MOSFET switches should be chosen to reflect switching voltages and the current requirement of the converter. Higher voltage supercapacitor bank such as MAXWELL 230 V 3.75 F (Figure 5.45) should be chosen for the supercapacitor bank. In order to increase UPS autonomy time, capacitor banks can connect in parallel to increase the capacity. DC-UPS capability of the new power converter will be discussed in detail in the next section.

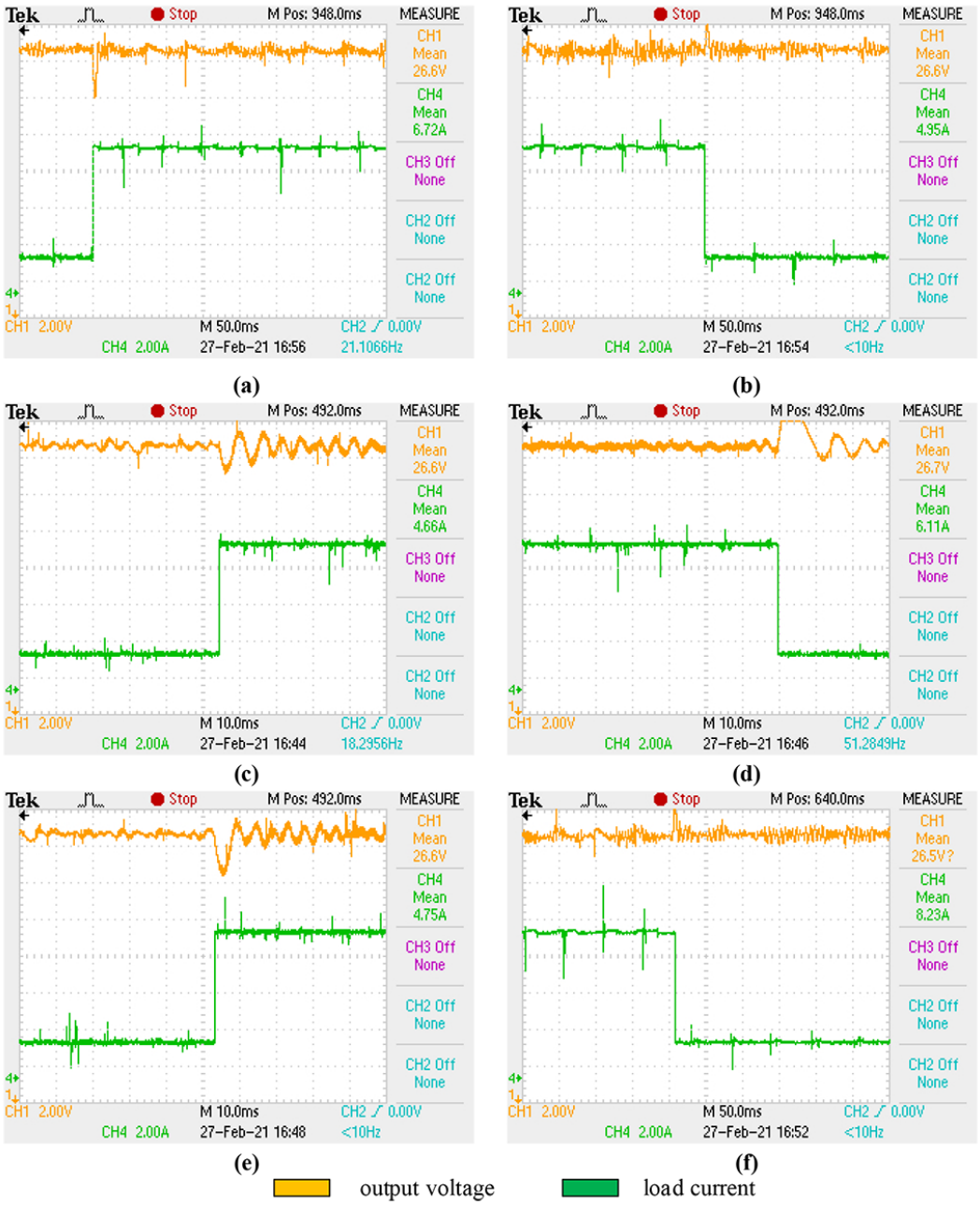


Figure 5.36: Transient response oscillogram of input stage for various load conditions: (a) current rising from 2 A to 8 A at 1 A/μs; (b) current falling from 8 A to 2 A at 1 A/μs; (c) current rising from 2 A to 8 A at 10 A/μs; (d) current falling from 8 A to 2 A at 10 A/μs; (e) current rising from 2 A to 8 A at 20 A/μs; (f) current falling from 8 A to 2 A at 20 A/μs

5.9 DC-UPS and sizing supercapacitor bank

Detailed discussion of the DC-UPS capability of the power converter is available in [9]. The converter can be easily modified to introduce inbuilt DC-UPS capability by over-sizing the capacitor bank. Figure 5.42(a) depicts the architecture of a typical 48-V Google server rack. Figure 5.42(b) depicts the proposed server rack power architecture with SC bank to store backup energy. In battery-based UPS systems, separate power supplies and extra charging circuitry are required to charge the battery bank. However, in the proposed solution separate power supply

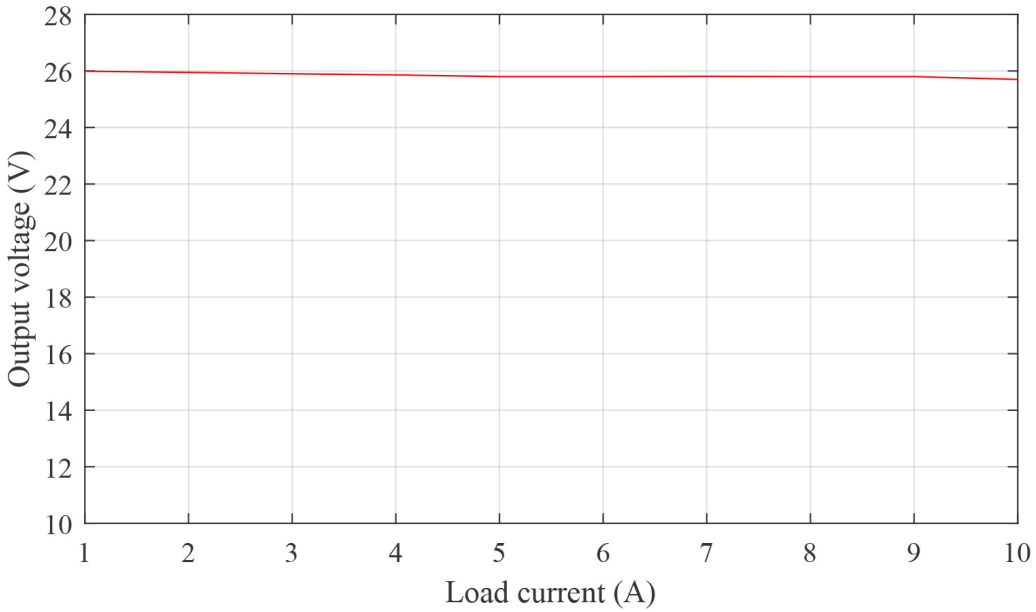


Figure 5.37: Medium-frequency input stage load regulation curve

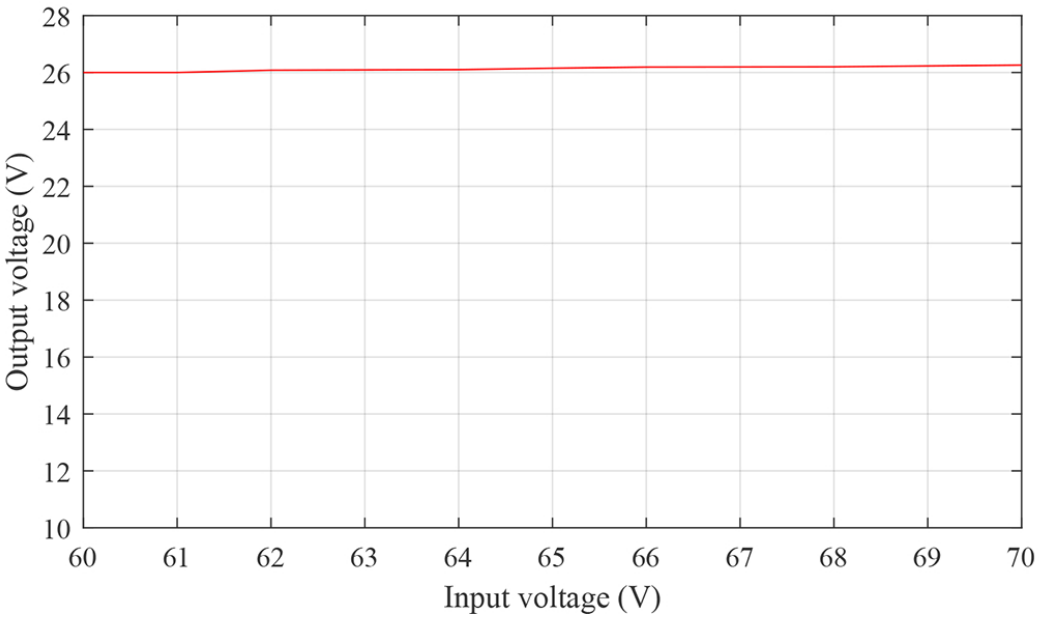


Figure 5.38: Medium-frequency input stage line regulation curve

or extra circuitry is not required, since energy storage is integral part of the power converter. Extra power supply can be used as redundant power line.

Currently the supercapacitor bank is operating between two voltage levels as depicted in Figure 5.43. Ripple voltage ΔV is kept at a low value to improve regulation [13]. The power converter toggles between two states by monitoring when output voltage drops below a threshold value. There will not be any impact of power interruptions at the stage where the converter is in forward mode due to the converter being disconnected from the main supply. When the converter is operating in flyback mode during a power interruption, as the output voltage drops below the threshold, it quickly toggles to forward mode powering load from stored energy in the SC bank. DC-UPS hours are determined by the size of the SC bank, and sizing supercapacitor

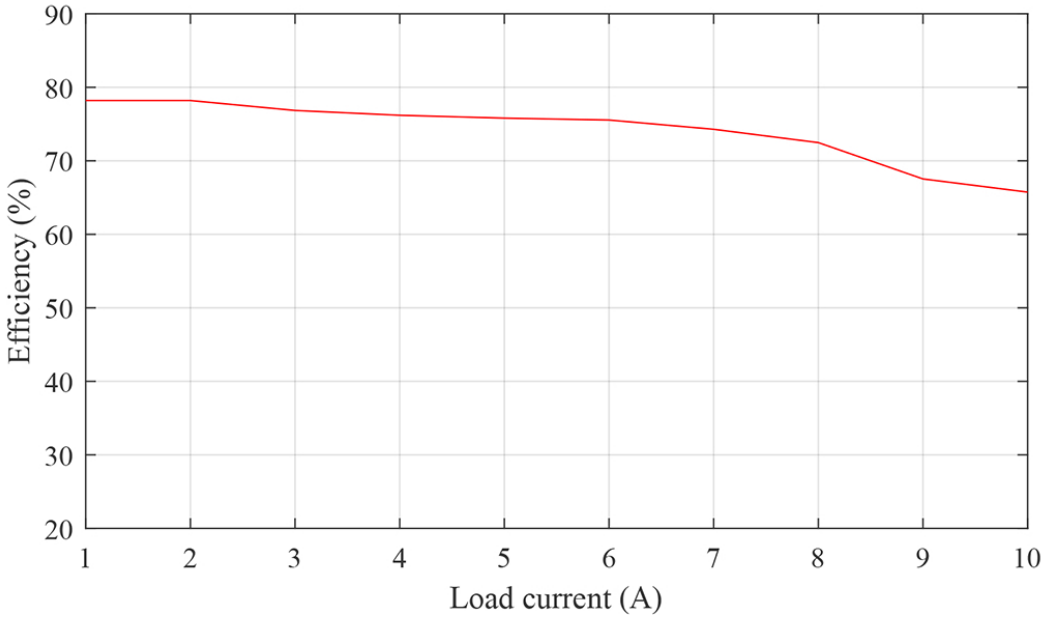


Figure 5.39: Efficiency of the pre-regulator stage with load current

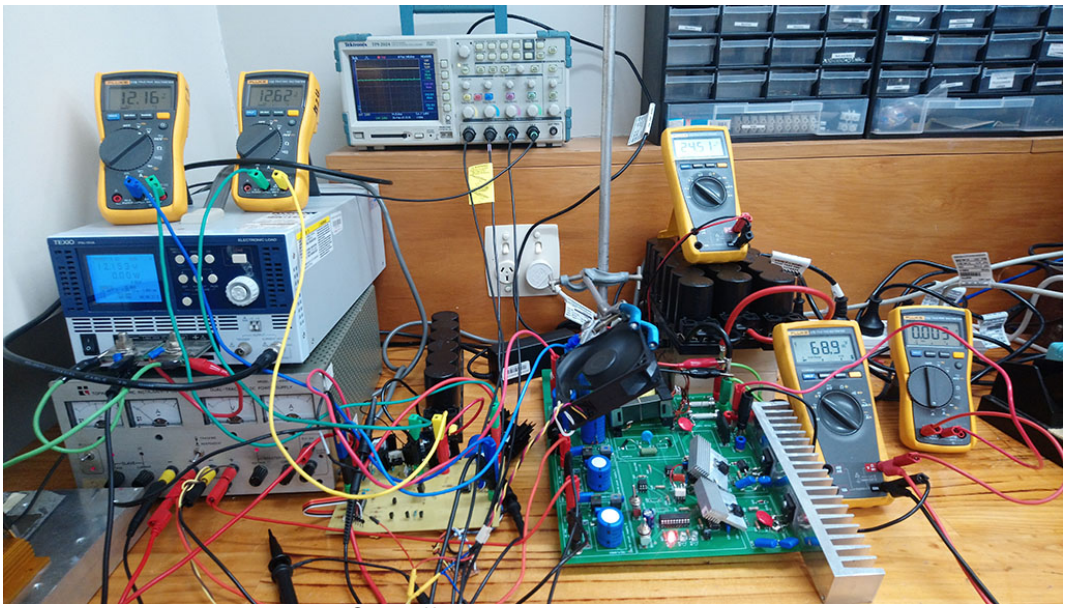


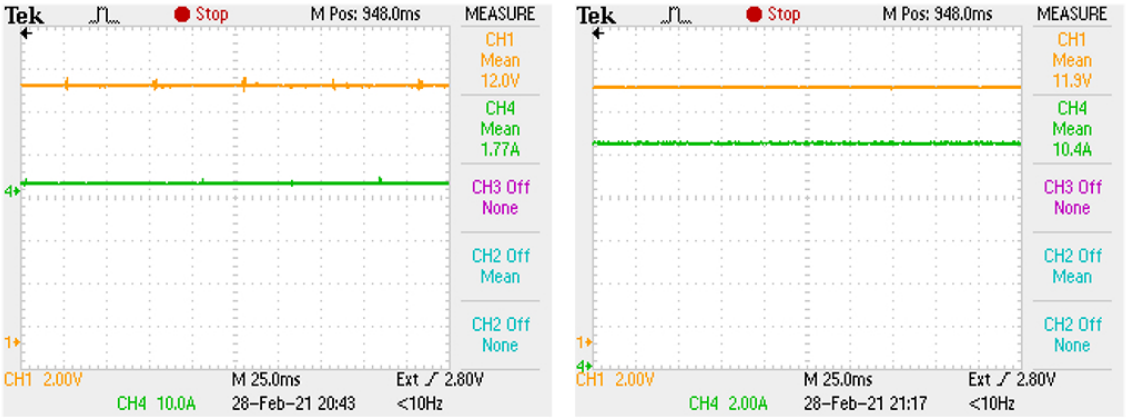
Figure 5.40: Overall power converter circuit, test setup

bank is an important aspect of the converter.

Although the capacitance of SCs is very high, the cell voltage is as low as 2.7 V. In order to use with higher voltages, capacitor banks are created connecting several SCs in series. However, this will reduce the capacity of the SC bank and increase the overall internal resistance.
When the capacitor bank is operated between two voltage levels, the available energy is given by:

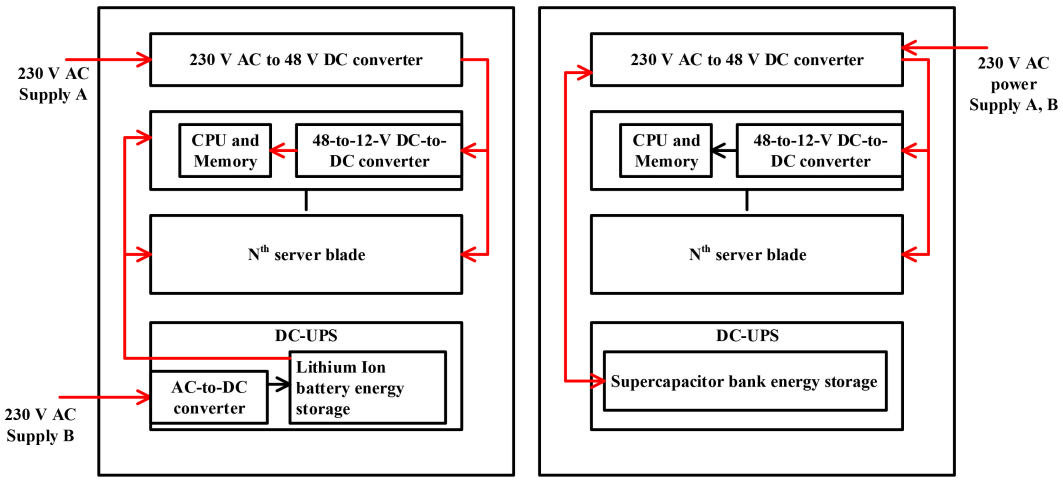
$$E = \frac{1}{2}C(V_2^2 - V_1^2) \tag{5.29}$$

Assume energy storage capacitor bank is made out of n identical series capacitors with C capacitance and r internal resistance. Then the total capacitance is C/n, and the total internal



(a) (b)

Figure 5.41: Voltage and current oscillogram obtained from overall circuit (a) at 1.77 A (b) 10.4 A test currents



(a) (b)

Figure 5.42: 48 V rack power architecture: (a) with battery based DC-UPS, (b) with proposed supercapacitor assisted DC-UPS

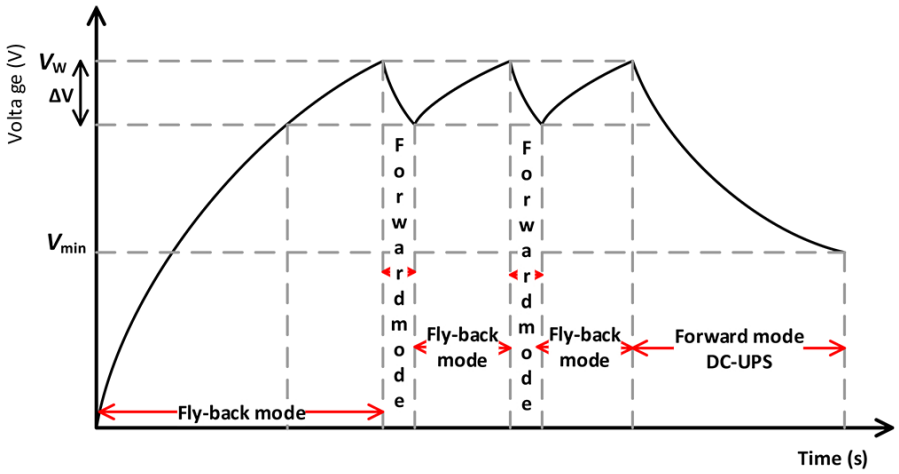


Figure 5.43: Pattern of utilising supercapacitor voltage for DC-UPS

resistance is nr. The capacitor will not be utilized up to its rated voltage of 2.7 V; instead, it will be charged up to 2.5 V to improve the cycle life. Basic parameters of the capacitor bank are listed in Table 5.6.

Table 5.6: Basic parameters of the supercapacitor bank for DC-UPS

Property	Value
Capacity of a individual SC	C
Rated voltage of SC	2.7 V
Maximum voltage	2.5 V
ESR of the SC	r
Number of capacitors in the bank	n
Rated voltage of SC bank	$2.5n$ V
Total capacitance	C/n
Total ESR	nr

When Equation (5.29) applies to the case suitable for Google 48 V architecture, where capacitor can be utilised between 100 V to 162 V, considering rectified DC voltage (325 V), initial voltage depends on the turns ratio of the isolation transformer (minimum required voltage to sustain 98 V at the load side). Then the available energy for DC-UPS is given by:

$$E_{\mathrm{C}} = \frac{C}{2n}((2.5n)^2 - 100^2) \tag{5.30}$$

where n represents number of capacitors connected in series.

Figure 5.44 visualises the DC-UPS capability of SC bank in watt-hours. The initial voltage of the SC bank is considered as 100 V, as discussed earlier. With the number of SCs and the capacity of a single capacitor, DC-UPS time is increasing. However, internal resistance, the bank's volume, and the cost also increase with the number of capacitors used.

Table 5.7 summarises properties of supercapacitor banks made from three commercially available SC types. As shown in Figure 5.45, commercial availability of high voltage SC modules is a favourable development for the proposed new technique. According to the Maxwell data sheet, the rated duty cycle for 5.45(c) is 500 000, and the projected DC life at room temperature is 10 years. These modules come with cell balancing and over-voltage monitoring circuits. They are popular in wind turbine pitch control systems and industrial UPS systems. A few capacitor modules can be used in a server rack in parallel to increase the capacity, which will further reduce the ESR of the overall capacitor bank. The high cost and low capacity of capacitor modules are barriers for supercapacitor based DC-UPS solutions.

The benefits of this new DC-UPS technique can be summarized as:

- Since the life cycle of capacitors are very high; the maintenance cost will be very low
- No additional circuits are required to charge the capacitor (as capacitor bank is part of the power-supply)
- Changing power source within (50 μS) this will be further buffered by output side supercapacitor bank
- Environmentally friendly solution as this is replacing batteries

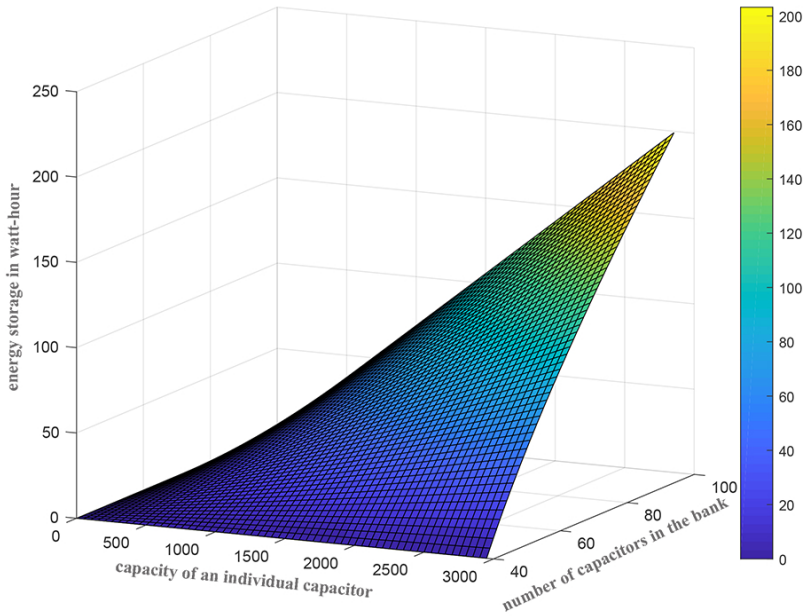


Figure 5.44: Sizing supercapacitor bank, UPS capability in Wh

Figure 5.45: Commercial supercapacitor modules: (a) Maxwell 90 V 10 F module; (b) Maxwell 125 V 63 F module; (c) Maxwell 230 V 3.75 F module

Table 5.7: Achievable DC-UPS autonomy in Wh for capacitor bank with 90 supercapacitors in series (240 V)

Supercapacitor	Type	Achievable UPS autonomy (Wh)	Cycle life
LSUC 2.7 V 3000 F	EDLC%	188.1	100 000
ESD SCAP 2.8 V 7500 F	Hybrid SC%	470.2	50 000
ESD SCAP 2.7 V 40 000 F	Capa battery	2507.7	20 000

- High power density of the storage, high current can easily be drawn

Replacing UPS with supercapacitor bank can save 30% to 75% total life time cost of battery based UPS [28]. Cost comparison for 200 kW UPS system with batteries, flywheels and supercapacitors is shown in Figure 5.47.Supercapacitor banks easily fit into existing standard UPS battery racks as shown in Figure 5.46.

Disadvantages of supercapacitor based DC-UPS solution can be summarised as:

- Higher self discharge rate compared to batteries.
- Low cell voltage, need to connect in series to create banks for higher voltages.
- Low energy density compared to batteries.

- Higher capital cost compared to batteries.

Figure 5.46: Supercapacitor modules easily fit into standard UPS battery racks [28]

	Batteries	Flywheel	Ultracapacitors
User Requirements			
Lifetime	15 years	15 years	15 years
Power	200 kW	200 kW	200 kW
Bridge Time	15 seconds		15 seconds
Inputs			
Useful Life (typical)	2 years	15 years	15 years
Float voltage	560V	560V	560V
Minimum voltage	440V	440V	280V
Discharge Time	30 seconds	30 seconds	30 seconds
Initial cost	$17,000*	$48,000	$60,000
Annual cost**	$4,450	$2,140	$550
Total Lifetime Cost	$83,785	$80,150	$68,290
Savings			**$15,495 (18%)**

*includes $10,000 for monitoring system
**includes floorspace, electrical cost, maintenance and replacement

Figure 5.47: Total cost of ownership comparison [28]

5.10 Chapter summary

This chapter presented the design and implementation aspects of the new medium-frequency switched-mode power converter stage. The prototype works at reasonable efficiency for a proof of concept implementation. However, transformer, snubbers, and MOSFETS switches used should be optimized to achieve the desired efficiency. The converter stage can be upscaled for 230 V AC to 100 V DC converter by choosing a higher voltage SC bank, designing the transformer

to handle desired power and up-scaling MOSFET switches used. DC-UPS duration can be improved by introducing an oversized supercapacitor bank. Next chapter summarises SCALDO assisted high current power converter design by discussing its limitations and opportunities for future extension.

Chapter 6

Conclusions and Future Work

6.1 Summary and conclusion

Recent advances in commercial supercapacitors have enabled the production of single-cell devices from 1 to over 70 000 F within the same standard canister sizes used for electrolytic and film capacitors. These new devices have allowed the development of a range of supercapacitor assisted (SCA) power converter techniques that are useful in various electronic applications. The new power converter technique detailed in this thesis is the latest addition to this SCA family.

Primary aim of the thesis was to develop a new SCA technique useful for new Google Architecture compatible power converter.

The overall converter comes in two separately developed parts (i) SC assisted electrically isolated bulk DC supply (ii) SCALDO based load side high current converter.

The load-end of the converter is an efficient SCALDO stage that operates at fractional hertz frequency to provide all the benefits of low-dropout regulators with added DC-UPS capability. The transformer-isolated input stage operates at a medium frequency (20 kHz), using a supercapacitor bank as an energy reservoir in series with the primary of the isolation transformer. By introducing an oversized supercapacitor bank, DC-UPS can be extended to several minutes, depending on the load.

At the early stage of the work, a generalized theory was developed to explain the overall family of SCA techniques, identified as Supercapacitor Assisted Loss Management (SCALoM) concept.

As the next step, the SCALDO converter was extended to handle high current with the development of a discrete LDO stage where parallel P-MOSFETs were introduced to reduce the dropout voltage. The LDO regulates a 10 A load current, keeping dropout voltage in the range of 0.1 to 0.5 V. Theoretical analysis was conducted to model the behaviour of the LDO, and this analysis helped us to identify specific parameters contributing to dropout voltage, regulation and current capability. Using this discrete LDO stage a 10 A, 26-to-12 V SCALDO stage was developed, which is the highest-end SCALDO implementation to date with the possibility of extending the technique to a 100-48 V version at the next stage.

Isolated front end design was inspired by the fast supercapacitor charger technique combined with the techniques adapted in common forward-mode and fly-back converter techniques. Several LTspice and MATLAB Simulink simulation models were developed to study the behaviour of this new power converter stage, and the impact of the component parameters was studied. These simulation models helped us to identify the technical feasibility of the converter. Technical implementation was the biggest challenge that we encountered. Many prototypes were built

targeting various load conditions and trying out different switch driver techniques. The same isolation transformer was used for the flyback and forward, two-way power transfer stages. The latest prototype can handle output current over 10 A at 26 V output voltage. Although prototype components are not optimised, significant success was achieved with the efficiency: at 1 A load current, the input stage works at 78% efficiency and at 10 A load current input stage works at 66% efficiency. The converter has two-stage DC-UPS embedded in it.

When the applications are considered, data centres require a high power backup power supply for 15−30 s to bridge external power sources such as diesel generators during power interruptions. Implementing the new power converter technique at rack level with supercapacitor-based energy storage may be a versatile solution for data centres. The technique comes with the added advantage of the $15 - 30$ s order DC-UPS within the converter based on supercapacitor based energy storage, to avoid battery banks. The technique is also useful for the following common applications:

1. Desktop computer power supplies- with added short term UPS capability
2. Renewable energy converters useful in solar or wind energy.

Slew rate tests show that the converter responds rapidly to fluctuations in load, and the converter is suitable for powering unstable loads.

The benefits of the new power converter can be summarised as:

- connected load always sees the DC output of a linear converter based on an LDO
- high current slew-rate capability
- high output load current capability
- transformer isolation at the primary side
- SC-assisted two-stage DC-UPS
- wide input voltage range
- surge absorbent capability (because of series SC)
- high ETEE (end-to-end efficiency)
- relatively low stress on switches
- low RFI/EMI issues and hence less filtering

6.2 Future research

This section discusses opportunities created by our study for future improvements into the 48 V DC output versions.

Optimising converter for efficiency

Theoretically, the medium frequency input stage should be able to deliver power at high efficiency. However, various practical losses in the implementation dropped its efficiency below 80%. Possible causes of losses are:

- MOSFET losses and inadequate gate driving
- Transformer losses
- Snubber losses

Currently, two IRFB4332PbF N-channel power MOSFET are used for switching the transformer. This MOSFET has its on-resistance rated at 33 mΩ, which is a cost-effective choice for the design. However, the MOSFET switch can be upgraded to one with low on-resistance as this has a direct impact on reducing switching losses in the power supply. Opportunities can be found to enhance efficiency in the isolation transformer used. Also, PCB tracks and external cables can be optimised according to the power converter's output current to reduce any conductance losses. Opportunities to optimise snubbers used for power MOSFET terminals can be explored. An issue in the power factor of the converter may also be a contributing factor for the low efficiency.

Improving the control loop

Currently, the controller circuit is implemented with a PIC16F690 microcontroller, and the whole controller logic is programmed to this IC. Due to various branches of execution such as reading input voltages, the controller has microsecond-order delays in the feedback PWM loop, which increases the ripple in the output. Commercially available PWM chips can be used to generate feedback-controlled PWM signals for MOSFET gate drivers, and power supply design can be altered accordingly. Alternatively, an analogue circuit could be designed to generate the feedback-controlled gate pulse. This may be be another direction for future study.

Quantify RFI/EMI level of the prototype and input/output filter design

Switch-mode power supplies generate RFIs/EMIs due to high-frequency switching and inductive components. These RFIs/EMIs reduce the quality of output and also introduce RFI noise into the input source as well. A study could be conducted to quantify the power converter's RFI/EMI levels, which could be a valuable measurement for future versions of this SCA concept. Carrying out an EMC test on the final version of the 48 V DC rail systems will qualify the technique to be acceptable into data center power converters.

Testing surge capability

It is expected that the new converter has good immunity to surges due to the series-connected supercapacitor. Testing the surge capabilities of the new power converter design is an interesting opportunity for future research. At the moment the research group has commercialised a surge absorber technique developed using supercapacitors (SCASA). By embedding a SCASA in the new power converter's input stage, surge performance can be enhanced, which is another direction for future research.

Power factor correction

To comply with international standards (European and Japanese equipment consuming 75 W or above should comply with IEC61000-3-2), and make effective use of input current the power factor should be maintained at a higher value (close to 1). Measuring the power factor of the prototype and exploring a strategy to enhance the power factor is another opportunity for future research.

Appendix A

Implementation Details Output SCALDO

A.0.1 SCALDO simulation details

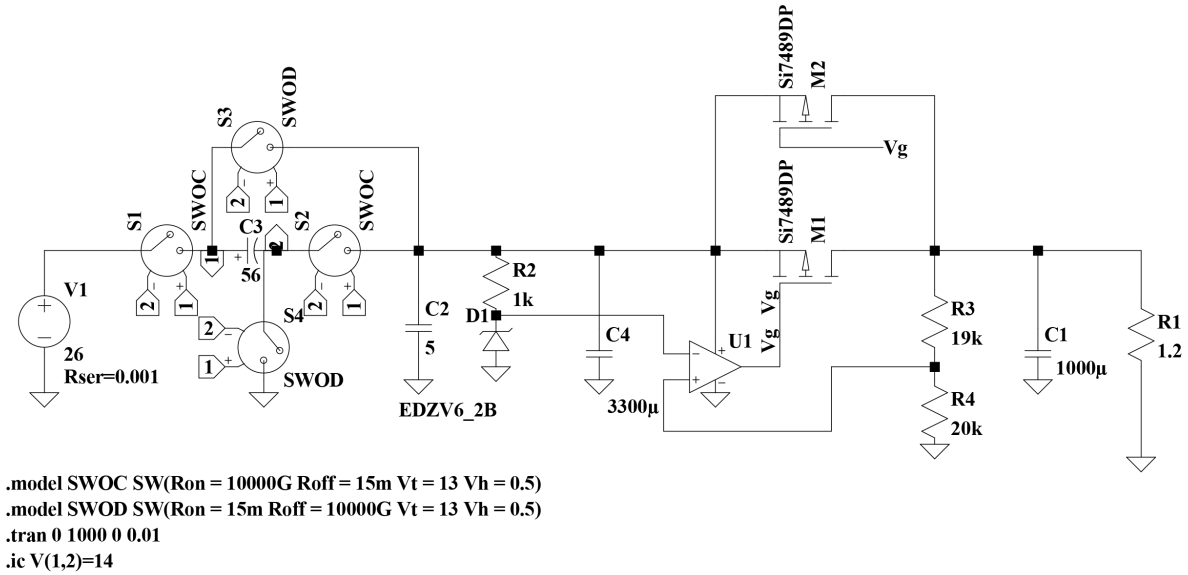


Figure A.1: SCALDO: LTspice model)

A.0.2 SCALDO implementation details

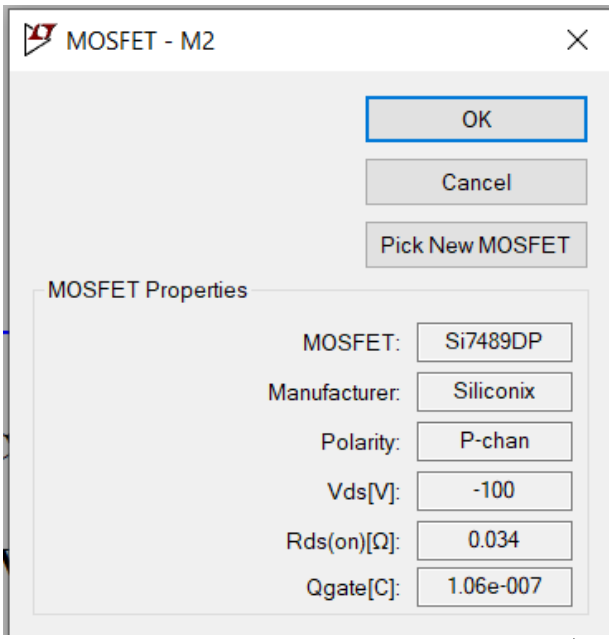


Figure A.2: LTspice MOSFET model used)

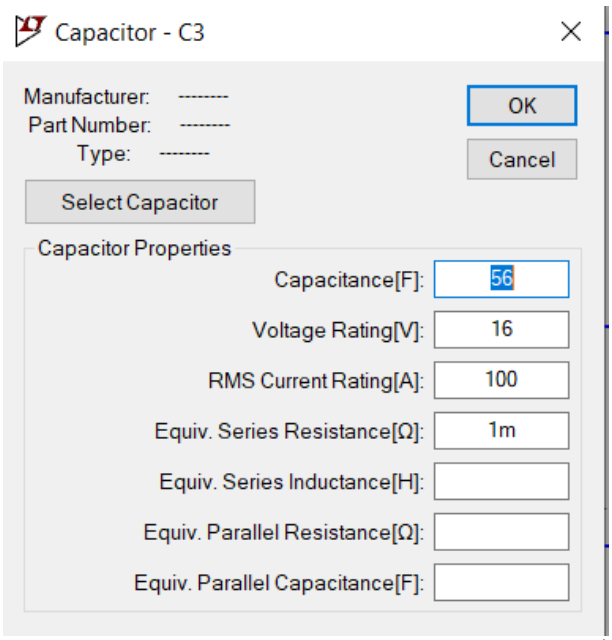


Figure A.3: LTspice supercapacitor model used)

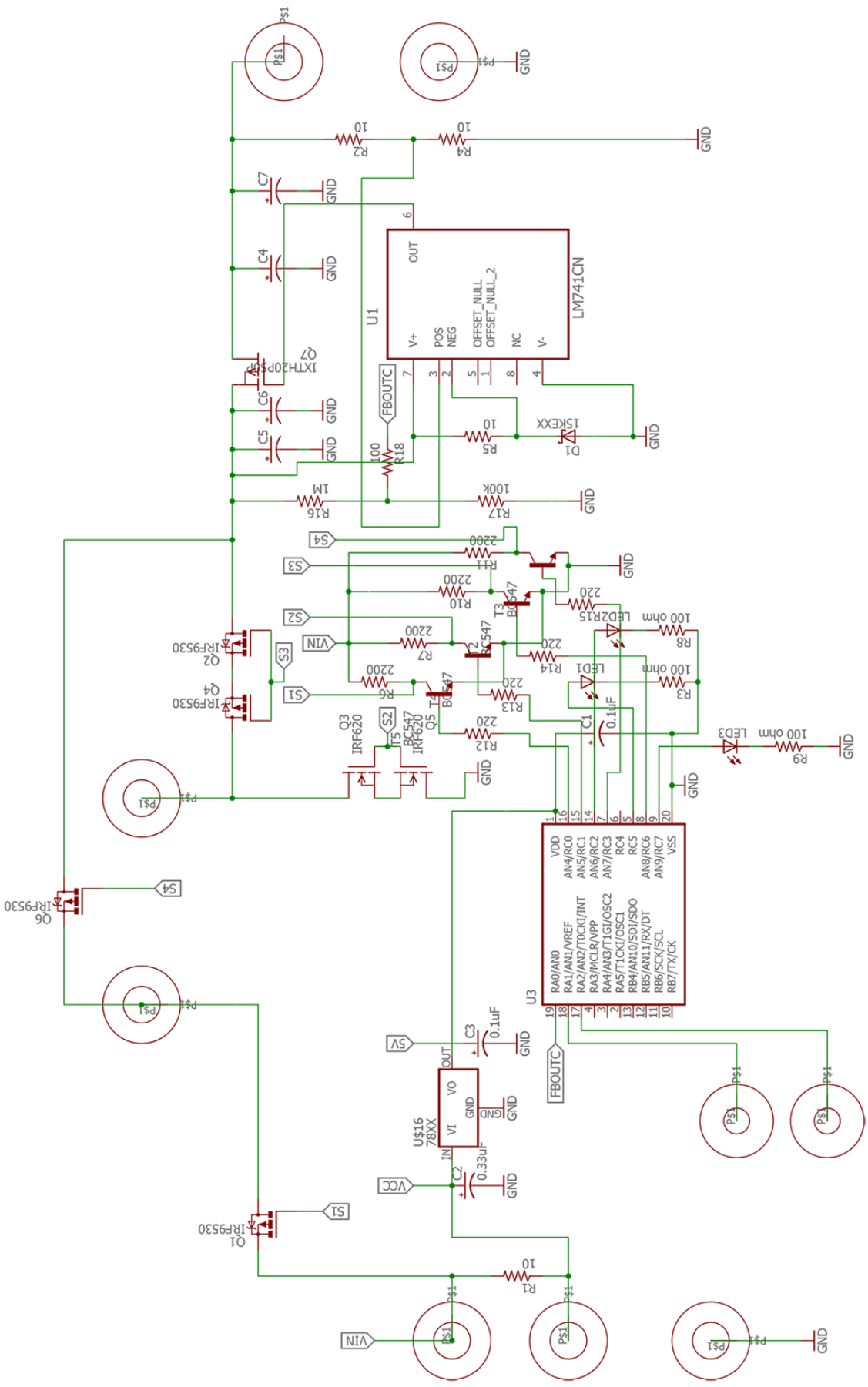


Figure A.4: Schematic diagram of SCALDO implementation (EAGLE)

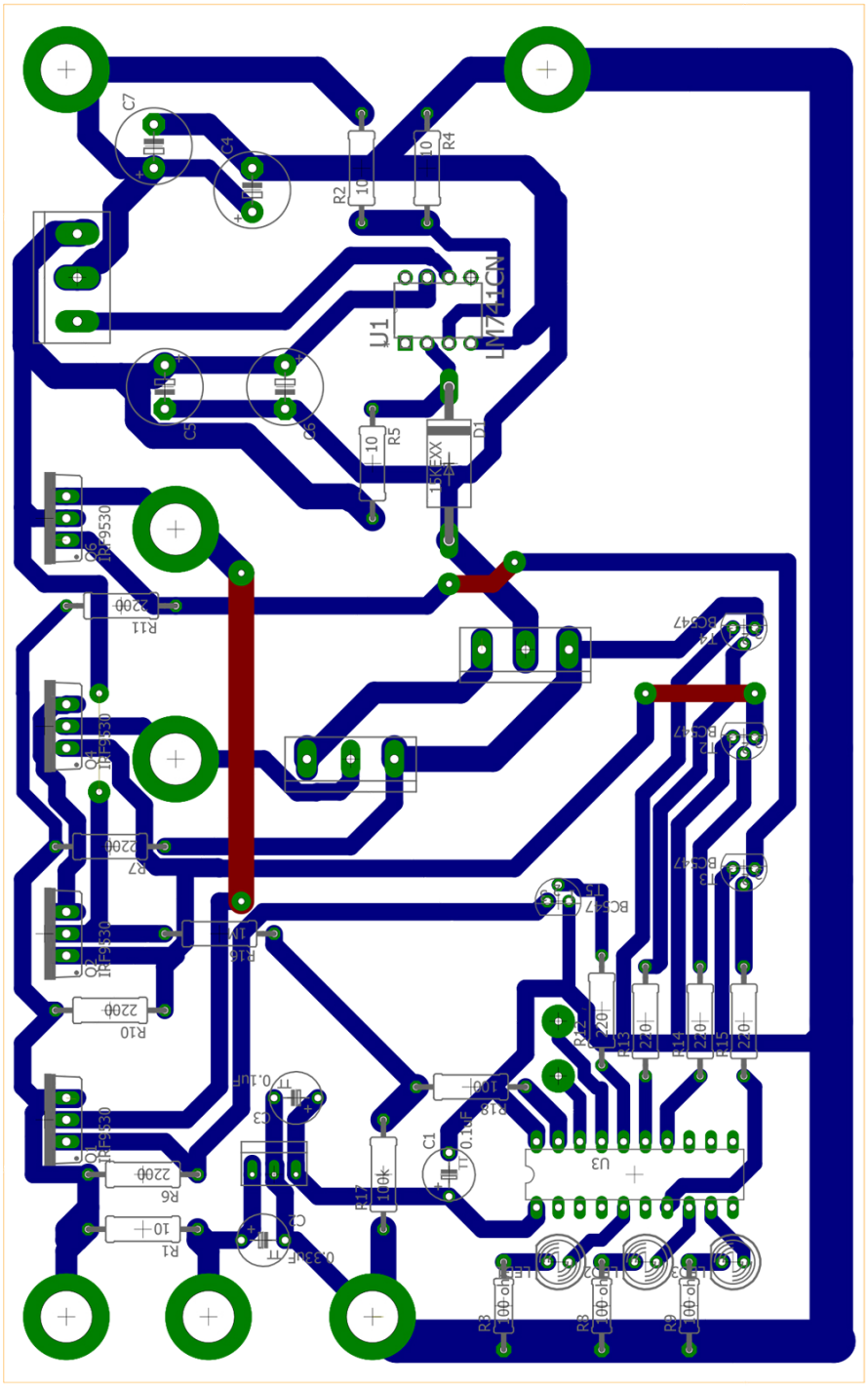


Figure A.5: SCALDO PCB (EAGLE)

VISHAY
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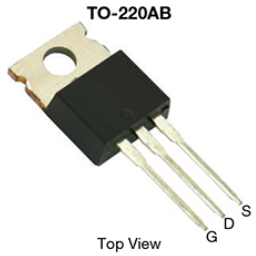
SUP70101EL
Vishay Siliconix

P-Channel 100 V (D-S) 175 °C MOSFET



FEATURES

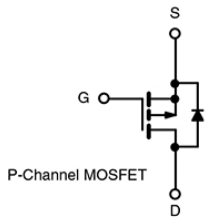
- TrenchFET® power MOSFET
- Package with low thermal resistance
- Maximum 175 °C junction temperature
- Low $R_{DS(on)}$ minimizes power loss from conduction
- Compatible with logic-level gate driving
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

PRODUCT SUMMARY	
V_{DS} (V)	-100
$R_{DS(on)}$ max. (Ω) at V_{GS} = -10 V	0.0101
$R_{DS(on)}$ max. (Ω) at V_{GS} = -4.5 V	0.0150
Q_g typ. (nC)	125
I_D (A)	-120
Configuration	Single

APPLICATIONS

- Battery protection
- Motor drive control
- Load switch



ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free and halogen-free	SUP70101EL-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-100	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current [d] (T_J = 175 °C)	T_C = 25 °C	I_D	-120	A
	T_C = 125 °C		-78	
Pulsed drain current (100 µs)		I_{DM}	-240	
Avalanche current	L = 0.1 mH	I_{AS}	-75	
Single pulse avalanche energy [a]		E_{AS}	281	mJ
Power dissipation	T_C = 25 °C [c]	P_D	375	W
	T_C = 125 °C [b]		125	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	UNIT
Junction-to-ambient	PCB mount [b]	R_{thJA}	40	°C/W
Junction-to-case		R_{thJC}	0.4	

Notes

a. Duty cycle ≤ 1 %
b. When mounted on 1" square PCB (FR4 material)
c. See SOA curve for voltage derating
d. Limited by package

Figure A.6: MOSFET used: SUP70101 data sheet

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SUP70101EL
Vishay Siliconix

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 µA	-100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	-1.5	-	-2.5	
Gate-body leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = -100 V, V_{GS} = 0 V	-	-	-1	µA
		V_{DS} = -100 V, V_{GS} = 0 V, T_J = 125 °C	-	-	-50	
		V_{DS} = -100 V, V_{GS} = 0 V, T_J = 175 °C	-	-	-250	
On-state drain current [a]	$I_{D(on)}$	V_{DS} ≤ -5 V, V_{GS} = -10 V	-120	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = -10 V, I_D = -30 A	-	0.0081	0.0101	Ω
		V_{GS} = -4.5 V, I_D = -20 A	-	0.0114	0.0150	
Forward transconductance [a]	g_{fs}	V_{DS} = -15 V, I_D = -25 A	-	60	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -50 V, f = 1 MHz	-	7000	-	pF
Output capacitance	C_{oss}		-	2180	-	
Reverse transfer capacitance	C_{rss}		-	170	-	
Total gate charge [c]	Q_g	V_{DS} = -50 V, V_{GS} = -10 V, I_D = -110 A	-	125	190	nC
Gate-source charge [c]	Q_{gs}		-	29	-	
Gate-drain charge [c]	Q_{gd}		-	30	-	
Gate resistance	R_g	f = 1 MHz	1.3	6.5	13	Ω
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = -50 V, R_L = 0.71 Ω I_D ≅ -70 A, V_{GEN} = -10 V, R_g = 1 Ω	-	20	30	ns
Rise time [c]	t_r		-	40	60	
Turn-off delay time [c]	$t_{d(off)}$		-	110	200	
Fall time [c]	t_f		-	40	60	
Drain-Source Body Diode Characteristics (T_C = 25 °C [b])						
Continuous current	I_S		-	-	-110	A
Pulsed current	I_{SM}		-	-	-240	
Forward voltage [a]	V_{SD}	I_F = -85 A, V_{GS} = 0 V	-	-1	-1.5	V
Reverse recovery time	t_{rr}	I_F = -85 A, dI/dt = 100 A/µs	-	110	170	ns
Peak reverse recovery charge	$I_{RM(REC)}$		-	-7	-11	A
Reverse recovery charge	Q_{rr}		-	0.38	0.57	µC

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure A.7: MOSFET used: SUP70101 data sheet

A.0.3 SCALDO PIC microcontroller code

```
/*
 * File:   newmain.c
 * Author: thilanga
 *
 * Created on February 14, 2021, 10:49 AM
 */

#include <stdio.h>
#include <stdlib.h>
#include <xc.h>

// CONFIG
#pragma config FOSC = HS        // Oscillator Selection bits (HS oscillator)
#pragma config WDTE = OFF       // Watchdog Timer Enable bit (WDT disabled)
#pragma config PWRTE = OFF      // Power-up Timer Enable bit (PWRT disabled)
#pragma config BOREN = OFF      // Brown-out Reset Enable bit (BOR disabled)
#pragma config CPD = OFF        // Data EEPROM Memory Code Protection bit (Data
    EEPROM code protection off)
#pragma config CP = OFF         // Flash Program Memory Code Protection bit (
    Code protection off)


#define _XTAL_FREQ 8000000

void ADC_Init()
{
   ADCON0 = 0x81; //turn on ADC and clock selection
   ADCON1 = 0x80; // all pins as analog inputs and setting reference voltage
   ADCON0 = 0b10000101;//reading RA1
   __delay_ms(2);
}

unsigned int ADC_Read_zero()
{
   GO_nDONE = 1;// initiating ADC conversion
   while(GO_nDONE); // waiting for the conversion
   return ((ADRESH<<8)+ADRESL); //return result
}

unsigned int ADC_Read_zero_avg(){
    int sum = 0;
    int i = 0;

  //calculating average voltage
    while(i < 5){
        sum = sum + ADC_Read_zero();
        i = i + 1;
        __delay_ms(1);
    }
    return (sum/5);
```

```
49 }
50
51 void main()
52 {
53
54    unsigned int LDO_INPUT_LOW = 581;//2.84 V(12.5 V)) minimum required LDO input
55    TRISA = 0xFF; //analog pin as input
56    TRISB = 0x00;//port B as output
57    TRISC = 0x00;// port C as output
58    PORTC = 0b00000100; //set initial value of port C
59    ADC_Init();
60
61    do
62    {
63         //SC charging
64         PORTC = 0b00100111;
65         __delay_ms(1);
66         while(ADC_Read_zero_avg() < LDO_INPUT_LOW);
67
68     //SC discharging
69         PORTC = 0b10001000;
70         __delay_ms(1);
71         while(ADC_Read_zero_avg() < LDO_INPUT_LOW);
72
73    }while(1);
74
75 }
```

Listing A.1: SCALDO PIC code

Appendix B

Implementation Details of Pre-regulation Stage

B.0.1 Simulink model details

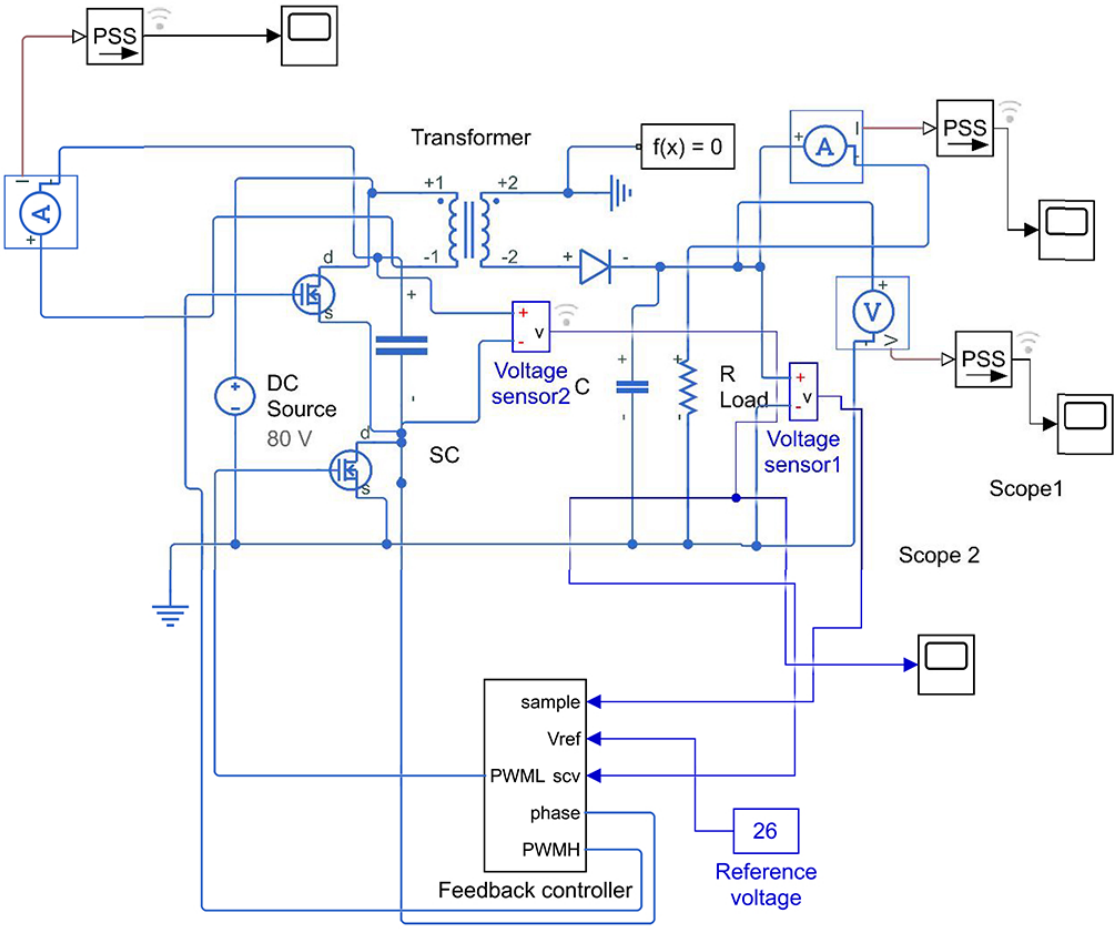


Figure B.1: MATLAB Simulink model of pre-regulation stage

B.0.2 Implementation details of pre-regulation stage

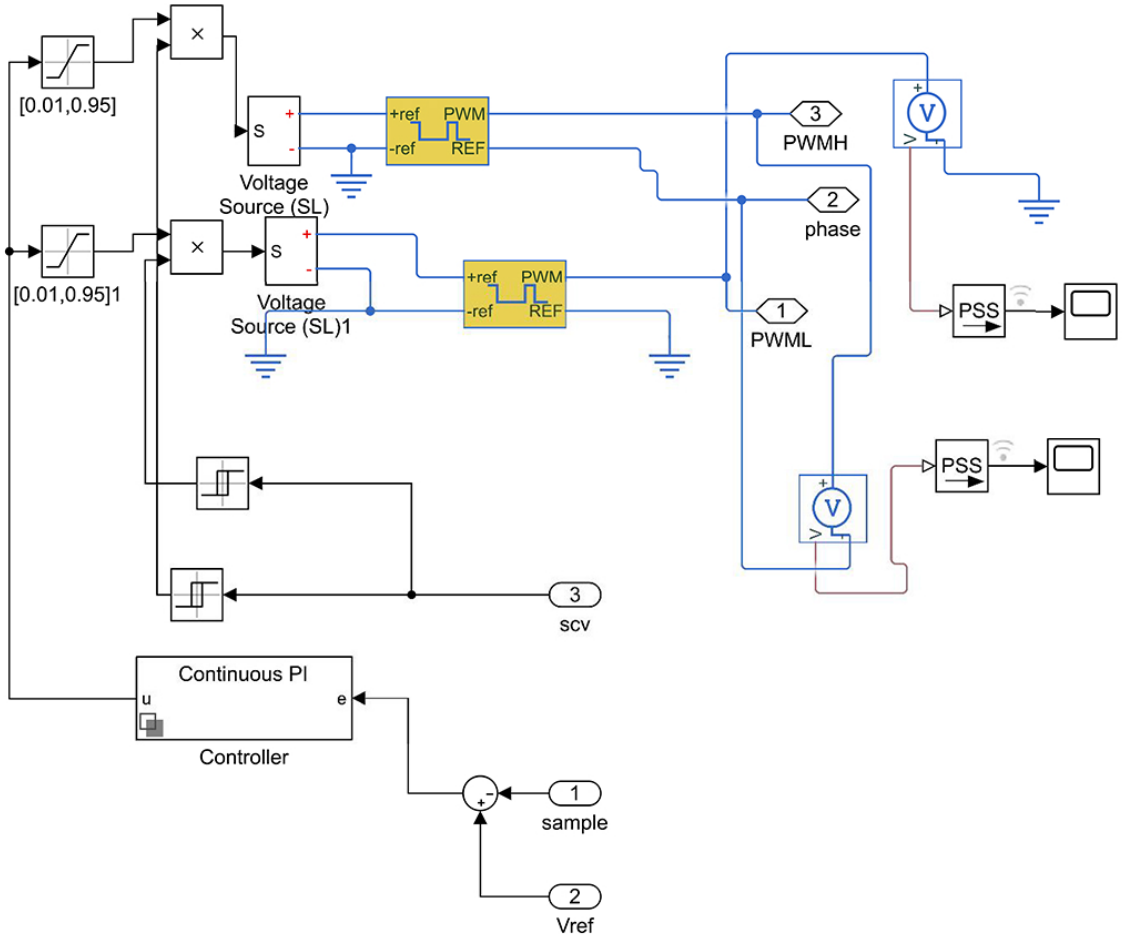


Figure B.2: MATLAB Simulink controller circuit

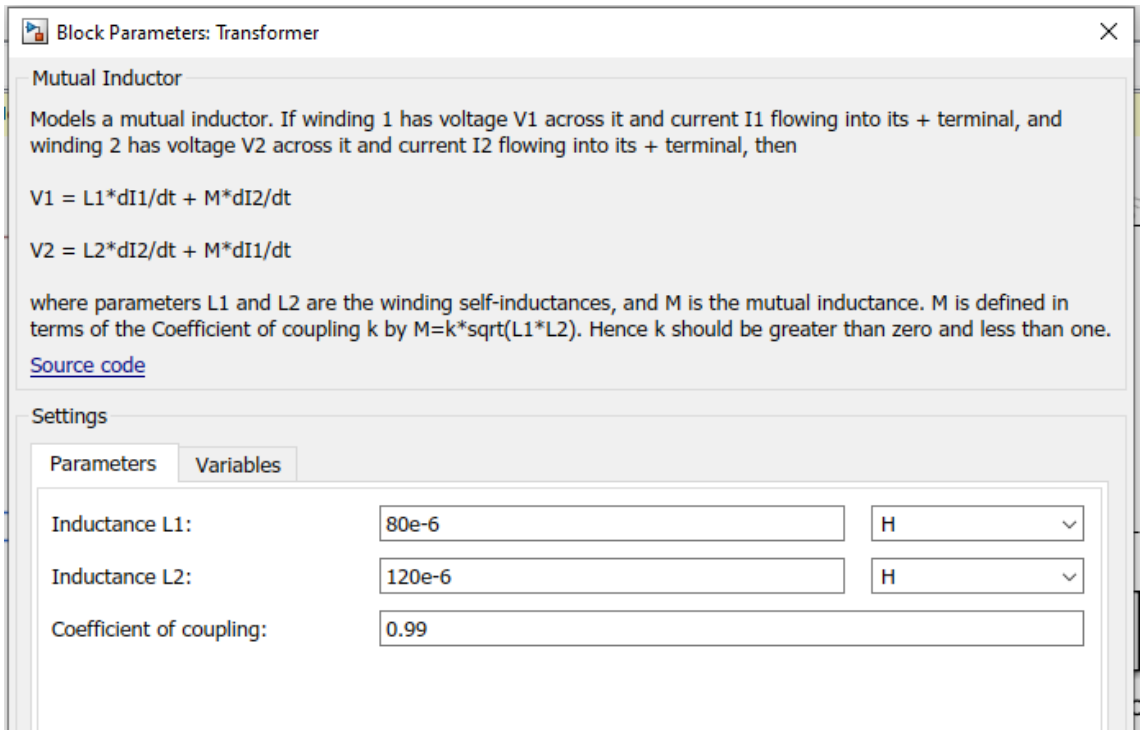


Figure B.3: Simulink transformer model

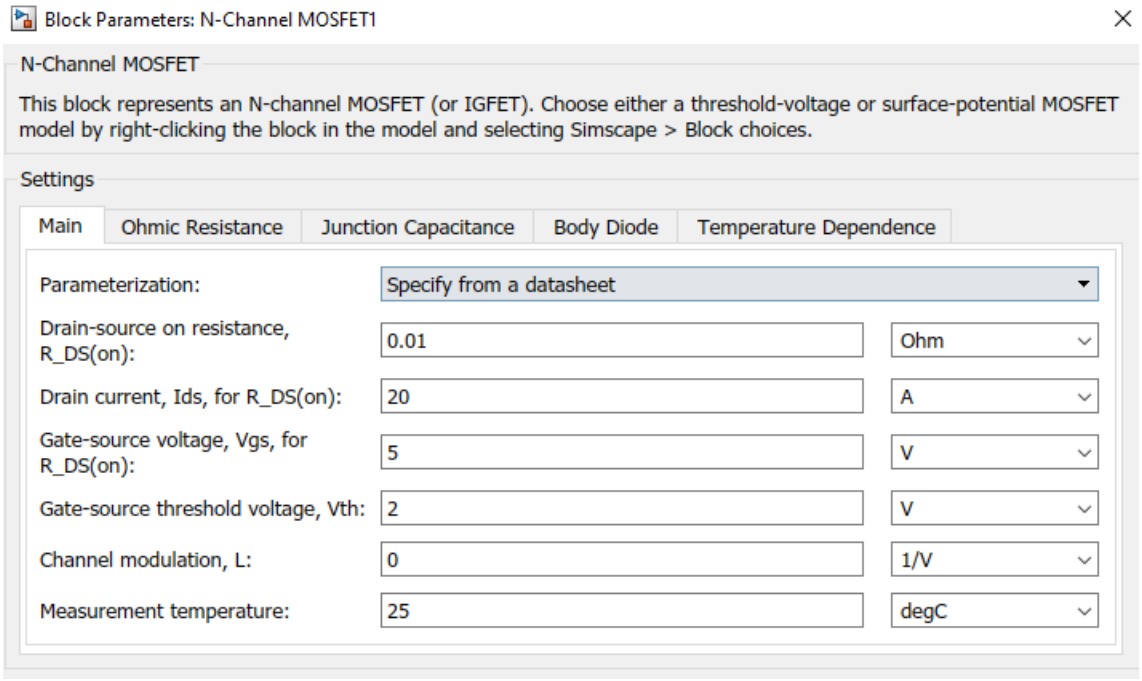


Figure B.4: Simulink MOSFET model used

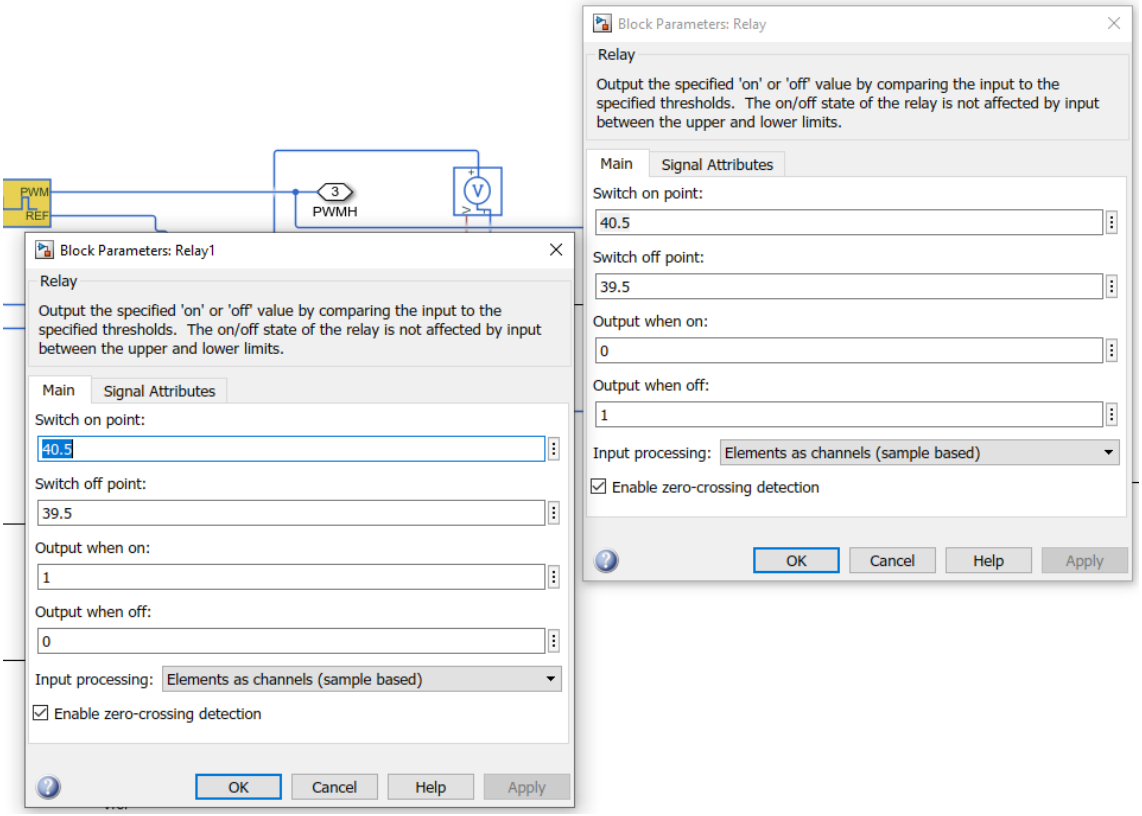


Figure B.5: Simulink relay models used for switches

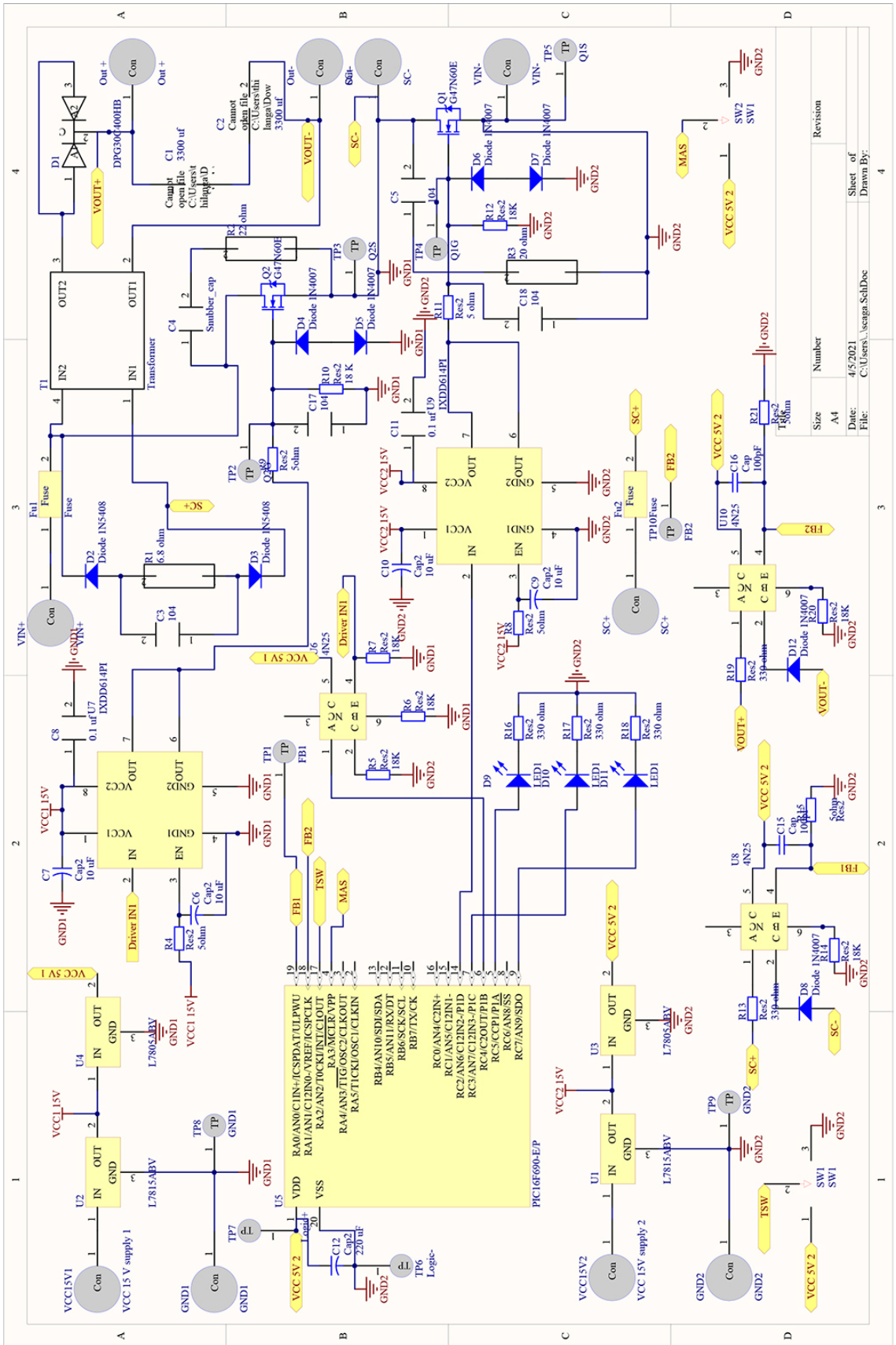


Figure B.6: Altium schematic for pre-regulator stage

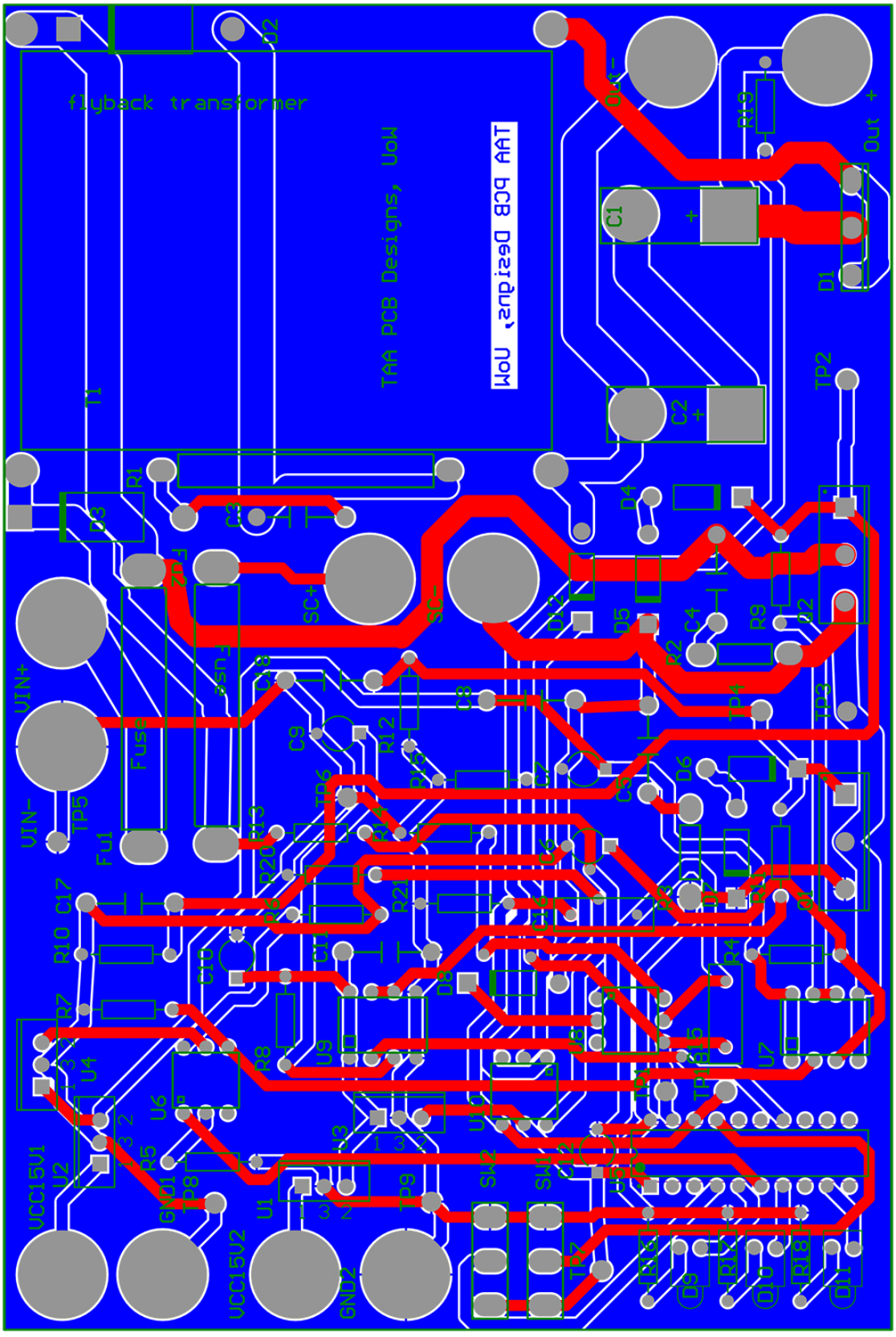


Figure B.7: Altium PCB design for pre-regulator stage

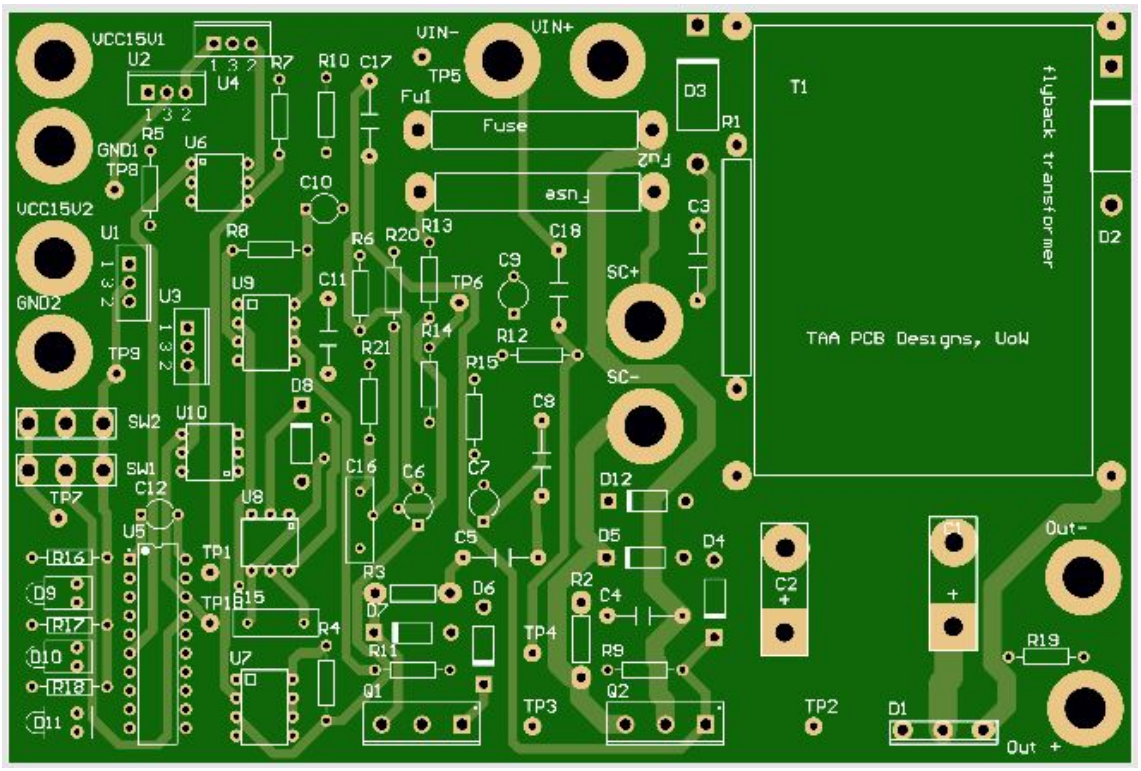


Figure B.8: Altium PCB front view

B.0.3 Pre-regulation stage PIC code

```
/*
 * File:   newmain.c
 * Author: thilanga
 *
 * Created on March 14, 2021, 3:47 PM
 */



#pragma config FOSC = HS        // Oscillator Selection bits (HS oscillator)
#pragma config WDTE = OFF       // Watchdog Timer Enable bit (WDT disabled)
#pragma config PWRTE = OFF      // Power-up Timer Enable bit (PWRT disabled)
#pragma config BOREN = OFF      // Brown-out Reset Enable bit (BOR disabled)
#pragma config CPD = OFF        // Data EEPROM Memory Code Protection bit (Data
    EEPROM code protection off)
#pragma config CP = OFF
#define _XTAL_FREQ 8000000

#include <stdio.h>
#include <stdlib.h>
#include <xc.h>
#include <pic.h>

int const DUTY_MAX = 50;
int duty_c;
int SC_MAX = 890;//4.35 V
int SC_MIN = 750;//4 V
int OUT_V = 274;//at $26 V pic input$
int TOGGLE_V = 260;//minimum output threhold for state change
int nc = 0;
int c_state = 0;//current state flyback = 0, forward = 1
unsigned int  sc_v, out_v,  sw3_v, sw4_v;//initial variable to store voltages

void flyback_mode(void){
    PORTC = 0b00001100;//RC3 LED indicates flyback
    PSTRCON=0b00001000;//switch on low side
    //CCPR1L = duty_c;//flyback_duty;
    return;
}

void forward_mode(void){
    PORTC = 0b00110000; //RC5 LED indicates forward
    PSTRCON=0b00000010; //switch on high side
    //CCPR1L = duty_c;//forward_duty;
    return;
}

void PWM_Init20(){
    //20kH
    T2CON = 0b00000100; // prescaler + turn on TMR2;
```

```
    PR2 = 0b01100011;
    CCPR1L = 50;  // set duty MSB DUTYMAX = 50
    CCP1CON = 0b00001100;
}

void ADC_Init()
{
   ADCON0 = 0x81; //turn on ADC and clock selection
   ADCON1 = 0x80; // all pins as analog inputs and setting reference voltage
   ADCON0 = 0b10000001;//reading RA0
   //ADCON0 = 0b10000101;//reading RA1
   __delay_ms(2);
}

void set_duty2(){

    if(out_v < OUT_V){//increase duty cycle when it got below
        if(duty_c < DUTY_MAX){
            duty_c = duty_c +1;
            CCPR1L = duty_c;
        }
    }
    else if(out_v > OUT_V){
        if(duty_c > 0){
            duty_c = duty_c - 1;
            CCPR1L = duty_c;
        }
    }
}


void ADC_Read_sw()
{
   ADCON0 = 0b10001001;
   __delay_us(5);//delay to aquare voltage
   GO_nDONE = 1;// initiating ADC conversion
   while(GO_nDONE); // waiting for the conversion
   sw3_v =  ((ADRESH<<8)+ADRESL); //return result

   ADCON0 = 0b10001101;
   //__delay_ms(2);
   __delay_us(5);
   GO_nDONE = 1;// initiating ADC conversion
   while(GO_nDONE); // waiting for the conversion
   sw4_v =  ((ADRESH<<8)+ADRESL); //return result

   //reading supercap voltage
   ADCON0 = 0b10000001;//reading RA0
   __delay_us(5);
   GO_nDONE = 1;// initiating ADC conversion
   while(GO_nDONE); // waiting for the conversion
   sc_v =  ((ADRESH<<8)+ADRESL); //return result
```

```
102
103     //reading output voltage
104     ADCON0 = 0b10000101;//reading RA1
105     __delay_us(5);
106     GO_nDONE = 1;// initiating ADC conversion
107     while(GO_nDONE); // waiting for the conversion
108     out_v =  ((ADRESH<<8)+ADRESL); //return result
109
110     //setting PWM;
111     set_duty2();
112 }
113
114 void main(void) {
115     //initialize the system
116     PORTA = 0x00;
117     TRISA = 0xFF; //analog pin as input
118     OSCCON=0x77;          // Select 8 MHz internal clock
119     TRISC = 0x00;         // Set All on PORTC as Output
120     ANSEL = 0x03;         // Set PORT AN0 to AN7 digital I/O
121     ANSELH = 0x00;        // Set PORT AN8 to AN11 as Digital I/O
122     PORTC = 0x00;         // Turn Off all PORTC
123
124     //initialising ADC register
125     ADC_Init();
126     PWM_Init20();
127     duty_c = DUTY_MAX;//set PWM duty cycle to max
128     flyback_mode();//initial state
129
130     do
131     {
132         ADC_Read_sw();
133         long auto_count=0;
134
135         while(sw3_v < 500){
136
137             if(auto_count > 12500 && c_state == 0 && out_v < TOGGLE_V){//change
    state when output voltage go below threshold value
138                 auto_count = 0;//cout is there to prevent unnecessary switching
    (to have a delay))
139                 c_state = 1;
140                 forward_mode();
141             }
142             else if(auto_count > 12500 && c_state == 1 && out_v < TOGGLE_V){
143                 auto_count = 0;
144                 c_state = 0;
145                 flyback_mode();
146             }
147             auto_count = auto_count + 1;
148             ADC_Read_sw();
149         }
150
151         //manual control switches
```

```
152         while(sw3_v > 500){
153              if(c_state == 1 && sw4_v > 500){
154                  c_state = 0;
155                  flyback_mode();
156                  //__delay_ms(3000);
157              }
158              if(c_state == 0 && sw4_v < 500){
159                  c_state = 1;
160                  forward_mode();
161              }
162             ADC_Read_sw();
163         }
164
165     }while(1);
166
167 }
```

Listing B.1: pre-regulation stage PIC code

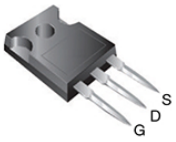
VISHAY
www.vishay.com

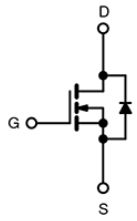
SiHG47N60E

Vishay Siliconix

E Series Power MOSFET

TO-247AC





N-Channel MOSFET

FEATURES

- Low figure-of-merit (FOM) R_{on} x Q_g
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ max. (Ω) at 25 °C	V_{GS} = 10 V	0.064
Q_g max. (nC)	220	
Q_{gs} (nC)	29	
Q_{gd} (nC)	57	
Configuration	Single	

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	SiHG47N60E-E3
Lead (Pb)-free and halogen-free	SiHG47N60E-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	600	V
Gate-source voltage			V_{GS}	± 30	
Continuous drain current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	47	A
		T_C = 100 °C		30	
Pulsed drain current [a]			I_{DM}	145	
Linear derating factor				3	W/°C
Single pulse avalanche energy [b]			E_{AS}	1800	mJ
Maximum power dissipation			P_D	357	W
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Drain-source voltage slope	V_{DS} = 0 V to 80 % V_{DS}		dV/dt	70	V/ns
Reverse diode dV/dt [d]				11	
Soldering recommendations (peak temperature) [c]	for 10 s			300	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 73.5 mH, R_g = 25 Ω, I_{AS} = 7 A
c. 1.6 mm from case
d. $I_{SD} \leq I_D$, dI/dt = 100 A/µs, starting T_J = 25 °C

Figure B.9: sihg47n60e data sheet

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	0.33	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	600	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 250 µA	-	0.66	-	V/°C
Gate-source threshold voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2	-	4	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
		V_{GS} = ± 30 V	-	-	± 1	µA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 480 V, V_{GS} = 0 V, T_J = 125 °C	-	-	10	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 24 A	-	0.053	0.064	Ω
Forward transconductance	g_{fs}	V_{DS} = 8 V, I_D = 3 A	-	6.8	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	2405	4810	9620	pF
Output capacitance	C_{oss}		115	230	460	
Reverse transfer capacitance	C_{rss}		1.7	5	10	
Effective output capacitance, energy related [a]	$C_{o(er)}$	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	170	-	
Effective output capacitance, time related [b]	$C_{o(tr)}$		-	604	-	
Total gate charge	Q_g	V_{GS} = 10 V; I_D = 24 A, V_{DS} = 480 V	74	148	220	nC
Gate-source charge	Q_{gs}		14.5	29	58	
Gate-drain charge	Q_{gd}		28.5	57	86	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 480 V, I_D = 24 A, V_{GS} = 10 V, R_g = 4.4 Ω	14	28	56	ns
Rise time	t_r		36	72	108	
Turn-off delay time	$t_{d(off)}$		47	93	140	
Fall time	t_f		41	82	123	
Gate input resistance	R_g	f = 1 MHz, open drain	0.13	0.65	1.3	Ω
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode	-	-	47	A
Pulsed diode forward current	I_{SM}		-	-	140	
Diode forward voltage	V_{SD}	T_J = 25 °C, I_S = 24 A, V_{GS} = 0 V	-	-	1.2	V
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = I_S = 24 A, dI/dt = 100 A/µs, V_R = 25 V	-	582	1164	ns
Body diode reverse recovery charge	Q_{rr}		-	11	22	µC
Reverse recovery current	I_{RRM}		-	31	62	A
Body diode reverse recovery time	t_{rr}	T_J = 25 °C, I_F = I_S = 24 A, dI/dt = 100 A/µs, V_R = 400 V	-	550	1164	ns
Body diode reverse recovery charge	Q_{rr}		-	10.7	22	µC
Reverse recovery current	I_{RRM}		-	38	62	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

Figure B.10: sihg47n60e data sheet

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