Supercapacitor assisted LDO (SCALDO) technique- an extra low frequency design approach to high efficiency DC-DC converters and how it compares with the classical switched capacitor converters

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***Abstract*—Supercapacitor assisted low dropout regulators (SCALDO) were proposed as an alternative design approach to DC-DC converters, where the supercapacitor circulation frequency (switching frequency) is in the order of few Hz to few 10s of Hz, with an output stage based on a low dropout regulator stage. For converters such as 12-5V, 5-3.3V and 5-1.5V, the technique provides efficiency improvement factors of 2, 1.33 and 3 respectively, in compared to linear converters with same input-output combinations. In a 5-1.5V SCALDO regulator, using thin profile supercapacitors in the range of fractional farads to few farads, this translates to an approximate end to end efficiency of near 90%. However, there were concerns that this patented technique is merely a variation of well-known switched capacitor (charge pump) converters. This paper is aimed at providing a broad overview of the capability of SCALDO technique with generalized theory, indicating its capabilities and limitations, and comparing the practical performance with a typical switched capacitor converter of similar current capability.**

I. INTRODUCTION

Commonly used techniques for DC-DC converters are (i) linear regulators (ii) switch-mode converters (iii) switched capacitor converters. In many portable products such as cellular phones, digital cameras, portable computers and smart phones power management system (PMS) is developed by mixing these three techniques to achieve best run time from a fully charged battery. In powering up mixed signal circuit blocks and RF circuits, RFI/ EMI issues in PMS could be a significant factor, while high current processor blocks may demand a DC rail with high current slew rate capability. Considering the advantages and disadvantages of each of these approaches, there is no single winner out of these three techniques. Commercial low dropout regulators (LDO) are very commonly used in portable electronic products, usually in tandem with switching regulators to offer low noise and fast current slew rate capability at the output [1-6]. This concept is commonly called point of load (POL) [7] and most portable devices are designed using weighted average efficiency concepts [8] to achieve the best run time from battery packs.

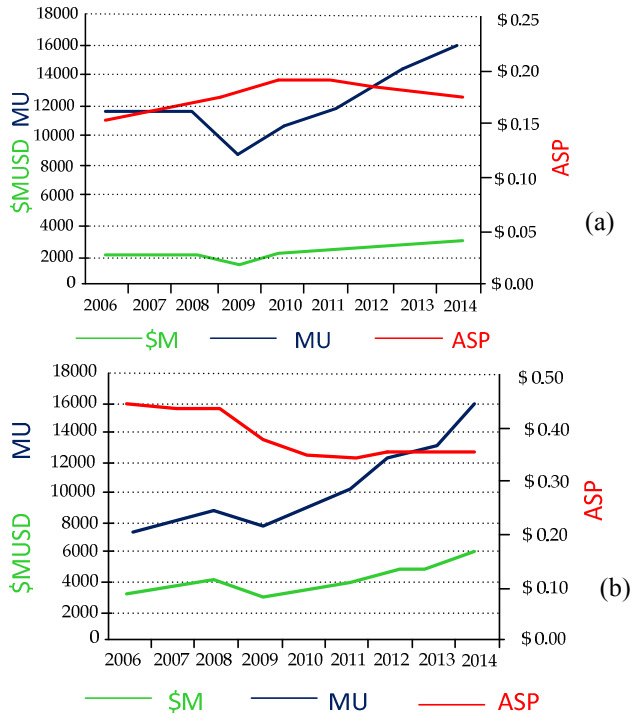


Figure 1. Worldwide market forecast as per market search reports (a) Switching regulators (b) LDO regulators (Source [9])

As per recent market research reports from Databeans indicate [9], LDO ICs are a large share of commercial power management IC market. Fig. 1 illustrates the commercial utilization of LDO and switching regulator families with predictions for the future years as per market search reports from Databeans Corp, USA [9], indicating the total business potential in millions of dollars (lower trace-$M), total unit sales in million units (middle trace-MU) and the average selling price (upper trace-ASP) of these components.

Making use of the known advantages of LDOs, new research and development directions [10-19] have indicated that supercapacitors with very low ESR values can be combined with LDOs to achieve high efficiency DC-DC converters, while keeping the switching frequency at extra low values such as few Hz to few 100s of Hz. In this technique supercapacitors are used as lossless voltage droppers to reduce the losses in the series path of a linear regulator. Following sections will provide a brief theoretical background (an overview only, with ideal supercaps), different possible configurations and some experimental results indicating how the technique differs from the classical switched capacitor converters.

II. BASISC THEORY

Fig.1 indicates the concept, where an array of *n* (identical) series supercapacitors, capacitance C_{sc} each, is placed in series with the input of the LDO. As the resultant capacitance of the series array is quite large, and in the order of fractional farads to few farads, it will not act as a blocking element for a reasonable period of time. In the first part of the cycle (Fig 2(a)), due to supercapacitor charging, the value of LDO input voltage, vin is dropped down to its minimum possible input voltage which is $V_{\text{in (min)}}$. In the second part of cycle, reconfigured supercapacitor array (all capacitors parallel in this phase) is connected to the input of the LDO as shown in Fig. 2(b) to reuse that stored energy in the supercapacitors until its terminal voltage drops back to $V_{\text{in (min)}}$.

Assuming that the supercapacitors are ideal with zero ESR, and the ground pin current of the LDO (hence the current consumed by control circuits) is zero, with t_1 and t_2 are the respective times for charging and discharging where, full cycle $T=t_1+t_2$, following relationships can be established.

Considering the charge balance of a single capacitor, $C_{sc,}$ during the entire cycle of duration *T*,

$$I_L t_1 = \frac{I_L}{n} t_2 \text{ which gives } t_2 = n t_1 \tag{1}$$

The average input current from the unregulated power supply during the entire cycle T is,

$$I_{avg} = \frac{I_L t_1 + 0 \times t_2}{t_1 + t_2} = \frac{I_L t_1}{t_1 + n t_1} = \frac{I_L}{1+n} \tag{2}$$

Therefore the end-to-end power efficiency of the generalized SCALDO regulator is given by ,

$$\eta = \frac{I_L V_{reg}}{I_{avg} V_p} = \frac{I_L V_{reg}}{\frac{I_L}{1+n} V_p} = (1+n)\frac{V_{reg}}{V_p} \tag{3}$$

For a SCALDO regulator, when n=1 as applicable to a case of 12-5V regulator, the efficiency of the regulator is,

$$\eta = (1+1)\frac{V_{reg}}{V_p} = 2\frac{V_{reg}}{V_p} \tag{4}$$

The above discussion based on the situations where $V_p - V_{in\ (min)}$ is much larger than $V_{\text{in (min)}}$ for the LDO.

In another possible practical case, an array of *n* parallel (identical) supercapacitors are connected in series with the LDO as shown in Fig.3(a) to keep the supercapacitors charging from the unregulated power supply during the first part of the cycle, while the LDO stage $V_{\text{in(min)}}$ keeps regulation of the output. At the end of charging when $V_{\text{in (min)}}$ for the LDO is reached, the controller transfers the switches to keep the group of supercapacitors in the series configuration as shown in Fig. 3(b) to release the stored energy into the LDO in order to keep the LDO working.

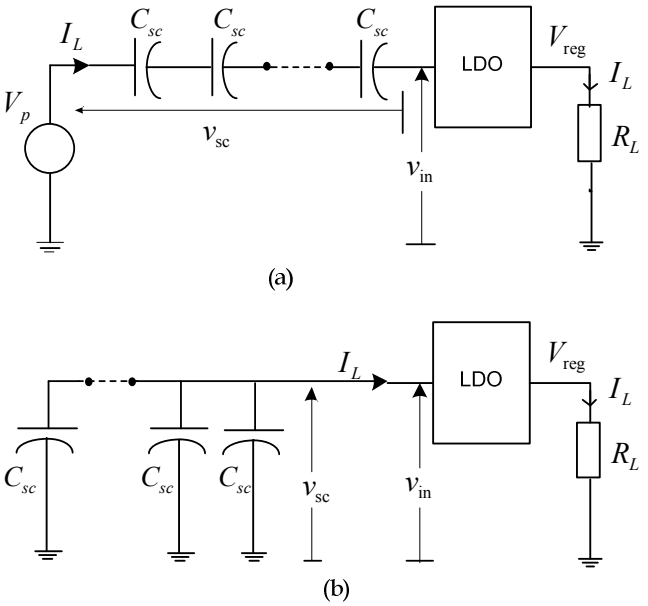


Figure 2. Concept of SCALDO regulator for Vp >(1+n)Vin (min) configuration (a) capacitors charging in series (b) capacitors discharging in parallel

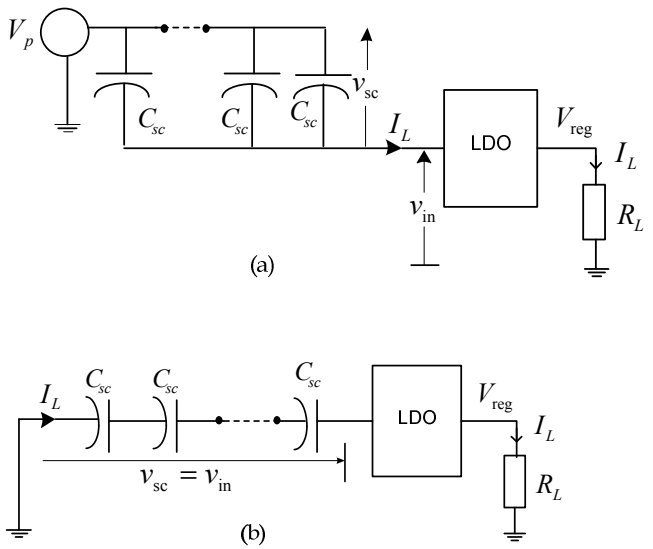


Figure 3. Concept of SCALDO regulator for Vp > (1+1/n)Vin (min) configuration (a) capacitors charging in parallel (b) capacitors discharging in series

Similarly, the end-to-end efficiency for the case shown in Fig. 3 can be derived as,

$$\eta = (1 + \frac{1}{n}) \frac{V_{reg}}{V_p} \qquad (5)$$

Applicability of the above configurations in practical DC-DC converters, demands the condition that the LDO input is always maintained within its specified range and this translates to several possible cases, which are summarized in the Table I. More details are in [11-19]. Based on Eqns. (3) and (5) it is important to note that by adjusting the parameter *n*, and, selecting input/output voltages, very high end-to-end efficiencies can be achieved. For example, if you require to build a 5V regulator from a unregulated nominal input voltage of 10.5, your configuration could work with a single supercapacitor, and 4 low speed switches, giving an estimated efficiency of (1.1)*(5/10.5) which works out to an efficiency value of 95.2%. Similarly for a case of 1.5V output from an unregulated input voltage of 4.8V nominal with 2 supercapacitors and seven low frequency switches, targeted ideal efficiency could be 93.7%.

III. APPLICATIONS

Given the above theoretical background, there are many possible configurations of this supercapacitor energy recovery technique to combine with an LDO. All these are basically step-down topologies. Few simple configurations are discussed in summary form using the details in the Table I given below. Table I depicts the details of three common configurations with respect to the use of switches and supercapacitors. Figs. 4(a) and 4(b) indicate the theoretical and measured efficiencies applicable to 12-5V and 5-3.3V proof of concept circuits. In these two figures the upper traces indicate the theoretical performance of the supercapacitor technique; middle traces indicate the practical performance of the supercapacitor technique; and, performance of standard linear regulator is shown by the lower traces. Figure 4(c) indicates the efficiency of charge pump type 5V regulator (TPS 60510).

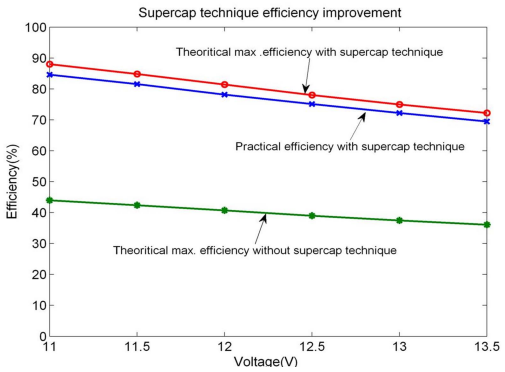
TABLE I. STYLES COMPARISON OF FEW COMMON LINEAR REGULATORS WITH SCALDO CONFIGURATIONS

Converter configuration	12V- 5V	5V - 3.3V	5V -1.5V
Applicable case	$V_p > 2\ V_{in(min)}$	$V_p < 2\ V_{in(min)}$	$V_p > 3V_{in(min)}$
Max theoretical end-to-end efficiency without SCALDO	42%	66%	30%
No. of supercaps used (n)	1	3	2
No of Switches required(k) [k=3n+1]	4	10	7
Efficiency improvement factor (η_r)	2	1.33	3
Estimated efficiency with SCALDO technique	84%	88%	90%

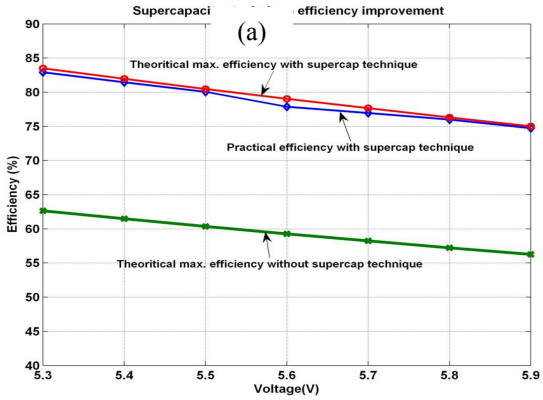
Given the high end-to-end efficiency, the technique can be easily applied to AC-DC converters or DC-DC converters, to provide commonly used output voltages such as 12V, 5V, 3.3V and 1.5V or lower DC rail voltages. More analytical and implementation details will be available in [18, 19]. Transient response of the overall technique, which is important in powering processor based systems discussed in [11].

IV. COMPARING THE NEW TECHNIQUE WITH SWITCH CAPACITOR CONVERTERS

Switch capacitor converters, commonly known as charge pumps [20] are popular DC–DC converter circuits to achieve a DC voltage higher than the supply voltage or with reverse polarity, based on high frequency switching. Lot of development work has happened in the last decade and some are indicated in [21-23]. On-chip charge pump converters are widely used in non-volatile memory circuits, dynamic random access memory circuits, low voltage circuits, continuous time filters, and RS-232C transceivers [21].



(a)



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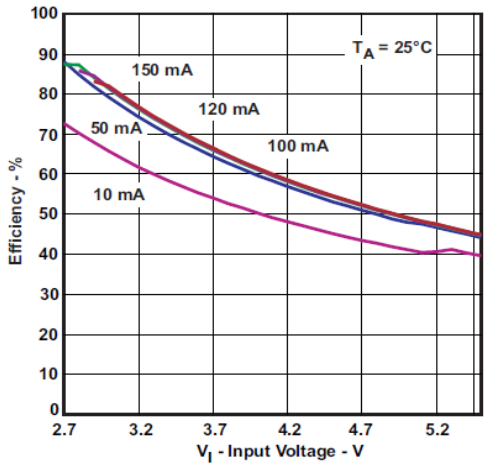


(c)

Figure 4. Graphs showing efficiency achievements for two different cases of SCALDOs and a typical charge pump (a) 12-5V SCALDO regulator (b) 5-3.3V SCALDO regulator (c) Voltage doubler charge pump for a typical (TPS 60510) 5V output with 150mA load current capability[25].

In order to compare the SCALDO technique with charge pump converters, in Fig. 5, a simple voltage doubler and inverter are considered. The doubler circuit in Fig. 5(a), which consists of a single capacitor and four switches, indicates the basic concept of the switch capacitor converter. The charge pump capacitor, C, is charged to the input voltage during the first half of the switching cycle. During this phase, switches S_1 and S_3 are closed; $S_2$and S_4 are opened and the capacitor C is connected in parallel to the supply voltage V_p and it gets charged up to V_p. During the second half of the switching cycle, switch S_2 and S_4 are closed; S_1 and S_4 are opened, and, C the pump capacitor is placed in series with the supply voltage V_P. The capacitor maintains its charge of V_PC from the previous phase. This means that during the release phase of circuit operation,

$$\left[V_{reg} - V_P\right]C = V_P C$$

or

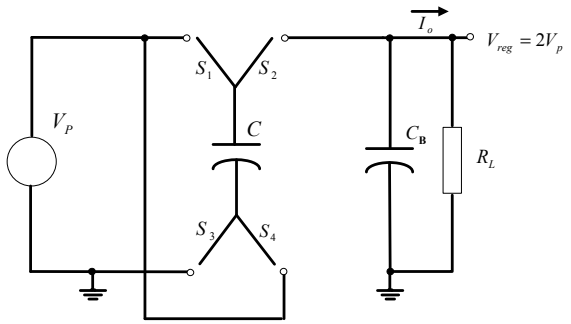
$$V_{reg} = 2\,V_P \qquad (6)$$

Thus, in the absence of a DC load, an output voltage has been generated that is twice the supply voltage.

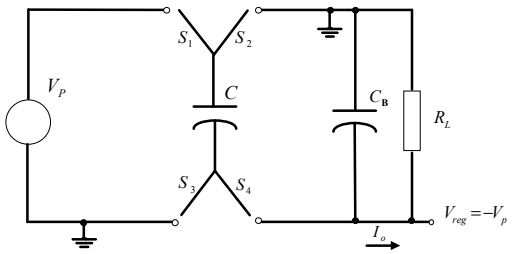
In the case of switch capacitor voltage inverter, in Fig. 5(b), switches S_1 and S_3 are closed; S_2 and S_4 are opened, the charge pump capacitor, C, is charged to the input voltage during the first phase of the switching cycle. During the next phase, switches S_1 and S_3 are opened; and, S2 and S_4 closed. Its voltage is inverted and applied to the load.

Fig. 6 shows the functional block diagram of TPS60150 switched capacitor voltage converter from Texas Instruments which produces a regulated output voltage of 5V for various input voltages [25]. Three external capacitors are required to generate the output voltage. The TPS60150 regulates the voltage across the flying capacitor, C_F to 2.5V and controls the voltage drop across switches while a conversion clock with 50% duty cycle drives the FETs. During the first half cycle, C_F will be charged to 2.5V ideally. During the second half cycle, C_F will then be discharged to output [25].

Compared to linear or switching regulators, the output voltages of the charge pump circuits are usually not regulated and they are designed to operate at a fixed switching frequency (of few 100 kHz) with a rated output load current and voltage. Because of practical limitations on the size of capacitors and switches, applications of charge pumps are limited mainly to low and medium power levels of several tens of milliwatts**.** This is clearly visible in Fig. 4(c) indicating the typical efficiency of a commercial charge pump (TPS 60510) from Texas Instruments, when compared with SCALDO results in Fig. 4 (a) and (b).



(a)



(b)

Figure 5. Basic principle of charge-pump circuits (a) Doubler circuit (b) Inverter circuit

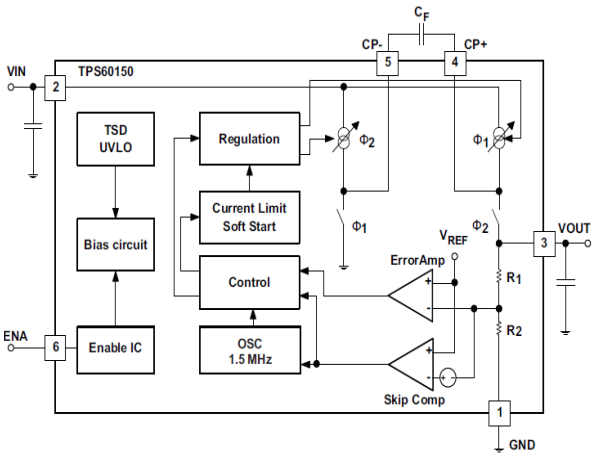


Figure 6. Block diagram of TPS60150 Switch capacitor voltage regulator[25]

Given the above simple summary, it is very clear to see that the SCALDO technique is quite different to the operation of charge pumps, due to three primary reasons (i) it uses a capacitor as a lossless voltage dropper, together with a linear low drop out regulator for precise output regulation (ii) extremely low switching frequency is variable, and, depends on the load current (iii) if an ultra LDO can be developed for the required output current, there is no limit to precise output regulation at high load currents. Third reason is due to the availability of single cell (commercially available) supercapacitors are in the range of fractional Farads to few 1000 Farads. Table II provides more details comparing the two techniques.

Given a summary of charge pump basics and the generalized theory of SCALDO technique, it is important to note that in the SCALDO approach capacitors are not used for any DC-DC conversion purpose. Very small ESR in modern supercapacitors (compared to much lower on-resistance of typical power MOSFETS), allows the designer to practically develop the approximate case of a lossless voltage dropper in the series path. SCALDO technique can be extended to provide high output currents in the order of 5 to 50A at DC rail voltages suitable for modern processors.

TABLE II. A COMPARISON SUMMARY OF SWITCHED CAPACITOR CONVERTERS AND THE SCALDO TECHNIQUE

Switched capacitor (charge pump) technique	**SCALDO Technique**
Basically a high frequency technique for voltage conversion.	A modified version of a linear regulator with a capacitor front end
Practically used to up-convert or invert a DC voltage.	Always a step-down configuration
Capacitors are in from few nF to few tens of μF.	Enormously large capacitors are used.
Fixed oscillator provides the switching frequency	Frequency is variable and depends on the load current.
Very high switching frequency (10 to few 100 kHz)	Extra low frequency (10Hz to few 100Hz)
Load regulation is not precise	Load regulation is provided by a linear-low drop out regulator
In one part of the cycle capacitor goes parallel to unregulated supply	Capacitor never comes parallel to the input unregulated supply
Technique is suitable only for very low load currents	Technique is applicable to very large load currents.
Significant dynamic losses in switches.	Negligible dynamic losses in switches.
Theoretically a voltage conversion factor for a given configuration	Theoretically an efficiency multiplication factor for a given configuration

V. CONCLUSION

Paper provides the essential design aspects of the SCALDO technique, highlighting its applicability to achieve very high end to end efficiency for DC-DC converters. It also provides a clear explanation to confirm that the new technique is not a variation of switched capacitor DC-DC converters.

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