High power linear AC Electronic Load for testing UPS Systems

A thesis submitted in partial fulfillment of the

requirements for the degree of

MASTER OF ENGINEERING

at

The University of Waikato

Hamilton, New Zealand

By

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THE UNIVERSITY OF
WAIKATO
Te Whare Wānanga o Waikato

2007

To

My Loving Amma and Thaththa

Abstract

Concept of a series bipolar transistor array for AC power control is already developed. However non-linearity issues, high power capability with load sharing at high voltages and digital control with better transient performance were not adequately adopted in early-developed stages.

This thesis is a description of the design approach of digitally controllable linear 230V/50 Hz AC line voltage capable electronic load with predictable characteristics based on spice simulation. The BJT array used in this project provides high power dissipation capability and uniform voltage and power distribution across the individual transistors. A set of optoisolators are used to have electrical isolation between power stage and digital control circuits. A Zilog Z8Encore! 64K series development kit is used in controlling the circuit.

Acknowledgements

First and foremost I would like to place on record my deep gratitude to those who encouraged me in this difficult task of preparing the thesis. Especially to my mother and my sister who pray for me and encourage me at very difficult situations during this period.

Mr. Nihal Kularathne was my supervisor for this research and I am really grateful for his guidance, encouragement and for the motivation throughout the whole period. It was a grate honour for me to have had the chance to work with him. I certainly could not have come this far without his assistance.

My thanks go to several technical staff members for their enormous support given to me at all times. Thanks to Michel Crosgrove for his generous support in finding me equipment, purchasing electronic components and making PCB's. Stuart Finlay was always concerned about my safety as I was handling high voltages for this research. Thanks to Stuart Finlay for his valuable advice and supplying me an isolation transformer and safety switches.

When I was struggling with programming microcontrollers at the latter part of my research, a friend Terry Cavo taught me to overcome the situation. I am grateful to Terry for his massive effort. I am also grateful to my sincere friends Tissa Senanayake and Mahima Senanayake for giving me their full support in finding the equation for the data obtained.

I had to learn C programming for this research and Daniel Ho helped me in obtaining valuable books to learn the essentials. Thanks to Daniel Ho for the great support and

useful hints. I would also like to thank Richard Conrey for his discussions and helpful comments to make my project success.

While writing this thesis, my sincere friends Uma Paranawidana and Ruwan Paranawidana have given me a big hand in several ways. Thanks to Uma and Ruwan for their unforgettable assistance on this daunting task. I would also like to thank Heidi Eschmann for helping in photocopying and scanning of documents.

My family has put up with a lot in the past eighteen months and their support has never been forgotten. Thanks to my husband Galinda and my little son Rowin for your patience, support and encouragement.

M.D.C.S.K. Jinadasa

University of Waikato
Hamilton, New Zealand
November 2007

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Chapter 1

Introduction

1.1 Background

With the development of technology related to power electronics and power conversion systems, testing methods for design verification and product function require sophisticated electronic equipment. The different power supply architectures and output combinations also dictate the need for versatile test instruments that can accommodate a broad range of specifications. As a result, one testing requirement that has been growing in importance is the method of loading a power supply under test. The need for a higher degree of load control due to test sophistication, such as the need for computer programmability, has increased the demand for programmable electronic loads.

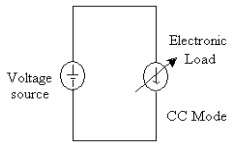
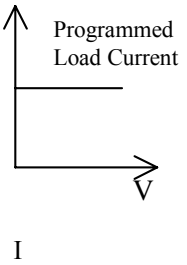
1.2 Electronic Loads

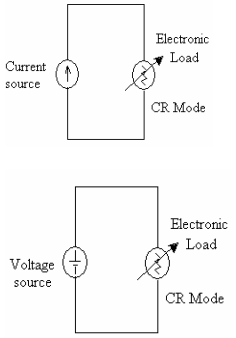
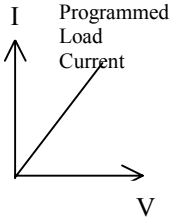
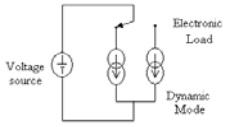
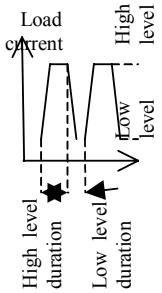
Electronic load is a combination of circuits designed to provide a variable load at the outputs of a power supply, usually capable of dynamic loading and frequently programmable. An electronic load offers a broad range of operating modes, providing versatile loading configurations needed for characterizing and verifying power supply design specifications.

Loads can be resistive, inductive or capacitive. Real load behavior is typically more complex. They are in different emulation modes of operation and these loads can be controlled by microcontrollers. DC Electronic loads can be constant voltage (CV), constant current (CC), constant resistance (CR), dynamic and also short circuit type. AC electronic load can be constant mode and rectified mode. Constant mode includes constant current (CC), constant resistance (CR) and constant power. Rectified load mode includes crest factor (CF), power factor (PF) and short circuit load.

Among these different loads CC mode has the highest performance and dynamic loads are very important in testing Uninterrupted Power Supply (UPS) systems. Dynamic loads are more expensive than the other loads [1]. CR mode is only mode of AC loads that can be used to test discontinuous square wave or quasi-square wave units under test.

Following table explains the basic types of loads used in industry for testing power supplies [2].

Description	Applications	Circuit model	Characteristics
Constant current mode (CC mode): AC /DC Current will sink accordance with the programmed value regardless of the input voltage. Load regulation is the power supply's ability to provide a stable output voltage under load variations. It is specified as a percentage deviation from normal output at a fixed input voltage and is calculated using the following formula $\%L.\mathrm{R} = \frac{V_{o(\max)} - V_{o(\min)}}{V_{o(normal)}} x100$	Used to test voltage sources and load regulation of AC and DC power supplies		

Constant Voltage (CV) mode: DC only Electronic loads will sink in enough current (if available) to control the source voltage to the programmed value.	Used to test current source. It is frequently used to test current limit characteristic of power supplies. It can also be used for testing battery chargers where CV mode load can emulate a battery's terminal voltage.		
Constant Resistance (CR) mode: AC/DC Electronics loads will sink a current linearly proportional to the input in accordance with the programmed resistance	Used to test either voltage or current sources, and is normally used in testing power source start up and current limit.		
Dynamic load: DC only Dynamic load operation causes electronic loads to periodically switch between two load levels. A power T pply's regulation and transient response can be evaluated by monitoring its output voltage under varying combination of load High/ Low current levels, High/ Low current level duration, and Rise/ Fall slew rate.	Used to test the transient response of a power supply. Most commonly used loads are dynamic. -		

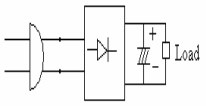
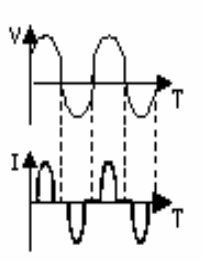
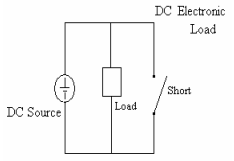
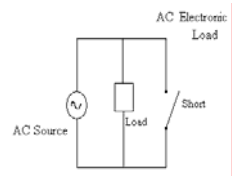
Crest Factor load (CF): AC only Crest factor is the ratio of the peak value to the rms value of a load current waveform. This term is often used to specify the maximum peak amplitude the AC power supply or UPS can source (relative to its maximum rms rating) without di $Crest\ \ Factor = \frac{I_{peak}}{I_{rms}}$	Most power-input circuitry (without power factor correction) consists of a rectifier diode and capacitor filter circuit, which generates a pulse AC line current. CF loads are used to simulate this current waveform		
Power Factor Load: AC only Power factor is the ratio of average power value to the product of V_{rms} and I_{rms}. $P.F = \frac{P_{av}}{V_{rms}\ x\ I_{rms}}$	These are the first active AC loads to simulate inductive and capacitive load by programming the power factor from 0 to unity		
Short Circuit Load: AC/ DC An AC/DC power supply's output terminals having very low resistance. A power supply's protection circuit should be activated to limit the currant output when this condition exists (Short circuit).	Used to simulate the short circuit conditions.	 	

Table 1: Different AC and DC loads

1.3 Testing of Power Supplies

Power supplies are used in a wide variety of products and test systems. As a result, the tests performed to determine operating specifications could differ from manufacturer to manufacturer or from end user to end-user. For instance, the tests performed in R&D environment are primarily for power supply design verification. These tests require high performance test equipment and a high degree of manual control for bench use. In contrast, power supply testing in production environments primarily focus on overall function based on the specifications determined during the products design phase. Automation is often essential due to large volume testing, which requires high-test throughput and test repeatability. Power supply test instruments must then be computer programmable. For both test environments, measurement synchronization is necessary to perform some tests properly and to obtain valid data. Proper selection of test gear will provide the best combination of measurement sophistication and test set programmability.

There are certain instruments that are essential to all tests, regardless of the implementation. They are electronic loads, digital oscilloscopes, digital multimeters, true rms Voltmeters, Watt meters, and ac power sources. Electronic loads can facilitate power supply testing in several ways. They are typically programmable. This capability enables finer control over loading values during testing. Electronic loads are usually designed with transistors, which provide increased reliability and easy programmability.

1.3.1 Testing of DC power supplies

DC power supply testing includes tests of,

- Load transient recovery time

  This is the time required for the output voltage of a power supply to settle within a predefined settling band following a load current induced transients as shown in the Figure 1.1.

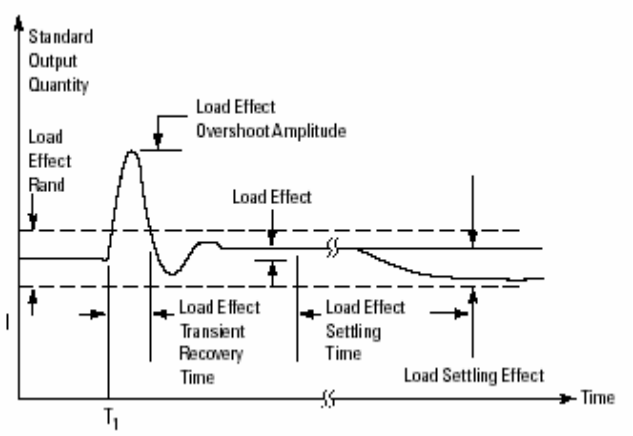


Figure 1.1: Load transient recovery time [3]

- Load effect (load regulation)

  Load effect or load regulation defines the ability of a power supply under test to remain within specified output limits for a predetermined load change as shown in the Figure 1.2.

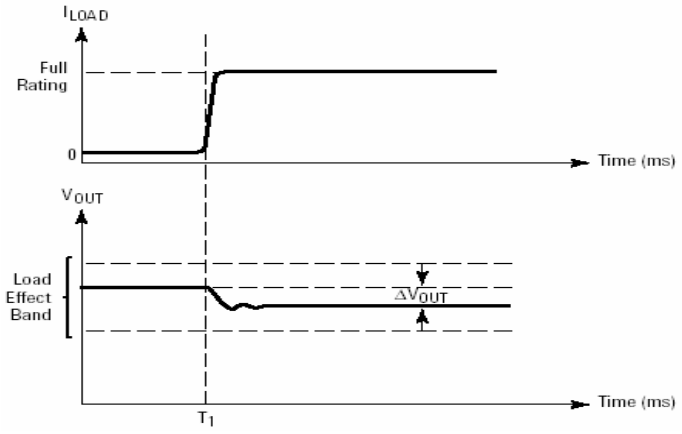


Figure 1.2: Load effect

- Current limit characterization

  Current limit measurement demonstrates the degree to which a constant voltage power supply limits its maximum output current to a preset value. Figure 1.3 shows typical operating characteristics of three types of current limiting power supplies [3].

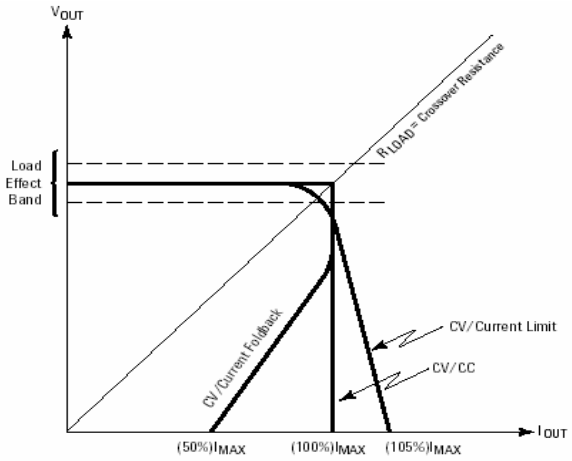


Figure 1.3:Typical Operating Characteristics of Three Types of Current Limiting Power Supplies

- Periodic and random deviation (PARD)

  PARD is the periodic and random deviation of the DC output voltage from its average value, over a specified bandwidth and with all other parameters constant [3]. This represents the noise and similar random deviation at the output of a power supply.

- Efficiency

  Efficiency of a power supply is simply the ratio of total output power to its total input power.

- startup delay

  Startup delay of a power supply is the amount of time between the application of ac input and the time at which the outputs are within their regulation specifications.

In order to effectively carryout these tests maximum ratings of voltage, current and power capability of the loads should be higher than those of the power supply to be tested. For dynamic tests, loads are required to change their outputs at fast slew rate and therefore electronic loads are preferred. In testing the load transient response, it is necessary to produce fast changes in load current in the range of 10A/μs to 100A/μs and the easiest way of doing it is the use of an electronic load, which employs solid state switching [4].

1.3.2 Testing of AC power systems

Systems such as automatic voltage regulators, power conditioners, and UPS systems require loads which can act as variable AC loads, which are capable of polarity reversal across the load. A test of UPS includes functional load testing, checking the protection settings and calibration of the unit [5]. Loads can be three phase or single phase. The work in the thesis is on single phase loads.

Functional load testing of an AC-AC converters can be divided into different operations. They are

- Steady state load test

  Under a steady-state test, checking of all input and output conditions at 0%, 50%, and 100% and testing of the following parameters: input voltage, output voltage, input current, output current, output frequency, input current balance for a three phase input, and output voltage regulation load is done. The analysis will reveal if input currents match across all phases of a module as well as determine if all modules equally share the load.

- Harmonic analysis

  Monitoring of the input and output of the AC-AC converters for harmonic content during the steady-state load test. Observing the harmonic content at 0%, 50%, and 100% load allows to determine the effectiveness of the input and output filters.

- Filter integrity

  The filter integrity tests indicate the failure of inductors and capacitors in the filters in AC-AC converters. Performing a relative phase current balance is a simple means of checking filter integrity.

- Transient response load test

  The transient response test simulates the performance of the AC-AC converters with large instantaneous swings in load.

- Module fault test

  Module fault test is performed to verify that the multi module system continues to maintain the critical load in the event of a module failure. The system should continue to maintain the load without significant deviation of voltage or frequency as verified by a recording oscillograph.

- Battery rundown test

  Battery rundown test detects the condition of the battery system and is simply done by measuring temperature, voltage, and current under load conditions.

These kind of testing are very expensive and variable loads are required to perform the tests. The best kinds of loads suitable for testing are electronic AC loads that can give constant load mode and rectified load mode [6].

Compared to a DC load, during load testing of an AC output systems, an AC load may require a good linearity property of the impedance at different instantaneous voltages of the AC cycle. If the load is not perfectly linear, the load current will create harmonics of the 50Hz or 60Hz AC line frequency. Therefore Total Harmonic Distortion (THD) measurement of AC output systems become an important issue.

Total Harmonic Distortion (THD) is essentially a measure of deviation from a perfect sinusoidal wave. THD is the ratio, expressed as a percentage, of the rms value of an AC signal after the fundamental component is removed to the rms value of the fundamental component. THD of current can be defined as;

$$THD = \frac{\sqrt{I_2^{\,2} + I_3^{\,3} + I_4^{\,4} ..... + I_n^{\,n}}}{I_1^{\,1}}$$

Linearity of a load can be determined by the THD of the load current. IEE Std-519 applicable harmonic limits, IEEE Recommended practices and requirements of harmonic control in electrical power systems specify the harmonic limits for utilities and consumers [5].

In an AC output system, the output voltage waveform may not be purely sinusoidal. In testing these, a load with sufficient linearity may be required.

A load with a high THD requires more energy to sustain than a load with low THD. The wasted energy dissipates as heat. That makes the load inefficient. To test UPSs etc. with high THD it is necessary to select loads with low THD to avoid the unnecessary heating of the UUT.

Selection of an electronic load for a particular test requires an analysis of performance specifications and product features. Input specifications include power, voltage, current and frequency. Measurement type, efficiency and emulation mode are other considerations while selecting a load.

1.4 Requirements

Development of an AC load with high voltage and high current capability and with very low THD and fast switching capability to test AC-AC converters is the aim of this research.

As discussed in section 1.3 an AC electronic load need to be developed to work under 230V/50Hz or 110V/60Hz.Generally the maximum voltage across the load will be 230√2V for 230V/50Hz system. Also they should have high power capability for testing of power conditioning systems such as UPS/Automatic Voltage Regulator /Power Conditioners etc.. The maximum ratings of the load should be higher than that of the unit under test.

In addition AC electronic loads need to meet the following requirements:

- Linearity
- Reliability
- Economy
- Stability
- Reproducibility

1.4.1 Linearity

Linearity of a system is the property that the output quantity of the system is proportional to the input quantity. Linearity of a load is a characteristic that makes the current curve a perfect replica of the voltage curve as shown in Figure 1.4 giving the current and voltage very low THD.

The objective of a DC electronic load is to have a variable resistance. Unlike in AC cases there is no instantaneous change in the output voltage and usually the output load current can only be changed by varying the impedance of the transistor. Therefore they are easy to design.

AC loads containing high-speed electronic switches, such as diodes, thyristors, or transistors could make the load non-linear because of their non-linear characteristics. In a transistor circuit large signal changes of ac voltage across the collector and the emitter make the device to operate in its saturation region, active region and cutoff region within a complete cycle, making it a non-linear device.

In this research, to implement an AC load, bipolar junction power transistors are used. The characteristics of the power BJTs are discussed in Section1.5 and Section 2.1.1 in Chapter 2. Non linear behaviour of an AC electronic load is as shown in the Figure 1.5 highlighting the possibility of non linear currents drawn by the load. In this project linearity is to be achieved using electrically isolated digitally control circuitry.

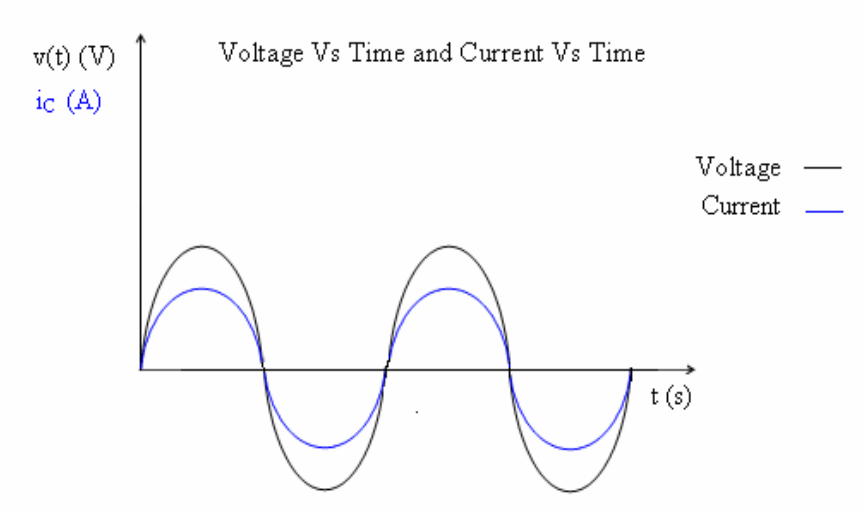


Figure 1.4: Voltage and current wave forms of a linear load

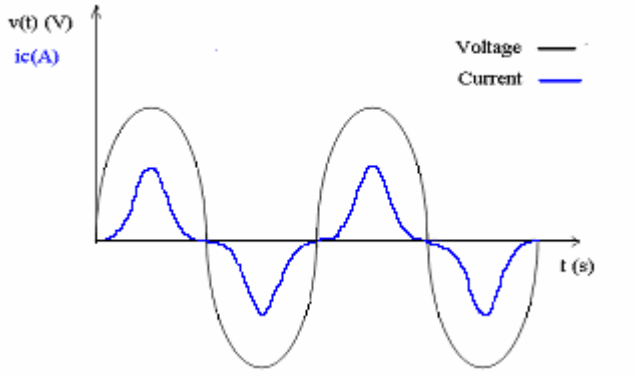


Figure 1.5: Voltage and current wave forms of an AC Electronic load

1.4.2 Reliability

The reliability of a device is related to the component count and the reliability of each component. Component reliability is a statistical function commonly expressed as the Mean Time Between the failures (MTBF) [7]. For a system comprising *n* non-redundant components, the system MTBF is expressed as

$$\frac{1}{MTBF} = \sum_{i=0}^{n} \frac{1}{MTBF_n}$$

Even when individual components are highly reliable, the MTBF for a large system could still be unacceptably short. For example, if the MTBF of one class of a component is 100,000 hours (about 11.5 years) and if there are 50 such components in the system, then the MTBF for that system is only 2,000 hours (83 days). The MTBF for *m* redundant components is $MTBF^m$ and judicious duplication of key components can be employed to increase the reliability of any system. Thus, two systems of components in redundant configuration each with a MTBF of 2,000 hours will have combined MTBF in excess of 450 years. This increase in reliability is only achievable if the system is designed so that transfer of function to the redundant set of components is time wise seamless and the failed components can be immediately replaced without interrupting the operation of the systems.

1.4.3 Economy

Clearly, the smaller the component count is to achieve the required functionality, the longer is the MTBF and the lower is the overall system cost.

1.4.4 Stability

The stability of a system is measured in terms of its ability to withstand disturbances of a given relative magnitude and the time required to attain normal functioning following a disturbance. The magnitude of a disturbance can be expressed in terms of the full load of the system. Clearly, a desirable property of a system is the ability to withstand significant disturbances and different kind of non- linear loads.

1.4.5 Reproducibility

The reproducibility of a system describes how closely the properties of its output approach the design requirements. This can be measured in terms appropriate to the output waveform. For DC this would be voltage and tolerance limits. For AC it would be in terms of Root Mean Square (RMS) value.

1.5 Research Objectives/ Specifications

The aim of this research is to implement a 230V/50Hz high power capable AC electronic load. A single BJT may not withstand the voltage level and power in a 230V AC load. Therefore series connected transistor array was proposed to share the voltage and power equally [8]. The design concept of the array is discussed in Chapter 3.

Objectives in developing high power capable variable AC impedance are given below.

- Equal power dissipation and voltage distribution across the individual transistors with reasonable device temperatures.
- 230V/50Hz line voltage capability
- 5A RMS current
- Low harmonic distortion of current waveform according to the IEE Std-519

- Digitally controllable
- Linear
- Fast transient response

1.6 System Overview

The AC electronic load consists of three major parts.

- The power transistor array
- Sampling circuit
- Digital control circuit

Basic concept of AC impedance control is achieved by base current diversion principle. BJT array is inserted between diode bridge points to achieve AC operational capability.

A combination of a high power transistor and a high voltage low power transistor are combined in a Darlington configuration to achieve higher gain. More details of complete circuits will be discussed in Chapter 2 and Chapter 3.
The complete block diagram of the system is shown in the figure 1.6 Set of opto isolators are used in the design to maintain the electrical isolation between the low voltage control circuitry and the high voltage power stage.

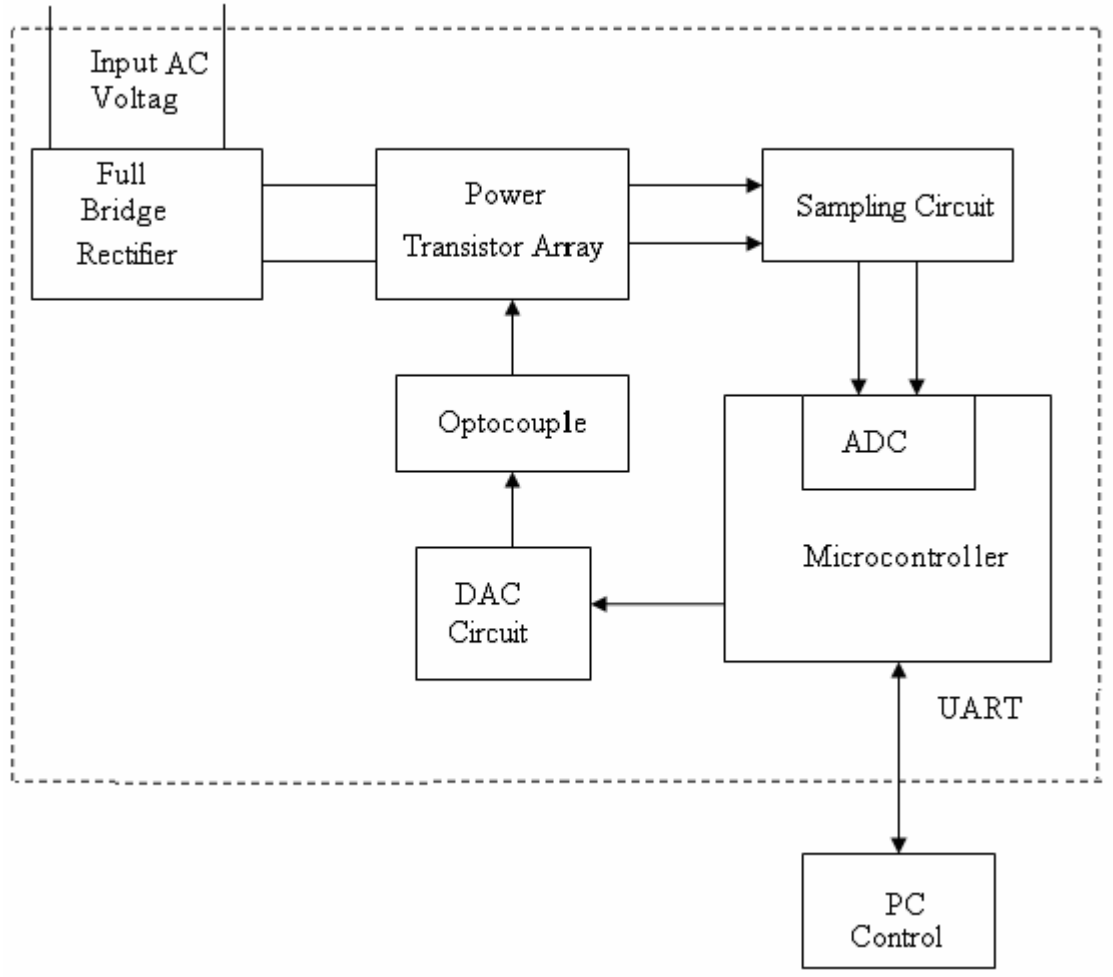


Figure 1.6: Complete block diagram of the AC Electronic load design

1.7 Thesis Outline

In this Chapter background, different loads, testing methods, requirements and objectives of the research were discussed. In addition the overall system overview is briefly reviewed.

In Chapter 2 the existing design techniques are examined and some related topics such as power transistor options, electrical isolation, sampling circuits are briefly discussed.

In Chapter 3 a theoretical overview of the design approach of power stage, advantages of the design, assumptions made and their effects are discussed.

Chapter 4 describes about the simulation carried out and its results.

In Chapter 5 the approach to digital control of the transistor array using microcontroller development system is discussed. In addition details of voltage sampler and digital to analog converter system are described.

Implementation aspects such as the selection of components, heat sink calculations and approach to measurements are discussed in Chapter 6.

Chapter 7 shows the performance of digitally controlled AC electronic load performance.

Chapter 8 summarizes the conclusions and its implications for future developments.

Chapter 2

Background and Related Work

2.1 Background work and literature survey

A literature survey carried out during the early stages of the thesis work indicated that a series connected BJT array can be used as the main control element of automatic voltage regulators [9]. In this case of the BJT array an approach to equally sharing the voltage and power among multiple transistors were discussed [10 - 13]. Based on the above work it was decided to use a similar technique for developing the AC electronic load, where multiple power BJTs were to share the dissipation.

2.2 Power Transistor options for electronic loads

Power transistors are able to handle voltages from few volts to several kilovolts and currents from few milliamperes to few hundred amperes. The operation of all power semiconductors is limited by a series of ratings which define the operating boundaries of the device. Among the commercially available power semiconductor devices usable options are the bipolar junction transistors (BJT), MOSFETs and IGBTs.

2.2.1 Bipolar junction Transistors

BJT is essentially a current operated device where the device pushed to conducting stage by controlling the current into the base junction. When a BJT is turned on, a forward voltage drop is developed across the device collector and emitter terminals giving rise to power loss and thus heat loss. BJTs have very high current carrying capabilities and therefore they are used in low to high power applications.[14]

Low current gain, complex drive circuitry, relatively low switching characteristics which limits the maximum operating frequency to low kHz range and negative temperature coefficient which leads to high increase in device temperature are some of the drawbacks of BJTs.

2.2.2 Metal Oxide Field Effect Transistors (MOSFET)

Power MOSFETs differ from BJTs in operating principles, specifications and performance
A power MOSFET has high input impedance and thus requires minimal gate current to turn on and off. This greatly simplifies the drive circuitry and reduces its cost. In addition they have very fast switching characteristics allowing them to operate into the MHz range [15] MOSFETs are merely resistors while switched on and give rise to power and heat loss in the device. They have positive temperature coefficient which stop thermal runaway.

The relatively low breakdown voltages limit the use of MOSFETs in high voltage applications. High on resistance especially at high breakdown voltages limits their current carrying capabilities.

2.2.3 Insulated Gate Bipolar Transistors (IGBT)

IGBT is a combination of a power MOSFET and a BJT having superior characteristics. Similar to MOSFETs they are voltage controlled devices. Their high input impedance makes the minimal gate drive requirements and low cost drive circuitry. Switching speed is comparable to MOSFETs and forward voltage drop and current densities are similar to BJTs thus low conduction losses. Their breakdown voltage is much higher than that of MOSFETs. These high performance along with high current capability make the IGBTs , a choice in high power and high voltage applications.

Possibility of uncontrollable latch-up under overstress conditions (high dv/dt or di/dt), lower switching speed and higher switching losses Compared to MOSFETs are some drawbacks of IGBTs.

2.2.4 Selection of the device option for the AC electronic load

In this research BJTs are selected from these super devices in order to have current controllability and high current capability.

2.3 Use of Darlington pair

It is well known that Bipolar junction transistors have low current gain at typical operating current levels and they require continuous high base current for allowing significant current to flow from collector to emitter. This is discussed in this Section 2.3.1. Therefore in order to have a high current gain with low base current the single transistors in the circuit shown in Figure 2.5 are replaced using Darlington pairs.

Darlington Transistor comprises of a medium power BJT connected to a power BJT as shown in the Figure 2.1. This provides a high current gain approximately equal to the product of the current gains of the two transistors. Darlington transistor has better transistor parameters than the single transistor but almost twice the base to emitter voltage [16]. Darlington pair is treated as a single compound transistor for analytical purposes.

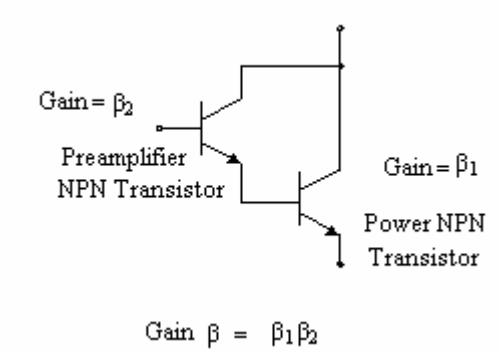


Figure 2.1 Darlington pair

2.3.1 Large signal models of BJT in the forward active region

In a transistor control signal, a base current can be used to cause the current in the collector to change from zero to a large value. In bipolar junction transistor current is conducted by both electron and holes. For the analysis only diffusion current components are considered and drift currents due to thermally generated minority carriers are usually very small and are neglected.

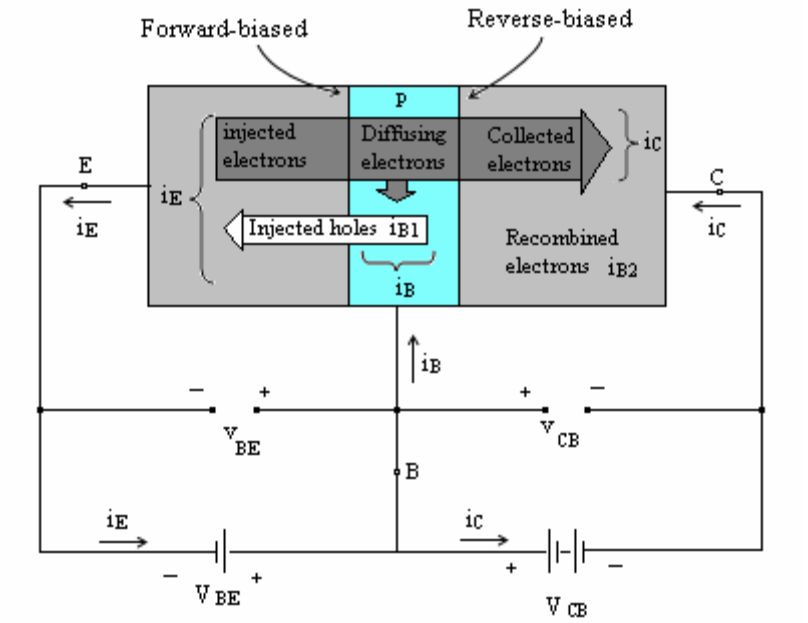


Figure 2.2 Current flow in an npn transistor biased to operate in the active mode [16]

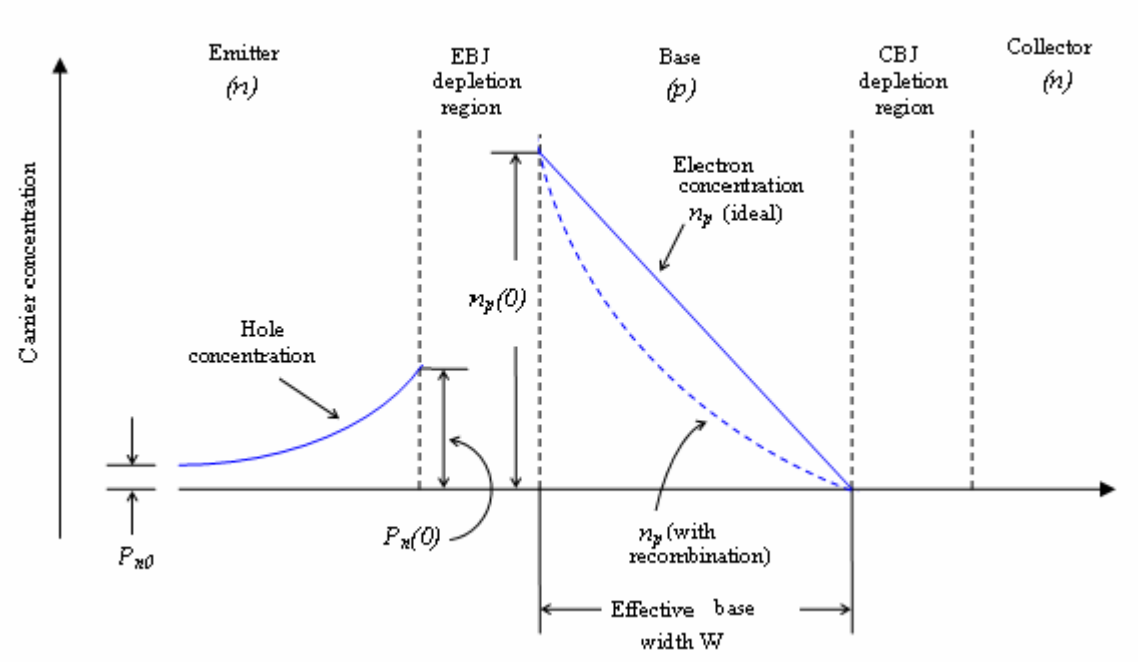


Figure 2.3 Profiles of minority carrier concentrations in the base and the emitter of an npn transistor operating in the active mode [16]

The electron concentration will be highest [denoted by $n_p(0)$] at the emitter and lowest (zero) at the collector. For a forward bias p-n junction the concentration $n_p(0)$,

$$n_p(0) = n_{p0}\, e^{v_{BE}/V_T} \quad \text{.....(2.1)}$$

where n_{p0} is the thermal equilibrium value of the electron concentration in the base region, v_{BE} is the forward base-emitter bias voltage and V_T is the thermal voltage, which is equal to approximately 25mV at room temperature.

The tapered minority carrier concentration profile as shown in Figure 2.3 causes the electrons injected into the base to diffuse through the base region towards the collector. This electron diffusion current I_n is directly proportional to the slope of the straight line concentration profile,

$$I_n = A_E q D_n \left(\frac{dn_p(x)}{dx} \right)$$

$$I_n = A_E q D_n \left(-\frac{n_p(0)}{W} \right) \text{.....(2.2)}$$

where A_E is the cross-sectional area of the base emitter junction, q is the magnitude of the electron charge, D_n is the electron diffusivity in the base, and W is the effective width of the base.[16]

The collector current $i_C = I_n$

Then from equation (1) and (2),

$$i_C = I_S \, e^{v_{BE}/V_T} \text{.....(2.3)}$$

$$I_S = A_E q D_n n_{p0} / W \text{.....(2.4)}$$

where I_S is called saturation current or current scale function.

Also $n_{p0} = n_i^2 / N_A$

where n_i is the intrinsic carrier density and N_A is the doping concentration.

Then

$$I_S = \frac{A_E q D_n n_i^2}{N_A W} \text{.....(2.5)}$$

Thermal voltage

$$V_T = kT / q \text{.....(2.6)}$$

where k is the Boltsman constant and T is the absolute temperature[16].

Figure 2.4 shows the output characteristics of a power bipolar transistor showing the saturation and quasi-saturation regions of operation. The current gain of the transistor is decreasing when proceeding from the forward active region through the quasi-saturation region into saturation region. This is because of the additional recombination current that must be supplied by the base electrode for sustaining carriers that are injected in to the collector drift region.

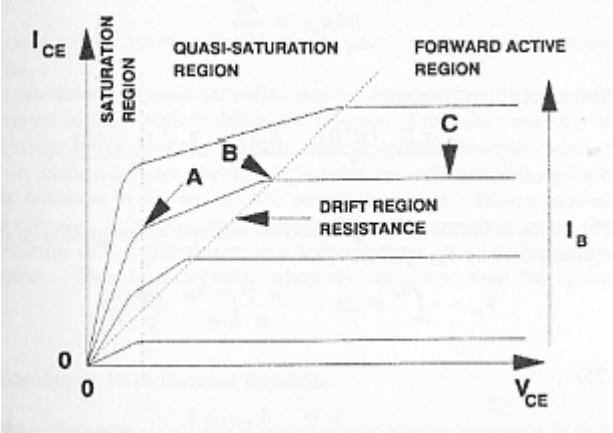


Figure 2.4: Output Characteristics of a power bipolar transistor

In a circuit if a transistor is replaced by Darlington pair, the operating point of the circuit will remain unchanged for all the practical values of transistor parameters. [17-18]

The DC current gain (h_{FE}) of the Darlington pair shown in the Figure 2.1 is given by,

$$h_{FE} = h_{FE1} * h_{FE2} + h_{FE1} + h_{FE2}$$

More application details of the Darlington pair are discussed in Chapter 3.

2.4 Need for a series connected array

When a transistor is used in 230V AC applications the instantaneous peak values often vary up to approximately 330√2 V for the range of input AC RMS voltages from 160V to 260V [14]. A single BJT may not withstand this voltage level and power. Therefore a series connected transistor array was used to share the voltage and power equally [8]. Figure 2.5 shows the basic transistor array configuration used in this research.

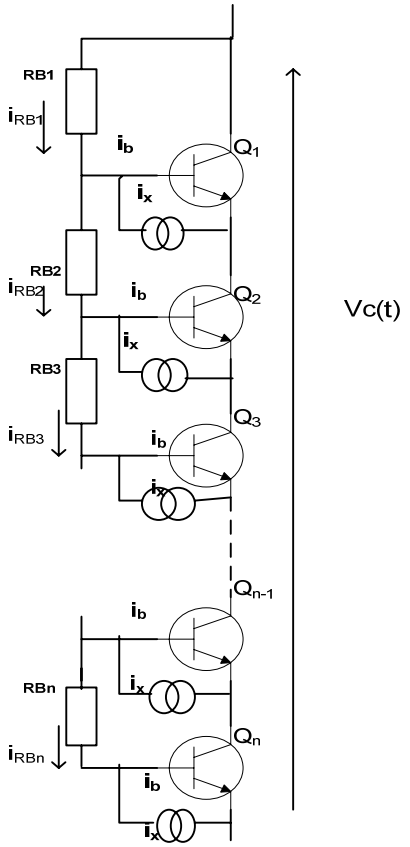


Figure 2.5: Transistor array

If all the transistors are to dissipate equal power, the base currents and collector current need to be equal. If the transistor gains are large and identical, and if each transistor has nearly identical collector currents it can be shown that,

$$R_{B1}(i_B + i_x)\, n + R_{B1}(i_B + i_x)\,(n-1) + R_{B1}(i_B + i_x)\,(n-2) + ... + R_{B1}(i_B + i_x) = v_C(t) - v_{BE}$$

If

$$R_{B1}=\frac{R_B}{n};\ R_{B2}=\frac{R_B}{n-1};\ R_{B3}=\frac{R_B}{n-2}.....;.R_{Bn}=R_B$$

Resistance across the array is given by,

$$R_{CE}=\frac{v_{BE}}{\beta\, i_B}+\frac{R_B}{\beta}\left(1+\frac{i_x}{i_B}\right)$$

Chapter 3 provides the details 0f the derivations.

2.5 Electrical Isolation

Isolation electrically separates the low voltage control circuitry from the high voltage power stage. Isolation offers many benefits including,

- protection for expensive equipment, the user and data
- improved noise immunity
- ground loop removal
- increasing common-mode rejection

Isolation requires signal to be transmitted across the isolation barrier without any direct contact. There are several methods available such as optical, capacitive, inductive .etc.

2.5.1 Optical isolation:

An optoisolator combines a photoconductor or a phototransistor with a high quality, long life light source in an encapsulated package that is light tight. The combination of various photosensors and light sources are available in a wide variety of packages. Typical optocouplers consists of a GaAs infrared-emitting diode and a silicon phototransistor mounted in a single package.
When forward current (I_F) is passed through the GaAs diode, it emits infra red radiation peaking at about 900nm wavelength. This radiant energy is transmitted through an optical coupling medium and falls on the surface of the NPN phototransistor

The voltage level output by the phototransistor is directly related to the amount of light detected from the emitter. If the output transistor is biased in the active region, the current transfer relationship for the optocoupler can be represented as;

$$I_C = K\left(\frac{I_F}{I_{F'}}\right)^p \text{.....(2.7)}$$

where I_C is the collector current, I_F is the input LED current, $I_{F'}$ is the current at which K is measured, K is the collector current when $I_F = I_{F'}$ and p is the slope of I_C *Vs* I_F on logarithmic coordinates [31].

The exponent p varies with I_F, but over some limit range of ΔI_F, p can be regarded as a constant. The current transfer relationship for an optoisolator will be linear only if p equals to one. For typical optocouplers p varies from approximately 2 at input currents less than 5mA to approximately 1 at input currents greater than 16mA. Reasonable linearity can be obtained by using a single optocoupler.

2.6 Sampling Circuit:

Voltage and current across the transistor array determines the effective AC resistance of the electronic load and they should be monitored for controlling purpose to achieve a linear resistance. For safety requirements high voltage samples should not be directly fed to the low voltage controlling circuits, directly. The sampling circuit has been designed to scale down the high voltage sample to a voltage level that can be fed to the control circuit.

Sampling circuit comprises with several stages such as voltage regulator, opto isolator, and amplifier. The basic diagram is shown in the Figure 2.6.The complete circuit diagram and operation will be described in the chapter 5

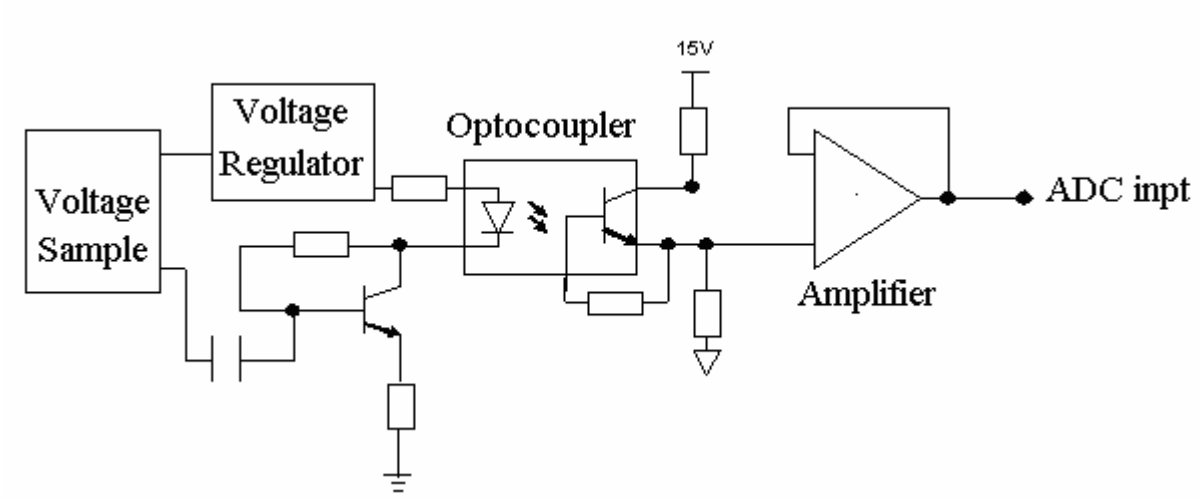


Figure 2.6 Basic blocks of sampling Circuit

Chapter 3

Power Stage –A Theoretical overview of design approach

3.1 Overview of the System

Developing a variable impedance with fast transient response using power transistors and conversion of the 230V/50Hz-supply input to a rectified output are the two main objectives of the power stage.

Power stage circuits includes a full bridge rectifier, bipolar junction transistor array and the associated circuits designed to achieve a uniform voltage and power distribution across each transistor.

In this research, a large signal circuit design approach was used to achieve the capability to share the power dissipation equally despite the wide variation of the instantaneous voltage over the AC cycle.

3.2 Rectification

As a transistor is incapable of handling negative voltage, rectification is required. The rectification has been done using four rectifier diodes and the power transistor array is connected at the bridge points as shown in Figure 3.1 to achieve ac operational capability. Figure 3.2 shows the rectified output of current and voltage of transistor array.

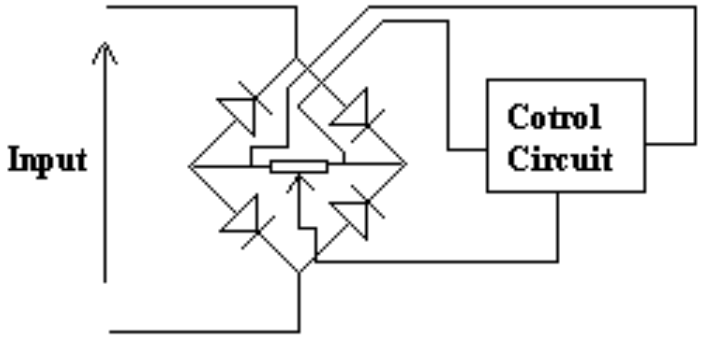


Figure 3.1: Basic Circuit blocks of the AC electronic load

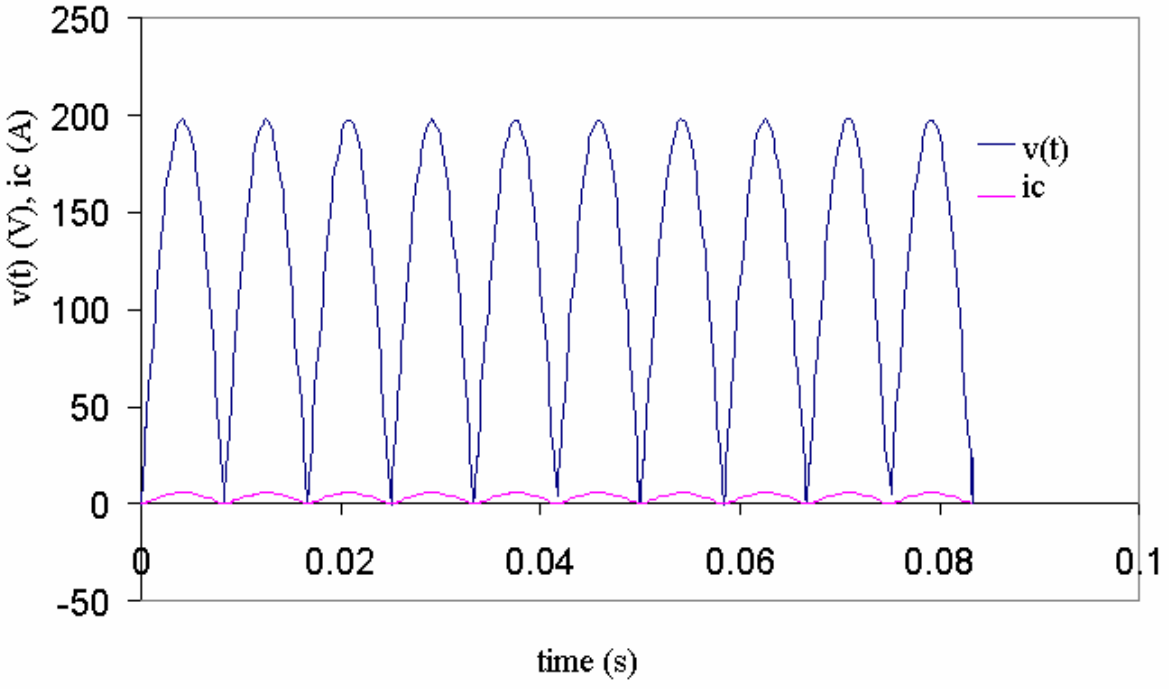


Figure 3.2: Practical rectified output at bridge points of the array

3.3 Transistor Array Design

A conceptual approach for changing the effective collector-emitter resistance of a BJT over a wide range is shown in Figure 3.3 with a transistor across a diode bridge to achieve AC capability. Large input voltage makes the voltage drop across diodes negligible compared to instantaneous voltages.

3.3.1 Concept

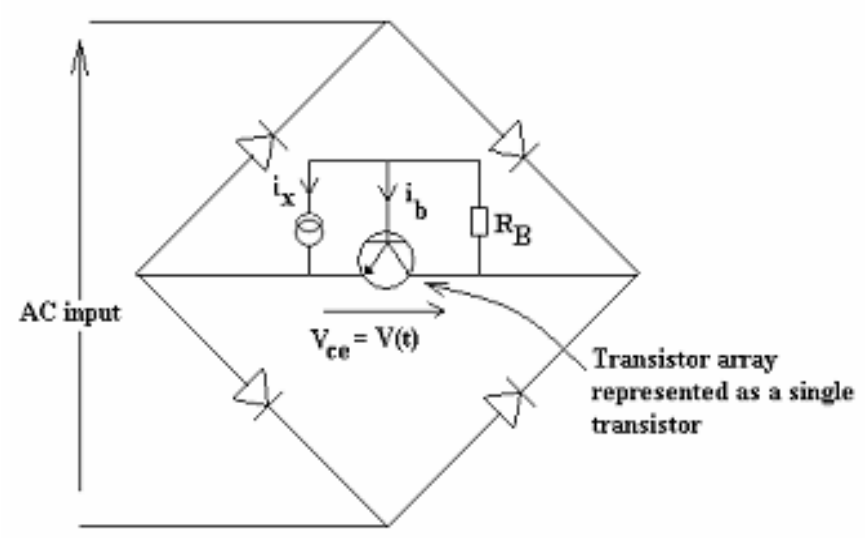


Figure 3.3 Simplified concept for variable resistance [20]

For a simplified case of a single transistor shown in Figure 3.3, impedance control is achieved by diverting a part of the base current using low voltage control circuit[20].

According to the Figure 3.3

When the transistor in active mode,

$$v(t) = v_{BE} + R_B(i_B + I_x) \text{.....(3.1)}$$

where *v(t)* - instantaneous collector-emitter voltage,

v_{BE} - base-emitter voltage,

i_B - instantaneous base current,

i_x - amount of base current diverted by control inputs

R_B - resistance between the collector and base.

Also

$$v_t = i_C R_{CE} \text{.....(3.2)}$$

and

$$i_C = \beta\, i_B \text{.....(3.3)}$$

Then from equation (3.1), (3.2) and (3.3) it can be proved

$$R_{CE} = \frac{v_{BE}}{\beta\, i_B} + \frac{R_B}{\beta}\left(1 + \frac{i_x}{i_B}\right) \text{.....(3.4)}$$

From the equation (3.4) it is evident that R_{CE} can be controlled by either varying R_B or the ratio $\frac{i_x}{i_B}$ which is defined as the base current diversion ratio (BCDR). If R_B is sufficiently large enough compared to base emitter resistance $\frac{v_{BE}}{\beta\, i_B}$ can be neglected.

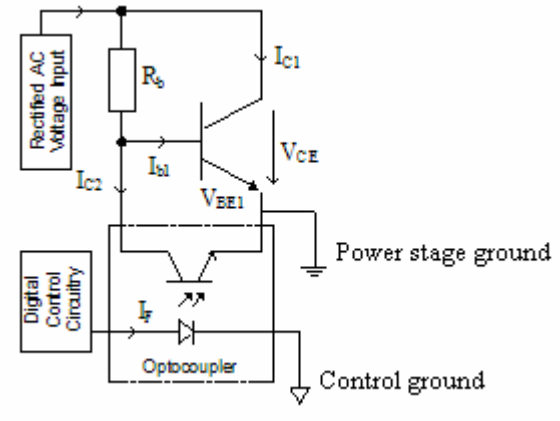


Figure 3.4 Base current diversion using an opto coupler

In the practical implementation when Darlington pairs are used for the transistor as shown in Figure 3.4, the low base emitter voltage permits the concept of controlling the BCDR using optoisolators, maintaining the necessary electrical isolation between transistor array and the control circuitry.

3.3.2 Application of the concept to multiple transistors in a series connected array

Series connected transistor configuration is a very important criteria for voltage and power sharing across the elements of the array and therefore is designed as shown in the Figure 3.5 in order to control a few hundreds of watts. It has also achieved equal power dissipation and uniform voltage distribution among the transistors.

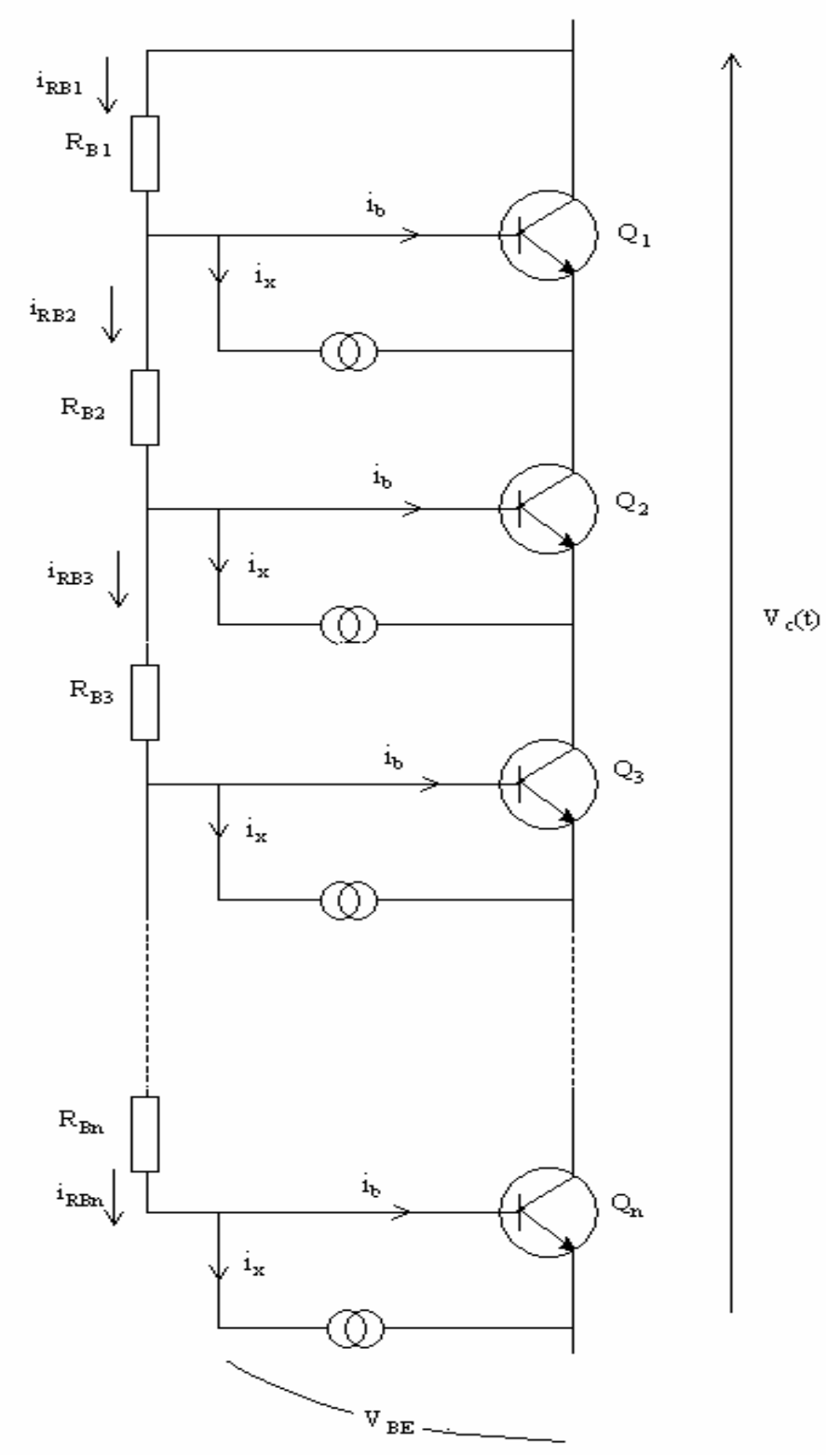


Figure 3.5 Series connected configuration of transistor array

As voltage distribution among the transistors is uniform, according to the Figure 3.5 the voltage across the m[th] transistor v_{CEm} is equal to $\frac{v_c(t)}{n}$, where $v_C(t)$ is the instantaneous voltage across the array and n is the number of transistors.

For equal power dissipation, the base current and collector current of transistors need to be equal.

Therefore $i_{B1} = i_{B2} = i_{B3} = \ldots\ldots\ldots\ldots\ldots = i_{Bn} = \boldsymbol{i_B}$ and

$$i_{C1} = i_{C2} = i_{C3} = \ldots\ldots\ldots\ldots\ldots = i_{Cn} = \boldsymbol{i_C}$$

If the transistor gains are large and identical, and if each transistor has nearly identical collector currents,

$$i_{C1} = \beta\, i_{B1},\quad i_{C2} = \beta\, i_{B2},\quad i_{C3} = \beta\, i_{B3}\,,\ \ldots\ldots\ldots\ldots,\ i_{Cn} = \beta\, i_{Bn}\,,\ (= \boldsymbol{\beta\, i_B})$$

and

$$\left.\begin{aligned} i_{RBn} &= i_B + i_x \\ i_{RBn-1} &= 2\left(i_B + i_x\right) \\ i_{RBn-2} &= 3\left(i_B + i_x\right) \\ &\ldots\ldots\ldots\ldots \\ &\ldots\ldots\ldots\ldots \\ &\ldots\ldots\ldots\ldots \\ i_{RB3} &= (n-2)\left(i_B + i_x\right) \\ i_{RB2} &= (n-1)\left(i_B + i_x\right) \\ i_{RB1} &= n\left(i_B + i_x\right) \end{aligned}\right\} \quad \ldots\ldots\ldots\ldots\ldots\ldots(3.5)$$

$$i_{RB1} R_{B1} + i_{RB2} R_{B2} + i_{RB3} R_{B3} + \ldots\ldots\ldots\ldots\ldots i_{RBn} R_{Bn} + v_{BE} = v_C(t) \ldots\ldots\ldots\ldots\ldots (3.6)$$

where R_{B1} to R_{Bn} are the resistors connected between the collector and the base of each transistor.

$$R_{B1}(i_B + i_x)n + R_{B1}(i_B + i_x)(n-1) + R_{B1}(i_B + i_x)(n-2) + \ldots\ldots + R_{B1}(i_B + i_x) = v_C(t) - v_{BE} \ldots\ldots\ldots (3.7)$$

If

$$\left.\begin{aligned} R_{B1} &= \frac{R_B}{n}; \\ R_{B2} &= \frac{R_B}{n-1}; \\ R_{B3} &= \frac{R_B}{n-2}; \\ &\ldots\ldots\ldots\ldots \\ &\ldots\ldots\ldots\ldots \\ &\ldots\ldots\ldots\ldots \\ &\ldots\ldots\ldots\ldots \\ R_{Bn} &= R_B \end{aligned}\right\} \ldots\ldots\ldots\ldots\ldots (3.8)$$

Equation (3.7) reduces to,

$$v_C(t) - v_{BE} = n\ R_B\ (i_B + i_x)$$

$$v_C(t) - v_{BE} = n\, i_B R_B\, (1 + \frac{i_x}{i_B}) \ldots\ldots\ldots\ldots\ldots (3.9)$$

Dividing by i_C

$$\frac{v_C(t)}{i_C} = \frac{n\, i_B R_B}{i_C} (1 + \frac{i_x}{i_B}) + \frac{v_{BE}}{i_C} \ldots\ldots\ldots\ldots\ldots (3.10)$$

Substituting $i_C = \beta\, i_B$ *and* $v_C(t) = R_{CE}\, i_C$ in equation (3.10)

$$R_{CE} = \frac{n R_B}{\beta}(1+\frac{i_x}{i_B}) + \frac{v_{BE}}{\beta i_B} \text{.....(3.11)}$$

In practice v_{BE} is small compared to $v_C(t)$, and the equation (3.11) is approximated to,

$$R_{CE} \approx \frac{n R_B}{\beta}(1+\frac{i_x}{i_B}) \text{.....(3.12)}$$

Also $i_c = I_S e^{v_{BE}/V_T}$, $i_B = i_C/\beta$ and $V_T = kT/q$

Then

$$i_B = I_S e^{qv_{BE}/kT}/\beta \text{.....(3.13)}$$

and from equation (2.7) in Chapter 2,

$$I_C = K\left(\frac{I_F}{I_{F'}}\right)^p$$

the equation (3.12) has become to,

$$R_{CE} \approx \frac{n R_B}{\beta}[1+\beta\frac{K\left(\frac{I_F}{I_{F'}}\right)^p}{I_S e^{qv_{BE}/kT}}] \text{.....(3.14)}$$

In the array of Darilington pair as shown in the Figure 3.6 the term $I_S e^{qv_{BE}/kT}$ in equation (3.13) can be replaced by the equivalent relationship for the Darlington pair [17-18]. For the specific case in the prototype, by plotting the collector current of the Darlington pair (I_C) versus the compound base emitter voltage (V_{BE}) and using a mathematical fit as shown in Figure 3.7,an approximate relationship can be as follows.

$$I_C = 6 \times 10^{-13}\ e^{20.4 V_{BE}}$$

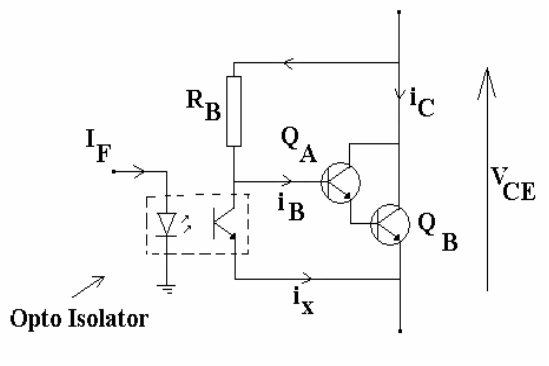


Figure 3.6: Use of Darlington pair

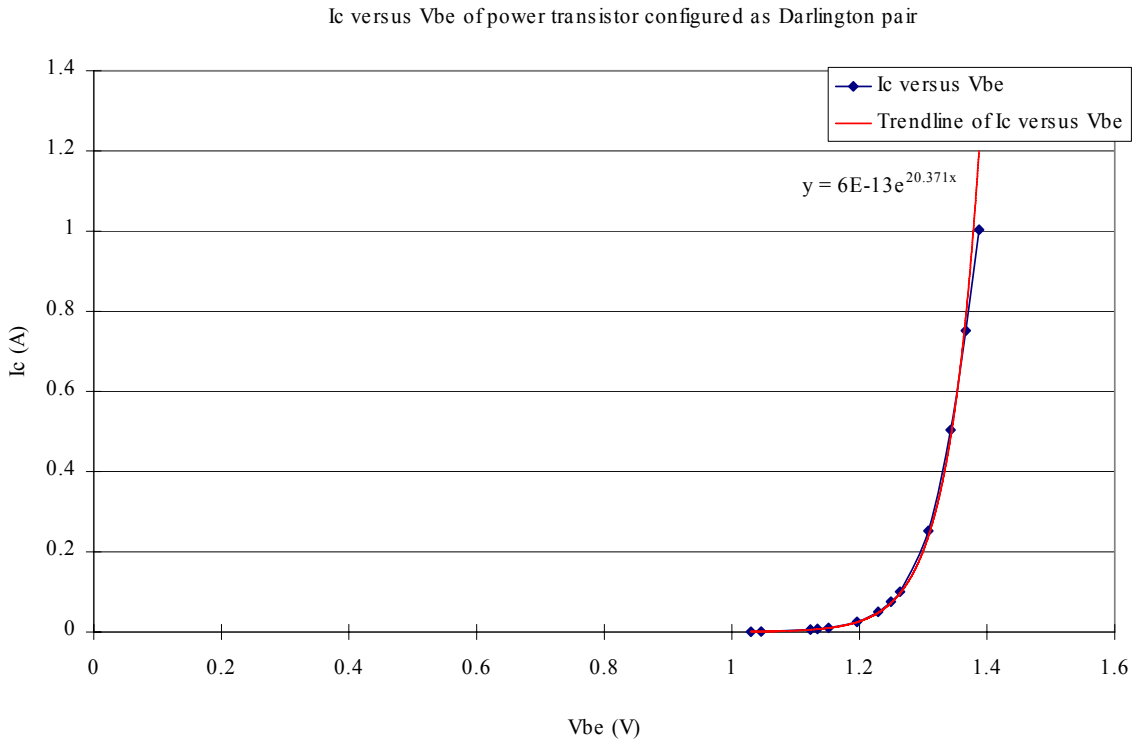


Figure 3.7: I_C versus V_{BE} of power transistor configured as a Darlington pair [20]

This depicts a reasonable mathematical fit for the transfer characteristics representing the equivalent of the term $I_S e^{qv_{BE}/kT}$ in equation (3.14). According to the Figure 3.7 it was evident that the R_{CE} value could be varied only if the effective $V`_{BE}$ for the Darlington pair was higher than 1.0V approximately.

The voltage drop $V`_{BE}$ is greater than 1.0V when the BCDR is low. Under high BCDR values i.e. diverting nearly the total base current, the effective resistance of the array is not controlled by the transistors except for the leakage effect.

If leakage effects are neglected at high BCDR values with the condition in equation (3.8), the effective maximum resistance of the array reaches the value given by the series combination of the resistors R_{B1} to R_{Bn} where

$$R_{CE\max} = R_B + \frac{R_B}{2} + \frac{R_B}{3} + \frac{R_B}{4} \ldots\ldots\ldots \frac{R_B}{n} \ldots\ldots\ldots \ldots\ldots\ldots (3.15)$$

At the other extreme, when the current through the input diodes of the optoisolator is zero, which is the case of minimum BCDR, the effective resistance of the array, from the equation (3.12), reduces to nR_B/β. Within these two theoretical limits the effective resistance of the array R_{CE}, can be controlled by varying the current through the emitter diodes of the optoisolator.

In this research four-element transistor array, as shown in the Figure 3.8, was used. In this case the range of the effective resistance is approximately $4R_B/\beta$ to $2.1R_B$ neglecting leakage currents of transistors. Due to the nonlinear behavior of the transistors including the dependence of β on the collector current [20], the effective resistance is a nonlinear function.

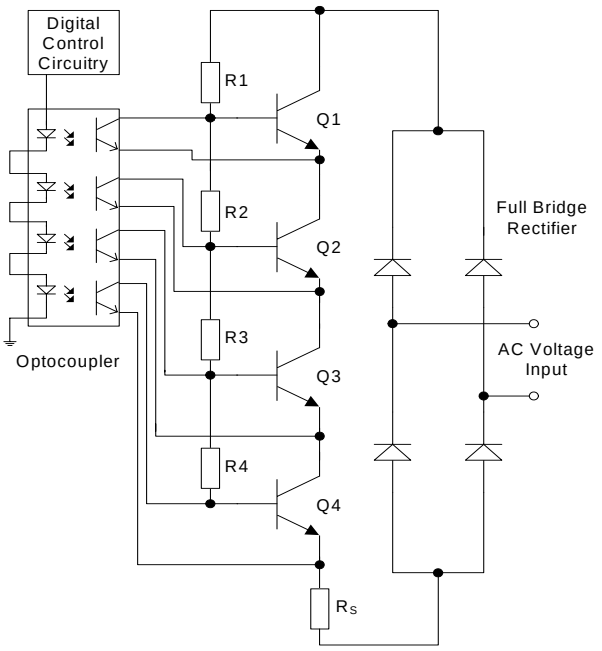


Figure 3.8: Transistor array

3.4 Controllability advantages of the proposed Technique

According to the equation 3.12 in the section 3.4.2, the array resistance R_{ce} can be controlled by both R_B and i_x. Resistance R_B operates at high voltage and low current. The current i_x is a low current due to the low voltage appearing across the base emitter junction of the transistor at all the time. Therefore i_x is easier to control than R_B.

3.5 Assumptions and their effects

Approximate analysis in this Chapter is carried out assuming the following.

1. Transistor gain β is constant over the entire range of instantaneous voltages occurring on an AC cycle (i.e for 230V AC 0- 230√2)

2. All transistors in the array are identical which is not the case in practical circumstances and that makes the power sharing and voltage sharing unequal.

3. Variable *p* of the optoisolator current transfer function is considered as a constant but it is variable within in a small range with the diode forward current I_F. Figure 3.9 shows the nonlinearity of the current transfer ratio of a typical optoisolator such as TLP521-5[22].

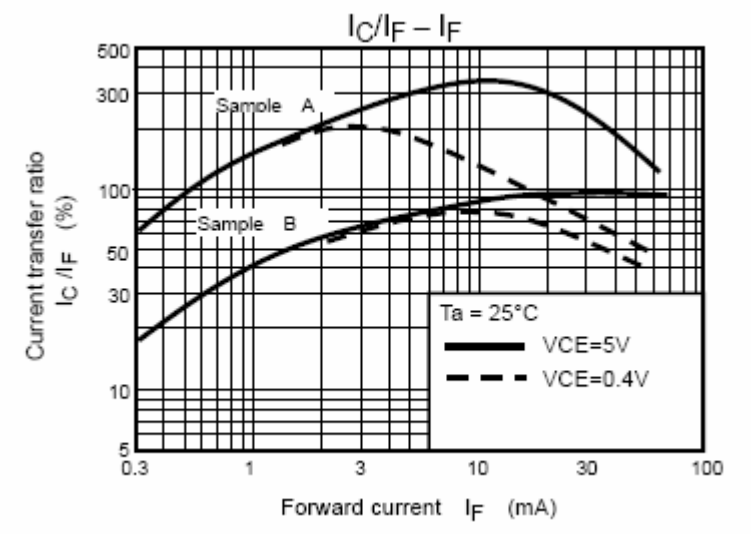


Figure 3.9: Current transfer ratio Vs forward current

4. Leakage currents occurring in the transistor (I_{CBO}) are neglected but at very high impedance requirements of a load this becomes the significant parameter.

3.6 Theoretical approach to correcting the non linear nature of the transistor array

- As shown in Figures 6.13, 6.14, 6.15 in Section 6.4.1 in Chapter 6 transistor array is non-linear and depending on V_{CE}.
- To correct this problem curve fitting technique was used as detailed in Chapter 6.

Chapter 4

Spice Simulation

4.1 Simulation Circuits

Spice simulation was used as a software tool to predict the non-linear behavior of the four-element transistor array and to predict the non linear behaviour of the circuit configuration shown in figure 4.1 under instantaneous voltage variation of the AC cycle. In this research Spice simulation is carried out using Protel DXP software package.

Figure 4.2 shows the simplified circuit diagram, used to predict the transient behavior of the transistor array. Darlington pairs are used instead of single transistor shown in the Figure 4.1 and 4.2. Two AC voltage sources are used in back to back configuration to achieve the rectified input across the array. The diversion of base current was carried out by injecting a suitable DC current component using a DC voltage source that is equivalent to the average DC current drive through the diodes of optoisolator. As there was no spice device library for a quad optoisolator, four separate voltage control current sources were used in the circuit. The actual circuit diagram used in the simulation is in the Appendix C.

In Figures 4.1 and 4.2, resistor R_4 represents the R_B value of the equation 3.4 which obtained in the array design in Chapter 3.

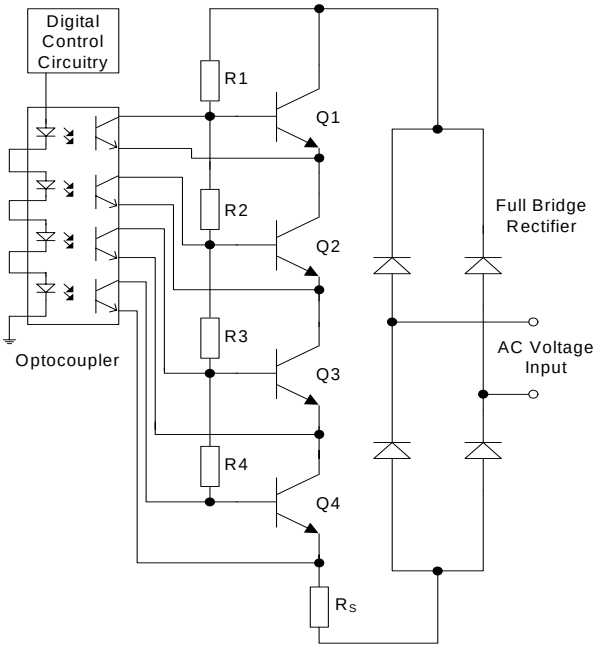


Figure 4.1: Transistor array

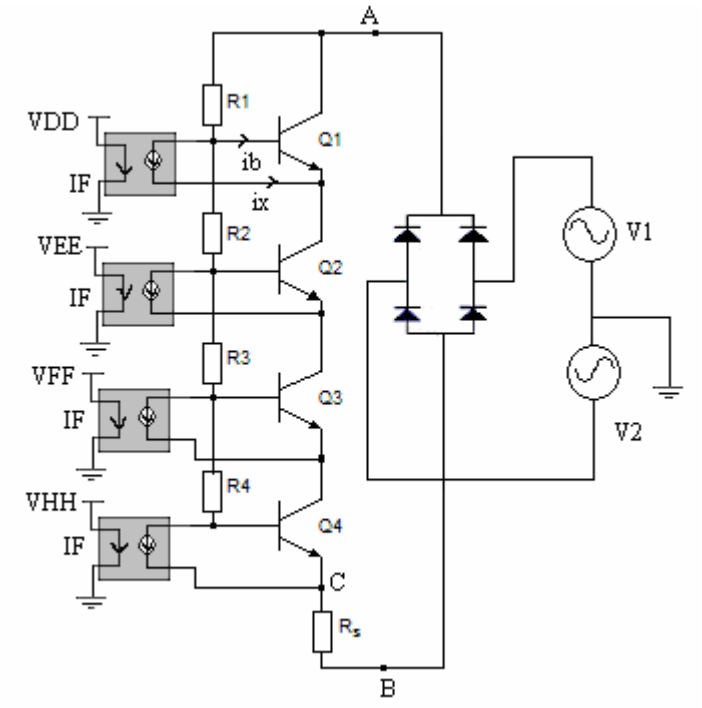


Figure 4.2: Simplified circuit used in Spice simulation.

Simulation was carried out for different R_1 to R_4 (R_B) values. Voltage across the array was observed across the points A and B in the Figure 4.2 and current through the array was monitored by observing the current through R_S. The voltage and current were obtained and the effective resistance across the array was calculated. Simulation was also carried out by changing the I_F current of the opto isolator to observe the resistance variation across the array.

The basic spice output data obtained were instantaneous values of voltage and current. The effective rms resistance was calculated by importing the probe current and voltage values into an Excel file and then calculating the rms equivalent of the resistance [21].

4.2 Simulation Results

The simulation results obtained for different settings of R_B values at different voltages and Figure 4.3 to 4.5 indicates the effective rms resistance value of the array versus I_F for different R_B settings.

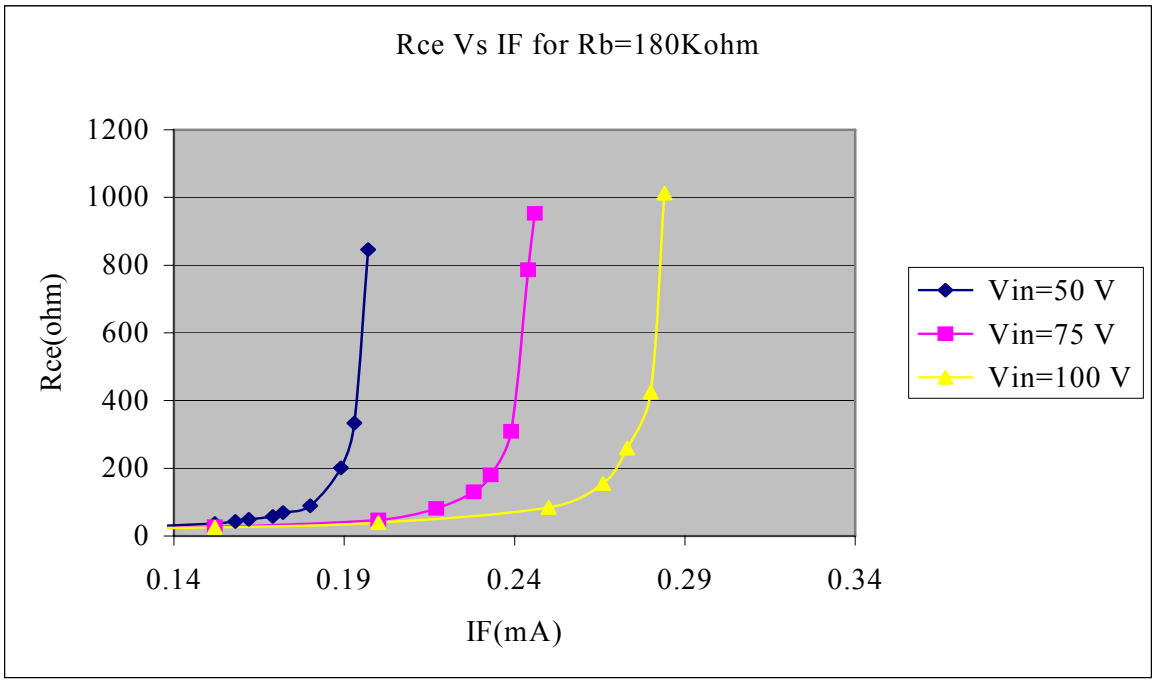


Figure 4.3 Variation of resistance with diode current when R_B=180KΩ

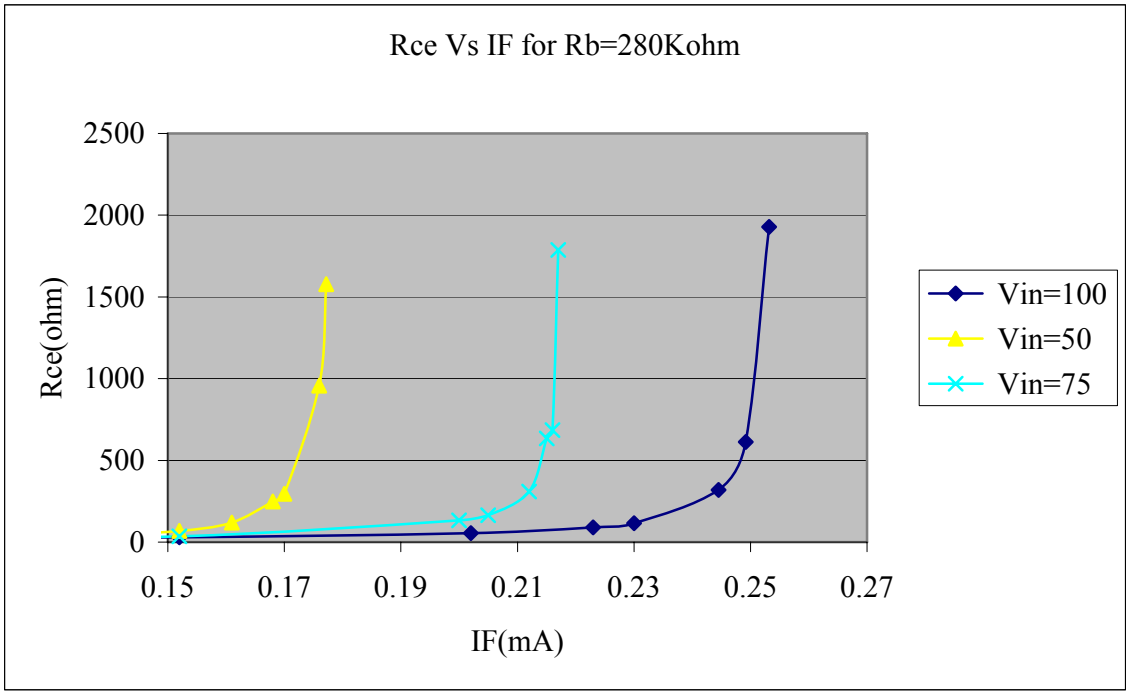


Figure 4.4 Variation of resistance with diode current when R_B =280KΩ

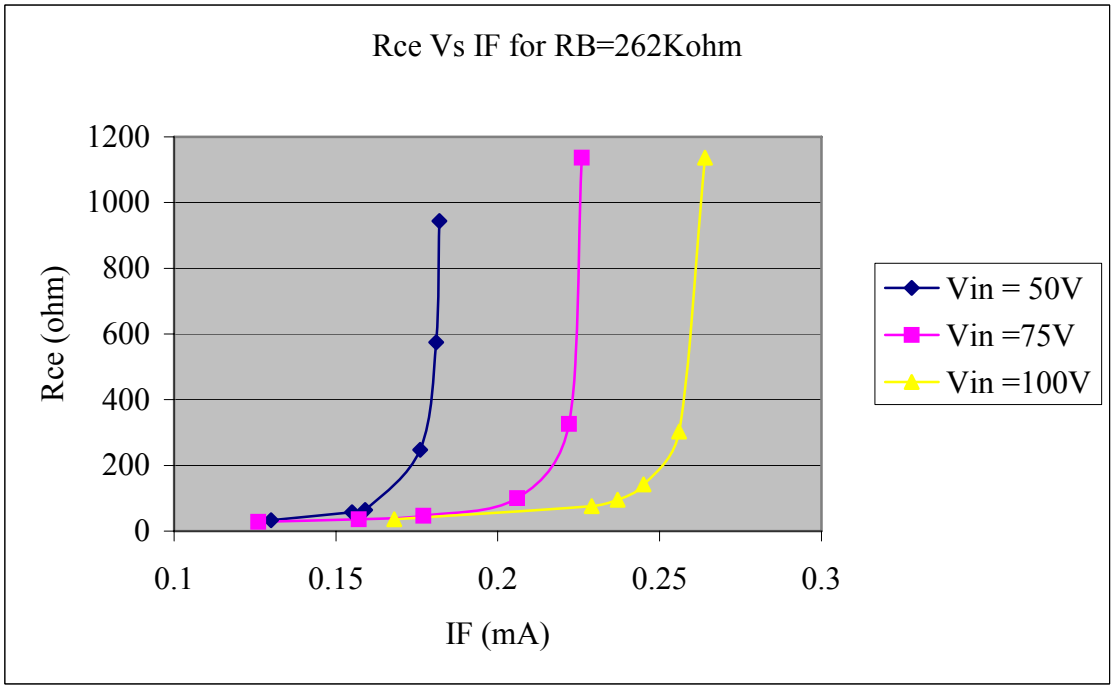


Figure 4.5 Variation of resistance with diode current when R_B =262KΩ

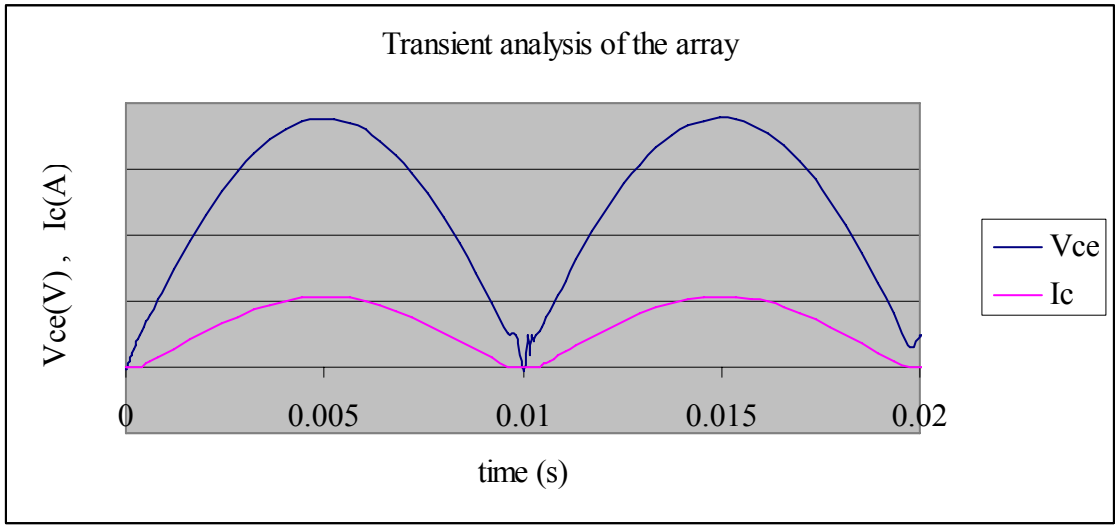


Figure 4.6: AC behavior showing the bridge output of the array using transient analysis of PSpice simulation

Figure 4.6 indicates the instantaneous current and voltage of the array during the ac cycle.

Appendix D indicates the raw values import in to Excel.

Spice simulations indicate that the transistor array has non-linear V-I characteristics.

4.3 Problems encountered

When carrying out the simulation to predict the large signal behavior and the transient performance of the array, there were many difficulties caused due to several reasons described below.

- The use of bipolar transistor array in an unconventional configuration where the transistor array was subjected to a varying rectified sinusoidal voltage input.
- The need to consider the nonlinearity effects added to the transistor array and its drive circuit (opto isolator) which affects the harmonic contents at the output.
- Certain mathematical simulation models for some components, which are used in the actual circuit, were not available and therefore different models have to be used. All the semiconductor device spice models used in the simulation are in the Appendix C.

Chapter 5

Approach to digital control and of the transistor array

5.1. Microprocessor Development System

In this research Zilog Modular Development System General-Purpose (MDS-GP) Application board was used to design the controlling part of the project. This MDS-GP board fully supports the Z8 Encore! 64K series processor modules and therefore 64K Z8x6423 is used. Photograph of the MDS-GP application board is shown in Appendix B. This development board was used due to the availability. The block diagram of the architecture of the Z8 Encore! 64K series is shown in Figure 5.1 [23]

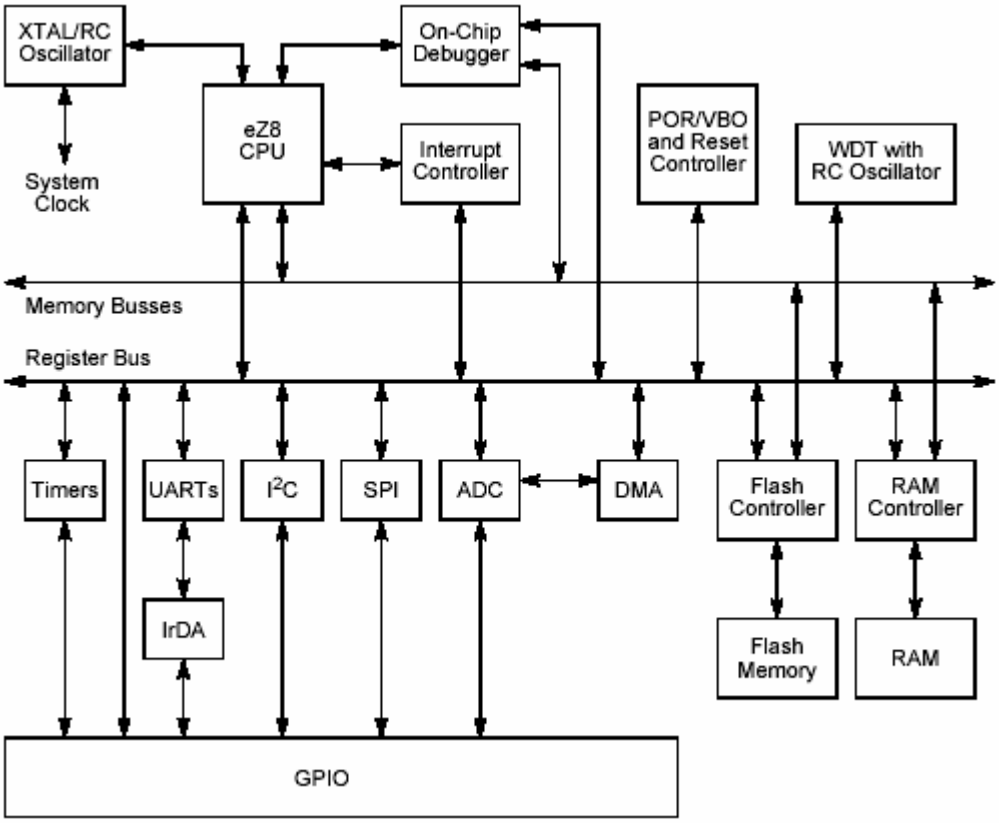


Figure 5.1: Z8 Encore! 64K Series block diagram.

Z8x6423 devices on the development board feature 20MHz eZ8 CPU, 64KB flash with in circuit programming capability and up to 4KB register RAM in an 80 pin Quad Flat Package (QFP). It provides 12 –channel, 10bit analog to digital converter (ADC) and up to four 16bit timers with capture, compare and PWM capability. It has up to 60 I/O pins and two full-duplex 9bit UARTs with Bus transceiver Driver Enable control. Each I/O pin is individually programmable.

5.2 Analog to Digital Converter

After the signal passes through the optocoupler and the amplifier of the sampling circuit it is fed to the analog to digital Converter (ADC) that converts an analog input signal to a 10-bit binary number. Z8 Encore! 64K series Zilog Z86423 microcontroller which was used in this research to control the circuit, comes in package with the 12 channel, 8 bit analog to digital converter (ADC). It accepts inputs from up to 12 different analog input sources. These inputs are converted to a 10bit long digital value that can be read by the microcontroller.

A block diagram of Analog to Digital converter of Z8 Encore system is shown in Figure 5.2 [23]

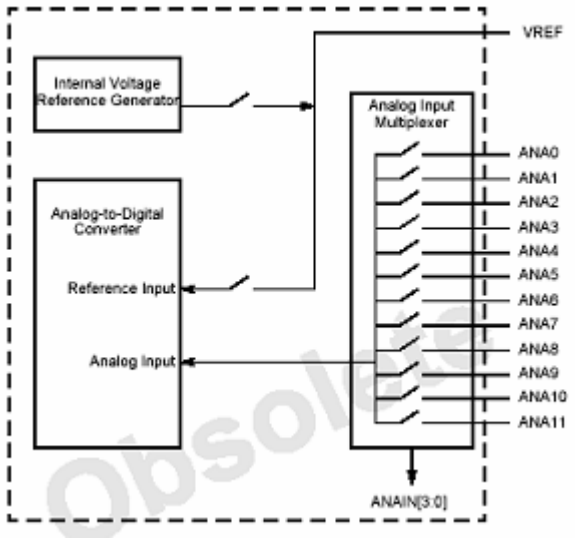


Figure 5.2 Analog to Digital Converter Block Diagram

Various conversion techniques exist to achieve analog to digital conversions. The conversion speed and accuracy of conversion differ for each of these methods.

The conversion techniques are:

- Sigma-Delta
- Successive approximation
- Flash
- Integrating
- Pipeline ADC

ADCs based on Flash or Successive Approximation technique use a resistor ladder or a resistor string. In such cases, the resistor accuracy directly affects the accuracy of conversion. Sigma-Delta converters do not have a resister ladder, but take a number of samples to converge on result. Such an over-sampling of the input takes many clock cycles. Therefore, for a given conversion rate, the Sigma-Delta converter requires a faster clock.

Z8 Encore! System which can work up to 20MHz, uses the analog to digital conversion with the Sigma-Delta conversion technique as it has several other advantages those indicated below.

- High resolution
- High input bandwidth
- Digital on-chip filtering.

The Sigma-Delta ADC architecture provides image attenuation below the amplitude resolution of the ADC in the frequency range of DC to half the ADC clock rate (one fourth of the system clock rate). The ADC also provides free conversion for frequencies up to one half the ADC clock rate. Thus Sigma-Delta ADC exhibits high noise immunity. Figure 5.3 shows the frequency response of analog to digital converter.[23]

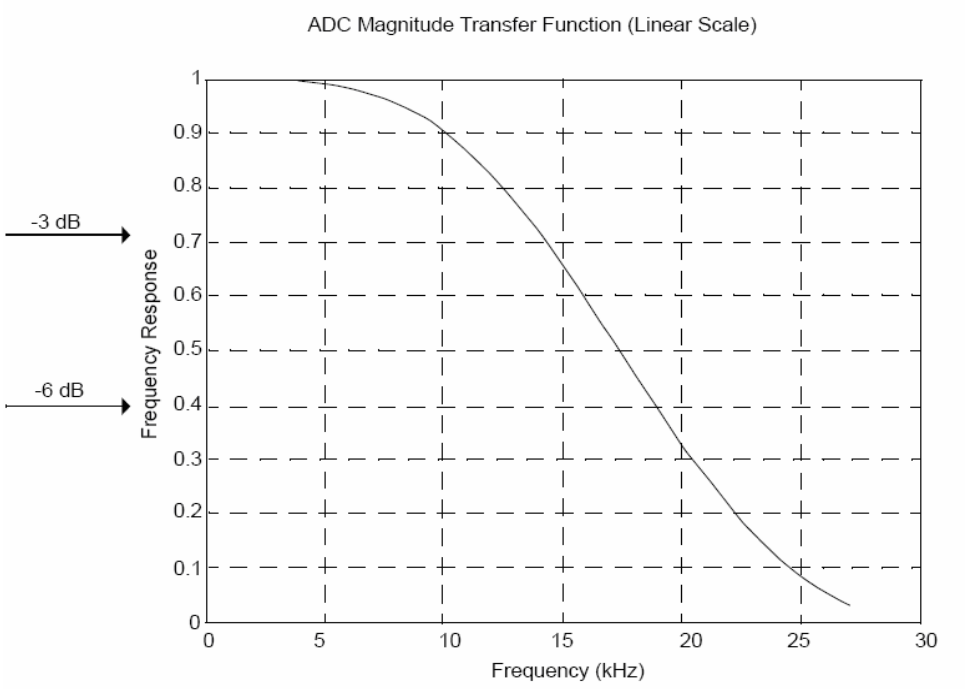


Figure 5.3 Analog to Digital Converter frequency response

As the frequency of the input is 50Hz and the sampling frequency is 1kHz, the effect of A to D converter at high frequencies is not a problem.

5.2.1 ADC reference Voltage

ADCs need a very stable reference voltage for accurate conversion. The maximum input voltage that can measure is its reference voltage. For an ADC of *n* bits, the measurable voltage range is divided into *2n* steps.

The step size or resolution of an ADC = $V_{REF}/ 2n$

Z8 Encore! System features a built-in reference voltage generator. It also supports external reference voltage. To select a type of reference voltage, the $\overline{VREF}$ bit in ADC control register is set accordingly.
The internal voltage reference is two volts in this system and it was selected in this research.
The step size for 10bit = 2 / 210 = 0.00195 V = 1.95mV.

5.2.2 Operation

5.2.2.1 Automatic power down

If the ADC is idle (no conversion in progress) for 160 consecutive system clock cycles, part of the ADC are automatically powered down. From this power-down state ADC requires 40 system clock cycles to power up. The ADC powers up when the conversion is requested using the ADC control register.

5.2.2.2 Modes of operation

There are two modes of operation. They are,

5.2.2.2.1 Single shot conversion

When single shot conversion is selected, ADC performs a single analog to digital conversion on the selected analog input channel. After completion of the conversion, the ADC shuts down.

5.2.2.2.2 Continuous conversion

When continuous conversion is selected, the ADC continuously performs an analog to digital conversion on the selected analog input channel. Each new data value over-writes the previous value stored in the ADC data registers. An interruption is generated after each conversion.

In this research single shot conversion was selected by clearing CONT of the ADC control register and enabled the desired analog inputs by configuring the general purpose I/O pins for alternate function disabling the digital inputs and outputs. Analog input channels are configured by selecting ANIN bits of the ADC control register. Enabling CEN in the ADC control register start the conversion.

Figure 5.4 shows the flow chart of the ADC conversion using single shot conversion.[23]

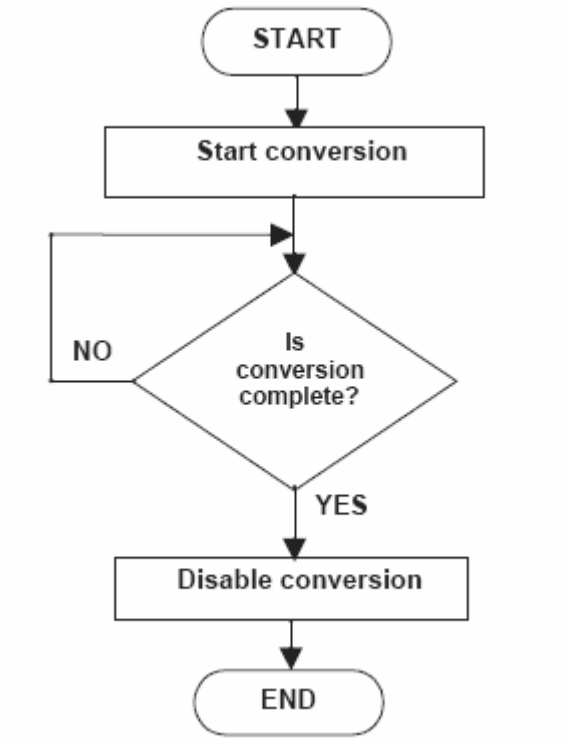


Figure 5.4: ADC flow chart

5.3 Digital to Analog Converter

The DAC08 series of 8-bit monolithic digital to analog converter was used because of the availability and very high-speed performance. It is a parallel input and current output, digital to analog converter. The maximum current output is 2mA. The functional block diagram is as shown in the Figure 5.5

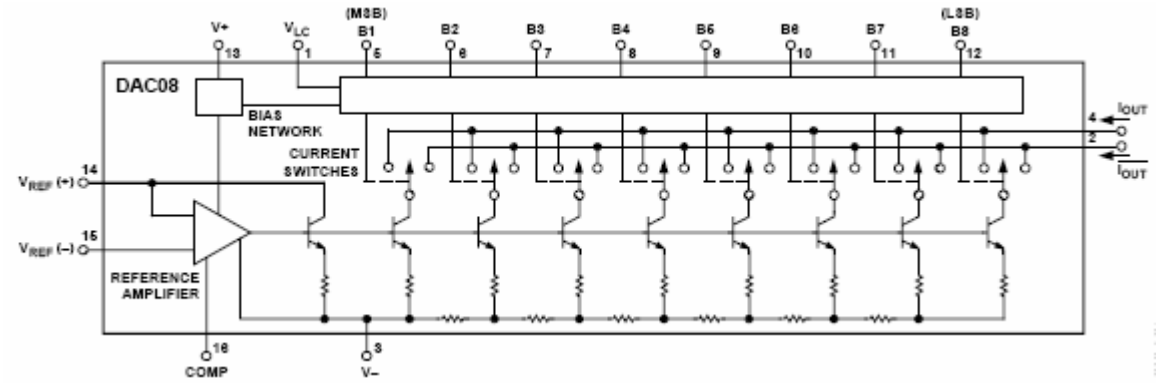


Figure5.5: Functional block diagram of DAC08

The output current is a product of a digital number and the input reference current I_{REF}. I_{REF} is the current through the R_{REF} connected to the pin 14 of the DAC08 as shown in the circuit configuration of Figure 5.6. The I_{REF} used in this application is 2mA. That current was set by the V_{REF} and R_{REF} (R_{14}). V_{REF} is set at 10V and R_{REF} was selected as 5KΩ. R_{14} and R_{15} shown in the Figure 5.6 are nominally equal.

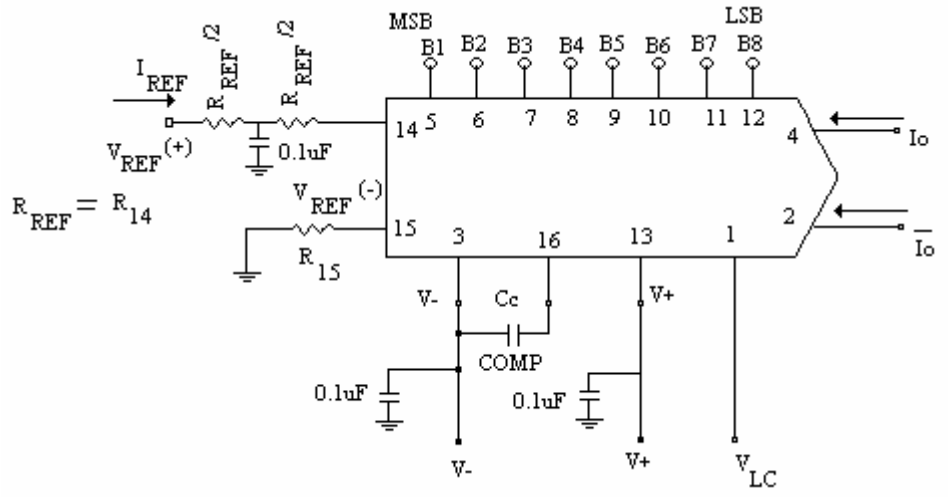


Figure 5.6: DAC 08 Circuit configuration

DC regulated power supply was used as a reference and therefore R_{14} was split up to two parts with the junction bypassed to ground with a 0.1µF capacitor. The logic threshold was adjusted over a wide range by placing an appropriate voltage at the control logic threshold pin (pin 1, V_{LC}). Pin 1 was grounded for TTL and DTL interface.

Both true (I_0) and complimented ($\overline{I_0}$) out puts were available. One out put ($\overline{I_0}$) was grounded through a resistor as it was not required. The reference amplifier was compensated by using a capacitor from pin 16 to *V*- . For fixed reference operation a 0.01µF capacitor is used.

The following Figure 5.7 with the DAC value table shows the basic unipolar operation output currents of the DAC08.

	B1	B2	B3	B4	B5	B6	B7	B8	I_O	$\overline{I_O}$	E_O	$\overline{E_O}$
FULL RANGE	1	1	1	1	1	1	1	1	1.992	0.000	–9.960	–0.000
HALF SCALE +LSB	1	0	0	0	1	0	0	1	1.008	0.984	–5.040	–4.920
HALF SCALE	1	0	0	0	1	0	0	0	1.000	0.992	–5.000	–4.960
HALF SCALE –LSB	0	1	1	1	0	1	1	1	0.992	1.000	–4.960	–5.000
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	0.008	1.984	–0.040	–9.920
ZERO SCALE	0	0	0	0	0	0	0	0	0.000	1.992	0.000	–9.960

Figure 5.7: Basic Unipolar operation output currents of the DAC08

5.4 Digital Control overview

The voltage across the array is monitored and fed to the analog to digital converter through the process shown in Figure 5.9. The main objective of the analog to digital conversion is to convert the analog signal (voltage from power stage) to a digital signal (bits) so that the microcontroller system can process the data to control the effective resistance of the array.

Microprocessor is programmed to give a required output to diode current value and sends the binary value to the output port. Binary signal of the output port of the microprocessor is fed to the digital to analog converter, which converts the binary value to analog current signal. The current from the digital to analog converter is fed to the optoisolator to get the required base current to keep the resistance across the array constant. Software flow chart is shown in the Figure 6.25.

The high voltage from the power stage must be scaled down to small voltage, as required from the analog to digital converter, in order to achieve the conversion. Figure 5.8 shows the block diagram of the analog to digital conversion subsystem.

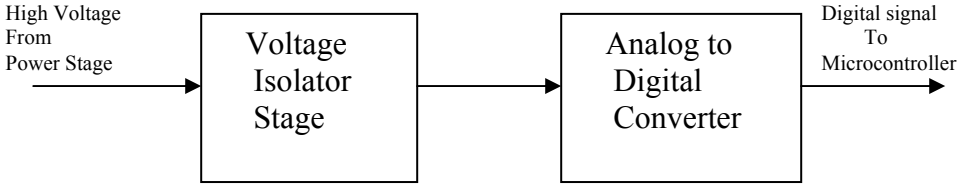


Figure 5.8 Analog to digital conversion subsystem

5.5 Signal Scaling

The analog signal from the power stage is scaled down to a lower value and then converted to a binary value when passing through the stages shown in Figure5.9.

The analog signal converts to binary codes after the signal passes through the power stage, voltage sampler, voltage reference and the analog to digital converter. As the analog to digital converter is single-end and 10bit, the range of the digital signal is in the range of 0 to 1023. The conversion process is shown in Figure5.9.

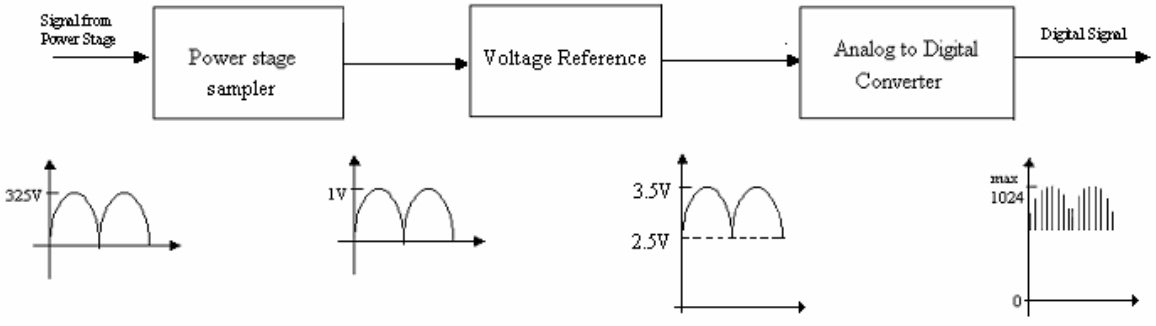


Figure 5.9: The conversion process of the signal

5.6 Voltage Sampler

The voltage from the output of the power stage is at high voltage and must be scaled down before feeding to analog to digital converter.

In this research two voltage samples have to be fed to the A-D converter. One sample voltage is the voltage across the array and the other is corresponds to the current through the array. The Figure 5.10 show the actual circuit of the voltage sampler used in this research.

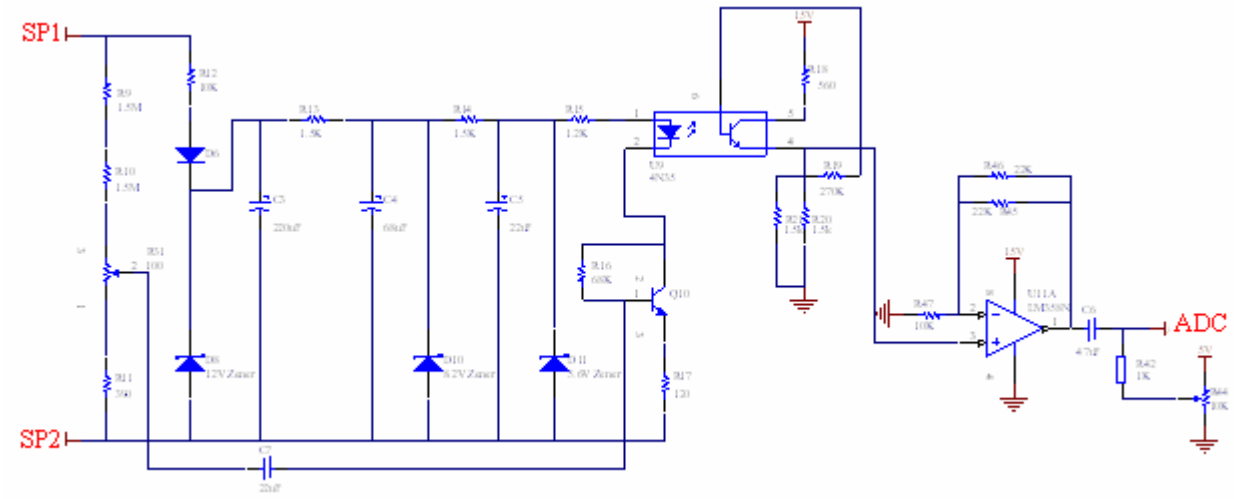


Figure 5.10 Actual circuit diagram of voltage sampler

The optocoupler in each circuit does a very important role. While scaling down the high voltage input to a lower level it provides an electrical isolation by decoupling the ground between power stage and low voltage control circuitry.

The resistor across SP1 and SP2 samples the voltage across the array. The circuit inside the dotted box in the Figure 5.10 provides a stable 8.2V DC rail. Normal regulator chips cannot be used because of the higher voltage range. The transistor Q10 gives an amplification of the sample voltage which can turn on the LED in the optocoupler U9 all the times passing the sampling voltage through it. A voltage level of 15V is applied to the collector of the optocoupler to shift the voltage level above zero volts. Another amplifier U11 is used to amplify the signal and prevent overloading the digital control circuit.

The outputs of voltage sampler is fed to the analog to digital converter. This voltage sample determines diode current required to keep the resistance of the transistor array constant

Figure 5.11 shows the output waveform of the voltage sampler with the input voltage of $230V_{RMS}$ /50 Hz from the main supply of the laboratory.

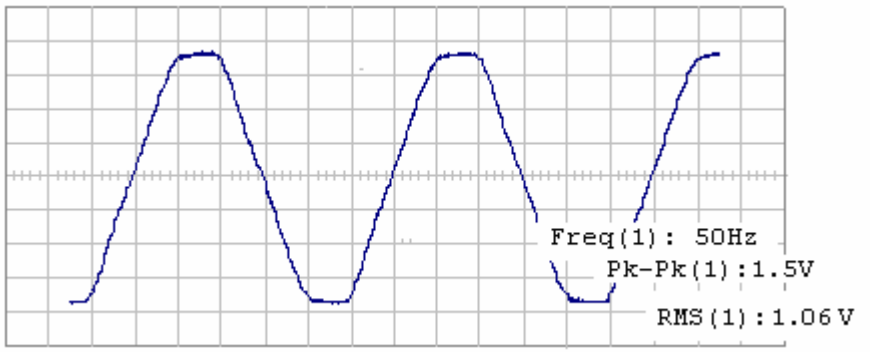


Figure 5.11 Output waveform of the voltage sampler

It is important to note here that the laboratory power supply is not a perfect sine wave. The peak is clipped due to the bus overloading. Therefore output waveform of the voltage sampler shown in Figure 5.11 is a clipped sine wave. The output RMS value of sampler is 583.3mV at 50Hz. That shows the amplitude of the output of voltage sampler is about 1/300 times of input voltage.

This explains that the voltage sampler can scale the high voltages to low voltages while maintaining the exact wave shape of the wave form. It is able to meet the requirement for the analog to digital converter.

Chapter 6

Implementation

6.1 Selection of components

6.1.1 Diode selection

Based on the specifications and the requirements rectifier diodes are selected in order to have safe operation.

Load design was for a 230V/50 Hz supply. The instantaneous peak values often vary up to approximately 260√2V for a range of input AC RMS voltages from 160V to 260V.

Fast recovery rectifier diodes with low noise and having high peak repetitive reverse voltage with low reverse recovery time were selected. Maximum rating of rectifier diode BYT08P-400 Fast recovery rectifier diode is shown in the Figure 6.1[24].

Symbol	Parameter			Value	Unit
V_{RRM}	Repetitive peak reverse voltage			400	V
I_{FRM}	Repetitive peak forward current	tp=5 µs F=5kHz		200	A
$I_{F(RMS)}$	RMS forward current			16	A
$I_{F(AV)}$	Average forward current	TO-220AC	Tc = 120°C δ = 0.5	8	A
		Insulated TO-220AC	Tc = 105°C		
I_{FSM}	Surge non repetitive forward current	tp = 10 ms Sinusoidal		100	A
T_{stg}	Storage temperature range			- 40 to + 150	°C
Tj	Maximum operating junction temperature			150	°C

Figure 6.1: Maximum rating of Fast recovery rectifier diodes

Following Figure 6.2 shows the characteristic curve of the diodes.[24]

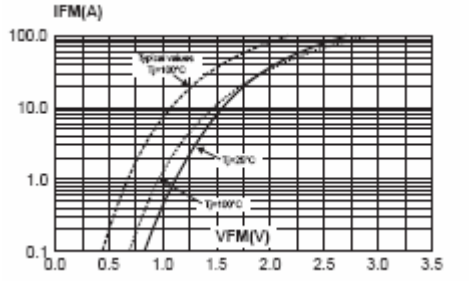


Figure 6.2 Forward voltage Vs forward current (maximum values)

6.1.2 Choice of bipolar junction power transistors

6.1.2.1 High power BJT transistor:

If 230V AC is supplied across the input of the bridge, the transistors should be capable of tolerating instantaneous voltage values with nominal peak value of 325V.

The following characteristics of the transistors are considered

- High power capability
- High current capability
- Maximum Junction temperature

In order to achieve required characteristics NPN 2N3773 complementary Silicon power transistors have been selected. The 2N3773 are Power Base power transistors having high safe operating area and designed for high power linear applications. They have high DC current gain and low saturation gain

Maximum ratings of power transistor of 2N3773 are shown in the Figure 6.3. [25]

Rating	Symbol	Value	Unit
Collector − Emitter Voltage	V_{CEO}	140	Vdc
Collector − Emitter Voltage	V_{CEX}	160	Vdc
Collector − Base Voltage	V_{CBO}	160	Vdc
Emitter − Base Voltage	V_{EBO}	7	Vdc
Collector Current − Continuous − Peak (Note 2)	I_C	 16 30	Adc
Base Current − Continuous − Peak (Note 2)	I_B	 4 15	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	150 0.855	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

Figure 6.3: Maximum ratings of power transistor of 2N3773

There are two limitations on the power handling ability of a transistor based on the following

1. Average junction temperature
2. Second breakdown.

Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation. i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 6.4 is based on the peak junction temperature, T_J(pk) of 200^0C.

Second breakdown pulse limits are valid for duty cycles to 10% provided T_J(pk) <200^0C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Therefore bigger and better heat sinks were used.

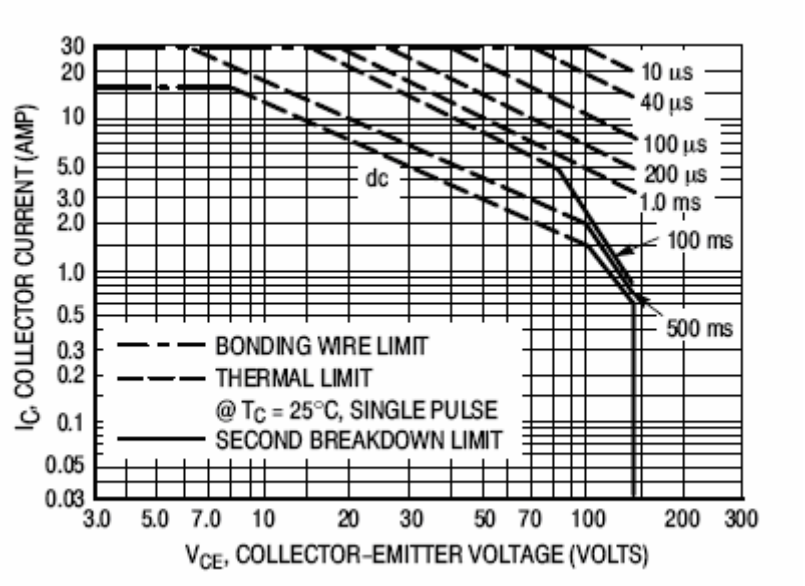


Figure 6.4: Forward biased safe operating area of power transistor 2N3773.[25]

6.1.2.2 Medium power transistor:

As a preamplifier transistors NPN 2N4923 plastic Silicon transistors were selected. They have excellent power dissipation capability and excellent safe operating area. The maximum ratings are shown in the Figure 6.5 [26].

The data of Figure 6.6 is based on $T_J(pk) = 150^0C$; Second breakdown pulse limits are valid for duty cycles to 10% provided $T_J(pk) \leq 150^0C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Small size heat sinks were used for these transistors, as there was no much increase in temperature of the transistor.

Rating		Symbol	Value	Unit
Collector–Emitter Voltage	2N4921 2N4922 2N4923	V_{CEO}	40 60 80	Vdc
Collector–Emitter Voltage	2N4921 2N4922 2N4923	V_{CB}	40 60 80	Vdc
Emitter Base Voltage		V_{EB}	5.0	Vdc
Collector Current – Continuous (Note 1)		I_C	1.0 3.0	Adc
Base Current – Continuous		I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C		P_D	30 0.24	W mW/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	–65 to +150	°C

Figure 6.5: Maximum ratings of 2N4923

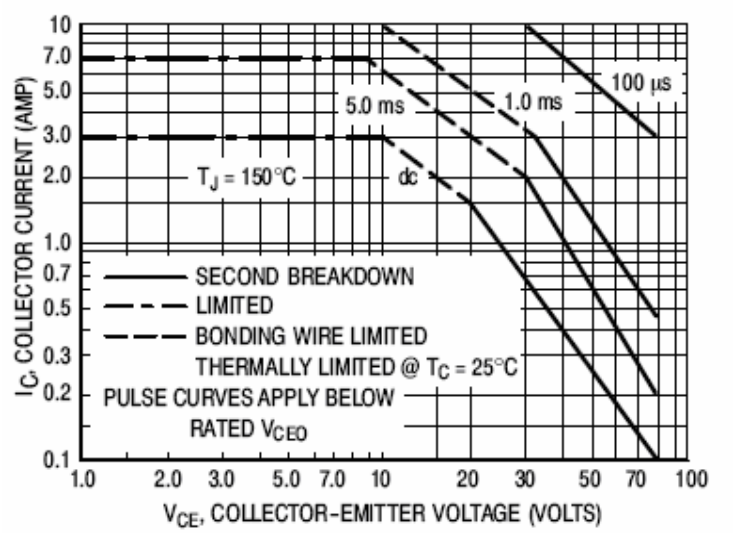


Figure 6.6 Forward biased safe operating area of medium power transistor 2N4923 [26]

The collector-emitter maximum voltage is 80V in this transistor. It is just enough to withstand the 230V input. Because of the availability of this transistor it is decided to use.

6.1.2.3 Selection of optocoupler

The TOSHIBA TLP521-4, rank A photocoupler was selected in order to get four channels in one package. Rectified input voltage to the load is about 200V DC and therefore applied voltage across collector and emitter of the phototransistor is less than the maximum rating of the optocoupler. The minimum current transfer ratio is 50%. The minimum isolation voltage is about 2500V RMS.

Maximum ratings at 25^0C are shown in the Figure 6.7 [22].

	Characteristic	Symbol	Rating		Unit
			TLP521–1	TLP521–2 TLP521–4	
LED	Forward current	I_F	70	50	mA
	Forward current derating	ΔI_F /°C	–0.93 (Ta ≥ 50°C)	–0.5 (Ta ≥ 25°C)	mA /°C
	Pulse forward current	I_{FP}	1 (100μ pulse, 100pps)		A
	Reverse voltage	V_R	5		V
	Junction temperature	T_j	125		°C
Detector	Collector–emitter voltage	V_{CEO}	55		V
	Emitter–collector valtage	V_{ECO}	7		V
	Collector current	I_C	50		mA
	Collector power dissipation (1 circuit)	P_C	150	100	mW
	Collector power dissipation derating (1 circuit Ta ≥ 25°C)	ΔP_C /°C	–1.5	–1.0	mW /°C
	Junction temperature	T_j	125		°C
Storage temperature range		T_{stg}	–55~125		°C
Operating temperature range		T_{opr}	–55~100		°C
Lead soldering temperature		T_{sol}	260 (10 s)		°C
Total package power dissipation		P_T	250	150	mW
Total package power dissipation derating (Ta ≥ 25°C)		ΔP_T /°C	–2.5	–1.5	mW /°C
Isolation voltage		BV_S	2500 (AC, 1min., R.H.≤ 60%) (Note 1)		Vrms

Figure 6.7 Maximum ratings of TLP521-4

Variation of the diode forward current and collector current and variation of current transfer ratio are shown in Figure 6.8 and Figure 6.9 [22].

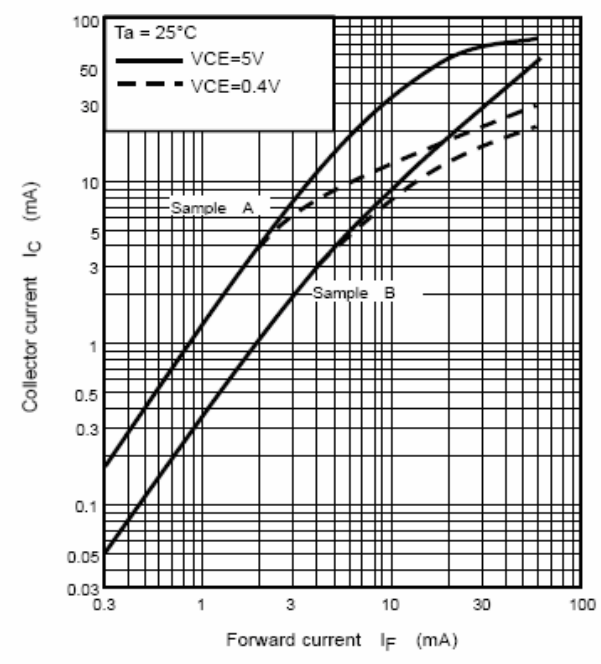


Figure 6.8 Forward current I_F Vs collector current I_C

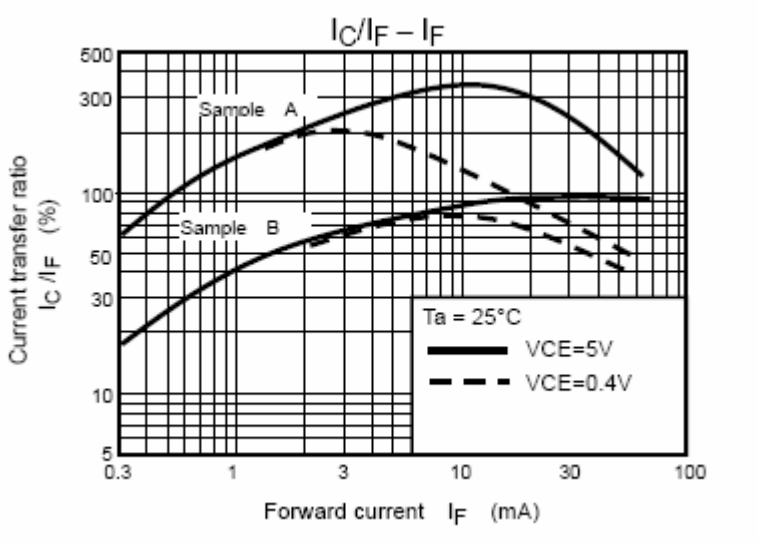


Figure 6.9 Variation of current transfer ratio

6.2 Heat Sink Design

Heat sinks are used to conduct heat between the case of the transistor and the ambient to keep the junction temperature of the power transistor within reasonable limits. There are various shapes of heat sinks are available in the market. The choice of proper heat sink depends on the allowable junction temperature the device can tolerate [27].

Thermal resistance of the heat sink to ambient, $R_{\theta sa}$ decides the type of heat sink and it can be found as flows.

The worst case design, the maximum junction temperature $T_{j,max}$, the maximum ambient temperature $T_{a,max}$, the maximum operating voltage, the maximum on state current are specified in the data sheets. The maximum The maximum power loss is calculated from the equation below taking the rms consideration in this ac cycle.

$$\frac{V_{CEpeak} * I_{Cpeak}}{2}$$

Then junction to ambient resistance, $R_{\theta ja}$ can be found from the equation

$$R_{\theta ja} = \frac{\left(T_{j,\max} - T_{a,\max}\right)}{P_{loss}} \quad [27]$$

Junction to case thermal resistance, $R_{\theta jc}$ can be obtained from the transistor data sheet.
Case to sink thermal resistance, $R_{\theta cs}$ value is 0.4 ^{0}C/W when it is used with heat sink compound [27].

Then $R_{\theta sa}$ can be found from the equation,

$$R_{\theta ja} = R_{\theta jc} + R_{\theta cs} + R_{\theta sa} \qquad [27]$$

In the data sheet of heat sinks contains the type of the heat sink matching to the resistance $R_{\theta sa}$.

6.2.1 Calculation and selection of heat sink

From the data sheet of 2N3773 power transistor following values were found.

$R_{\theta jc}$ =1.17 ^{0}C/W

$T_{j,max}$= 200 ^{0}C

$T_{a,max}$ = 25 ^{0}C

Total maximum power dissipation = 150W

Then $R_{\theta ja}$ = (200 – 25)/150 = 1.66^{0}C/W

Also $R_{\theta sa}$ = 1.66 -1.17-0.4 =0.45 ^{0}C/W

From the ABL manufacturers, heat sinks which have $R_{\theta sa}$ of 0.42^{0}C/W and dimensions 50x125x200 mm were selected.

Total power loss,

$$150 \geq \frac{V_{CEpeak} * I_{Cpeak}}{2}$$

The maximum voltage applies across the transistor V_{CEpeak} = 320/4 V

Then from above equation I_{cpeak} can be calculated.

Then maximum I_{CEpeak} will be 3.75A.

Maximum rms current will be I_{CEpeak} /√2

6.3 Implementation of power Stage

Four 2N3773 power transistors and 2N4923 medium power transistors were combined as Darlington pairs to make the transistor array as shown in the Figure 6.10. Darlington configuration allows an effective increase of the gain of the composite transistor pair. Power transistors were mounted on separate heat sinks of adequate capacity in order to have better heat sinks to control the temperature of the transistors. Good heat sink design is very important since the gain of the power transistor is highly influenced by the temperature as discussed in the Section 6.2

The transistors were powered by the main supply through a rectifier bridge in order to give unidirectional positive current flow through the transistors and get the alternating current effect at the input of the diode bridge.

For the purpose of safety and protection while carrying out the tests an isolation transformer and variac were used. As the maximum current rating of the variac is 2A, the maximum experimental rms collector current through the power transistor has to be limited maximum of 2A.

The voltage across the transistor array was fed to the sampling circuit and output was fed to the Analog to Digital Converter of the MDS-GP development board. DC voltages 15V and 5V required in the sampling circuit shown in Figure 5.10 in Chapter 5 was supplied by a DC power source.

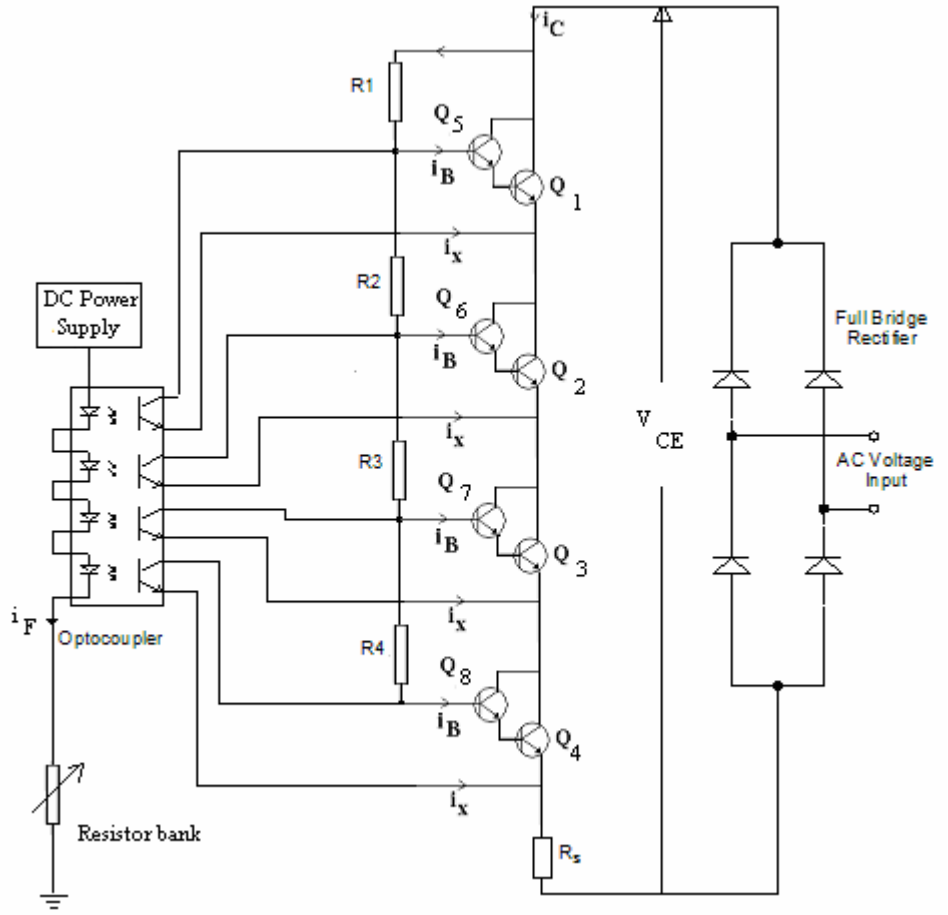


Figure 6.10: Initial Stage of the AC electronic load

6.4 Digital Control

To decide the digital controlling criteria the behavior of the array was taken in to consideration as discussed in section 6.4.1. The mathematical approach discussed in Section 6.4.2 was used when programming the microcontroller.

6.4.1 Observation and measurements on the behavior of the array without the digital control

The behavior of the transistor array was observed initially without the control circuitry. At this stage diode current was controlled manually by using a resistor bank in series with the optoisolator diodes as shown in the Figure 6.10 and using a DC power source with voltage of 10V.

The voltage across the array V_{CE} and current through it I_C was monitored. The oscilloscope captures of voltage across the array and the collector current without the digital controller is shown in the Figure 6.11 indicating the nature of the current harmonics and non linear impedance behaviour of the array at different instantaneous voltages.

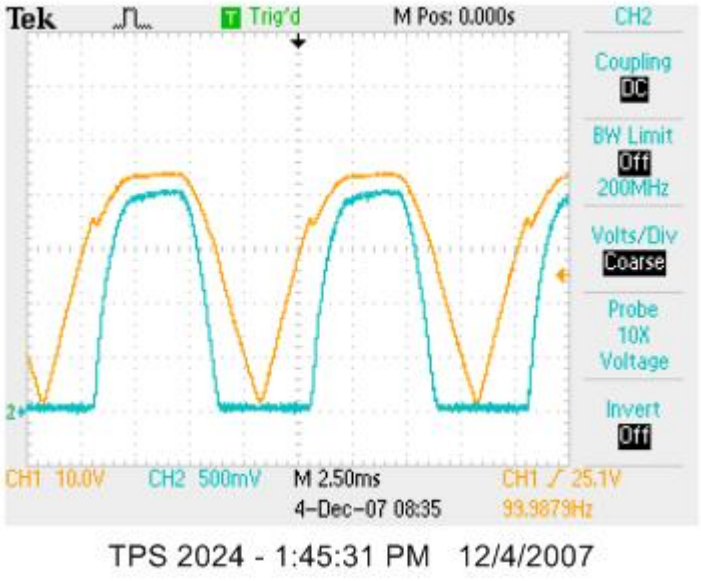


Figure 6.11: Oscilloscope captures of voltage across the array and collector current

The circuit was tested and current through the array was measured for different values of diode current (i_F) with two different set of values of R_1 to R_4 *(i.e*R_B*)* while maintaining the rms voltage across the array constant.

For a fixed set of R_1 to R_4(R_B) value, the resistance across the array was calculated at different voltages and they were plotted against the diode current as shown in Figure 6.12, Figure 6.13 and Figure 6.14. These three figures corresponds to three different values of R_1 to R_4(R_B). When looking at the graphs it is obvious to see that the resistance across the array is not linear.

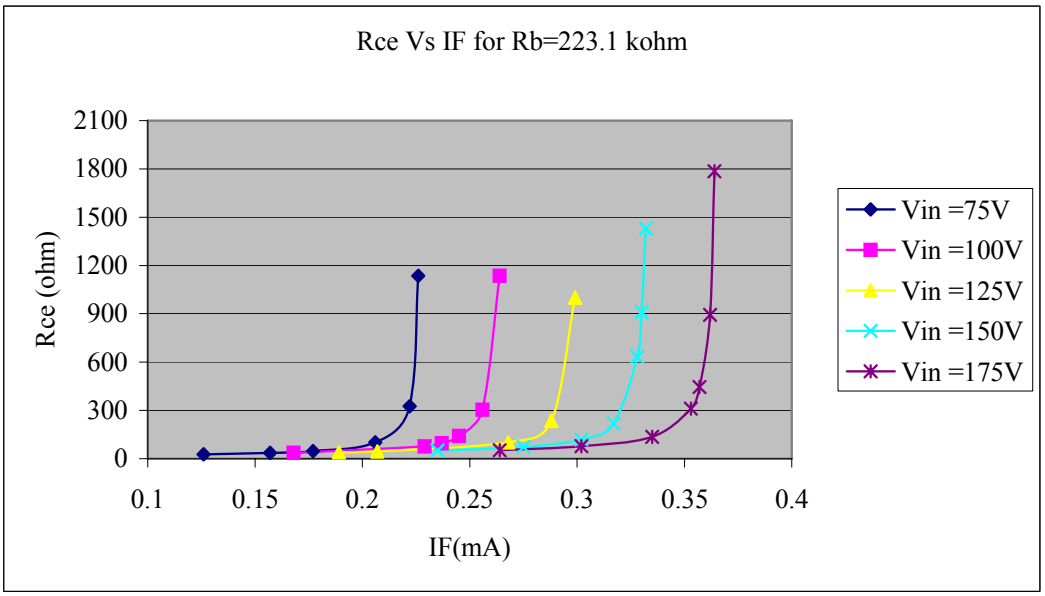


Figure 6.12: Variation of the resistance of the array with the diode current of optoisolator when R_B =220KΩ [Measured values]

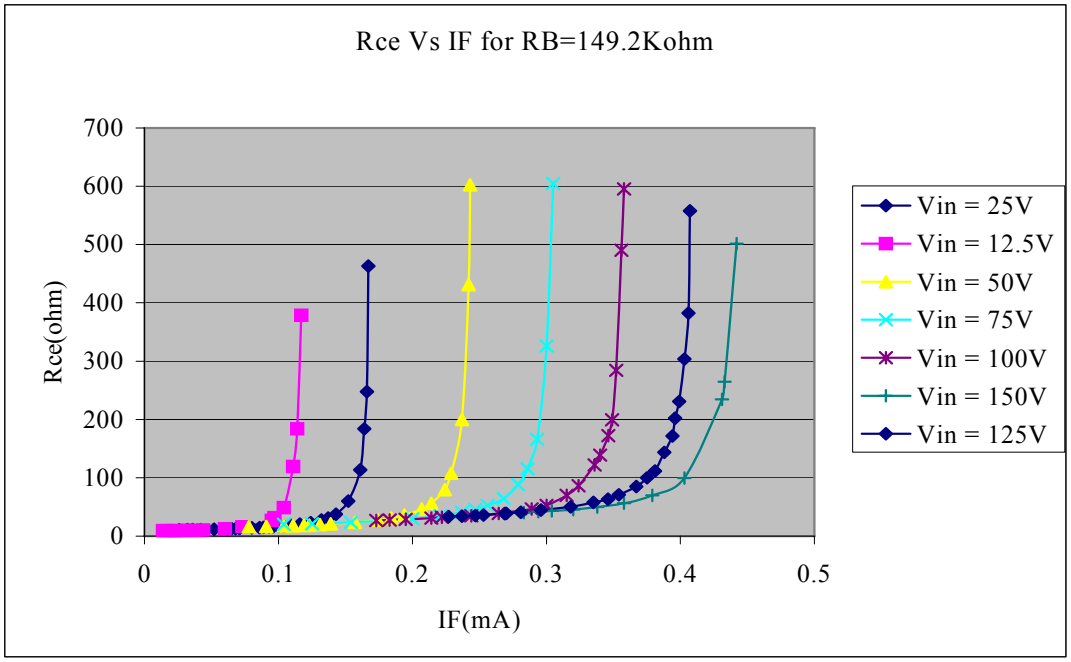


Figure 6.13: Variation of the resistance of the array with the diode current of optoisolator when R_B=150KΩ [Measured values]

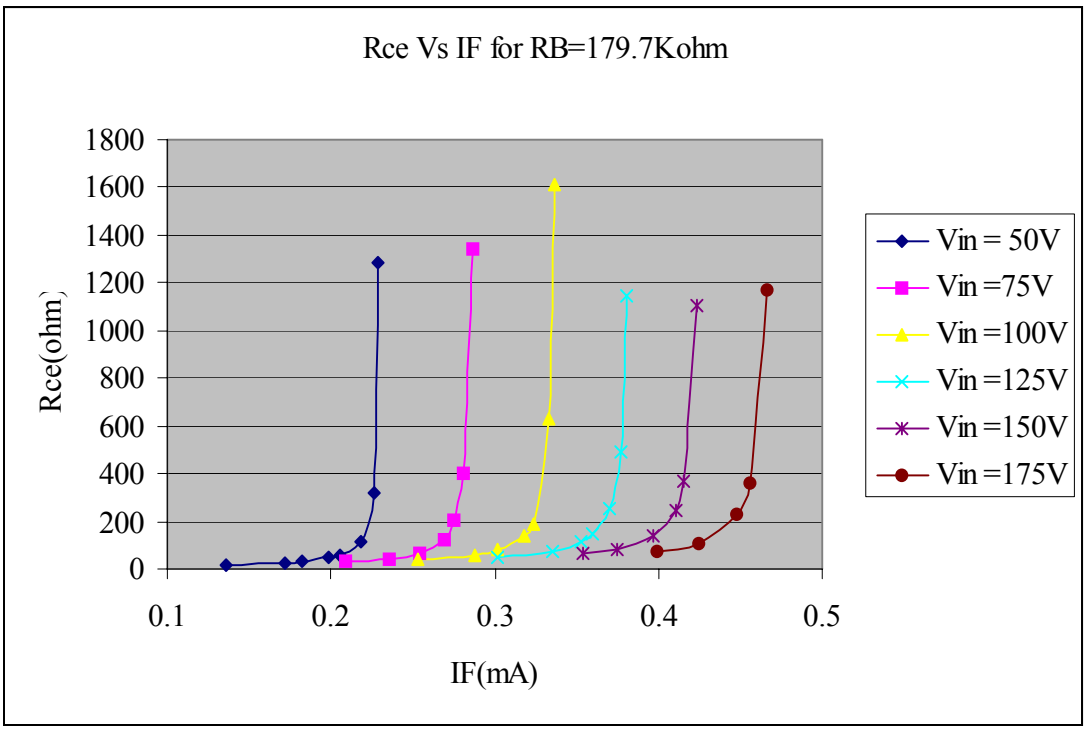


Figure 6.14: Variation of the resistance of the array with the diode current of optoisolator when R_B =180KΩ [Measured values]

In theory if all transistors are identical,

$$R_1 = \frac{R_B}{4}, R_2 = \frac{R_B}{3}, R_3 = \frac{R_B}{2}, R_4 = R_B$$

However due to non-identical transistor parameters of the four transistors of the array, R1 to R4 were adjusted slightly to have approximately equal voltages among them.

6.4.2 Mathematical Approach

In order to control the diode current of the optoisolator it is required to find the actual relationship of the resistance with the voltage across the array (V_{CE}) and the diode current (i_F).

It has been already proved in the Chapter 3 that the approximate R_{CE} is given by the equation 3.12.

$$R_{CE} \approx \frac{n\,R_B}{\beta}(1+\frac{i_x}{i_B})$$

And also it is known that

$$v_C(t) - v_{BE} = n\,R_B\,(i_B + i_x) \text{.....(6.1)}$$

and $V_C(t)$ is the voltage across collector and emitter V_{CE} and i_x is the collector current I_C of opto isolator given by the following equation

$$I_C = K\left(\frac{I_F}{I_{F'}}\right)^p$$

Compare to V_{CE} , V_{BE} is very small and can be neglected

Then the equation (6.1) becomes

$$v_{CE} = n\,R_B\,(i_B + i_x)$$

$$i_B = \frac{v_{CE}}{nR_B} - i_x \text{.....(6.2)}$$

Substituting value of i_B of equation (6.2) and i_x(=I_C)value in equation (3.12)

$$R_{CE} \approx \frac{n\,R_B}{\beta}\left[1+\frac{K\left(\frac{I_F}{I_{F'}}\right)^p}{\left\{\frac{V_{CE}}{nR_B}-K\left(\frac{I_F}{I_{F'}}\right)^p\right\}}\right] \text{.....(6.3)}$$

If V_{BE} is very small and therefore it is neglected, then it is proved that

According to Equation 6.1 R_{CE} is a function of V_{CE} and I_F.

For a fixed R_{CE}, equation 6.1 can be re arranged as follows.

$$\frac{R_{CE}\beta}{n\,R_B}\left\{\frac{V_{CE}}{nR_B}-K\left(\frac{I_F}{I_{F'}}\right)^p\right\} \approx \frac{V_{CE}}{nR_B}$$

$$\left[\frac{R_{CE}\beta}{n\,R_B}-1\right]V_{CE} = K\beta R_{CE}\left(\frac{I_F}{I_{F'}}\right)^p$$

$$V_{CE} = \frac{K\beta\, n\,R_B\,R_{CE}}{\left(\beta R_{CE}-n\,R_B\right)}\left(\frac{I_F}{I_{F'}}\right)^p \text{.....(6.4)}$$

Taking logarithmic value of V_{CE} and I_F in equation 6.4

$$\ln V_{CE} = p\,\ln I_F + \frac{K\beta\, n\,R_B\,R_{CE}}{\left(\beta R_{CE}-n\,R_B\right)I_{F'}{}^p} \text{.....(6.5)}$$

This equation proves that for a fixed known resistance of the array, logarithmic value of voltage across the array varies linearly with the logarithmic value of the diode current. It gives a straight line with gradient p and the intercept C depends on the expected array resistance R_{CE}.

Based on the relationship in Equation 6.5 & the experimental results of the measurements as per Figures 6.12 to 6.14 (which are also tallying with simulations as per details in chapter 4), following relationships can be established.

a. For lower R_{ce} values constant p is highly variable (2.9 to1.89) & C is variable from 29.84 to 19.8.
b. For higher R_{ce} values (over 100Ω) p is approximately constant around 1.8 (tallies with Opto isolator data sheet values (1.8 to 2) C value falls within 19.8 to 18.47.

The graphs in figures 6.15 to 6.23 indicate these relationships. R2 value shown in the figures shows accuracy the equation is.

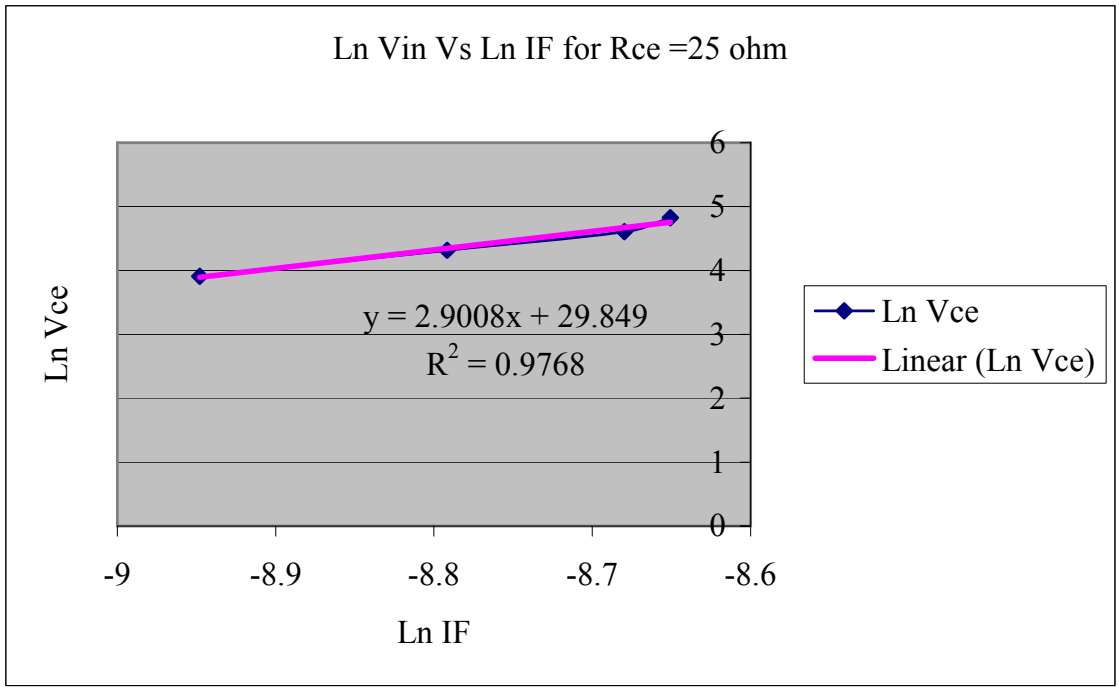


Figure 6.15: *Ln* V_{in} Vs *Ln* I_F for *Rce* =25 ohm

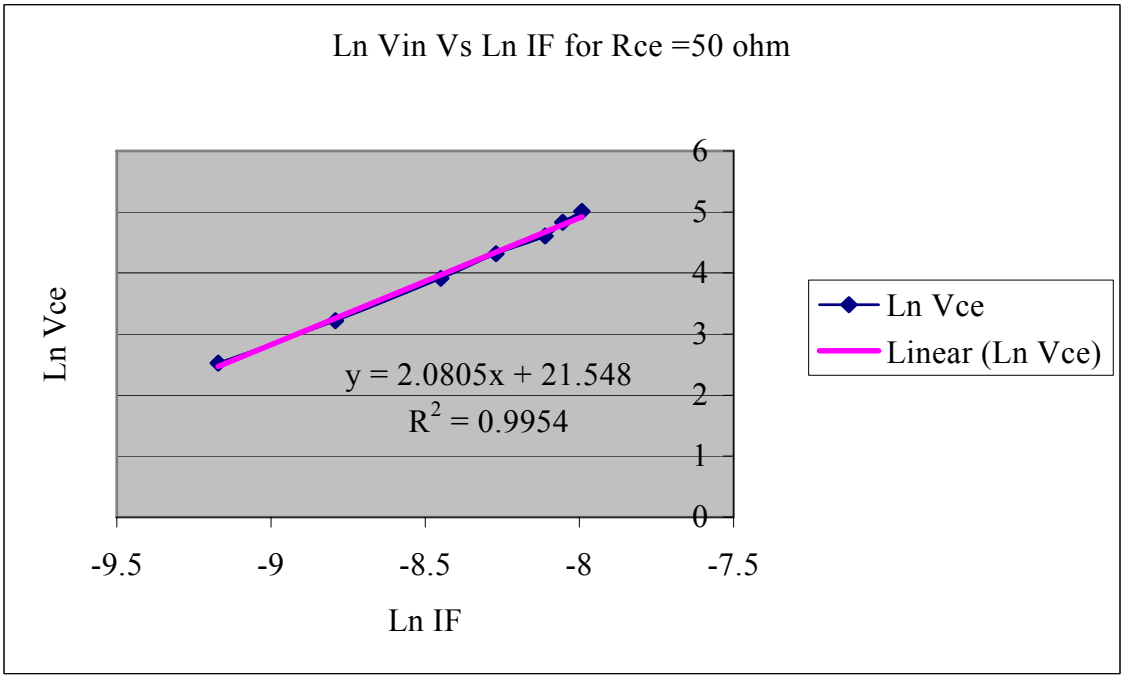


Figure 6.16: *Ln* V_{in} Vs *Ln* I_F for *Rce* =50 ohm

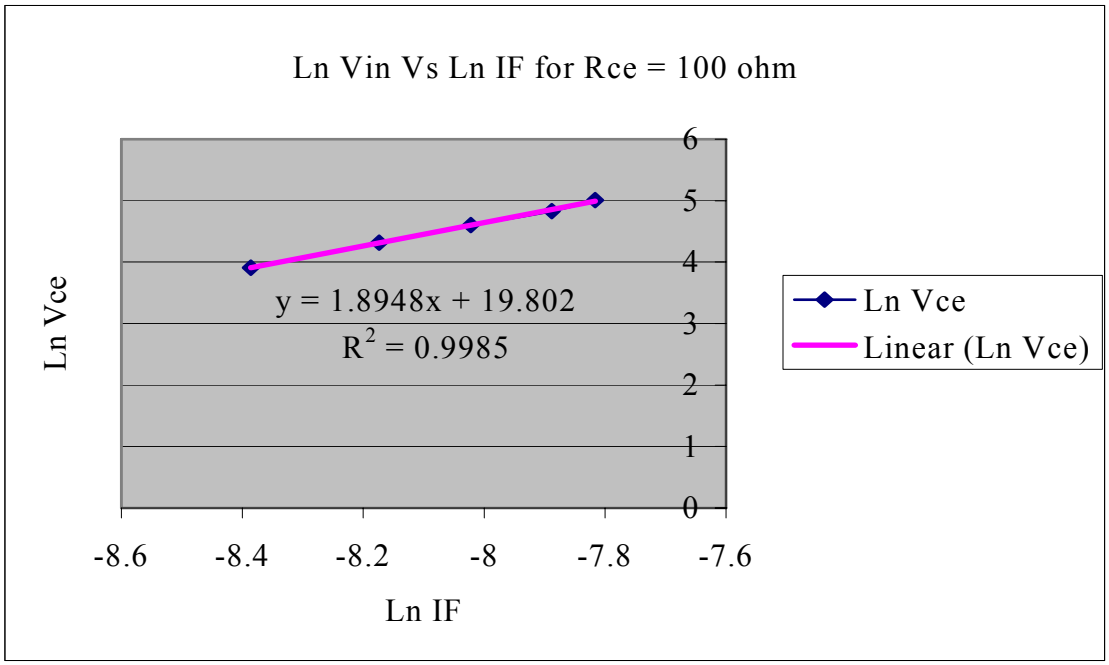


Figure 6.17: *Ln* V_{in} Vs *Ln* I_F for *Rce* =100 ohm

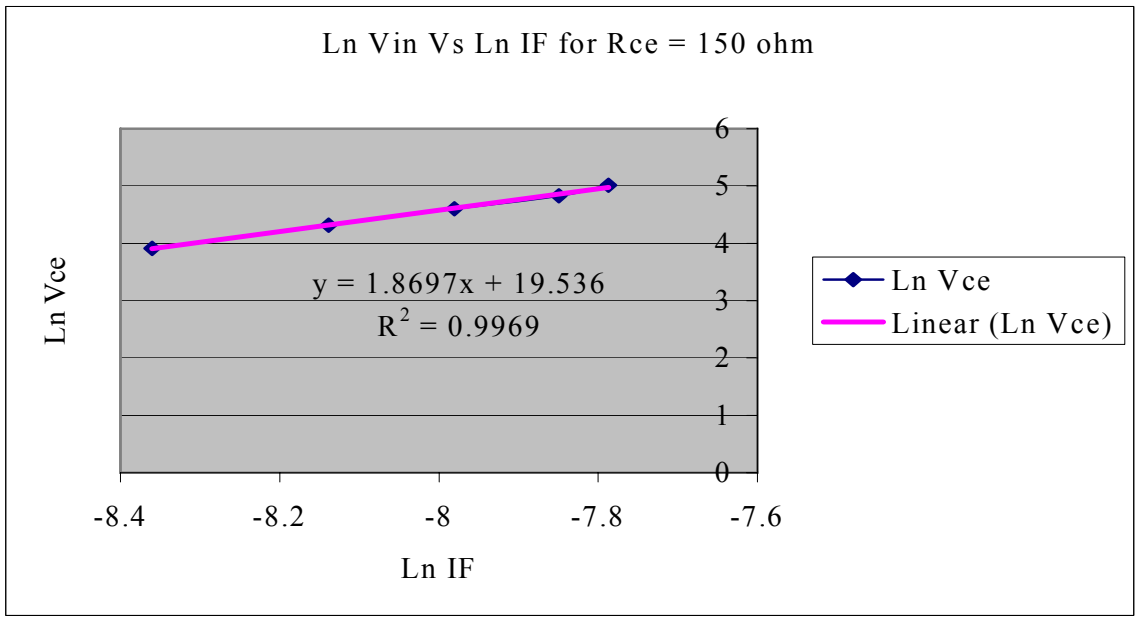


Figure 6.18: *Ln* V_{in} Vs *Ln* I_F for *Rce* =150 ohm

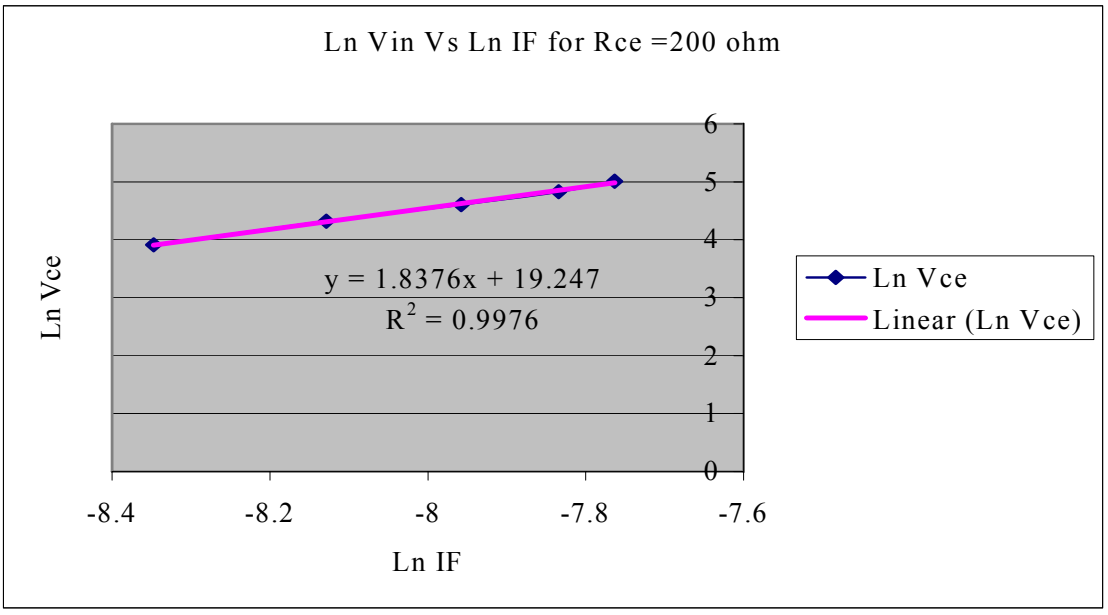


Figure 6.19: *Ln* V_{in} Vs *Ln* I_F for *Rce* =200 ohm

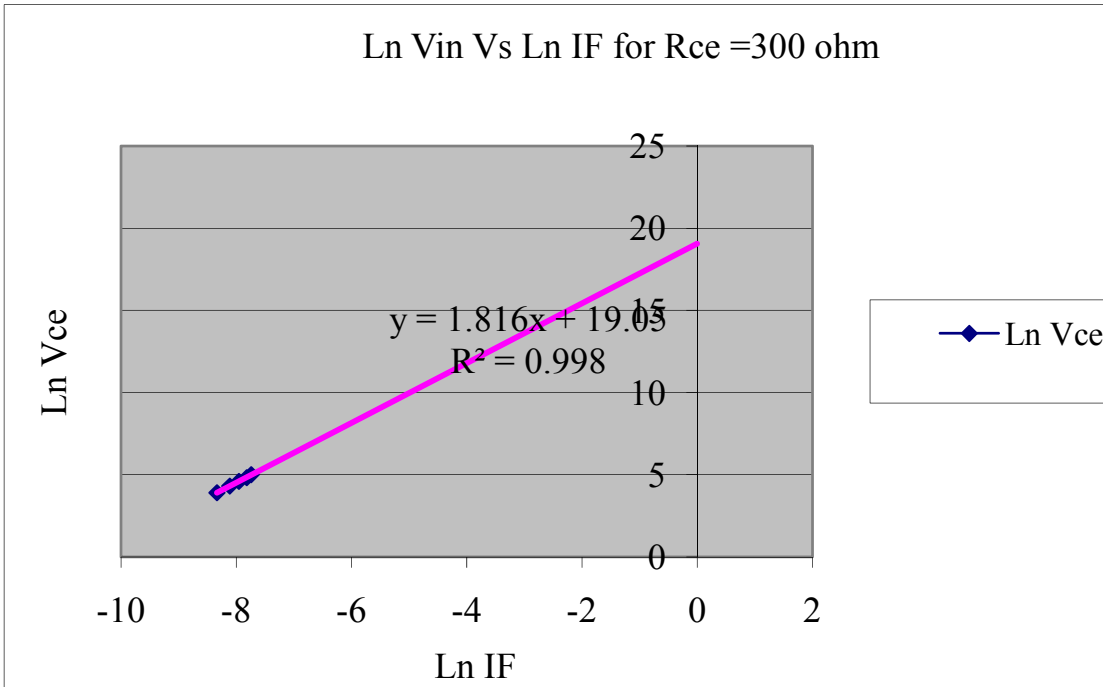


Figure 6.20: *Ln* V_{in} Vs *Ln* I_F for *Rce* =300 ohm

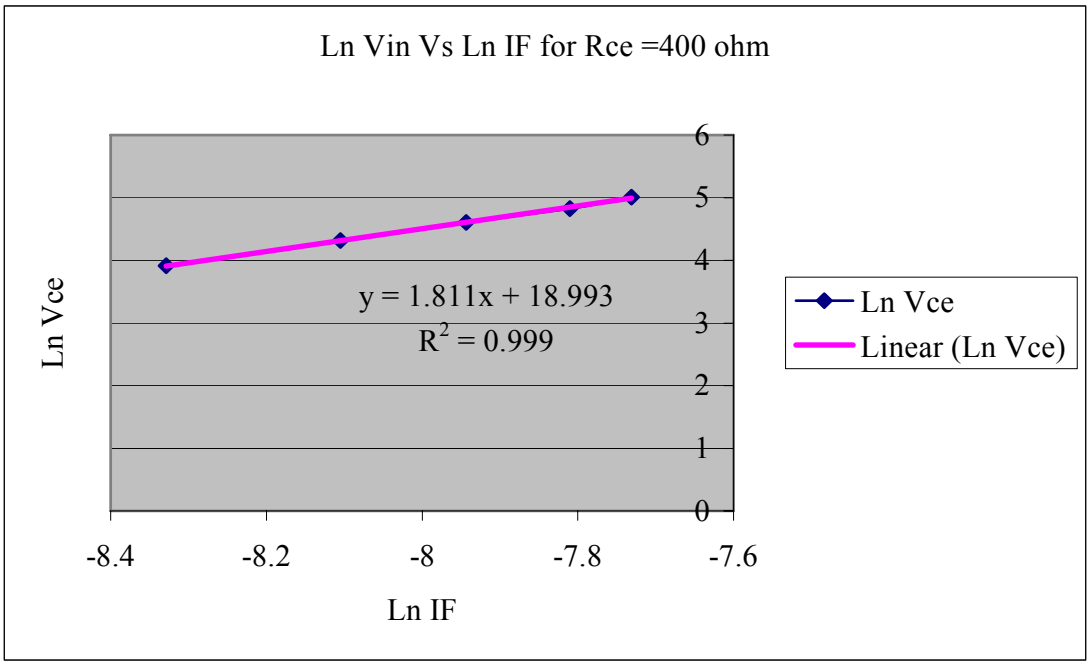


Figure 6.21: *Ln* V_{in} Vs *Ln* I_F for *Rce* =400 ohm

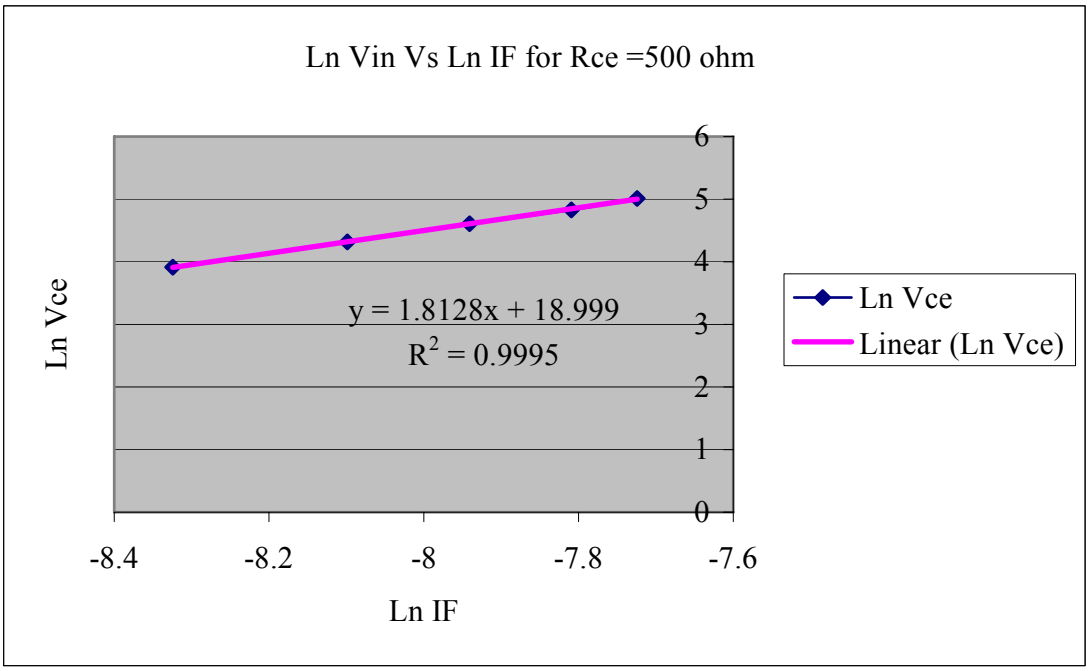


Figure 6.22: *Ln* V_{in} Vs *Ln* I_F for *Rce* =500 ohm

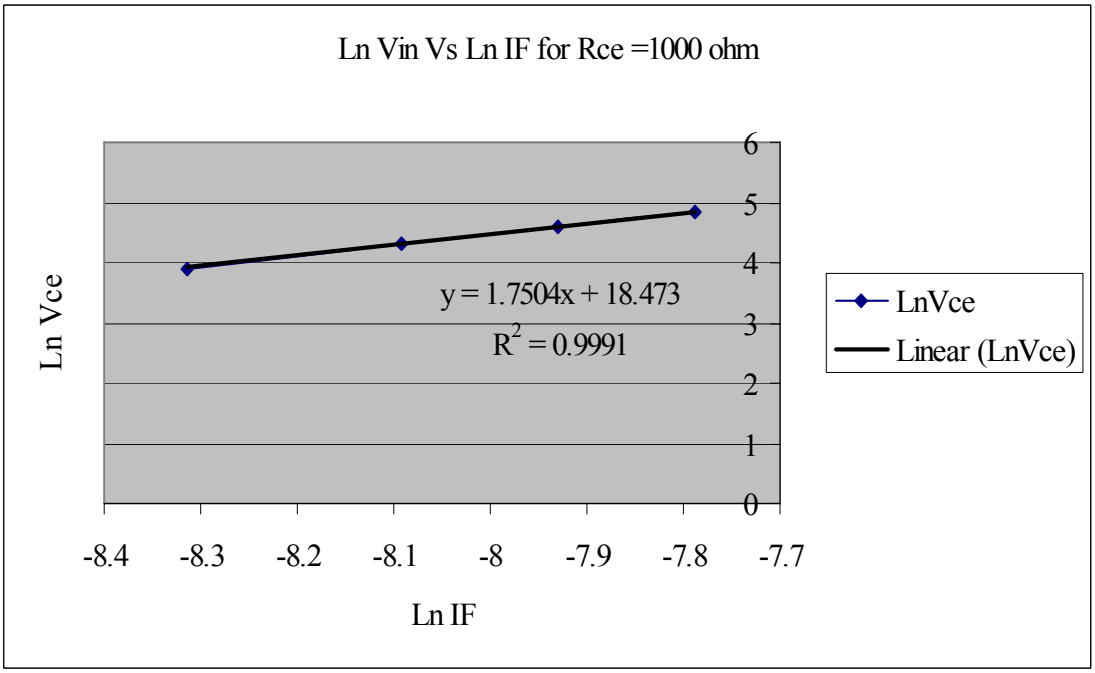


Figure 6.23: *Ln* V_{in} Vs *Ln* I_F for *Rce* =1000 ohm

With the closer look on these graphs and equations it can be seen that the resistance value below 50Ω, the gradient of the line is nearly changing. However the gradient p value has a limited range for a given optoisolator and hence in that region the resistance across the array is less dependent of the voltage V_{ce} and therefore difficult to controll by the diode current of the optoisolator. In the range of *Rce* values above 100Ω, p is nearly a constant and within the data sheet values allowing the control of resistance.
When the base current of the transistors were fully diverted by the diode, leakage currents through transistors. This makes the resistance to be very large value. In that region again the resistance cannot be easily controlled by the diode current.

6.5 Digital Control algorithm

According to the graphs obtained in Section 6.4.2 for a fixed resistance value the relationship of the voltage across the array with the diode current can be written as

$$\ln V_{ce} = m \ln I_F + C \text{.....(6.6)}$$

The gradient m is nearly a constant value and intercept C is varied with the resistance value.
If the voltage value is known, required I_F for fixed resistance can be obtained by the equation (6.6).

$$I_F = e^{\left[\frac{\ln V_{CE} - C}{m}\right]} \text{.....(6.7)}$$

For different resistances *m* and *C* value should be fed to the program to achieve different values for *Rce*.

The voltage from the array was sampled at a frequency of 1kHz and A to D converter reads the voltage value at every 1ms and converted to a binary value and then solving the equation (6.7) microcontroller outputs the binary current value proportional to the required I_F. In every 1ms the binary value from the controller was fed to the digital to analog converter. It converts the binary value to analog current and fed to the optoisolator diode.

The microprocessor was fast enough to carry on the real time correction. The process of controlling the base current is shown in the flow chart in Figure 6.24.

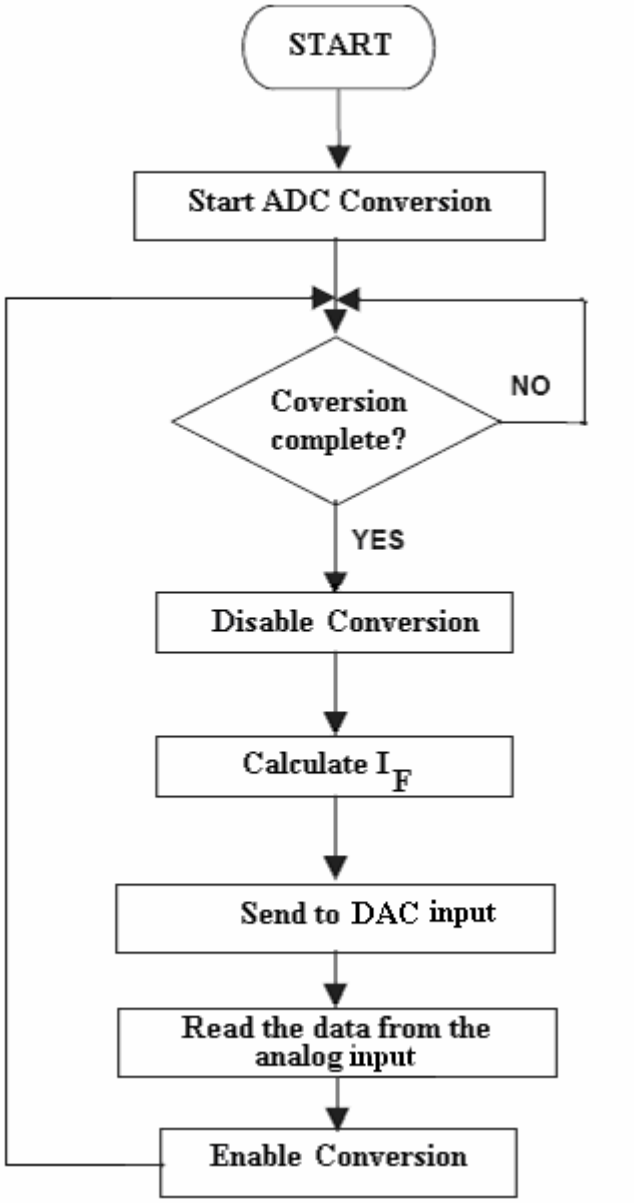


Figure 6.24: Software Flow chart

6.6 Program Code

The C code used in the research is given below [28]

```
// Project : AC Load

/*****************************************************************************/

#include <ez8.h>
#include <stdio.h>
#include <uart.h>
#include <math.h>



/*****************************************************************************/
//Defining Global variables//
/*****************************************************************************/

unsigned int ADC1_value; //variable for store ADC0
float DAC_value;
unsigned char counter;
unsigned int count;
float m;
float a;
float Iref;

/*****************************************************************************/
//Function prototypes//
/*****************************************************************************/

void ADCconversion1 (void);
void Calculation (void);
void OneMSDelay (void);
void DAC conversion(void);
void hyperterm_send Char(unsigned char chr);
unsigned char hyperterm_readChar();
void hyperterm_CRLF();
```

```
/*************************************************************************/
//----Main----//
/*************************************************************************/

void main()
{
        PBADDR = 0x02; // Setting Port B for Alternate function
        PBAF   = 0x03; // Selecting PB0 and PB1 for Analog inputs
        PBADDR = 0x01; // selecting port B as a input
        PBDD   = 0xFF;
        PBADDR = 0x03; // selecting open drain mode
        PBOC   = 0xFF;
        PBADDR = 0x04;  //selecting high drive disable
        PBHDE  = 0x00;

        PFADDR = 0x01; // Selecting Port F as output by selecting data direction
        PFDD   = 0x00;
        PFADDR = 0x03; // selecting open drain mode
        PFOC   = 0xFF;
        PFADDR = 0x04;  //selecting high drive disable
        PFHDE  = 0x00;
        PFOUT  = 0x00; // Output is Port F
        PFCTL  = 0xFF; // Port F subregisters are accessible

        PAADDR = 0x02; // Setting Port A for Alternate function
        PAAF   = 0x30; // Setting Alternate function for UART (Port A bits 4 & 5)
         PACTL |= 0x20;
         U0BRH  = 0x00; // Set Baud rate (=38400 bits/s) high and low registers
         U0BRL  = 0x09;
         U0CTL0 = 0xC0; // Enable UART to transmit

/*--Begin Program--*/


       while(1)                         // Loop forever
         {
                    ADC conversion1();
                    hyperterm_sendChar();
                    Calculation();
                    hyperterm_sendChar();
                    DAC conversion();
                     hyperterm_sendChar();
                     OneMSDelay();              // One ms Delay

          }
}

/*------End Main-------*/
```

```
/*************************************************************************/
/---Calling Functions-----//
/*************************************************************************/

// first Function//

void ADCconversion1 (void)

{
   unsigned char temp;

        ADCCTL |= 0x01;  // Select Channel ANA1 for one input
ADCCTL &=~0x10; // Selecting single shot conversion

        ADCCTL &=~0x20;  // clear VREF to enable internal voltage reference
ADCCTL |= 0x80;  // Start ADC Conversion

   while
        ((ADCCTL & 0x80)==0x80);      // wait until ADC finishes
        ADC1_value = ADCD_H;         // store 10bit ADC result to ADC0_value
        ADC1_value = ADC1_value << 2;

        temp = ADCD_L;
        temp = temp >> 6;

        ADC1_value = ADC1_value + temp;

                                                                    }

// Second function//

void Calculation (void)

{
                DAC_value = ADC1_value*217.75;
                DAC_value = log (DAC_value);
                DAC_value = DAC_value -C;
                DAC_value = DAC_value /m;
                DAC_value = exp (DAC_value);
                DAC_value = DAC_value*0.002;


}
```

```
//third Function//

void DAC conversion(void)

{
    PFOUT = DAC_value;
}



// Fourth Function//

void OneMSDelay(int count)

{
   int i,j;

     for
        (i=0; i<count; i++);
        {
             for
                (j=0; j<count; j++);
        }
}
```

Chapter 7

Results

The load was tested for different resistance values with digital control and without digital control. All the given values of load current and load voltage included in this chapter are RMS values.

7.1 Variables m and C

While testing with digital control it was required to change the code of the microcontroller for different resistance values. To measure the THD for different values of current while keeping voltage constant and for different values of voltage while keeping current constant, the variables *m* and *C* in equation 6.7 are required to input to the controller programming code. The variables *m* and *C* values reference to a particular resistance is given in the Table 7.1.

For constant load voltage of 100V,

I(A)	R ce(Ω)	m	C
0.1	1000	1.7504	18.473
0.2	500	1.8128	18.999
0.5	200	1.8376	19.247
0.7	150	1.8697	19.536
1	100	1.8948	19.802
1.3	75	1.9131	19.999
1.5	65	1.9182	20.072

Table 7.1: Required m and C value at constant voltage of 100V

For constant load voltage V of150V,

I(A)	*R ce(Ω)*	*m*	*C*
0.15	1000	1.7504	18.473
0.3	500	1.8128	18.999
0.5	300	1.8169	19.053
0.75	200	1.8376	19.247
1	100	1.8948	19.802
1.5	65	1.9182	20.072

Table 7.2: Required m and C value at constant voltage of 150V

For constant load current of I of 1A,

V	*R ce(Ω)*	*m*	*C*
50	50	2.2687	23.118
75	75	1.8948	19.802
100	100	1.9131	19.999
125	125	1.6769	19692
150	150	1.8697	19.536

Table 7.3: Required m and C value at constant voltage of 100V

While carrying out testing without digital control different load current values were obtained by changing the diode current of optoisolator manually using a resistor bank.

The waveforms of current and voltage of the load, fast Fourier transform (FFT) and total harmonic distortion (THD) were obtained using a waveform analyzer under two conditions for the different values of constant resistance across the array.

7.2 Oscilloscope captures

7.2.1 At bridge points

Oscilloscope captures of the wave form of the load voltage and current at bridge points are with controller and without controller when the resistance of the array is 50Ω are shown in Figure 7.1 and Figure 7.2. The voltages are shown in yellow and currents are shown in blue.

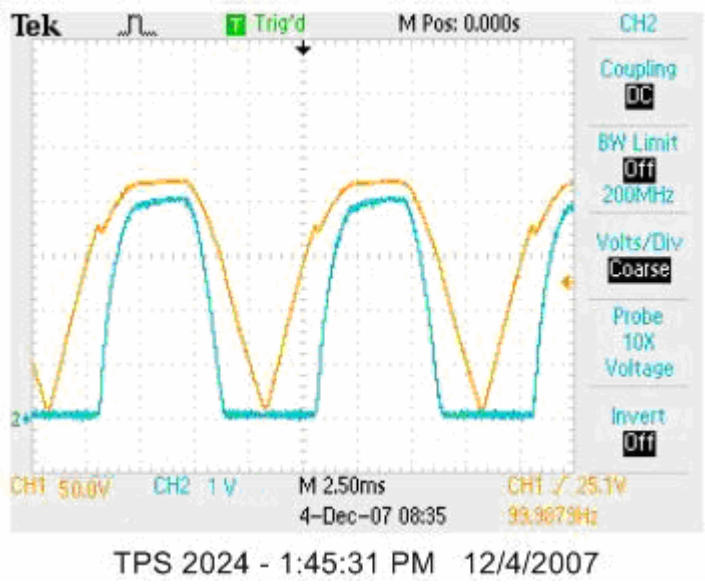


Figure 7.1: Voltage and current at bridge points without controller

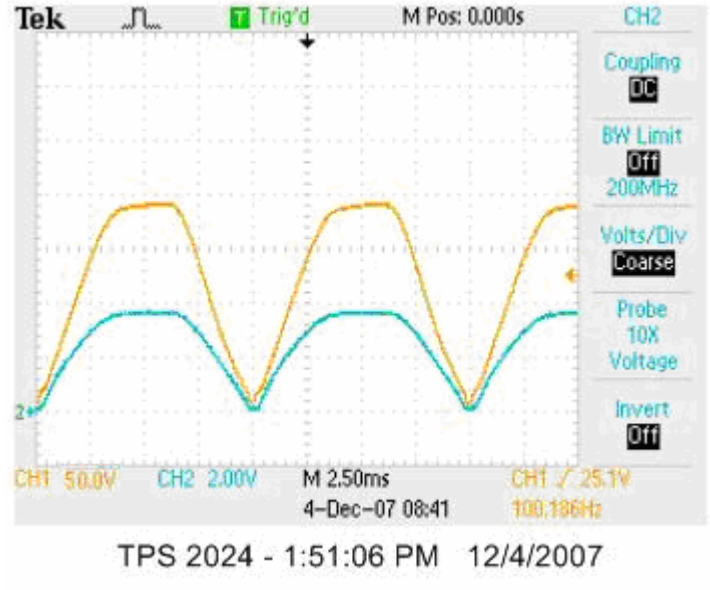


Figure 7.2: Voltage and current at bridge points with controller

7.2.2 Across the load bridge points

Oscilloscope captures of the wave form of the load voltage and current through the load with controller and without controller when the resistance of the array is at different values are shown in Figure 7.3 and Figure 7.9.

7.2.2.1 Voltage wave form of the load

Voltage waveforms of the load with and without digital controller are shown in Figure 7.3 and 7.4.

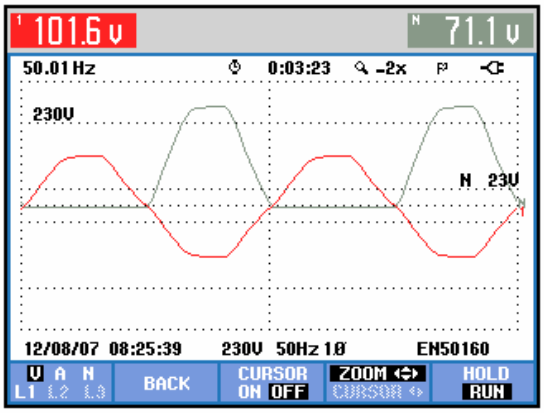


Figure 7.3: Voltage waveform of the load with the digital control

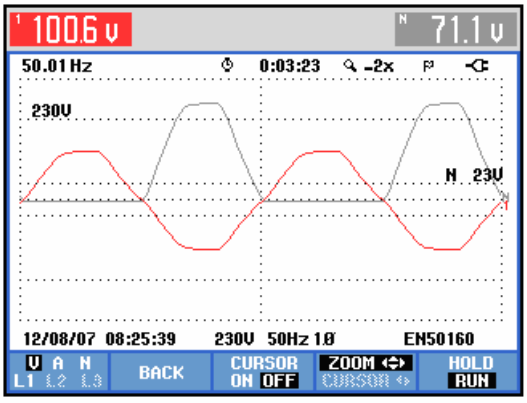


Figure 7.4: Voltage waveform of the load without the digital control

7.2.2.2 Current wave form of the load

The current waveform of the load when resistance is 75Ω is shown Figure 7.5 and 7.6.

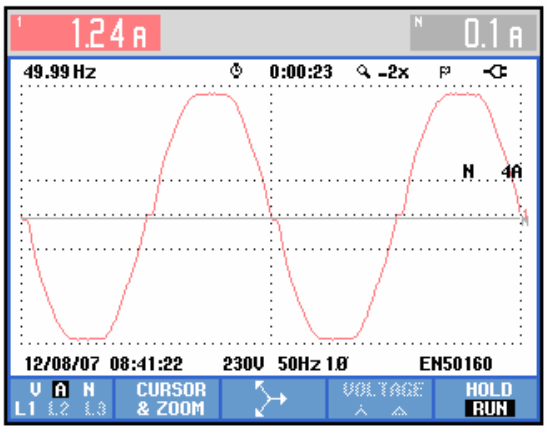


Figure 7.5: Current waveform of the load with the digital control when resistance is 75Ω

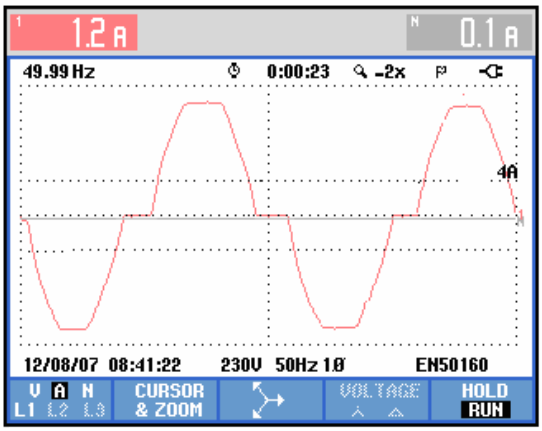


Figure 7.6: Current waveform of the load without the digital control when resistance is 75Ω.

The current waveform of the load when resistance is 200Ω is shown Figure 7.7 and 7.8.

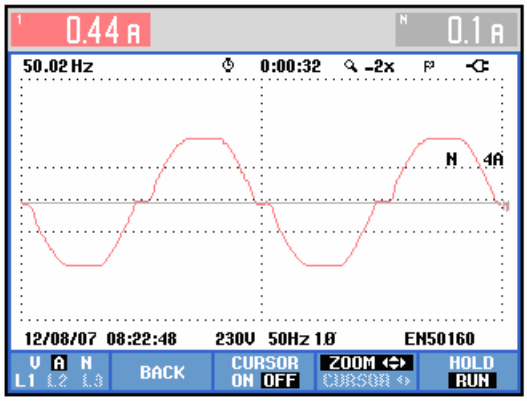


Figure 7.7: Current waveform of the load with the digital control when resistance is 200Ω

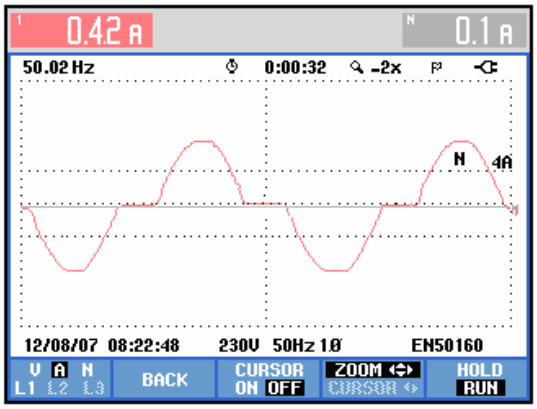


Figure 7.8: Current waveform of the load without the digital control when resistance is 200Ω

The current waveform of the load with the controller when resistance is 500Ω is shown Figure 7.9. It was unable to get this measurement of the load without controller because of some practical problems.

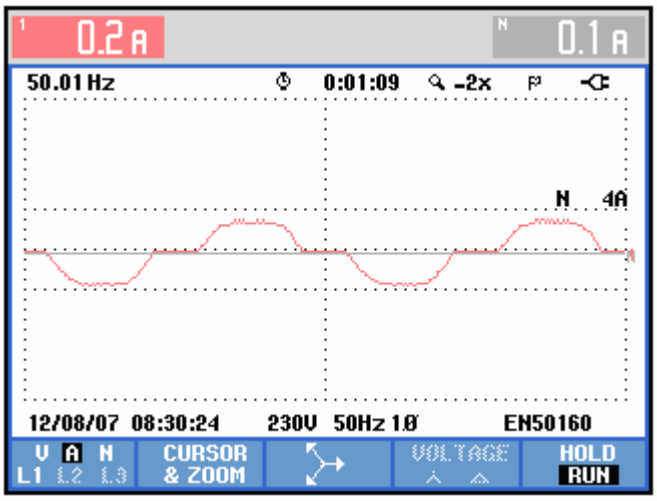


Figure 7.9: Current waveform of the load with the digital control when resistance is 500Ω

7.3 Fast Fourier transforms

Fast Fourier transform of the load current with the digital control is shown in Figure 7.10.

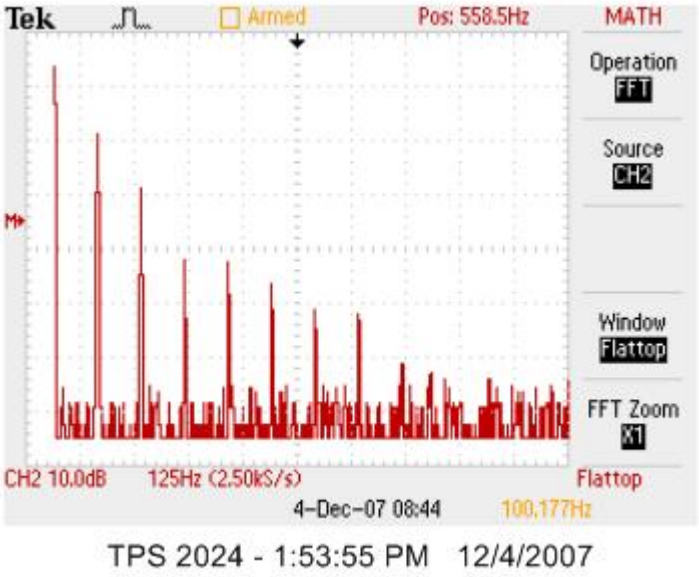


Figure 7.10:Fast Fourier transform of the load current with the digital control

Fast Fourier transform of the load current without the digital control is shown in Figure7.11.

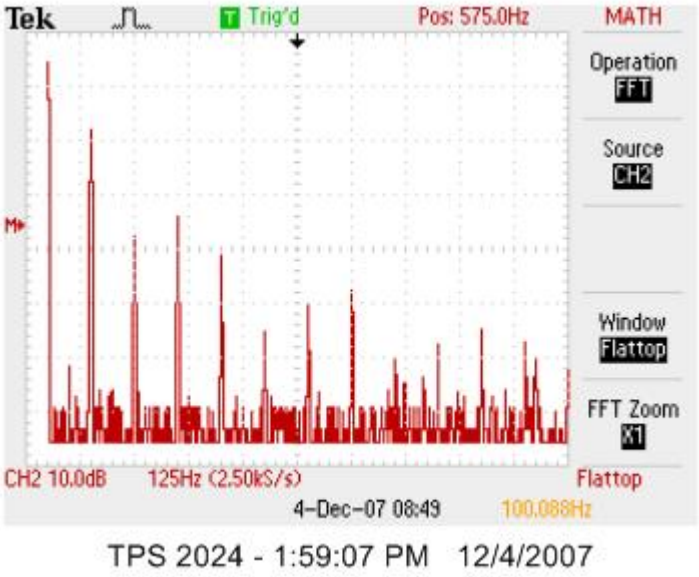


Figure 7.11:Fast Fourier transform of the load current without the digital control

7.4 Total Harmonic Distortions

7.4.1 THD of the load current with constant load voltage

Figure 7.12 and Figure 7.13 compares the THD of the current of the load with controller and without controller at 0.2A with constant voltage is 100V.

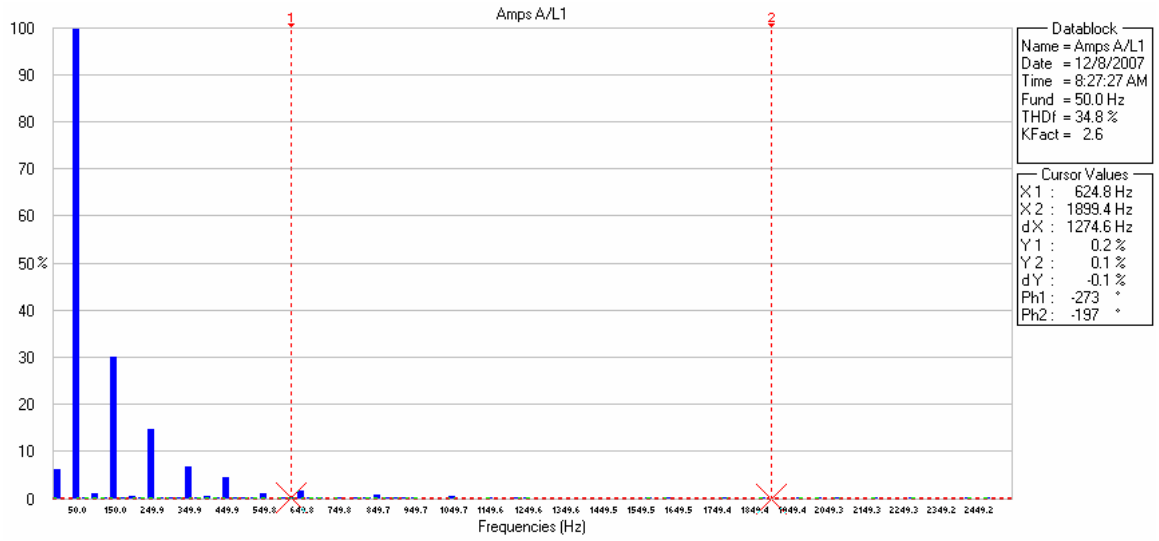


Figure 7.12. THD of the load current with controller at 0.2A

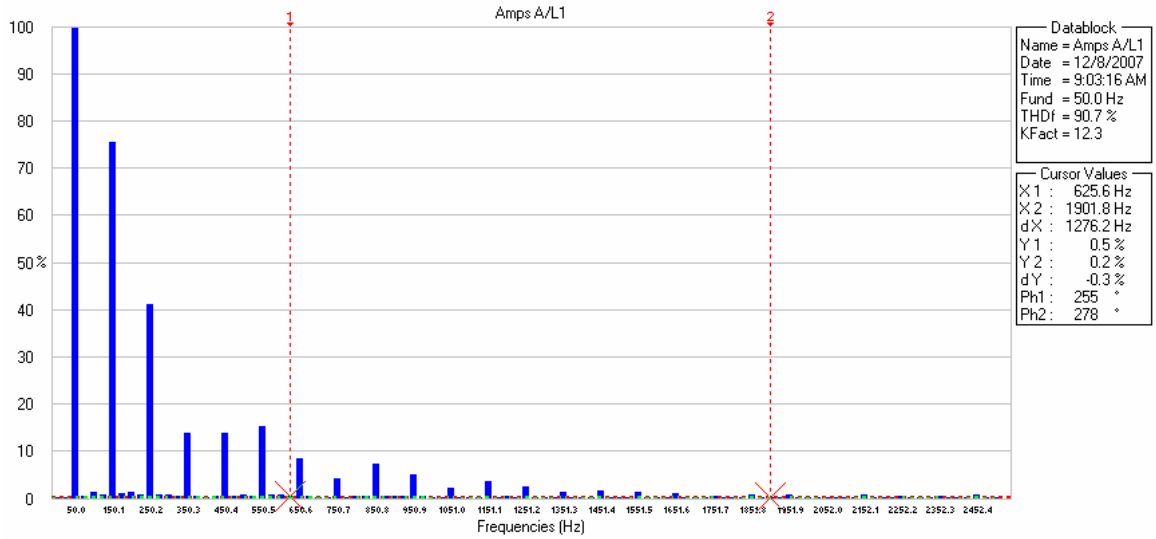


Figure 7.13. THD of the load current without controller at 0.2A

Figure 7.14 and Figure 7.15 compares the THD of the current of the load with controller and without controller at 1.3A with constant voltage is 100V.

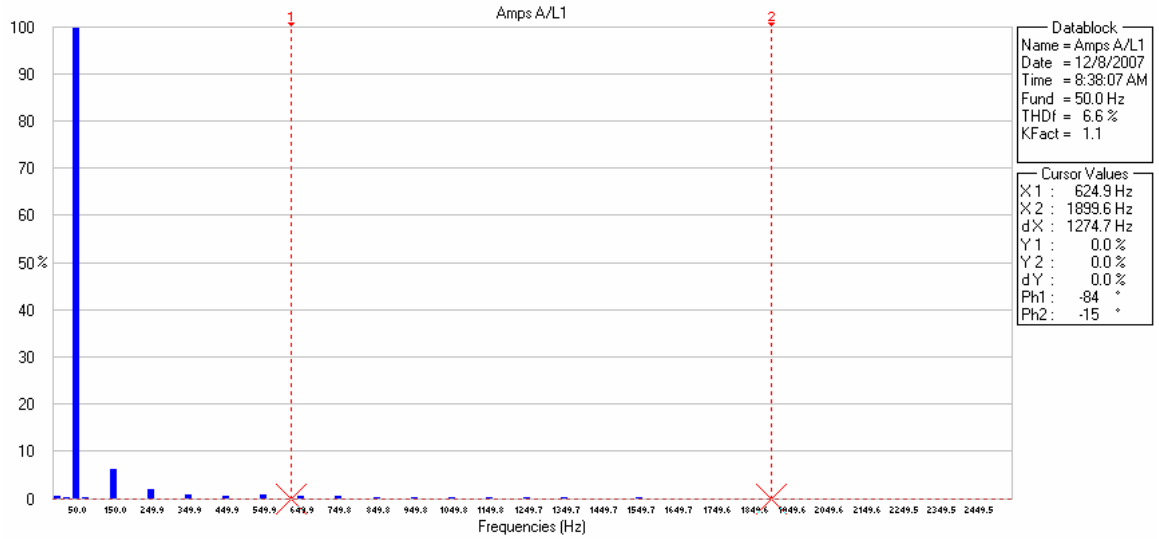


Figure 7.14. THD of the load current with controller at 1.3A

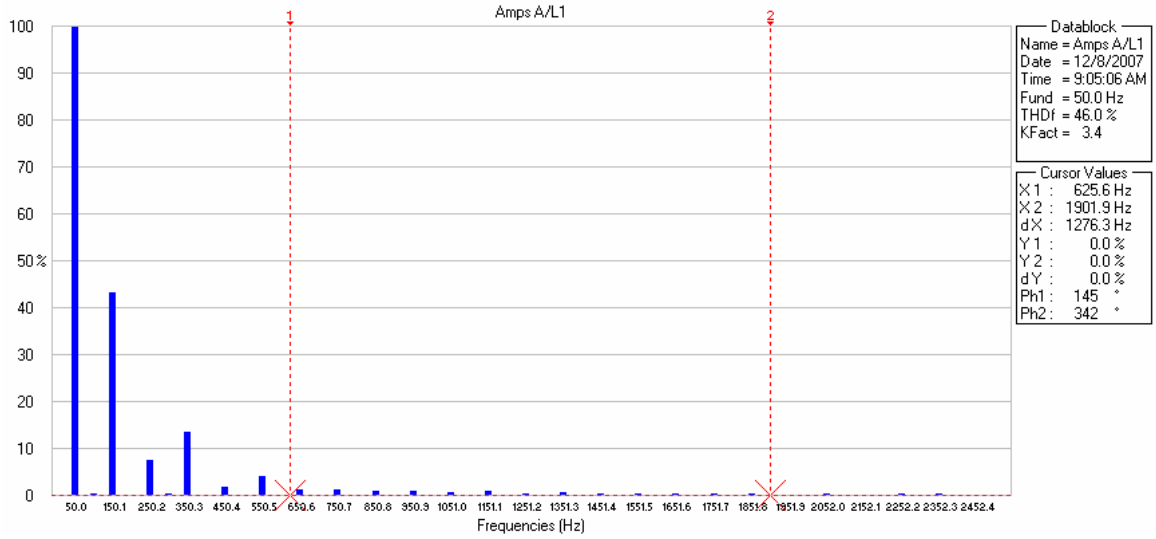


Figure 7.15. THD of the load current without controller at 1.3A

Figure 7.16 and Figure 7.17 compares the THD of the current of the load with controller and without controller at 1.5 A with constant voltage is 100V.

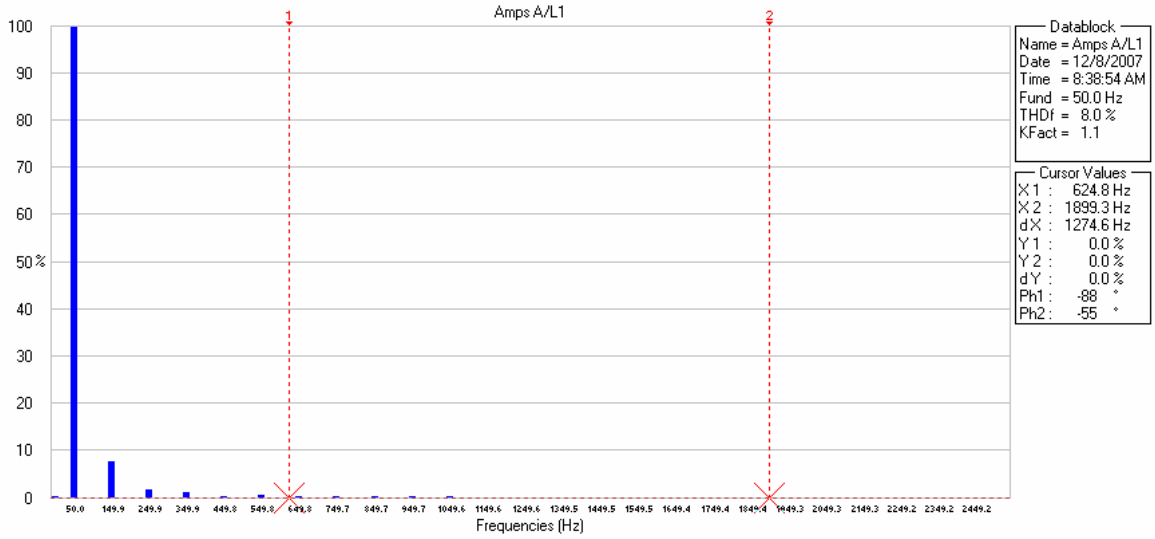


Figure 7.16. THD of the load current with controller at 1.5A

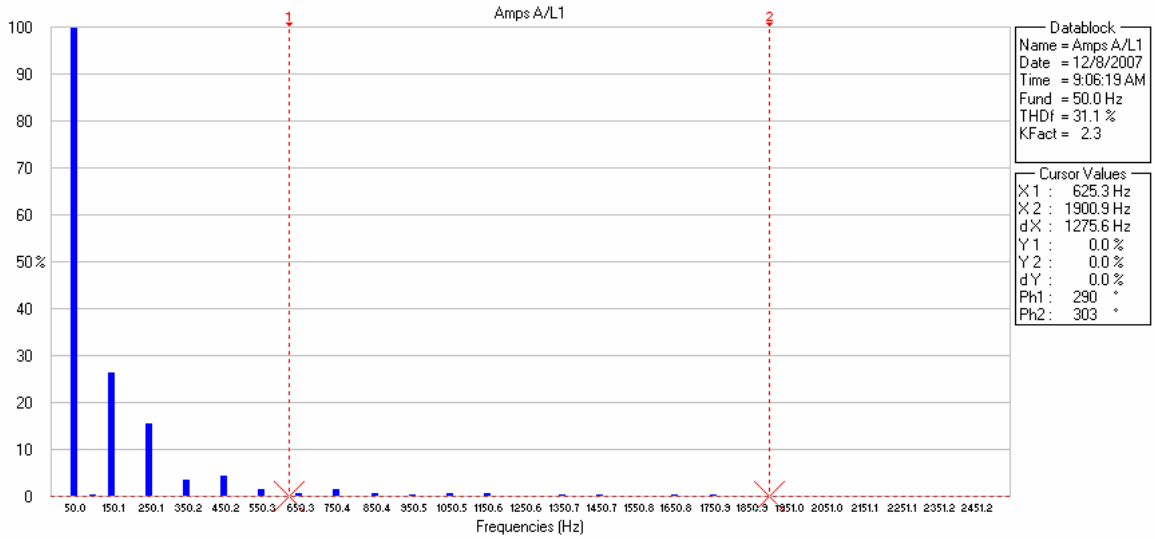


Figure 7.17. THD of the load current without controller at 1.5A

7.4.2 THD of the load voltage with constant load current

Figure 7.18 and Figure 7.19 compares the THD of the voltage of the load with controller and without controller at 50 V with constant current of 1A.

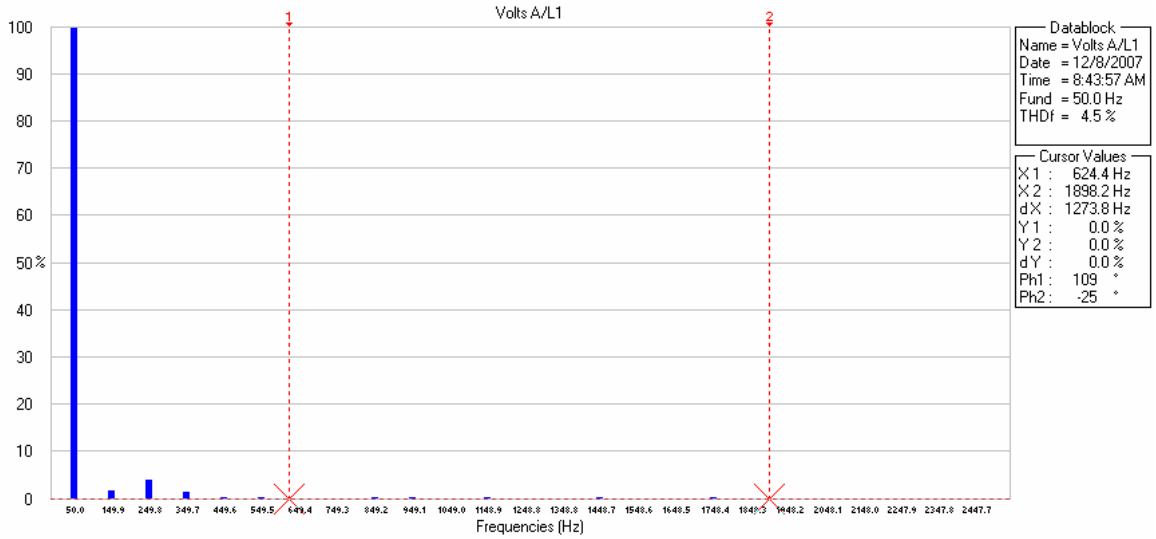


Figure 7.18. THD of the load voltage with controller at 50V.

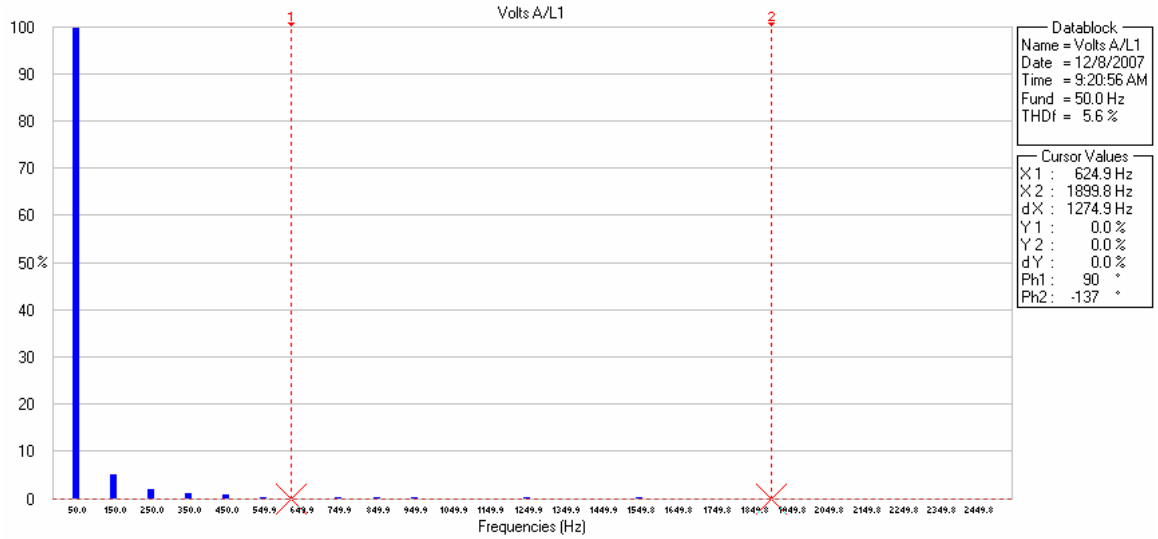


Figure 7.19. THD of the load voltage without controller at 50V.

Figure 7.20 and Figure 7.21 compares the THD of the voltage of the load with controller and without controller at 125 V with constant current of 1A.

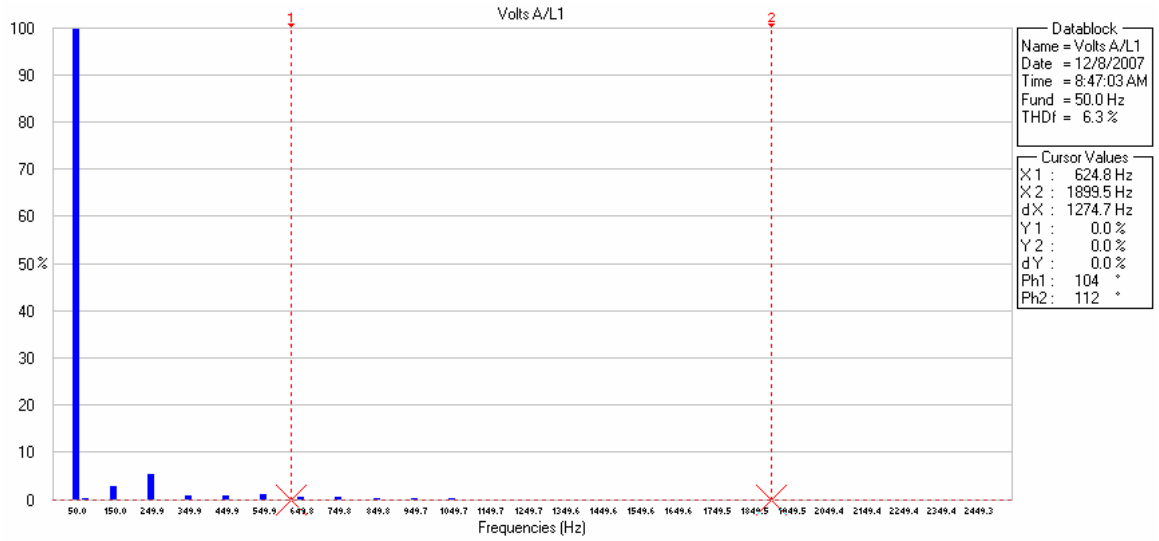


Figure 7.20. THD of the load voltage with controller at 125V.

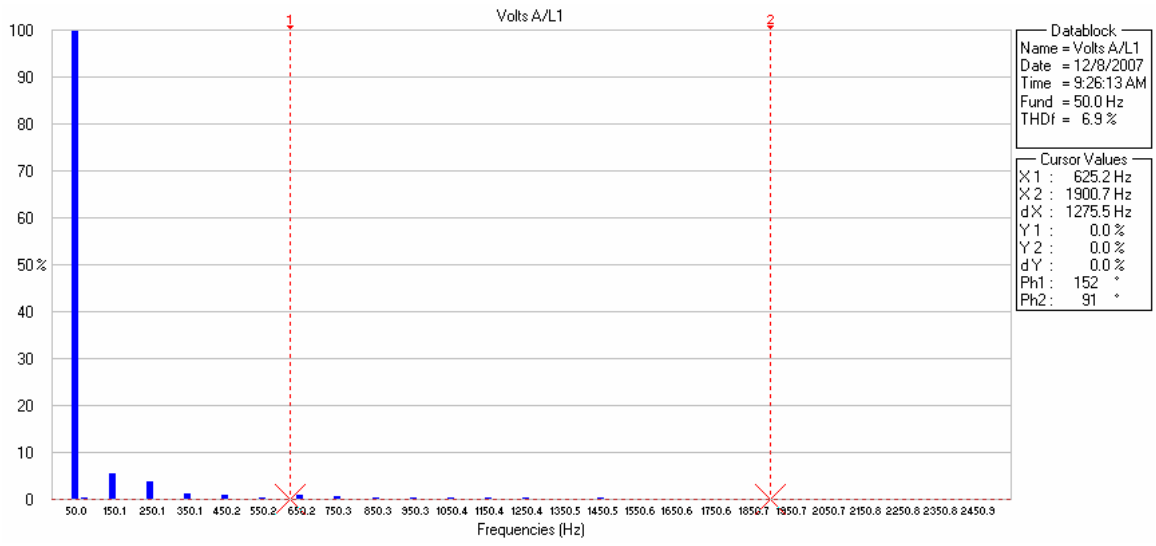


Figure 7.21. THD of the load voltage without controller at 125V.

7.5 Variation of THD with voltage and current

7.5.1 THD Vs Load current at different voltage levels

The variation of THD with current at two different constant voltages for the load with digital controller and without controller is shown in Figure 7.22. For the load with controller variation of THD is marked in pink and blue. For the load without controller variation of THD is marked in yellow and green.

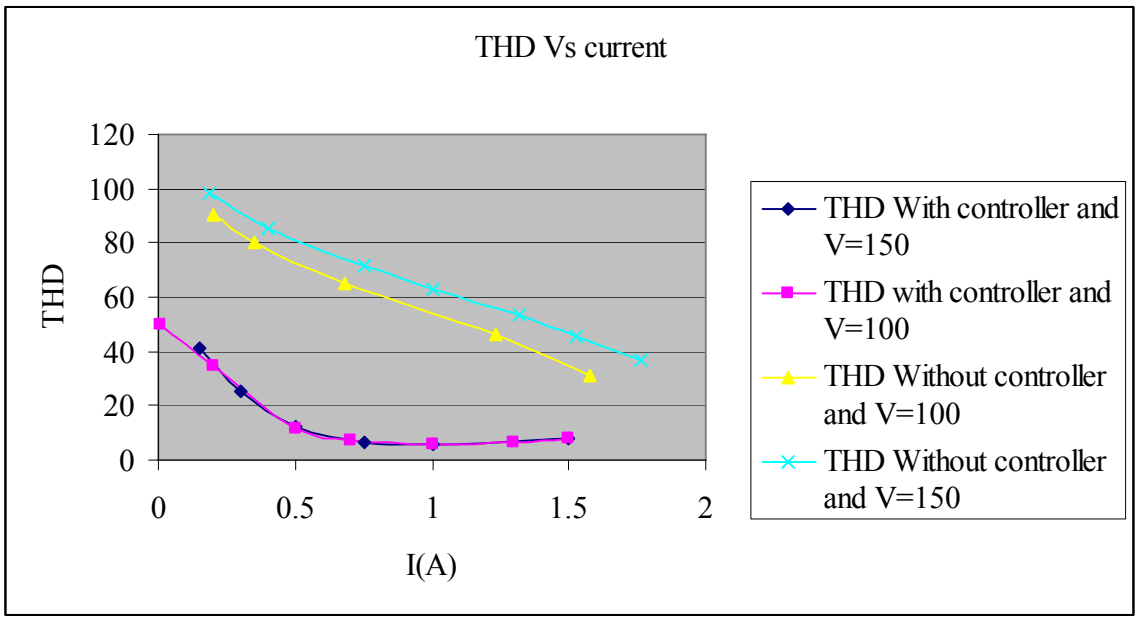


Figure 7.22: THD Vs Load current at constant voltages

7.5.2 THD Vs Load voltage at different voltage levels

The variation of THD with voltage at a constant current for the load with digital controller and without controller is shown in Figure 7.23. For the load with digital controller, variation of THD is marked in blue. For the load without controller variation of THD is marked in pink.

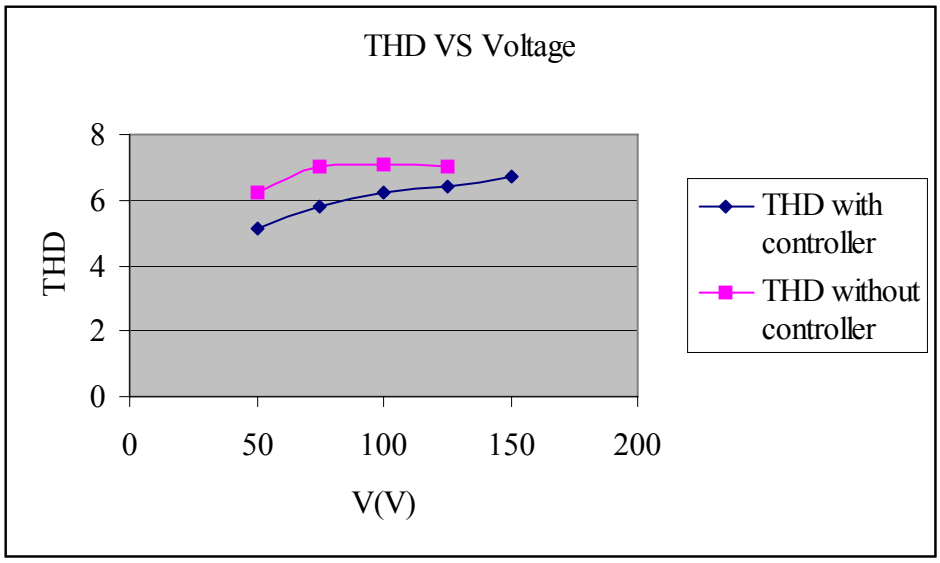


Figure 7.23: THD Vs Load voltage at constant current

Chapter 8

Conclusion and Future Developments

8.1 Summary of the Thesis

This thesis describes the approach to develop a digitally controllable AC electronic load based on power BJTs in a series connected array.

Approximate theoretical analysis followed by simulations and experimental results obtained indicate a reasonable digital approach using commercial optoisolators for electrical isolation.

Due to non-linear behaviour of optoisolator and the base emitter junctions of transistors digital controllability varies for different ranges of required array resistance values. The experimental results indicate the total harmonic distortions for different operational conditions of the array.

Due to time constraints a programming interface between the PC and the microprocessor was not developed and required programming parameters were directly fed to the micro-program.

8.2 Conclusion

The project indicated that digital control of a series BJT array could be used to arrive at an electronic AC load with reasonable linearity within a 50-cycle waveform. RMS value of the effective resistance of the array can be digitally corrected for reducing non-linearity. However the amount of digital correction possible, depend on the range of resistance required. Further research is recommended.

8.3 Future Developments

- Replace power transistor with higher capacity and
- Develop a PC based program to link an Excel program and the micro-controller algorithm to automatically adjust the resistance behaviour of the array.(This will lead to a time variable electronic AC load for AC-AC converter testing).
- Increasing the sampling time of the micro-controller sub-system for more accurate impedance control of the array.
- Modifications to the primary technique developed to accommodate MOSFETs or IGBTs for higher power and voltage capability.

Appendix A

Circuit diagrams

A.1 Circuit diagram of DAC circuit

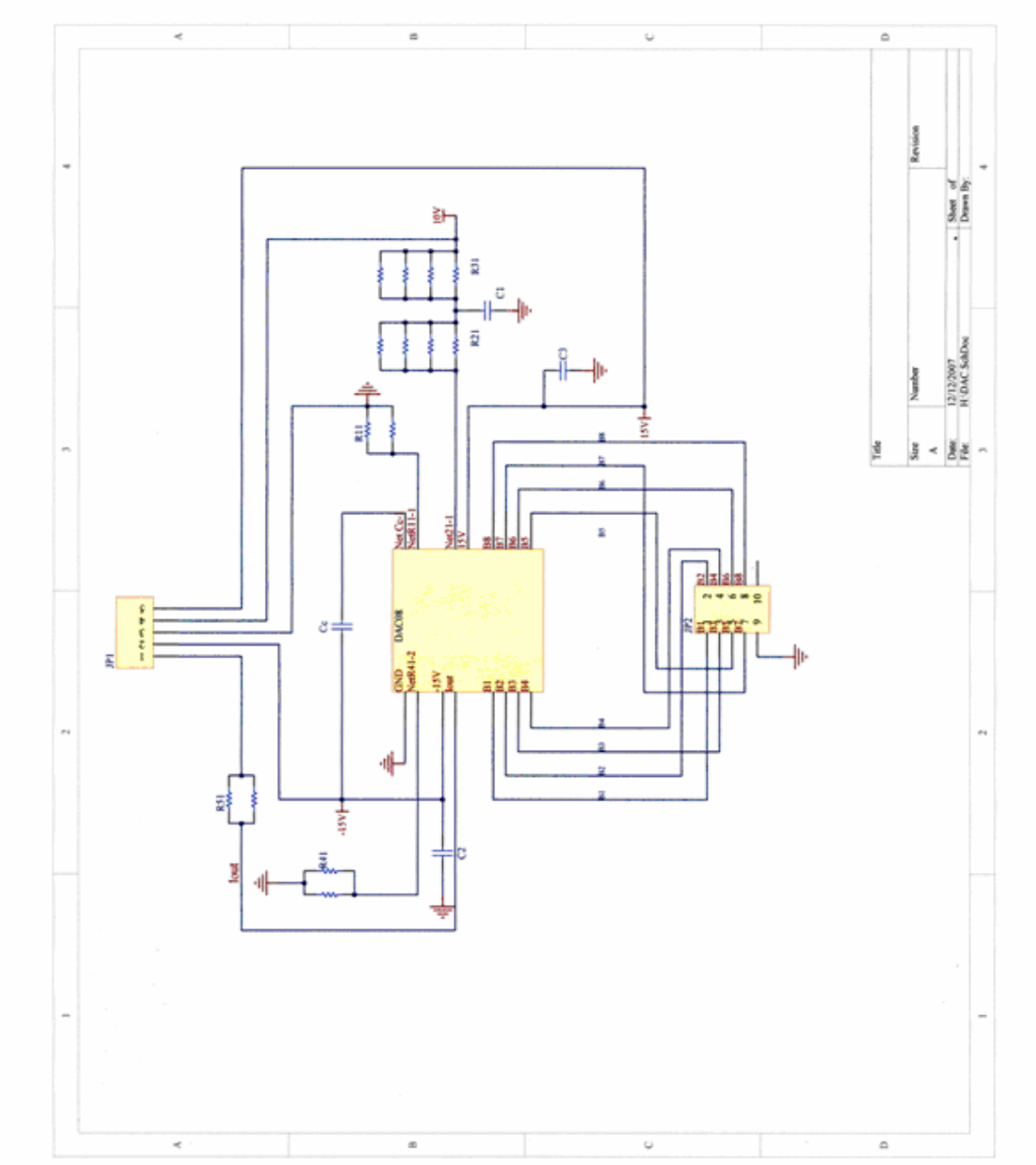


Figure A.1 DAC circuit

A.2 Circuit diagram of Voltage sampling circuit

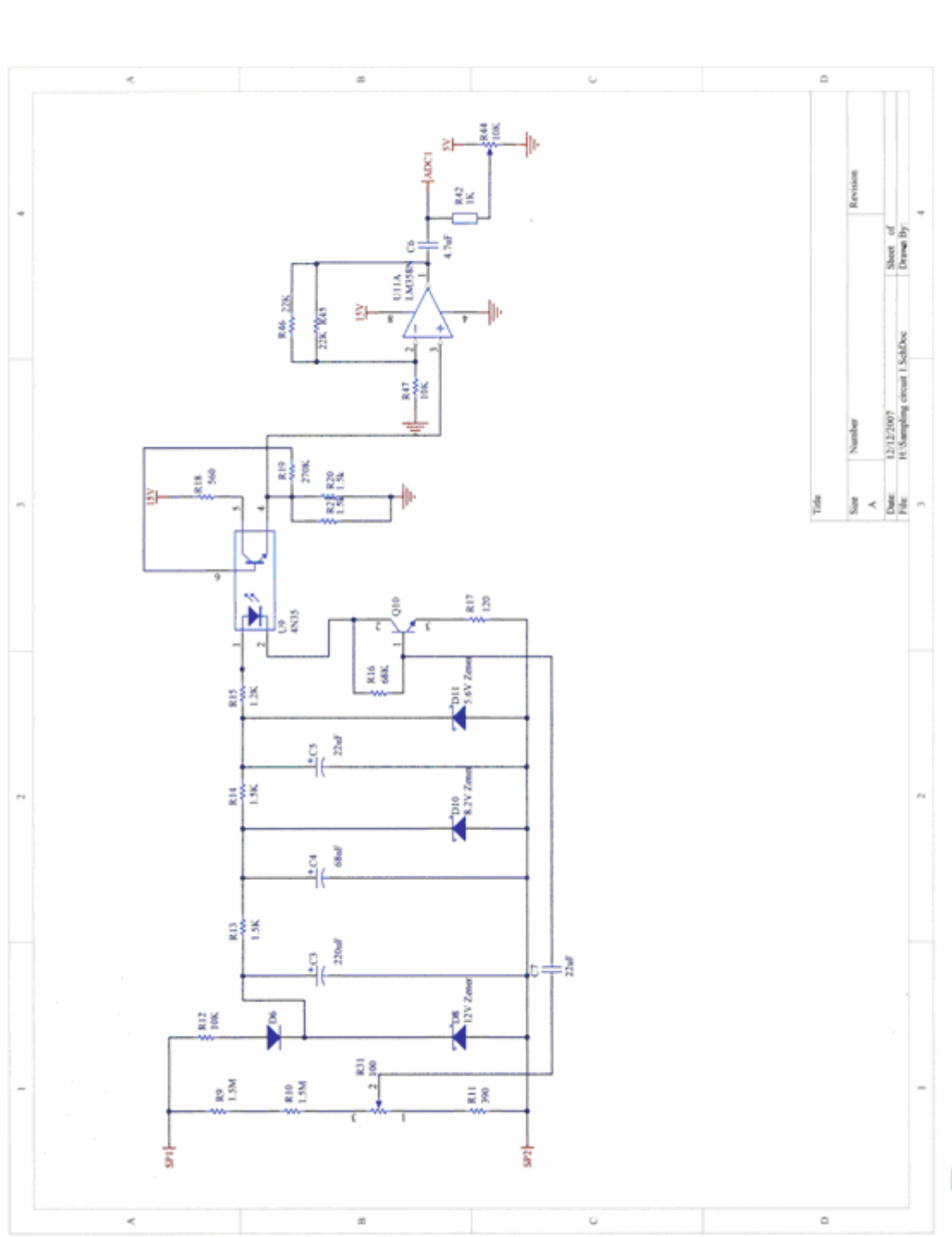


Figure A.2: Sampling Circuit

A.3 Circuit diagram of the power stage

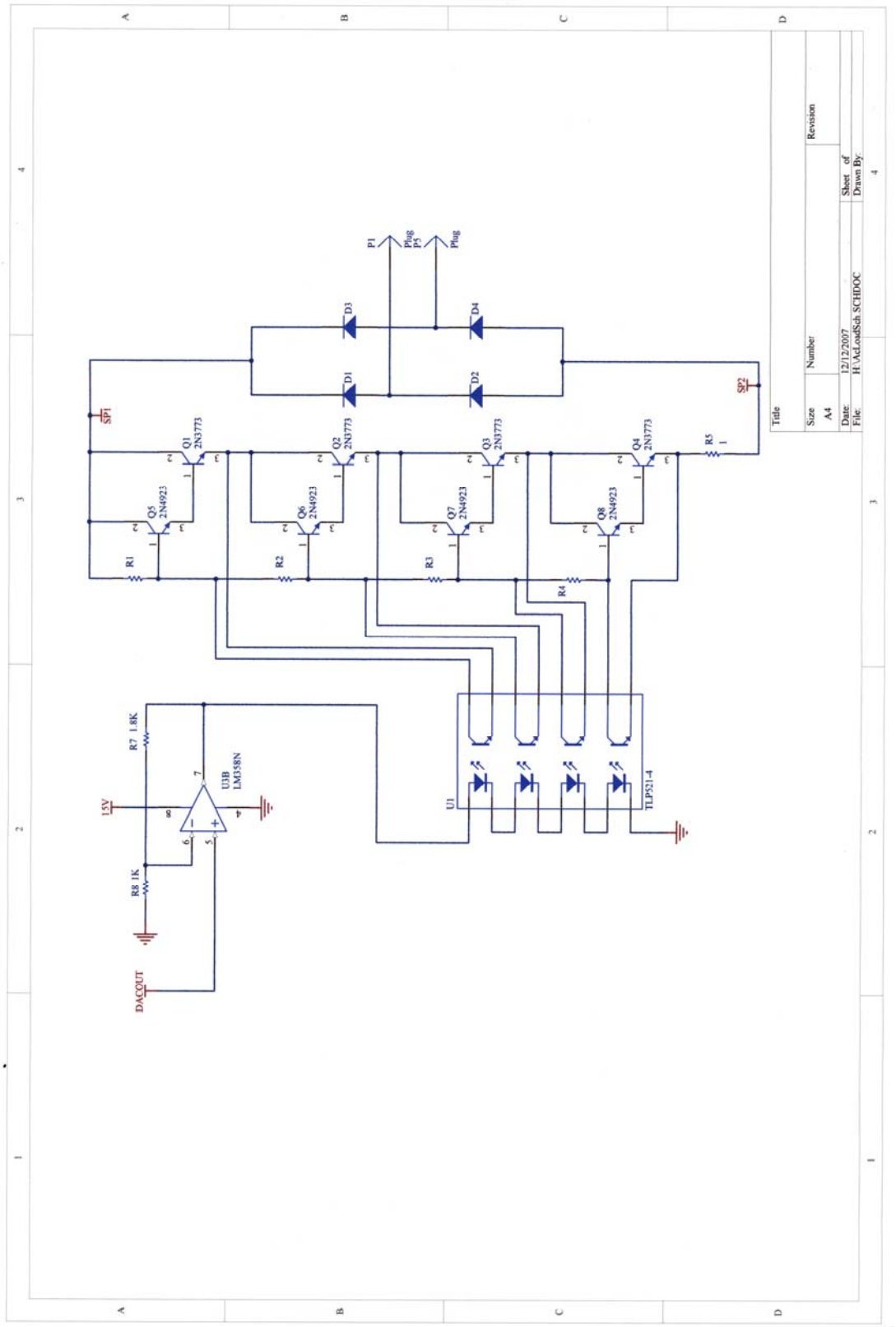


Figure A.3: AC Load circuit power stage

Appendix B

B Photograph of Circuits and test bench

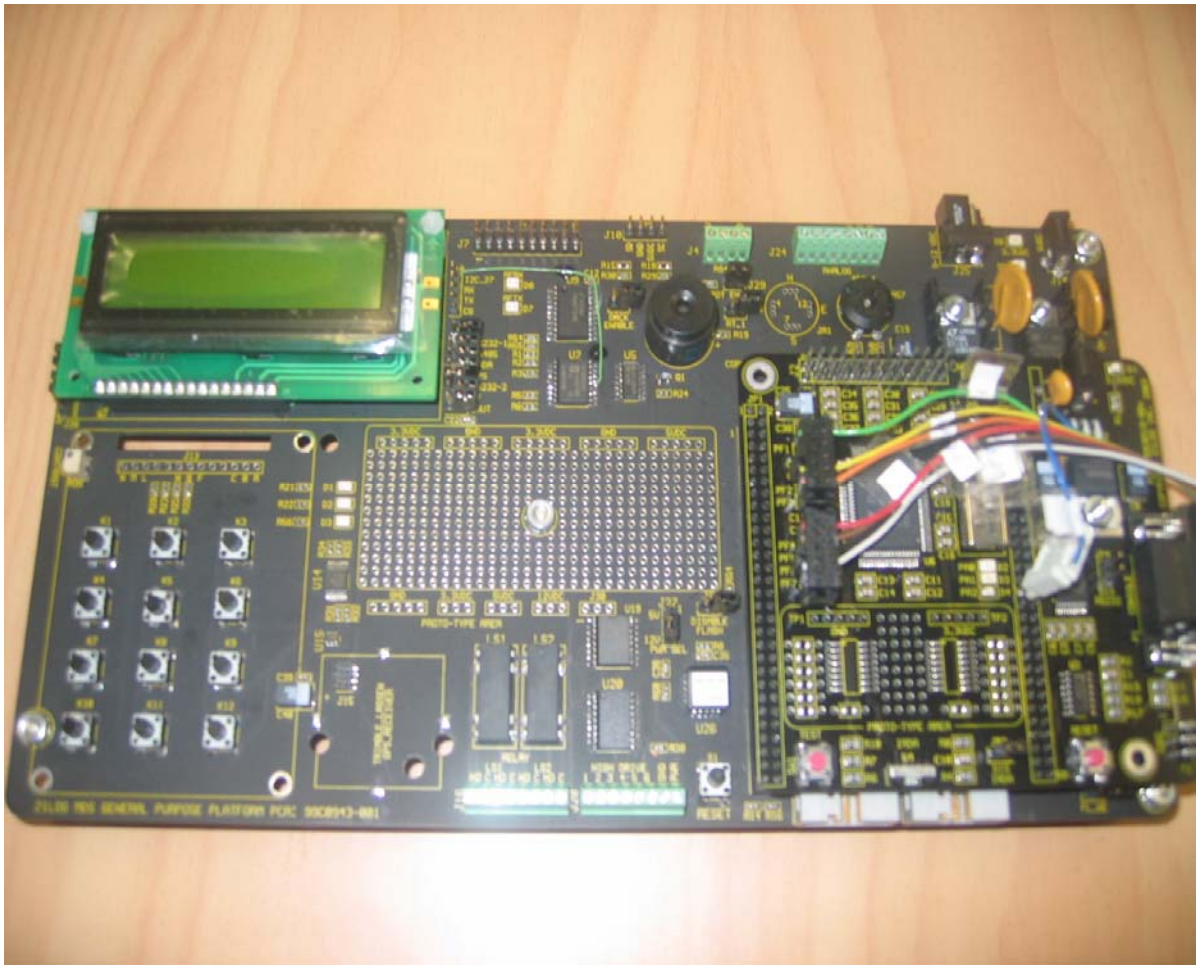


Figure B.1: Photograph of Zilog Z8Encore! Microprocessor development board

Figure B.2: Photograph of Transistor array

Figure B.3: Photograph of the test bench

Appendix C

C Simulation Circuit

The circuit model used in spice simulation carried out in Protel DXP software package is shown in the Figure C.1.

Spice models of components used for the simulation are included under this topic. Due to the unavailability of exact simulation models of transistors used in this research approximate models are used. Simulation model for optoisolator could not be found. Therefore spice model of current controlled current source was used.

C.1 Simulation Circuit

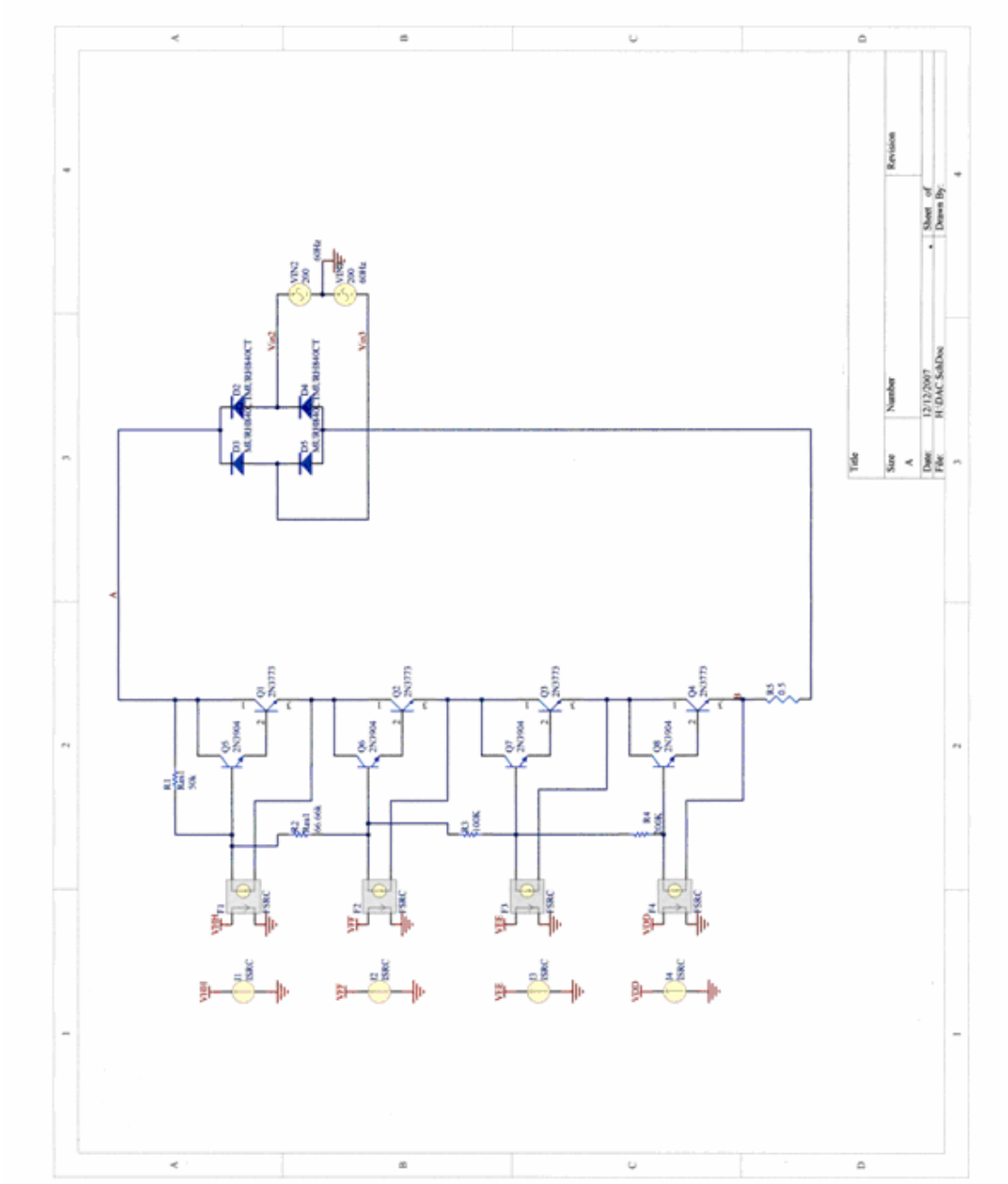


Figure C.1: Simulation circuit

C.2 Simulation Models of Components

C.2.1 Model of bipolar junction 2N3773 power transistor

* Model Format is SPICE3

+IS=1.67939e-15 BF=172.42 NF=0.85 VAF=13.8801
+IKF=1.96101 ISE=6.91738e-10 NE=4 BR=17.242
+NR=0.831086 VAR=95.687 IKR=7.57195 ISC=1.05925e-13
+NC=1 RB=0.597488 IRB=0.0999999 RBM=0.597488
+RE=0.0001 RC=0.0540301 XTB=0.1 XTI=4
+EG=1.206 CJE=1e-11 VJE=0.75 MJE=0.33
+TF=1e-09 XTF=1 VTF=10 ITF=0.01
+CJC=1e-11 VJC=0.75 MJC=0.33 XCJC=0.9
+FC=0.5 CJS=0 VJS=0.75 MJS=0.5
+TR=1e-07 PTF=0 KF=0 AF=1

C.2.2 Model of bipolar junction 2N3904 power transistor

* Model Format is SPICE3

+IS=4.17439e-12 BF=177 NF=1.01607 VAF=31.616
+IKF=0.224431 ISE=8.2776e-09 NE=2.54056 BR=12.0174
+NR=1.03892 VAR=40.2977 IKR=2.07162 ISC=1.45589e-12
+NC=1.04368 RB=57.3173 IRB=0.00111027 RBM=0.1
+RE=0.000101834 RC=0.233307 XTB=0.70994 XTI=3.76865
+EG=1.05 CJE=5.16878e-08 VJE=0.618039 MJE=0.425797
+TF=9.86989e-09 XTF=1.35723 VTF=0.995785 ITF=0.999971
+CJC=1.95067e-10 VJC=0.400281 MJC=0.417714 XCJC=0.803125
+FC=0.556633 CJS=0 VJS=0.75 MJS=0.5
+TR=1e-07 PTF=0 KF=0 AF=1

C.2.3 Model of Rectifier diode BYT08P

The spice model of BYT08P is unavailable and therefore model of mr754rld fast recovery rectifier diode was used.

* Model Format is SPICE3

+IS=5.86764e-08 RS=0.00170261 N=1.7374 EG=0.6
+XTI=0.5 BV=400 IBV=2.5e-05 CJO=1.33832e-09
+VJ=0.4 M=0.708966 FC=0.5 TT=5.45339e-06
+KF=0 AF=1

Appendix D

Sample Simulation data in Excel

s	RCE	s	Vce	s	Ic	a	b	c	d
0.009765	3.73E+03	0.009765	2.21E+01	0.009765	4.98E+00	27.03424	4.98E+00	7.668613	5.941483
9.96E-03	3.71E+03	9.96E-03	2.24E+01	9.96E-03	5.05E+00	27.46005	5.05E+00	7.847689	6.034431
1.02E-02	3.68E+03	1.02E-02	2.28E+01	1.02E-02	5.13E+00	27.88586	5.13E+00	8.026764	6.127379
1.04E-02	3.66E+03	1.04E-02	2.31E+01	1.04E-02	5.21E+00	28.31166	5.21E+00	8.205839	6.220327
1.06E-02	3.63E+03	1.06E-02	2.34E+01	1.06E-02	5.29E+00	28.73747	5.29E+00	8.384915	6.313275
1.07E-02	3.61E+03	1.07E-02	2.38E+01	1.07E-02	5.36E+00	29.16328	5.36E+00	8.56399	6.406223
1.09E-02	3.58E+03	1.09E-02	2.41E+01	1.09E-02	5.44E+00	29.58909	5.44E+00	8.743066	6.49917
1.11E-02	3.56E+03	1.11E-02	2.45E+01	1.11E-02	5.52E+00	30.0149	5.52E+00	8.922141	6.592118
1.13E-02	3.53E+03	1.13E-02	2.48E+01	1.13E-02	5.60E+00	30.4407	5.60E+00	9.101216	6.685066
0.014958	3.52E+00	0.014958	3.78E+01	0.014958	10.74973	48.54161	10.74973	12.32522	11.56859
0.015358	3.51E+00	0.015358	3.75E+01	0.015358	10.68358	48.23199	10.68358	12.25896	11.50233
0.015758	3.55E+00	0.015758	3.68E+01	0.015758	10.35236	47.15336	10.35236	11.92554	11.16979
0.016158	3.60E+00	0.016158	3.55E+01	0.016158	9.854211	45.31401	9.854211	11.4247	10.66995
0.016558	3.69E+00	0.016558	3.36E+01	0.016558	9.1161	42.75135	9.1161	10.68162	9.928877
0.016958	3.79E+00	0.016958	3.12E+01	0.016958	8.249228	39.49693	8.249228	9.809117	9.058617
0.017358	3.95E+00	0.017358	2.84E+01	0.017358	7.19101	35.61042	7.19101	8.742524	7.995574
0.017758	4.14E+00	0.017758	2.51E+01	0.017758	6.063468	31.14428	6.063468	7.605425	6.862597
0.018158	4.44E+00	0.018158	2.14E+01	0.018158	4.809346	26.17768	4.809346	6.337622	5.600839
0.018558	4.84E+00	0.018558	1.72E+01	0.018558	3.556195	20.7809	3.556195	5.067594	4.339074
0.018958	5.76E+00	0.018958	1.28E+01	0.018958	2.225646	15.05165	2.225646	3.709282	2.994835
0.019358	8.68E+00	0.019358	8.14E+00	0.019358	0.938534	9.083289	0.938534	2.373309	1.68464
0.019758	7.42E+02	0.019758	3.06E+00	0.019758	0.004124	3.063938	0.004124	-0.66145	0.627755
0.020042	2.12E+02	0.020042	4.90E+00	0.020042	0.023055	4.919315	0.023055	1.274413	0.683036
0.020178	5.29E+02	0.020178	2.05E+00	0.020178	0.003879	2.057352	0.003879	-1.64576	0.627726
0.020262	2.79E+02	0.020262	4.90E+00	0.020262	0.017564	4.919053	0.017564	1.257022	0.671388
0.020344	1.02E+03	0.020344	4.66E+00	0.020344	0.004577	4.666362	0.004577	0.992563	0.628965
0.020453	2.11E+01	0.020453	5.97E+00	0.020453	0.282824	6.255922	0.282824	1.652966	0.998974
0.020576	1.09E+01	0.020576	7.41E+00	0.020576	0.677736	8.082943	0.677736	2.093467	1.415166
0.020768	7.15E+00	0.020768	9.63E+00	0.020768	1.347623	10.97771	1.347623	2.802849	2.103222
0.020958	6.05E+00	0.020958	1.19E+01	0.020958	1.959475	13.8113	1.959475	3.435889	2.725194
0.021339	5.01E+00	0.021339	1.61E+01	0.021339	3.214367	19.33194	3.214367	4.719772	3.994214
0.021739	4.53E+00	0.021739	2.03E+01	0.021739	4.487078	24.8194	4.487078	6.011351	5.276684
0.022139	4.20E+00	0.022139	2.42E+01	0.022139	5.749285	29.90843	5.749285	7.288222	6.54674