Supercapacitor-assisted Arc Management (SCA^{2}M) Technique for DC Circuit Breakers in Low-voltage Applications

A thesis

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by

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Abstract

Direct Current (DC) circuits are gaining popularity due to their compatibility with renewable energy. However, their development is hindered by the lack of mature DC protection, such as circuit breakers. Unlike alternating current (AC), DC lacks natural zero-crossing points, making arc extinction harder and causing severe contact degradation. Additionally, DC fault currents rise faster than AC, emphasising the need for effective arc extinguishing in DC circuit breaking.

Three types of DC circuit breakers (DCCB) exist: mechanical, solid-state, and hybrid. Mechanical DCCBs use mechanical switches, solid-state DCCBs rely on semiconductor switches, and hybrid DCCBs combine both. Despite extensive research, no technologies have achieved viable commercial-scale production due to high costs and technological immaturity. As a cost-effective alternative, manufacturers modify mechanical AC circuit breakers for DC applications by connecting multiple poles in series. However, this approach increases power loss, contact resistance, and overall switch size. For small-scale DCCBs, permanent neodymium magnets are incorporated within the circuit breaker to aid in arc extinguishment as a simple supplementary technique.

This research is the initial step taken by the Waikato Power Electronics Research Group (WaiPER) in New Zealand to address the DCCB arcing issue, with promising experience gathered from two decades of past work based on non-traditional supercapacitor applications known as supercapacitor-assisted (SCA) techniques, achieving multiple patents and industry products.

This thesis aims to develop an electric arc-management technique for mechanical contact-pair based DCCBs using the rapid discharge capability of commercial supercapacitors (SC). A transformer-based circuit reduces the DC loop current during circuit breaker opening, thereby decreasing arcing time, arc energy and contact degradation while extending breaker lifespan. A 2-kW, 80-A prototype demonstrates the concept for approximately 50% arcing time reduction with 55% arc energy reduction, with visual and analytical comparisons of arcing with and without the SC-based technique. The technique is further developed for better performance, achieving 64% reduction in arcing time and 67% reduction in arc energy using a two-transformer-based implementation. Tests were further conducted for multiple circuit breakers of the same rating for different voltage and current values. Successful current reduction in the DC loop is based on a low-voltage

SC–MOSFET combination which eliminates the need for high-voltage auxiliary circuits and forced cooling, thus keeping costs low. Also, since the SC-MOSFET loop is galvanically isolated from the main DC loop, the prototype is intrinsically protected from natural events such as lightning overvoltage and current surges.

Preface

This thesis is submitted in partial fulfilment of the requirements for the PhD degree at the University of Waikato, New Zealand, within the Power Electronics Group. The work was carried out from April 2022 to October 2025 and was supervised by Prof Nihal Kularatna, A/Prof Alistair Steyn-Ross, and Dr Nicoloy Gurusinghe. This work was supported by the Ministry of Business, Innovation and Employment, New Zealand under the Strategic Science Investment Fund - Advanced Energy Technology Platform programme "Architecture of the Future Low Carbon, Resilient, Electrical Power System" contract number UOCX2007. Listed below are the publications produced as part of this project.

Journal Article

(1) C. Dassanayake et al., "Supercapacitor-based Pulse Energy Pumping Approach for Arc Extinguishing in Mechanical DC Circuit Breakers," in *IEEE Transactions on Industry Applications*, vol. 62, no. 2, pp. 2438-2449, March-April 2026, doi: 10.1109/TIA.2025.3603759.

Peer Reviewed Conference Papers

(1) C. Thilanka Dassanayake, R. Sri Gunathilaka, N. Gurusinghe and N. Kularatna, "Supercapacitor based approaches for arc energy absorption in direct current circuit breakers," *IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society*, Brussels, Belgium, 2022, pp. 1-6, doi: 10.1109/IECON49645.2022.9968979.

(2) C. Dassanayake, N. Kularatna, A. Steyn-Ross, K. Gunawardane and N. Gurusinghe, "Plasma Absorption Techniques in Direct Current Circuit Breakers," *2023 IEEE 3rd International Conference on Industrial Electronics for Sustainable Energy Systems (IESES)*, Shanghai, China, 2023, pp. 1-6, doi: 10.1109/IESES53571.2023.10253737. **(Conference best paper award!)**

(3) C. Dassanayake, N. Kularatna, A. Steyn-Ross, K. Gunawardane and N. Gurusinghe, "Arc Absorption Options Based on Passive Components in DC Circuit Breakers," *IECON 2023- 49th Annual Conference of the IEEE Industrial Electronics Society*, Singapore, 2023, pp. 1-6, doi: 10.1109/IECON51785.2023.10312678.

(4) C. Dassanayake, N. Kularatna, A. Steyn-Ross, N. Gurusinghe and K. Gunawardane, “Arc Characteristics in Multiple Pole DC Circuit Breakers,” *2023 IEEE Fifth International Conference on DC Microgrids (ICDCM)*, Auckland, New Zealand, 2023, pp. 1-6, doi: 10.1109/ICDCM54452.2023.10433616. **(Best student paper award!)**

(5) C. Dassanayake, N. Kularatna, A. Steyn-Ross, N. Gurusinghe and K. Gunawardane, “Preliminary experiments quantifying the arcing process in a DC circuit breaker development project,” *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA, 2024, pp. 2986-2993, doi: 10.1109/APEC48139.2024.10509082.

(6) C. Dassanayake, N. Kularatna, A. Steyn-Ross and N. Gurusinghe, “Self-Powered and Self-Controlled Hybrid DC Circuit Breaker for Low Voltage Applications,” *2024 IEEE Sixth International Conference on DC Microgrids (ICDCM)*, Columbia, SC, USA, 2024, pp. 1-4, doi: 10.1109/ICDCM60322.2024.10665083.

(7) C. Dassanayake, N. Kularatna, A. Steyn-Ross and N. Gurusinghe, “Supercapacitor Assisted Arc Management Approaches for Direct Current Circuit Breakers-A Comparison with State of the Art and Potential New Directions,” *IECON 2024 - 50th Annual Conference of the IEEE Industrial Electronics Society*, Chicago, IL, USA, 2024, pp. 1-6, doi: 10.1109/IECON55916.2024.10905355.

(8) C. Dassanayake, N. Kularatna, A. Steyn-Ross and N. Gurusinghe, “Galvanic Isolation Switch Activation Mechanism for Hybrid DC Circuit Breakers Using Very High Current Capability of Supercapacitors,” *2024 13th International Conference on Renewable Energy Research and Applications (ICRERA)*, Nagasaki, Japan, 2024, pp. 1796-1799, doi: 10.1109/ICRERA62673.2024.10815517.

(9) C. Dassanayake, N. Kularatna, A. Steyn-Ross, N. Gurusinghe, T. Lamara and C. Tricarico, “Supercapacitor-Based Arc Reduction Technique for DC Circuit Breakers,” *2025 IEEE Seventh International Conference on DC Microgrids (ICDCM)*, Tallinn, Estonia, 2025, pp. 1-5, doi: 10.1109/ICDCM63994.2025.11144655.

Dedication

To my loving Parents!
To my loving Wife!
To my loving Sister and Brother!

Acknowledgements

I am grateful to many individuals and institutions for their support in making my PhD journey a success.

First and foremost, I express my sincere gratitude to my chief supervisor, Professor Nihal Kularatna. He mentors PhD students in a distinctive manner, emphasising hands-on experience in electronics. He advocates practical learning through the motto, “burning is learning”, granting us the opportunity to work with laboratory equipment and components as an engaging and instructive experience. He consistently encouraged us to understand why components fail and to avoid repeating the same mistake by burning the second component with the same fault. By the end of my PhD, I had collected many burnt transistors and other electronic components—a tangible record of my learning journey. Working under his supervision has been not only a privilege but also a deeply rewarding experience.

I am equally indebted to my second supervisor, Associate Professor Alistair Steyn-Ross, an exceptional physicist who refined the analytical rigour of this research and guided me towards excellence in academic writing throughout my PhD. His kind support and invaluable guidance empowered me to confront challenges and recognise my own strengths.

My third supervisor, Dr Nicoloy Gurusinghe, recommended me to his PhD supervisor, Professor Nihal Kularatna, while I was conducting research with him at the Sri Lanka Technological Campus. Without his introduction, I would not have secured such an outstanding chief supervisor for my research career. I worked with Dr Gurusinghe for nearly one and a half years before my PhD; he was my first supervisor—the one who directed my attention toward genuine research—and he continuously supported my work through advice and manuscript proofreading.

I also extend my gratitude to Associate Professor Kosala Gunawardane, who served as my fourth supervisor during the earlier-stage of my research.

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I gratefully acknowledge several industrial experts who contributed to my work. Dr John J. Shea (Schneider Electric, USA) provided me with the excellent reference book *Electrical Contacts* by P. G. Slade, which enabled me to explore the fundamentals of plasma phenomena in DC circuit interruption. I am also thankful to Dr Markus Abplanalp (Senior Principal Scientist at ABB) and Professor John Shen (Simon Fraser University, Canada) for their assistance in addressing key technical questions.

During the final year of my PhD, I benefited greatly from extensive discussions with two industrial experts: Dr Tarek Lamara, Head of the Research and Development team at Sécheron Hasler in Geneva, Switzerland—a pioneer in DC circuit breakers for railway systems—and Mr Claudio Tricarico, a senior research engineer at Sécheron. Dr Lamara facilitated a five-week industrial visit to Sécheron, which stands as one of the most significant milestones of my research journey.

I am also thankful to Professor Michael Cree for providing his high-speed camera to capture images of the electric arc.

I gratefully acknowledge the Future Architecture of the Network (FAN) project of the Advanced Energy Technology Program (AETP), funded by the Ministry of Business, Innovation and Employment, New Zealand, for providing three years of financial support, a publication scholarship, and travel grants for conferences and industrial visits.

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Finally, I extend my wholehearted gratitude to my loving parents, wife, sister, and brother for their unwavering support in every imaginable way, enabling me to achieve my dreams.

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Acronyms and Abbreviations

AC	alternating current
ACCB	alternating current circuit breaker
AETP	advanced energy technology program
CB	circuit breaker
DC	direct current
DCCB	direct current circuit breaker
ESR	equivalent series resistance
FAN	future architecture of the network
HV	high voltage
IGBT	insulated gate bipolar transistor
LV	low voltage
MCB	miniature circuit breaker
MOSFET	metal-oxide-semiconductor field-effect transistor
MOV	metal oxide varistor
MV	medium voltage
SC	supercapacitor
SCA^{2}M	supercapacitor-assisted arc management
SCALDO	supercapacitor-assisted low-dropout regulator
SCALED	supercapacitor-assisted light emitting diode
SCASA	supercapacitor-assisted surge absorber
SCATEP	supercapacitor-assisted transient energy pump
SCATMA	supercapacitor-assisted temperature modification apparatus
TVS	transient voltage suppression

Chapter 1

Introduction to Electrical Circuit Protection and Circuit Breaker Research

1.1 Electrical Circuit Protection

In an electrical circuit, two key elements are voltage and current, which interact with the three fundamental passive components: resistors, capacitors, and inductors. When voltage or current exceeds its applicable limits, it results in an overvoltage or overcurrent scenario, requiring appropriate protection such as interrupting and isolating a fault quickly using circuit breakers (CB) and other protective devices. Additionally, secondary protections such as transient-voltage surge protection, over/under-voltage protection, harmonic filtering, and uninterruptible power supplies may also be necessary.

1.2 AC vs DC Circuit Breaking

Today, there is a global movement away from environmentally harmful non-renewable energy sources toward renewable alternatives, driven by the need to address global warming caused by emissions from fossil fuel combustion. Consumer demand and government regulations are driving the global adoption of more efficient renewable energy technologies [1]. As renewable energy sources become more widespread, DC microgrids and DC loads are gaining popularity globally because they eliminate the losses associated with DC-to-AC power conversions required to interface with an AC grid, resulting in fewer conversion steps and increased efficiency [2]. Additionally, DC systems offer several advantages, including ease of integration with renewable energy sources such as solar PV and wind power, no reactive power losses, higher transmission efficiency due to the absence of reactive power, skin effect, and simpler conductor design, improved controllability, and reduced electromagnetic interference [3]. However, because DC systems are purely resistive without any reactance component, fault currents rise more rapidly in DC circuits [4].

With the growing adoption of DC renewable energy sources and DC loads, the need for effective DC circuit protection methods, including direct-current circuit breakers (DCCB), is becoming increasingly critical. DCCBs are essential for ensuring safety in both industrial and residential electrical systems. Table 1.1 lists common DCCB applications together with their corresponding electrical ratings.

Table 1.1: Electrical ratings for various DCCB applications [5]

Category	**Voltage rating**	**Current rating**	**Response time**
Electrical power distribution networks	5 kV	1 kA	2 ms
DC microgrids	48 V	-	4 ms
Electric transportation	1.5 kV	4 kA	<6 ms
High-voltage DC (HVDC) transmission	200 kV	2 kA	3 ms
Marine sector	1.5 kV	4 kA	5 ms
Aviation sector	500 V	10 kA	-

A significant obstacle to the expansion of DC networks is the immaturity of the present DCCB technology. Protecting DC networks is complex and costly because, unlike AC electricity, DC lacks zero crossings that naturally extinguish arc formation as illustrated in Fig. 1.1. For a 50-Hz AC waveform, a zero crossing occurs every 10 ms. Thus, DC arcs are more intense and harder to extinguish compared to AC arcs.

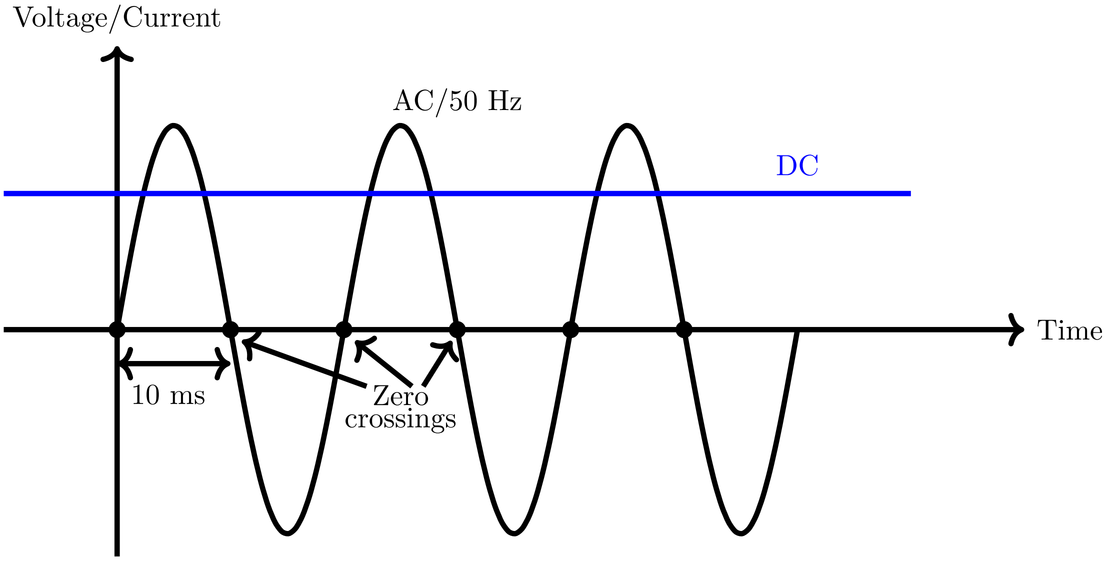


Figure 1.1: Zero crossings are naturally available in alternating current, however not in direct current waveforms.

ACCBs represent a well-established technology, utilising an arc chamber paired with arc absorption circuitry made from commercially available components. AC breakers take advantage of two zero-crossings per AC cycle to extinguish the electric arc generated by inductive energy within the AC circuit loop. Commercial DC breakers are essentially modified versions of AC breakers in which the contacts of three-phase generic ACCB poles are connected in series to increase DC switching capacity [6, 7]. In some cases, permanent magnets are incorporated into the CB to enhance its breaking capacity. Typically, a small neodymium magnet, or a pair of magnets, is placed inside the device. These magnets are positioned at a ninety-degree angle to the direction of the electric arc, allowing the magnetic field to influence the arc trajectory, drawing it toward the arc chamber and facilitating rapid arc extinction [8–10].

1.3 Research Goal

The research aims to introduce a novel supercapacitor-assisted arc management technique for DCCBs to enhance cycle life by reducing electrical arcing during contact separation. To achieve this goal, the very high-current pumping capability of supercapacitors (SC) is utilised, with a simple transformer technique used to transfer the SC's energy from the SC loop to the DC circuit loop containing the mechanical CB, thereby suppressing arcing.

1.4 Background and Motivation

The presented research is fully funded by New Zealand MBIE Future Architecture of the Network (FAN) project. The proof-of-concept prototype of the supercapacitor-assisted arc management (SCA^{2}M) technique for CBs for the FAN project in New Zealand is documented in this thesis. The FAN project was initiated to explore new pathways for developing an infrastructure model that integrates more DC into the existing AC network, with a focus on renewable energy to help reducing the global warming. The concept of the FAN project is depicted in Fig. 1.2. High-voltage (HV), medium-voltage (MV), and low-voltage (LV) DCCBs play a vital role in network protection within this project. HVDC transmission systems, MVDC industrial zones, and LVDC distribution networks and loads each require appropriately rated CBs. Investigating novel technologies to realise reliable and cost effective DCCBs is a significant component of the FAN project. Presented work is focused on developing a cost effective and reliable low-voltage DCCB suitable for LV applications.

The Power Electronic Research Group at the University of Waikato, New Zealand, is interested in non-traditional applications of SCs. The inventions developed by the group, under the supervision of Prof Nihal Kularatna, include:

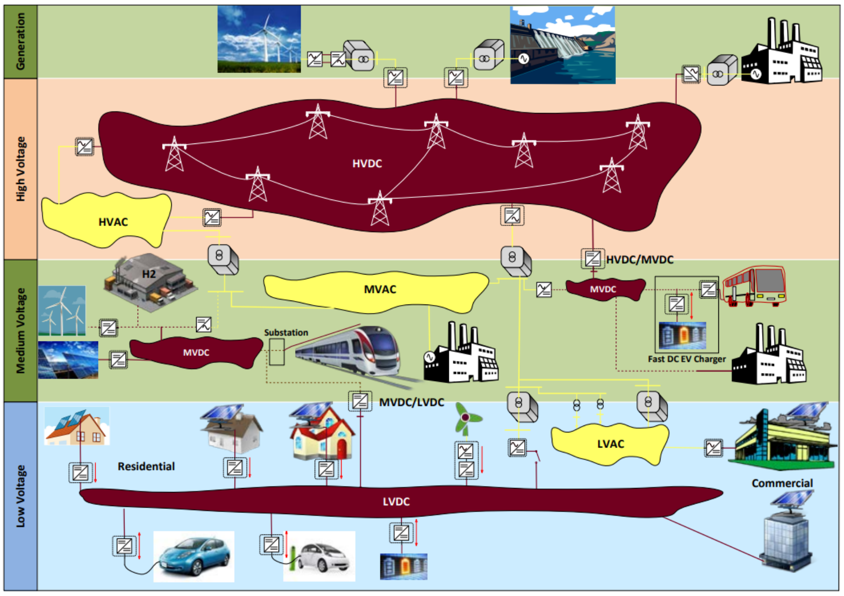


Figure 1.2: The concept of the Future Architecture of the Network Project in New Zealand where DC circuit breakers are crucial for all the connecting points from any power source to a load [11]

- Supercapacitor-assisted surge absorber (SCASA) - A high performance, low component count surge absorber [12–16]
- Supercapacitor-assisted low dropout regulator (SCALDO) - An extra low-frequency DC-DC converter technique with similar efficiency to inductor-based switch mode power supplies [17–22]
- Supercapacitor-assisted temperature modification apparatus (SCATMA) - Rapid heat transfer technique into flowing water based on a low DC voltage SC bank [23,24]
- Supercapacitor-assisted light emitting diode (SCALED) - Very low-frequency LED converter technique for renewable systems with built-in energy storage capability [25–30]

The presented DCCB research is inspired by the patented SCASA innovation that was developed to absorb power-line surges using SCs. In the SCASA method, a high-voltage impulse superimposed on a 230-V AC power line is absorbed by a low-voltage SC.

1.5 Supercapacitors for DC Circuit Breaking

Supercapacitors have capacitance values nearly a million times greater, as well as relatively low equivalent series resistance (ESR) values, compared to conventional electrolytic or film capacitors of the same canister size. However, their DC voltage ratings are relatively low, typically ranging from 2.5 to 4.2 V. With the experience of developing SC-assisted techniques during the past 20 years, the power electronics team considered the possibility of using SCs for DCCBs, based on the fact that it is easy to find a tiny SC where its energy storage capability of $\frac{1}{2}CV^2$, is significantly higher than the stored energy of a typical inductive DC loop, $\frac{1}{2}LI^2$. Thus, the SC possesses sufficient storage capacity to absorb the inductive energy in the DC loop during DC circuit interruption.

SCA^{2}M controls the arc in a DC circuit loop during CB opening using a SC-based technique. The high-current pumping capability of SCs is effectively utilised in a galvanically isolated circuit to drive the DC loop current toward zero by providing an energy pulse to reduce the arc energy, thereby reducing arc duration and arc energy. By managing arc energy, contact-point degradation can be reduced, thereby enhancing contact lifetime.

1.6 Thesis Structure

This thesis provides the first comprehensive analysis of the supercapacitor-assisted arc management (SCA^{2}M). The design and analysis of the arc management technique developed for generic mechanical CBs in DC applications are presented. The chapters of the thesis are organised as follows.

- Chapter 1 (the present chapter) has provided a general overview of electrical circuit protection and a comparison of AC and DC circuit interruption, along with the project background and motivation.
- Chapter 2 provides an overview of DCCBs from both research and commercial perspectives and discusses their characteristics during circuit breaking, specially about the electrical arcing and the contact point deterioration.
- Chapter 3 discusses preliminary arc-extinguishing techniques for DCCBs using experimental results obtained by the author. It also presents a novel circuit topology which is developed into a self-powered and self-controlled hybrid DCCB.
- Chapter 4 introduces SCs for DCCBs and briefly discusses their technology. It also presents a novel galvanic isolation switch activator topology developed for hybrid DCCBs. Additionally, the supercapacitor-assisted surge absorber technique (SCASA) is explained, including the author's motivation for developing a novel DCCB technique based on SCASA.
- Chapter 5 provides a detailed, step-by-step explanation of the arc-management technique. It includes mathematical analyses along with simulation and experimental results.
- Chapter 6 presents further experimental measurements from the 2-kW, 80-A DC prototype circuit and concludes on the new arc management technique.
- Chapter 7 outlines key achievements, potential future research directions, and an established international collaboration related to this work.

Chapter 2

Essentials of DC Circuit Breaking

2.1 Scope

When electric current flows through a conductor, a magnetic field is generated around it. This magnetic field causes parasitic inductance to appear in the wiring, which is influenced by the geometry of the circuit loop. Thus, part of the electrical energy provided by the source is stored in the parasitic inductance as magnetic energy $\frac{1}{2}Li^2$, where L is the parasitic inductance and i is the loop current. During CB opening under fault conditions or manual tripping, most of the stored magnetic energy is released across the mechanical contacts as an electric arc. This electric arc damages the contact points and reduces the lifetime of the CB. The generation of the electric arc is further detailed in Section 2.3.2.

Two types of cycle lifetimes are defined for CBs: mechanical and electrical. The mechanical cycle lifetime refers to the total number of open–close operations a CB can safely perform under no-load conditions, before mechanical components such as springs and actuators wear out and fail. The electrical cycle lifetime refers to the total number of open–close operations a CB can safely perform under load, including normal operation, overload, and short-circuit conditions. During these operations, the contact points of the CB degrade due to electrical arcing. The electrical cycle lifetime is shorter than the mechanical cycle lifetime.

Contact point degradation during fault interruption is significantly lower in AC than in DC, due to the minimal arcing in AC. This is demonstrated in Fig. 2.1, which shows results from a test using a commercially available 2-A AC miniature CB to interrupt AC and DC circuits. Under identical environmental conditions, two identical breakers were subjected to 150 trip cycles with a 20-A fault current for both AC and DC tests. Contact surfaces were imaged using optical magnification, and degraded regions exhibiting pitting and corrosion were outlined in black [31].

In DC applications, the absence of natural current zero crossings, as illustrated in Fig. 1.1, results in intense arcing [5,8], leading to a greater reduction in operational lifespan. Therefore, the use of traditional ACCBs in DC applications is limited [6]. When ACCBs are used in DC systems, they are susceptible to intense electrical arcing, which can significantly reduce their operational lifespan [6]. Effective, reliable, and cost-effective

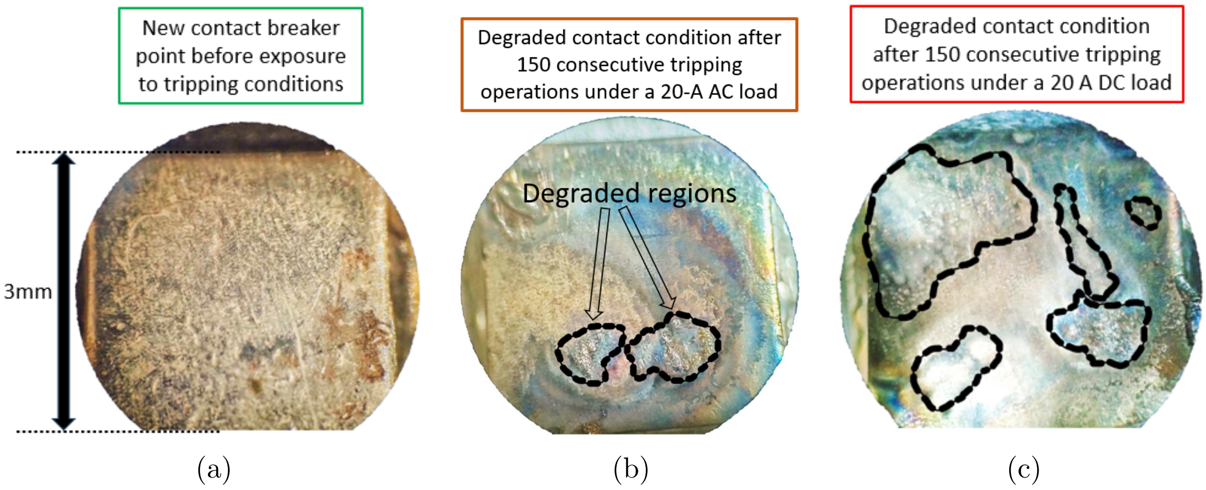


Figure 2.1: Degradation, corrosion, and pitting of circuit breaker contact. (a) New AC miniature circuit breaker; (b) 50 Hz AC case after 150 consecutive breaking operations; (c) same contact after 150 consecutive breaking of DC operations.

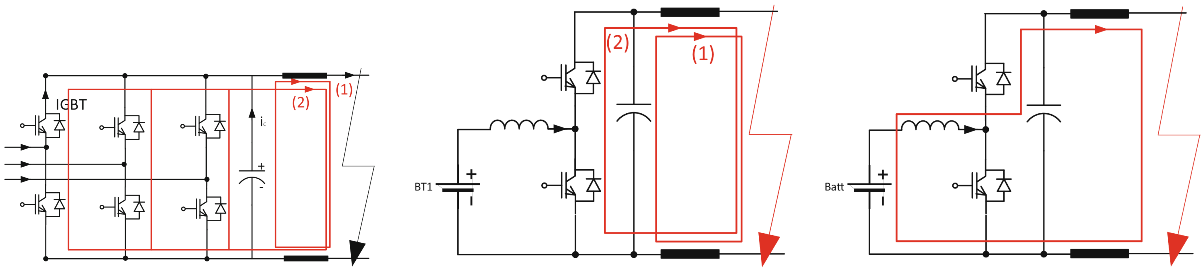
DCCB technology is essential for fast fault detection and interruption in DC networks. It prevents equipment damage, minimises downtime, and maintains system stability [32]. DCCBs protect sensitive infrastructure in solar power plants, wind farms, electric transportation systems, and DC transmission and distribution networks.

2.2 DC Fault Types

In a DC system, there are two main types of fault: line-to-ground and line-to-line. These are commonly referred to as short-circuit events, as they create unintended low-impedance paths that result in currents significantly higher than those seen during overloads—situations where the circuit exceeds its rated capacity for an extended period.

Any short-circuit current typically comprises two components: (i) a transient current generated by the capacitor at the output of the power converter, and (ii) the sustained current supplied by the power source. The time-course of this current depends on which power sources are involved in the event, as well as their associated peak magnitudes and time constants.

Figure 2.2 illustrates the fault current paths associated with several cases. Figure 2.2(a) shows that the capacitor at the output stage of an AC-DC converter starts pumping fault current as the capacitor is the closest energy-storage element. Freewheeling diodes in electronic switches are also in the fault current path. Figure 2.2(b) shows the case associated with a DC-DC boost converter. After capacitive discharge begins, the fault current continues to flow from the power source, as illustrated in Fig. 2.2(c), where the power source is a battery [33].



(a) (b) (c)

Figure 2.2: Fault currents associated with power converters. (a) AC-DC converter; (b) boost converter fault creating a fault current through body diodes and output capacitor; (c) fault current via DC source in a boost converter [33].

2.3 DCCB Types and Evolution

Traditionally, fuses have been used to interrupt fault currents in electrical circuits. Fuses are single-use devices that must be replaced after interrupting a circuit. In most modern applications, where quick restoration of service is essential, this limitation makes fuses an unsuitable solution.

There are three types of DCCBs: (i) mechanical, (ii) solid-state, and (iii) hybrid. Mechanical DCCBs use mechanical switches, solid-state circuit breakers (SSCB) rely on semiconductor switches, and hybrid DCCBs combine both switch types. Mechanical breakers use moving contacts to interrupt current during a fault, generating an electric arc that degrades the contact surfaces and reduces the breaker's lifespan.

Semiconductor switching technology was introduced into DCCB design during the 1980s [34]. The integration of semiconductor switches into circuit protection devices was driven by advancements in power electronics with the invention of metal oxide field effect transistors (MOSFET) and insulated gate bipolar transistors (IGBT). The application of semiconductor technology in DCCBs has expanded due to its high-speed switching capabilities and superior performance compared to traditional mechanical switches but face challenges such as high cost, thermal management issues [34], and limited scalability with immature semiconductor technology [35–37]. Additionally, because SSCBs have short disconnection times, coordinating the timing between upstream and downstream DC breakers can be challenging within DC grid systems [38]. Moreover, achieving reliable, cost-effective, energy-efficient devices remains a major challenge in the development of commercially viable DCCBs for large-scale deployment.

All three types of DCCBs can be represented as shown in Fig. 2.3. Mechanical DCCBs use a mechanical switch in the main current path, with a commutation path comprising passive components such as inductors and capacitors.

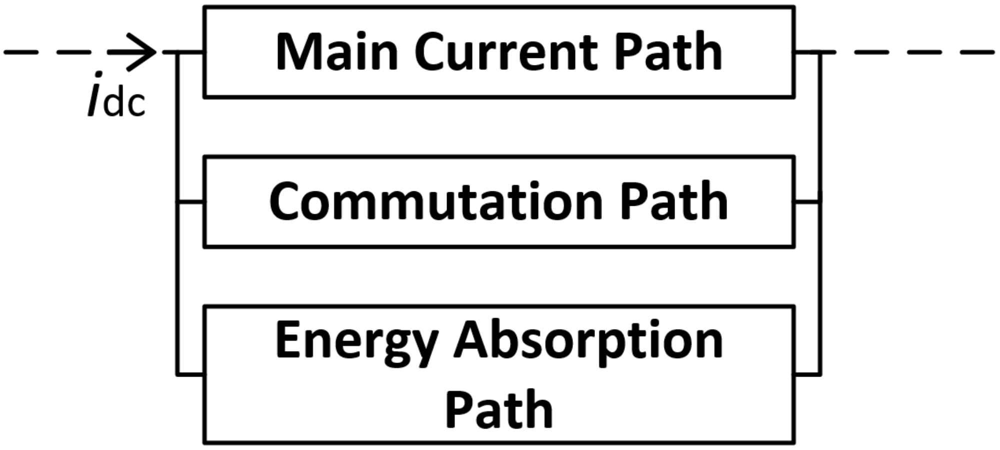


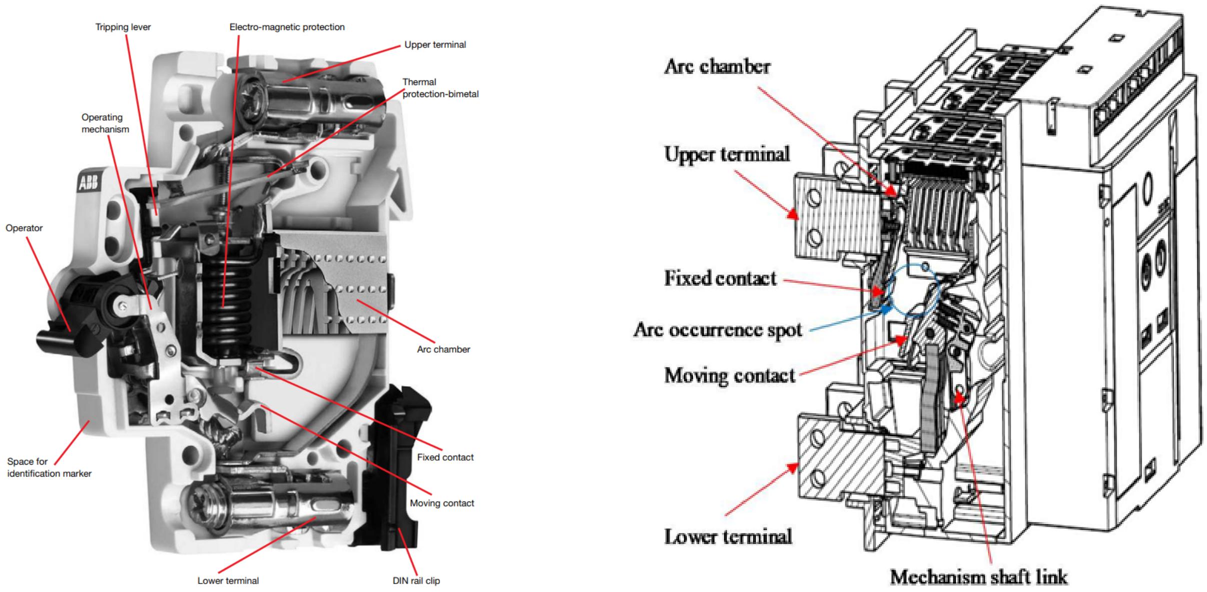
Figure 2.3: General arrangement of the DCCB

SSCBs use semiconductor switches in the primary current path and do not require a separate commutation path. In hybrid DCCBs, the primary current path includes either a mechanical switch or a combination of mechanical and semiconductor switches, while the commutation path utilises solid-state switches. For all DCCB types, metal oxide varistors (MOV) are connected in parallel with the switching device in the energy absorption path to dissipate residual energy stored in the line inductance. As the DCCB undergoes multiple tripping cycles, the MOVs experience repeated energy absorption events, resulting in performance degradation [39], which in turn degrades the overall performance of the DCCB. For particular applications, transient voltage suppression (TVS) diodes are used in place of MOVs. While MOVs are more robust for handling high-voltage and high-current surges, for circuits that require accurate voltage clamping with extremely fast response times, TVS diodes are the better choice.

2.3.1 Mechanical DCCBs

Mechanical DCCBs are constructed solely with mechanical switches, so represent the simplest form of switching technology. Mechanical DCCBs can be grouped into broad categories such as miniature circuit breakers (MCB), molded case circuit breakers (MCCB), air circuit breakers (ACB), and vacuum circuit breakers (VCB); classifications are based on voltage and current ratings, and arc extinguishing mechanisms. Similar groupings apply to ACCBs. Figure 2.4 shows sectional views of two mechanical CBs used in industrial applications.

There are two common operating principles inside mechanical DCCBs: thermal tripping via a bimetal strip for overload faults, and electromagnetic tripping for short-circuit faults [33] as illustrated in Fig. 2.5. Thermal limits are shown in red, electromagnetic tripping limits for various breaker types, such as type B and type C, appear in grey. The triggering mechanism is mechanically linked with the metal contact points. Thermal



(a) (b)

Figure 2.4: Sectional view of (a) a miniature circuit breaker, [40] (b) an air circuit breaker [9]

tripping characteristics exhibit an inverse-time characteristic, where the tripping time decreases with increasing overcurrent under overload conditions.

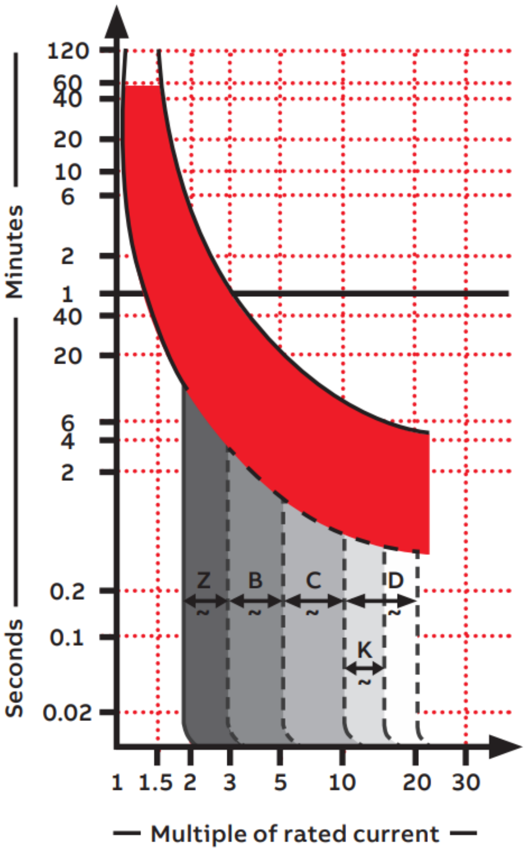


Figure 2.5: Thermal and electromagnetic tripping characteristics for a mechanical CB [41]

Electromagnetic tripping activates when the overcurrent exceeds a predetermined threshold, resulting in near-instantaneous interruption. This threshold is typically adjustable in most CBs, except for MCBs (shown in Fig 2.4(a)), which are manufactured only for low current ratings, usually below 125 A.

In the open state, mechanical switches have galvanic isolation between the two contacts with very high resistance to withstand the supply voltage. One is a fixed contact and the other is a moving contact as shown in Fig. 2.4. The arc chamber (arc grid) consists of metal splitter plates designed to split and cool the arc and facilitate rapid arc extinction. As the arc enters the splitter plates in the arc chamber, it divides into multiple smaller arcs, as shown in Fig. 2.6. This tends to build a high voltage (arc voltage) opposite to the source voltage, and that helps to extinguish the arc current.

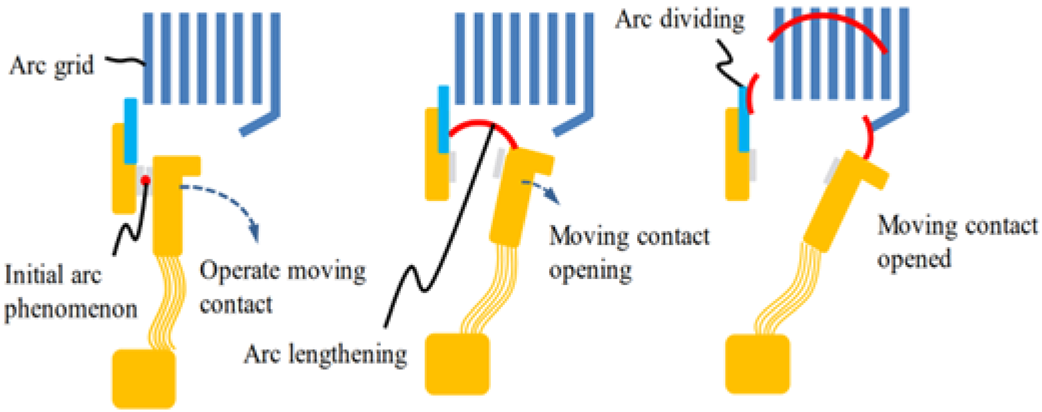


Figure 2.6: Arc extinction process in a circuit breaker [9]

The size of the arc chamber also influences arc extinguishing time. As shown in Fig. 2.7, reducing the chamber width enables faster arc extinction [42]. Arc characteristics are further explained in Section 2.3.2.

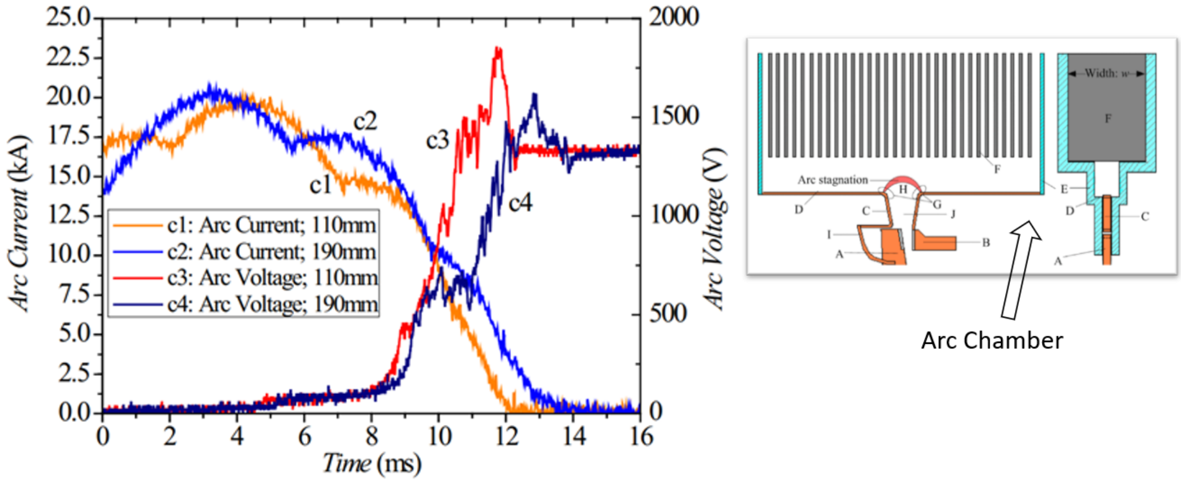
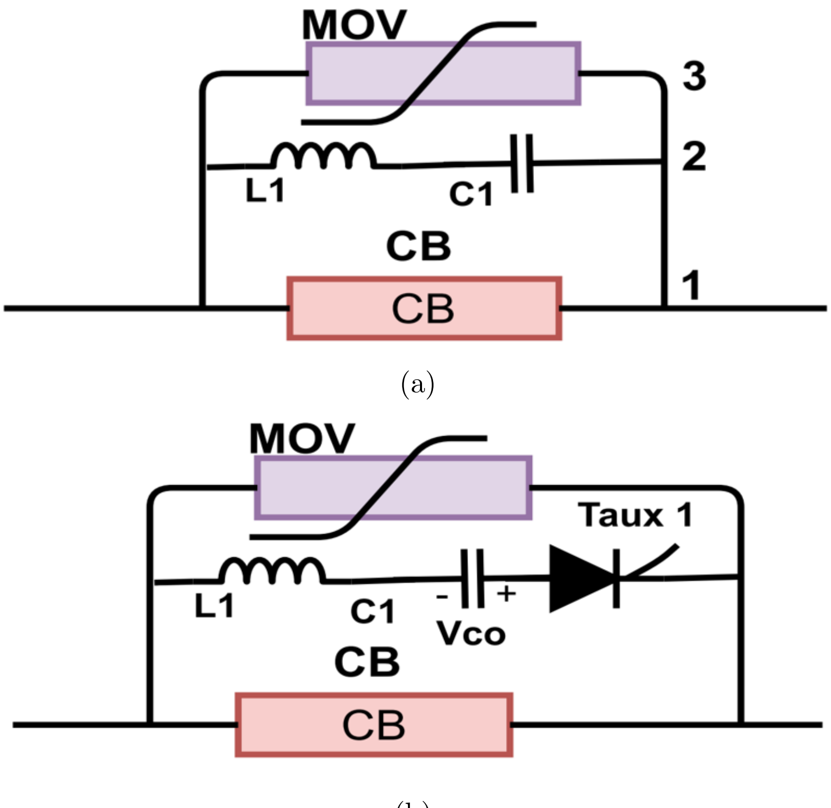


Figure 2.7: Variation of DC arc voltage and current characteristics with arc chamber width (left), and arc chamber configuration (right) [42]

The on-state resistance of mechanical CBs is very low, typically in the range of microohms to milliohms [6], making them well suited for minimising continuous conduction losses. Typically the on-resistance changes with their rated current value. For low-current-rated MCBs, the on-resistance is in the milliohm range, while for high-current-rated MCCBs or ACBs, it is in the microohm range. However, mechanical DCCBs exhibit significantly longer response times (milliseconds to tens of milliseconds) compared to SSCBs, which respond in a few microseconds [34].

Numerous studies are currently underway to develop an effective DCCB. Certain mechanical DCCB techniques generate an overvoltage exceeding the source voltage to reduce the DC current to a zero-crossing point [43]. An alternative approach uses *LC* resonant circuits connected in parallel to the mechanical contact to generate artificial zero-crossing points [34, 44–47]. Resonant circuits can be classified as passive or active, as illustrated in Fig. 2.8.



(a)

(b)

Figure 2.8: (a) Passive and (b) active resonant DCCBs [34]

Passive resonant circuits function with an initially uncharged capacitor that is charged by the fault current; the stored energy is then used to apply a reverse current into the DC circuit loop, creating a resonance condition. In contrast, active resonant DCCBs utilise a pre-charged capacitor to generate the reverse current [43]. Active resonant DCCBs require a fast mechanical or solid-state switch to introduce the pre-charged capacitor into the *LC* circuit [34, 44, 45, 47].

Another approach inserts a transformer whose primary winding is excited by a different power source, typically using high-voltage capacitors; the secondary winding is connected either in parallel with a series capacitor [48] or directly in series [49,50] with the mechanical breaker to reduce and then zero the current in the main DC circuit loop.

2.3.2 Electric Plasma Generated During DC Circuit Opening

When a DC electric current flows through a conductor under normal load operation, magnetic energy $\frac{1}{2}LI^2$ is stored in the line inductance. During a fault, the CB opens, generating a voltage, U_{arc}, across the contact points. As the contacts begin to separate, the contact resistance, R_c increases rapidly due to the reduction in effective cross-sectional area, "a" leading to a sharp rise in current density as given in the Eq. 2.1 [51], where ρ denotes the resistivity of the contact material,

$$R_c = \frac{\rho}{2a} \tag{2.1}$$

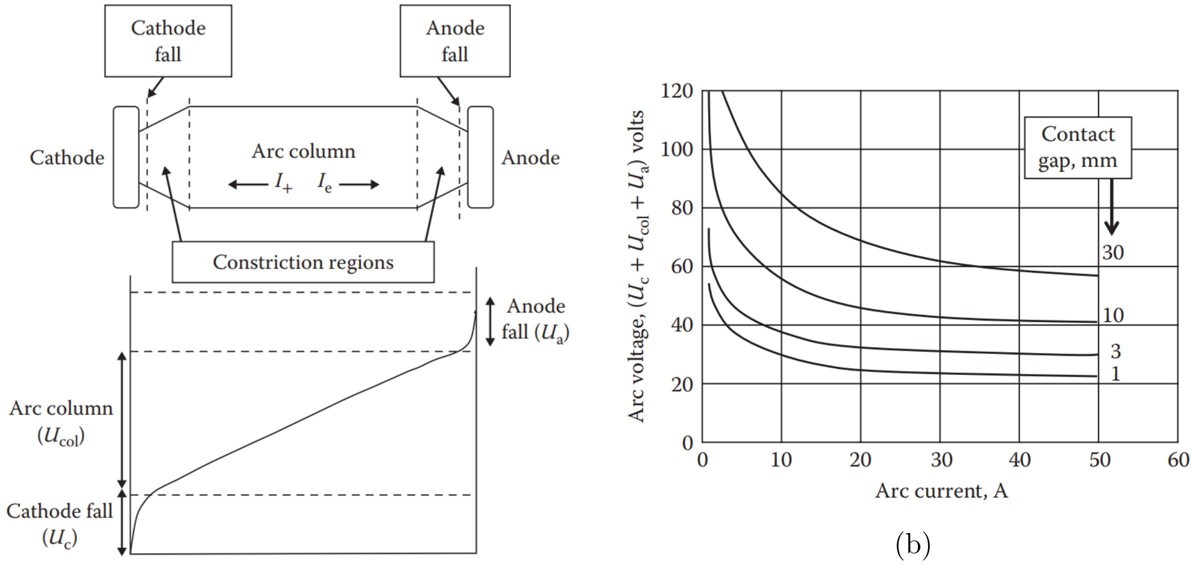
This leads to a significant increase in the contact spot temperature, T_{c}, which can potentially reach the material's melting point. The contact spot temperature is given by Eq. 2.2, where T_a represents the ambient temperature, and temperatures are expressed in kelvin (K) [51].

$${T_c}^2 = {T_a}^2 + {U_{\text{arc}}}^2 \times 10^7 \quad \text{K} \tag{2.2}$$

When the contact spot temperature reaches the melting point of the metal contacts, a molten metal bridge forms between the separating contacts. This molten bridge sustains the connection until it becomes unstable and ruptures. The rupture of the molten bridge releases metal vapor into the contact gap. Following this rupture, an electric arc emerges near the former bridge location, facilitated by the discharged metal vapour [51].

During circuit interruption, the sudden voltage, U_{arc}, generates a strong electric field across the contact points due to their initially minimal separation distance. This intense electric field ionises not only the metal vapour but also the surrounding air, further contributing to arc formation. Since metal vapour typically has a lower ionisation potential than nitrogen or oxygen in air, it is more readily ionised, which enhances arc stability and conductivity.

For a stationary arc, the voltage drop near the electrodes is higher than that in the central region, as illustrated in Fig. 2.9(a). This holds true for both the initial arc and the multiple arcs generated after the main arc strikes the splitter plates in the arc chamber. Additionally, a higher arc voltage results in a lower arc current, as shown in Fig. 2.9(b).



(a)

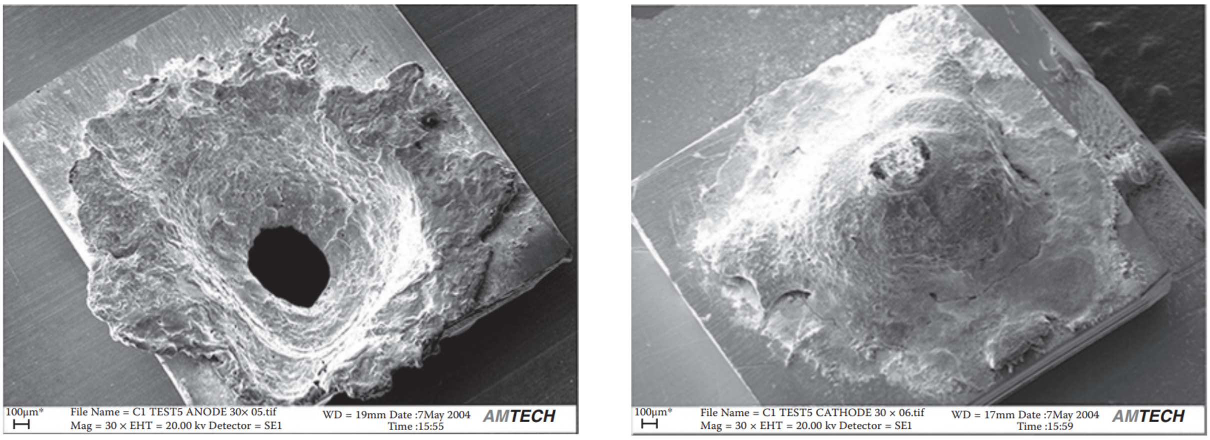
(b)

Figure 2.9: (a) Voltage–distance and (b) voltage–current characteristic of stationary arc [51]

Typically, the contact breaker points melt and evaporate when the arc voltage reaches approximately 10 V to 20 V, and the resulting metal vapour initiates an electric arc that persists until the contact points separate to a critical distance [51]. Table 2.1 shows the minimum arc voltages required to initiate an electric arc across different contact materials; minimum voltages all lie between 10 V and 20 V.

Table 2.1: Minimum arc voltage required to initiate an electric arc for different contact materials [51]

Contact material	$U_{\mathbf{min}}$ **(V)**
Al	11.2
Ag	12
Au	12.5
Cu	13
Fe	12.5
Ni	13.5
Pd	14
Pt	14
Rh	13
W	13.5
Sn	13.5
C	20
Ag (In/SnO_2)	11



(a) Anode (b) Cathode

Figure 2.10: Metal mass transfers from anode to cathode during the arc [51]

During the electric arc, contact material is transferred from one contact point (anode) to the other (cathode), as illustrated in Fig. 2.10, and some of the metal mass is released into the atmosphere, causing degradation of the contact breaker points. Figure 2.11 illustrates mass transfer between the electrodes. References [9, 42, 51–57] further explain arc characteristics.

Typical DC arc voltage and current characteristics during a fault are shown in Fig. 2.12.

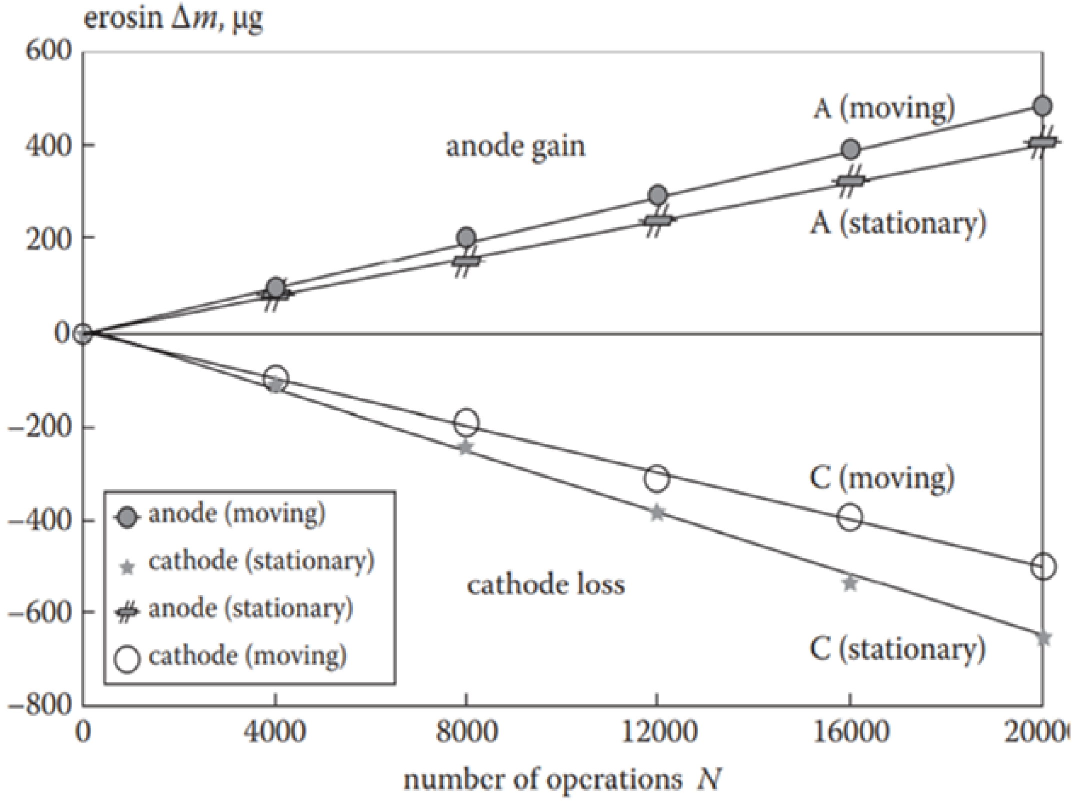


Figure 2.11: The DC erosion of Ag/CdO contacts with the number of operations, for a range of opening velocities with moving anode and fixed cathode, and moving cathode and fixed anode, for V = 62.5 V DC, I = 4 A and opening velocity 0.1 ms^{-1} [51].

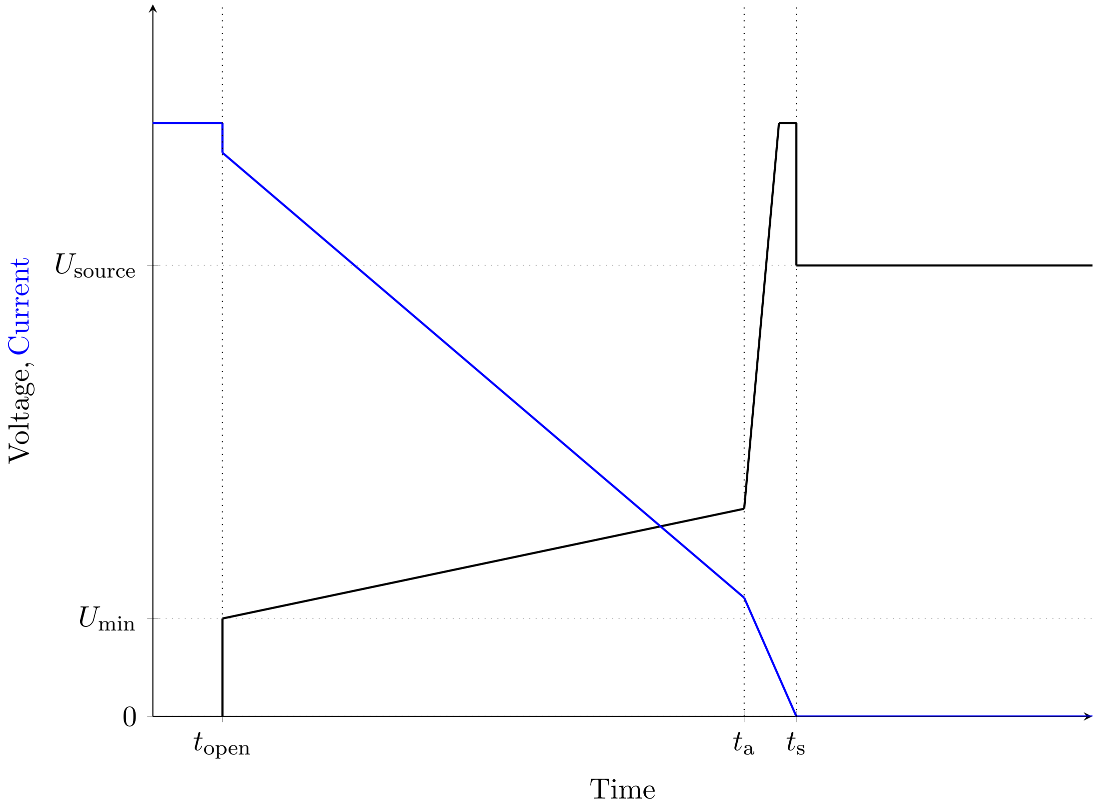


Figure 2.12: Arc voltage (black trace) and current (blue trace) behaviour from contact opening time (t_{open}), to arc extinguishing time (t_{s}).

The initial phase of Fig. 2.12 on the time axis, t_{open}, corresponds to contact opening, which occurs after a delay of several milliseconds due to the mechanical response time following fault detection. The interval from t_{open} to t_{s} represents the period of electrical arcing.

When the contacts begin to open at t_{open}, the arc current (blue line) suddenly drops by a small amount and the corresponding arc voltage jump (minimum arc voltage $U_{\min}$) can be seen. Then the arc current decreases gradually and the arc elongates during t_{open} to t_{a} as the contacts separate. During this period, the arc voltage increases gradually while the arc resistance rises rapidly (further details provided in Section 2.4.1). Beyond t_{a}, the energy supplied by the DC source becomes insufficient to sustain the arc due to rising arc resistance, causing the arc current to collapse abruptly. This rapid current decay causes a sharp increase in voltage, which peaks briefly before decaying to the source voltage U_{source} as the arc is fully extinguished at t_{s}. The final portion of energy stored in the line inductance accounts for this transient voltage peak. Note that the arc voltage might not have settled to the source voltage exactly at the moment the arc current reaches zero in real arcs, as the arc voltage takes some time to settle to the source voltage due to the effects of plasma and circuit parasitic capacitance. Observed waveform slopes vary continuously with time and depend on circuit parameters. Modelling a real arc involves complex physical processes; these dynamics are discussed further in Chapter 5.

Our research focuses managing the DC electric arc by shortening the arcing time

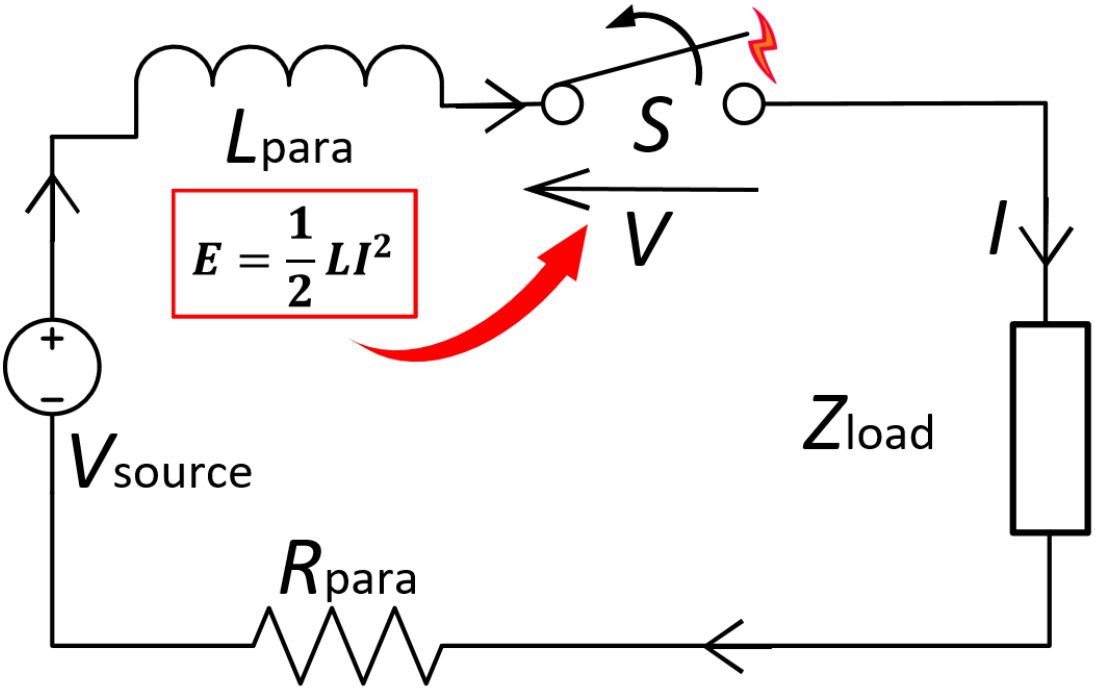


Figure 2.13: Part of the energy stored in the line inductance is dissipated as an electric arc across the contact points during circuit interruption.

t_s-t_{open} using a SC-based approach. Reducing arcing time decreases the total energy dissipated across contact points, thereby minimising contact-breaker degradation and extending CB lifespan.

An illustrative example, based on preliminary measurements of arc-voltage and arc-current characteristics, was derived using the simplified DC circuit shown in Fig. 2.13, with DC source voltage V_{source}, mechanical switch S, load impedance Z_{load}, line inductance L_{para}, and the circuit loop's parasitic resistance R_{para}.

Although the parasitic resistance and inductance are depicted as lumped elements in the Fig. 2.13 to illustrate energy transformation, they are, in reality, distributed throughout the circuit wiring. The test bench comprised an MCB rated at 10 A, a load of 0.5 Ω, and a loop inductance of 660 μH, where the fault is initiated by manual tripping. The source voltage was set to 25 V to a steady-state DC loop current of 36 A before the fault [58]. During the circuit breaking of S, most of the $\frac{1}{2}L_{\text{para}}I^2$ magnetic energy will be dissipated as an electric arc across the switch, while some of the remaining energy will be dissipated trough the load and the parasitic resistance in the circuit loop. Experimental waveforms for the arc voltage and current are shown in Fig. 2.14. After arc initiation, arc resistance increases from near zero as the two contact points move apart, increasing their separation. Thus, arc voltage increases as arc current reduces. Figure 2.15 illustrates how arc resistance varies with time.

Experimental results indicate that the arc initiates when the voltage across the contacts reaches 13 V (opposing the source voltage); the arc voltage then increases to a peak

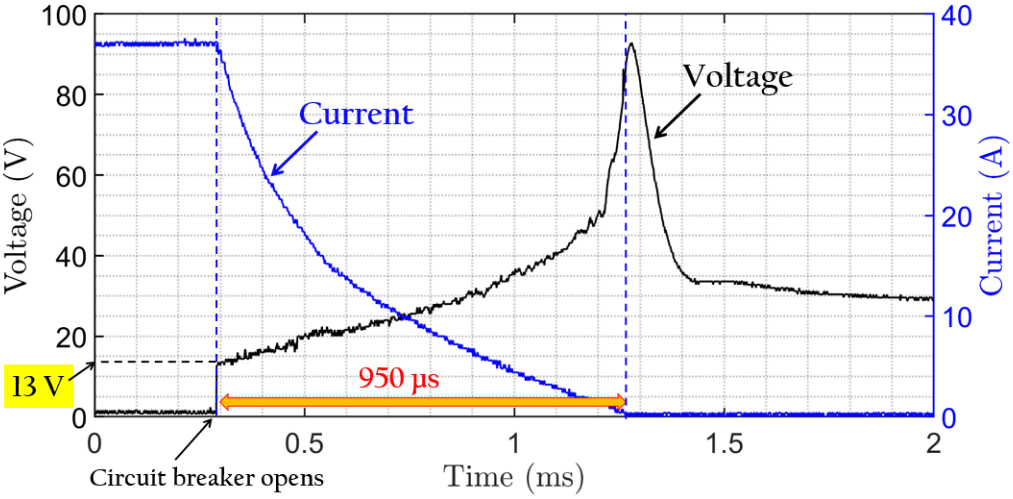


Figure 2.14: During circuit breaking, arc voltage rises gradually then peaks abruptly at termination while current diminishes gradually [58].

value before decreasing and stabilising at the source voltage. These results prove that 13 V is the minimum voltage required to generate the arc by melting and vaporising the copper contacts; thus, ionised metal vapour initiates an electric arc. This value aligns with literature indicating that the minimum arcing voltage for copper contacts is typically 13 V as shown in Table 2.1, while for most other metals, it ranges from 10 V to 20 V [51].

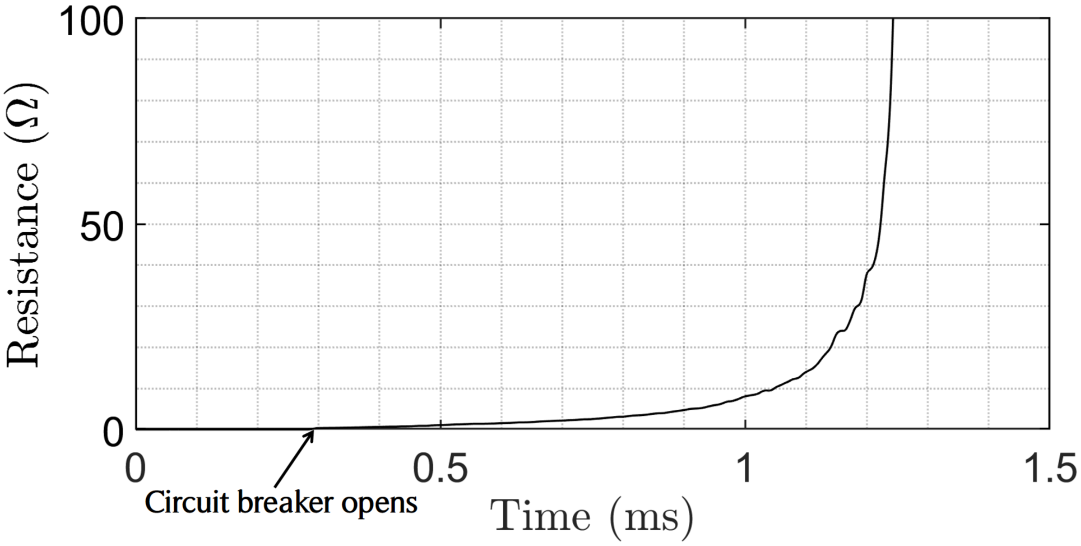


Figure 2.15: Arc resistance variation with time during circuit breaking

According to Fig. 2.14, the arc extinguishes at 950 μs for a loop inductance of 660 μH [58, 59]. There is still a minute current flow after 950 μs (persisting for an additional 30 μs), which cannot be clearly seen in Fig. 2.14 due to measurement uncertainty. Consequently, the peak of the arc voltage does not appear to align exactly with the current zero point. Arc extinguishing time is determined by the following factors:

- DC loop current and parasitic inductance

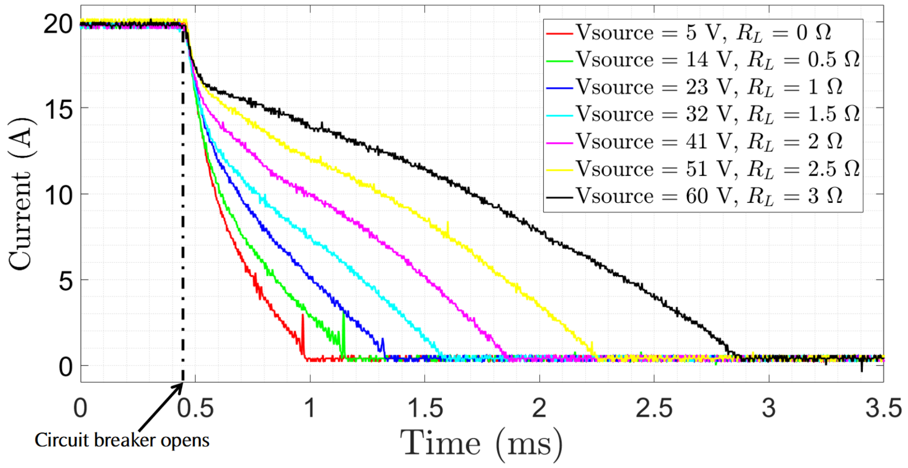


Figure 2.16: Electric arcing times increase with supply voltage.

- DC source voltage: arc voltage always builds to oppose the source voltage; this helps to stop the current flow from the source. For higher DC source voltages, the arcing time increases as illustrated in Fig. 2.16 [60].
- Contact point material, number of poles/contact pairs in series and contact separation speed
- The time required for the stored energy in the parasitic inductance to be completely de-energised.

A similar experiment was conducted by replacing the single-pole CB with three poles connected in series. Arc voltage and current waveforms are shown in Fig. 2.17, where three distinct 13 V voltage steps correspond to arc initiation at each pole [59]. The results show that replacing a single pole with three series-connected poles reduces the arc extinction time by approximately a factor of four, from 950 μs to 230 μs. This improvement arises because as the number of poles increases, multiple arcs are generated, one at each pole, resulting in a higher cumulative arc length and thus greater total arc resistance. Consequently, the arc extinguishes more rapidly in the three-pole configuration [61].

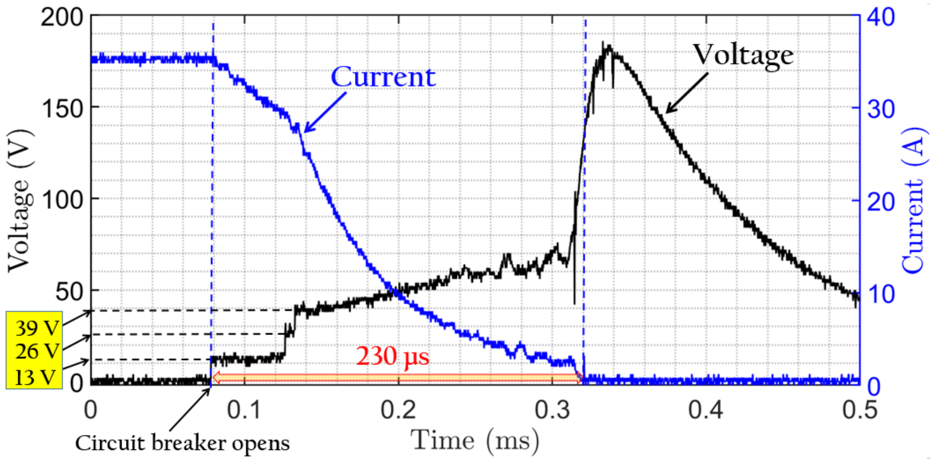
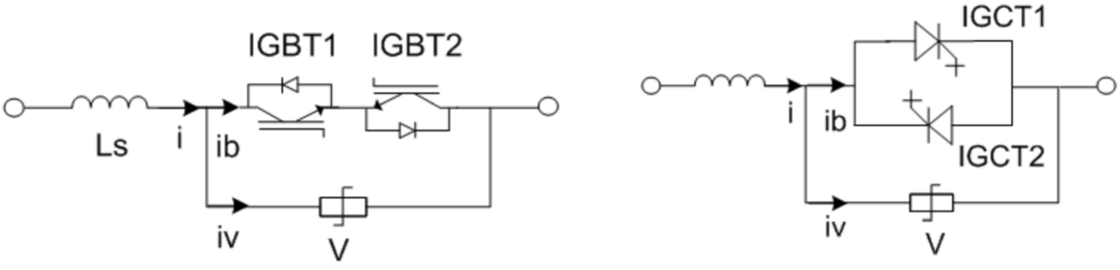


Figure 2.17: DCCB arc voltage and current characteristic for a DCCB consisting of three series-connected poles

The apparent misalignment between current zero and the peak of the arc voltage is higher in Fig. 2.17 than in Fig. 2.14, due to the expanded time scale in the Fig. 2.17.

2.3.3 Solid-State DCCBs

Only semiconductor switches are used in SSCBs during circuit interruption. Semiconductor switches such as MOSFETs, IGBTs, Integrated Gate-Commutated Thyristors (IGCT) and traditional thyristors are commonly used in these DCCBs. These solid-state switches are controlled by electronic signals, thus additional control circuits, voltage/current sensors and DC power supplies are required [62]. Figure 2.18 illustrates two general configurations of SSCBs, with Fig. 2.18(a) and Fig. 2.18(b) showing DCCB implementations based on the IGBTs and IGCTs, respectively.



(a) (b)

Figure 2.18: (a) IGBT, (b) IGCT-based solid-state DCCBs [63]

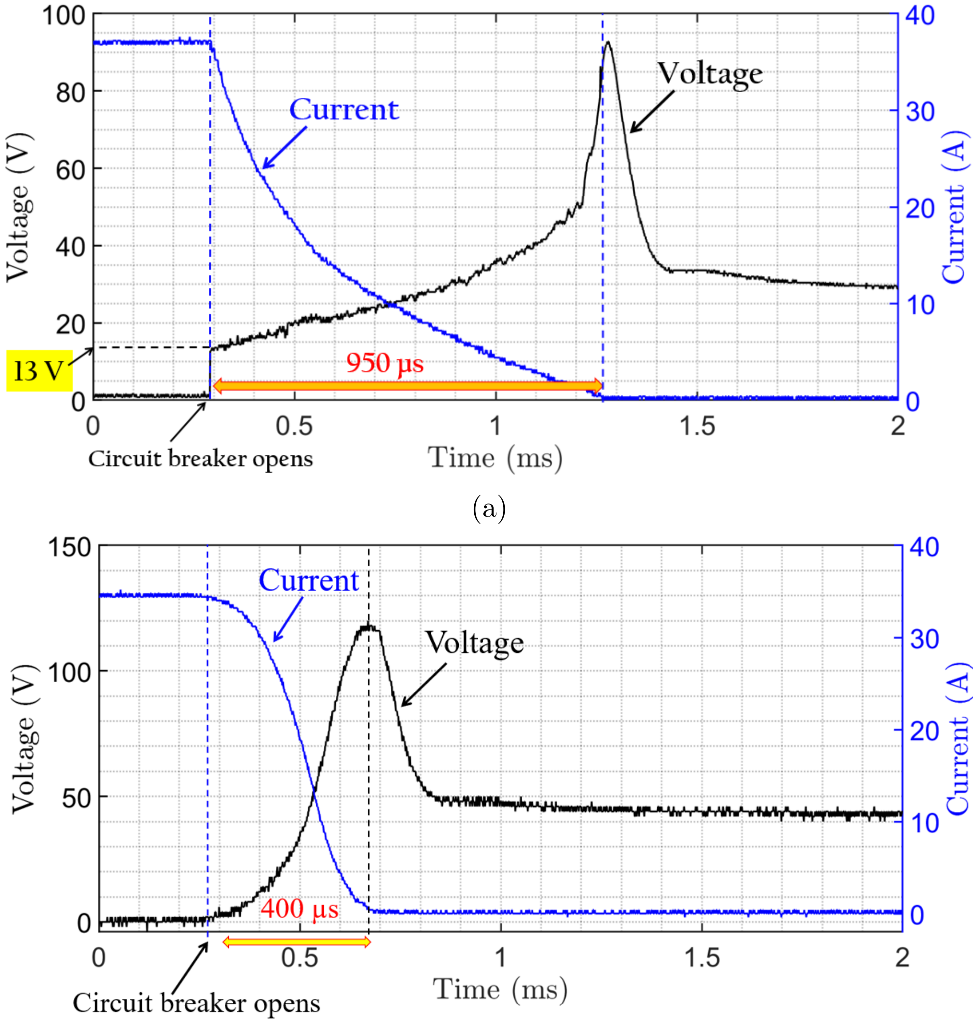
In order to provide galvanic isolation, a separate mechanical switch is required to maintain insulation between load and source *after* the fault is cleared. Certain research articles detail how the gate driver circuits are implemented to drive power electronic switches [64–66]. Exceptional cases are also available which do not require separate DC power supplies/gate drive circuits for solid-state [67, 68] and hybrid [69, 70] DCCBs.

SSCBs have fast response times in the range of microseconds. Their on-resistance is in the range of milliohms, which is higher than that of mechanical switches. Consequently, one of the major issues with SSCBs is the high on-state conduction losses. Therefore, appropriate cooling, using either a refrigerant or a water-cooling method, should be provided for the switches; however, this increases the overall cost [71]. Also, though the high-speed response is an advantage for solid-state switches, the same can be a disadvantage for some applications where the timely coordination of several SSCBs is essential [38].

Various new DCCB topologies for SSCBs have been proposed [34, 38, 72–80]. Some approaches involve generating a current reversal during CB opening using an LC resonant circuit, similar to techniques used in mechanical DCCBs and applicable to hybrid configurations [48–50, 81–87]. However, none of these are commercially manufactured in mass scale due to high cost and limited reliability. SSCBs have recently been introduced for certain applications such as in the marine and military industries by manufacturers including ABB [88] and Astrol [89]. Wide-bandgap semiconductor technology introduces high-performance electronic switches, however, the technology is still not well matured, so the cost is still high in SSCBs [35–37]. As a partial solution, researchers tend to use a mechanical contact with very low on-resistance during normal load operation, but deviate the fault current to another path which may include capacitors and/or semiconductor switches in hybrid DCCBs. Consequently, continuous conduction heat losses are minimised, and continuous forced cooling is not required in these hybrid DCCBs.

2.3.4 Current Interruption Through Semiconductor Switches

Unlike mechanical switches, solid-state switches do not have mechanical contact separation during the switching-off period. Therefore, there is no possibility of an electric arc forming within a semiconductor switch. Thus, the $-L\frac{di}{dt}$ inductive voltage transient remains unconstrained by the formation of a metallic plasma arc at approximately 10–20



(a)

(b)

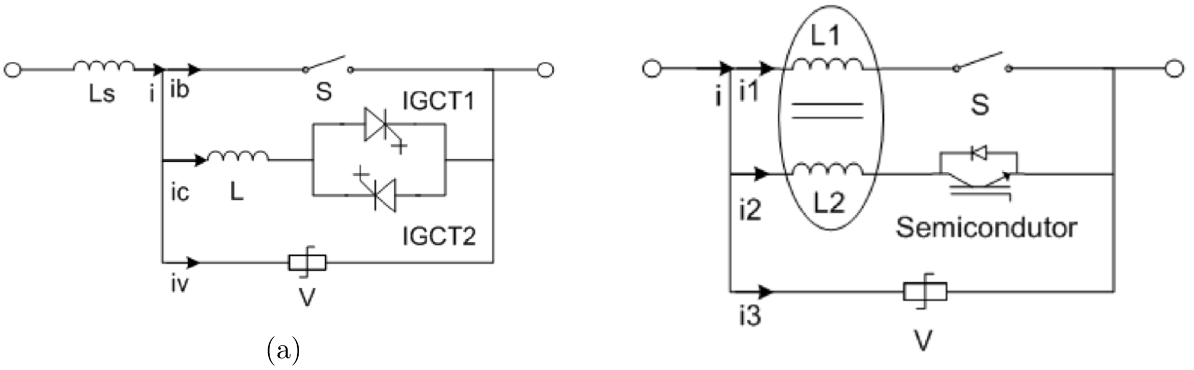
Figure 2.19: Voltage and current characteristics of circuit breakers (a) mechanical circuit breaking [58] and (b) solid-state circuit breaking.

V, as occurs in mechanical circuit breaking. Figure 2.19 compares the voltage across the breaker and circuit current characteristics of mechanical and solid-state circuit breaking. Figure 2.19(a) is identical to Fig. 2.14. A MOSFET is used as the SSCB to obtain the oscillograms in Fig. 2.19(b). Both experiments were conducted under similar fault current conditions. The two figures demonstrate two main aspects: (i) arc generation is not observed in the SSCB, and (ii) the SSCB extinguishes fault current more quickly than the mechanical CB.

The resulting high voltage spike generated in the SSCB can damage nearby electronic switches and components unless they are protected by energy absorption devices such as MOVs or TVS diodes. Some MOSFETs and IGBTs have inbuilt zener diodes which can absorb the residual circuit-loop energy.

2.3.5 Hybrid DCCBs

The significant disadvantages of mechanical DCCBs are their slow response times and the formation of an electric arc across the contacts during breaker opening. For SSCBs, the major disadvantage is the need for continuous cooling due to high continuous conduction losses. Thus, designers tend to use a mechanical contact with very low on-resistance during normal load operation, but redirect the inductive transient current to an alternative path via solid-state switches as illustrated in Fig. 2.20.



(a)

(b)

Figure 2.20: Hybrid DCCBs: (a) IGCT-based conventional DCCB (b) coupled inductor-based commutation-boosted DCCB [63].

In addition to the low conduction heat losses, this approach eliminates the electric arc associated with mechanical circuit breaking. However, due to the presence of solid-state switches, complex control systems with additional power supplies are still required. Additionally, a fast-response mechanical switch is required to rapidly commutate the fault current to the solid-state path. Thus hybrid DCCB technology is expensive and complex to manufacture in mass-scale for commercial usage.

One hybrid DCCB approach uses superconducting material to enhance current commutation from the mechanical switch path to the solid-state switch path [76, 90–92]. However, maintaining the very low temperatures required for the superconductivity is challenging and costly.

Another technique is to use multi-port DCCBs which share expensive components such as solid-state switches between multiple DCCBs in order to reduce cost [93].

In summary, the implementation of hybrid or solid-state DCCBs is complex because of the requirement for regulated DC power supplies, transistor gate drivers, and multiple transistors connected in parallel or series to handle the main breaker's rated current and voltage. However, the simpler approach of relying on a purely mechanical contact-based DCCB is also not ideal due to heavy arcs and slow response times.

2.4 Cost-effective Approaches for Enhancing DCCB Performance Using Traditional ACCBs

Two cost-effective approaches for DC circuit breaking involve modifying conventional ACCBs by connecting multiple poles in series or using permanent magnets inside the breaker to enhance arc extinction.

2.4.1 Multiple Pole-based Arc Extinguishing

The first approach uses multiple poles in a standard ACCB connected in series. A configuration with n poles, S_1, S_2...S_n connected in series is illustrated in Fig. 2.21.

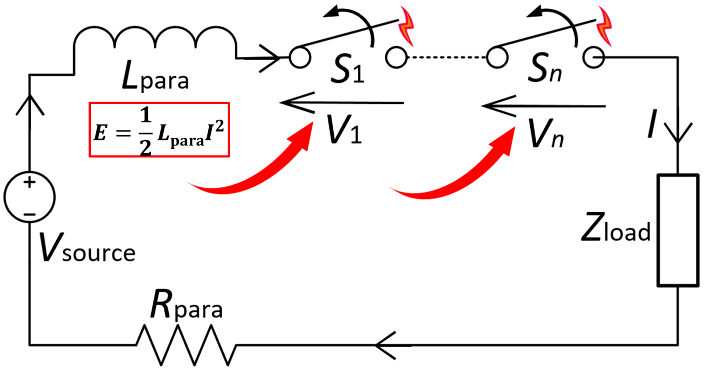


Figure 2.21: DC circuit breaker operation in which multiple poles of a generic mechanical breaker are connected in series [58]

During circuit opening with n poles, n arcs are generated across distinct pairs of contacts, distributing arc energy across the contacts and increasing the total arc path resistance by extending the arc length, as illustrated in Figs. 2.21 and 2.22. As total arc resistance increases, arc voltage opposing the supply voltage, rises, enabling faster arc extinction.

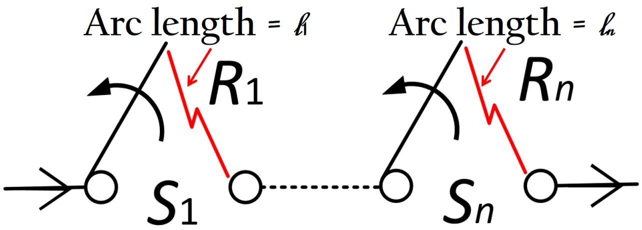


Figure 2.22: Total arc resistance increases with cumulative arc length during circuit interruption.

As shown in Fig. 2.22, an arc forms across each contact pair. The arc resistance of the n^{th} pole, R_n can be considered as a variable resistor,

$$R_n = \frac{\rho_n \ell_n}{A_n} \tag{2.3}$$

where ρ_n is the resistivity of the arc, ℓ_n is its length, and A_n is its cross section [61]. All three parameters vary with time. Resistivity, ρ_n is dependent on temperature: when the temperature is high, arc resistivity is low, thus forced cooling of the arc can extinguish the arc by increasing ρ_n rapidly. As the total arc length ℓ_1+...ℓ_n increases, so does the increasing total arc resistance R_1+...R_n, enabling faster arc extinction with additional poles. The effective cross-sectional area of the arc A_n depends on the geometry of the contact points and the intensity of the arc discharge.

Figure 2.23 provides experimental confirmation that increasing the number of poles

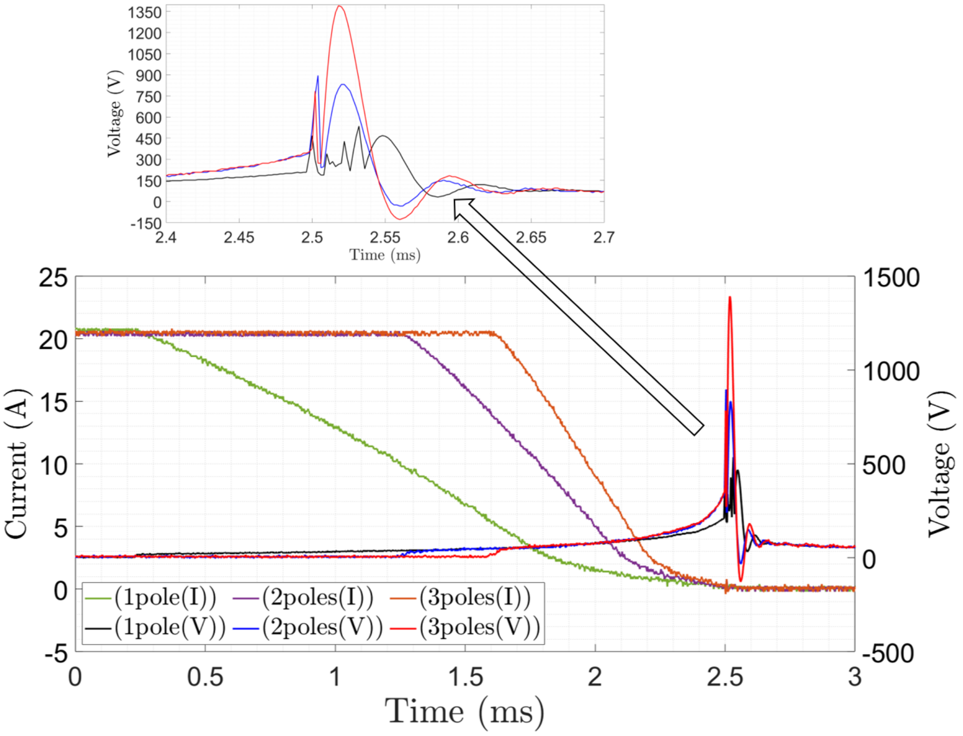


Figure 2.23: Arc extinguishing time decreases with an increasing number of poles; tests used a 2-A rated miniature circuit breaker.

reduces the time required to extinguish the arc current. The green, purple, and orange oscillograms represent arc current waveforms, while the black, blue, and red oscillograms represent arc voltage waveforms for the single-pole, two-pole, and three-pole cases, respectively. The peak arc voltage increases, and the time to interrupt the arc current decreases as the number of poles increases.

Circuit breaker manufacturers: Schneider Electric [7], ABB, Allen-Bradley, Terasaki, and Hager publish catalogs demonstrating how to connect up to four poles in series to enhance the breaking capacity of their CBs. This approach serves as a simple remedy for rapid arc extinction, which is challenging due to the absence of natural current zero crossings.

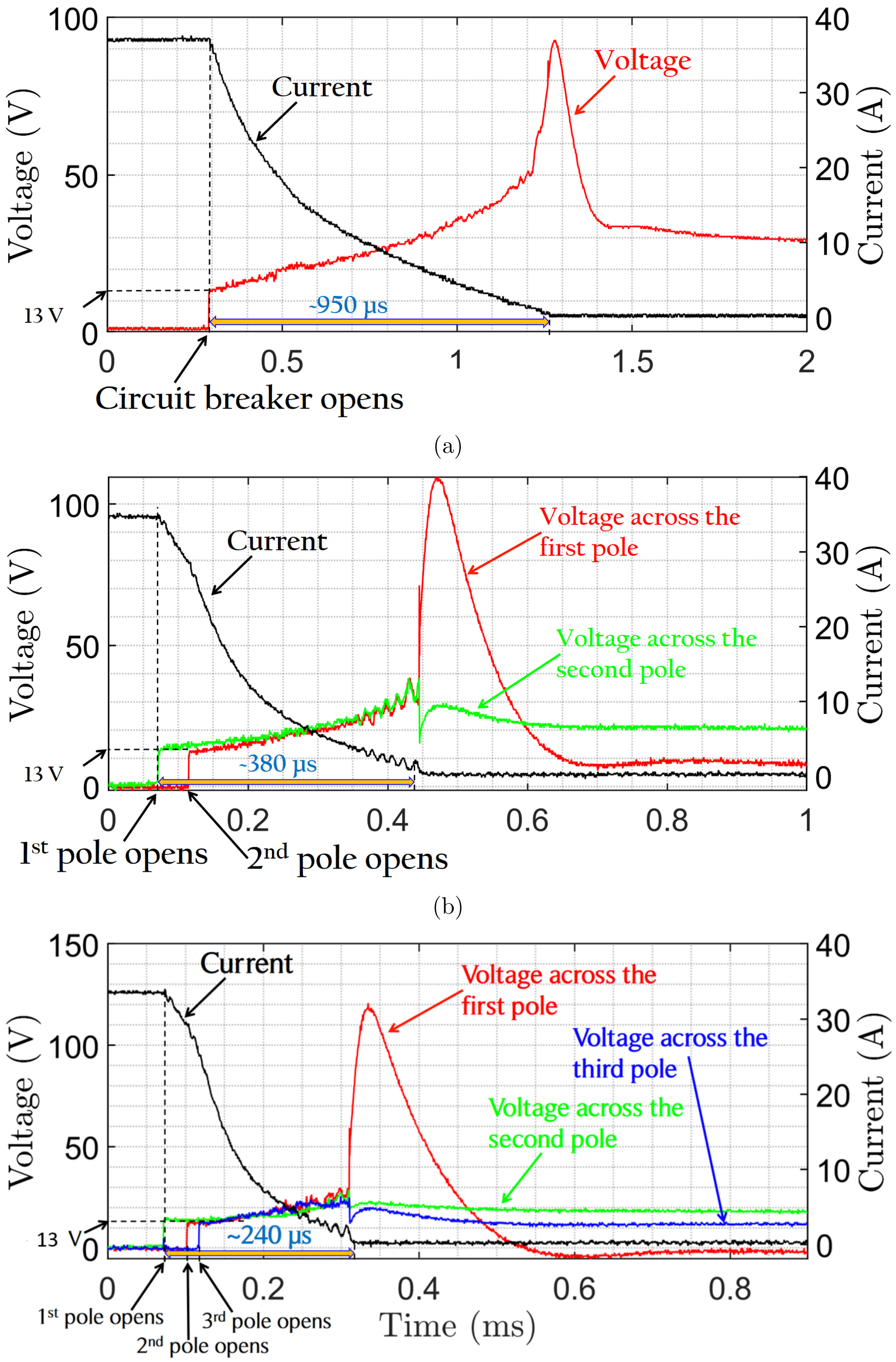
This technique is cost-effective due to its simplicity and lack of additional components; however, it has several disadvantages, including increased power loss from additional contact point resistance and a larger overall breaker size [6].

2.4.2 Demonstration of Multi-pole DC Circuit Breaking

Further experimental work was conducted to investigate the effect of the number of poles in series using a setup with a 25-V DC source, 36-A DC loop current, and 660-μH line inductance. The breaker was manually tripped to obtain the arcing phenomena. The arc voltage and current characteristics are shown in Fig. 2.24, where subfigures (a), (b), and (c) illustrate the characteristics for single-pole, two-pole, and three-pole circuit breaking, respectively.

When the breaker opens, the arc current decays from 36 A to zero within 950 μs as illustrated in Fig. 2.24(a) for the single-pole case. As the arc current starts to decrease, arc voltage suddenly jumps to 13 V and then increases gradually, reaches a peak of around 90 V and settles down to the source voltage. Figure 2.24(b) depicts the arc voltage and arc current patterns where the circuit is maintained in similar conditions except for the number of poles used in the breaker. The arc extinguishing time was heavily reduced from 950 μs to 380 μs. The peak of first pole's arc voltage also increases from 90 V to 110 V. The sudden jump of 13 V can be seen for each pole in the initial stage of the circuit breaking. A small delay of around 40 μs is observed between the opening of first and second poles due to the randomness of arc initiation between the poles. The arc extinguishing time can be further reduced to 240 μs by using three poles in series, as illustrated in Fig. 2.24(c).

Figures 2.24(b) and 2.24(c) show that the arc voltage across a single pole reaches a peak; however, arc voltages across the other poles do not exhibit such a peak. During the arcing stage, arc voltages across the poles coincide, causing the total instantaneous arc voltage to increase rapidly with the number of poles. Additionally, the peak arc voltage across the first pole increases from 90 V to 110 V and then to 120 V.



(a)

(b)

(c)

Figure 2.24: Arc voltage and current characteristics tested for a 10-A rated miniature circuit breaker (a) single-pole (b) two-pole and (c) three-pole circuit breaking

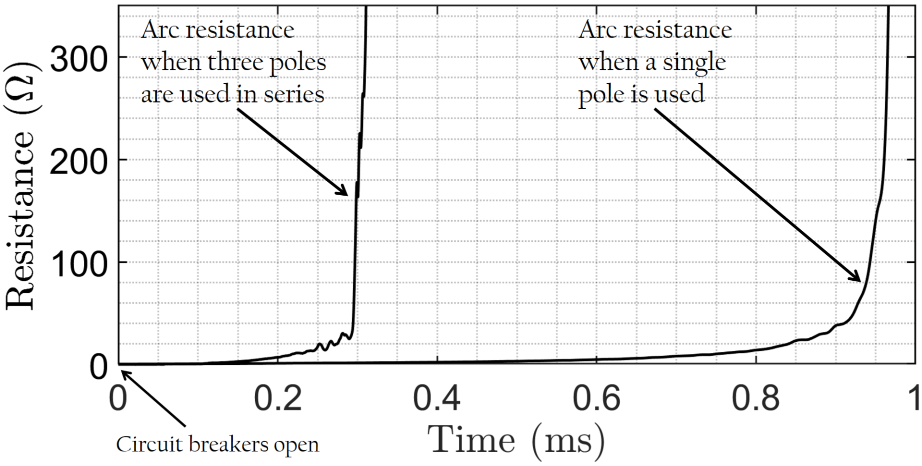
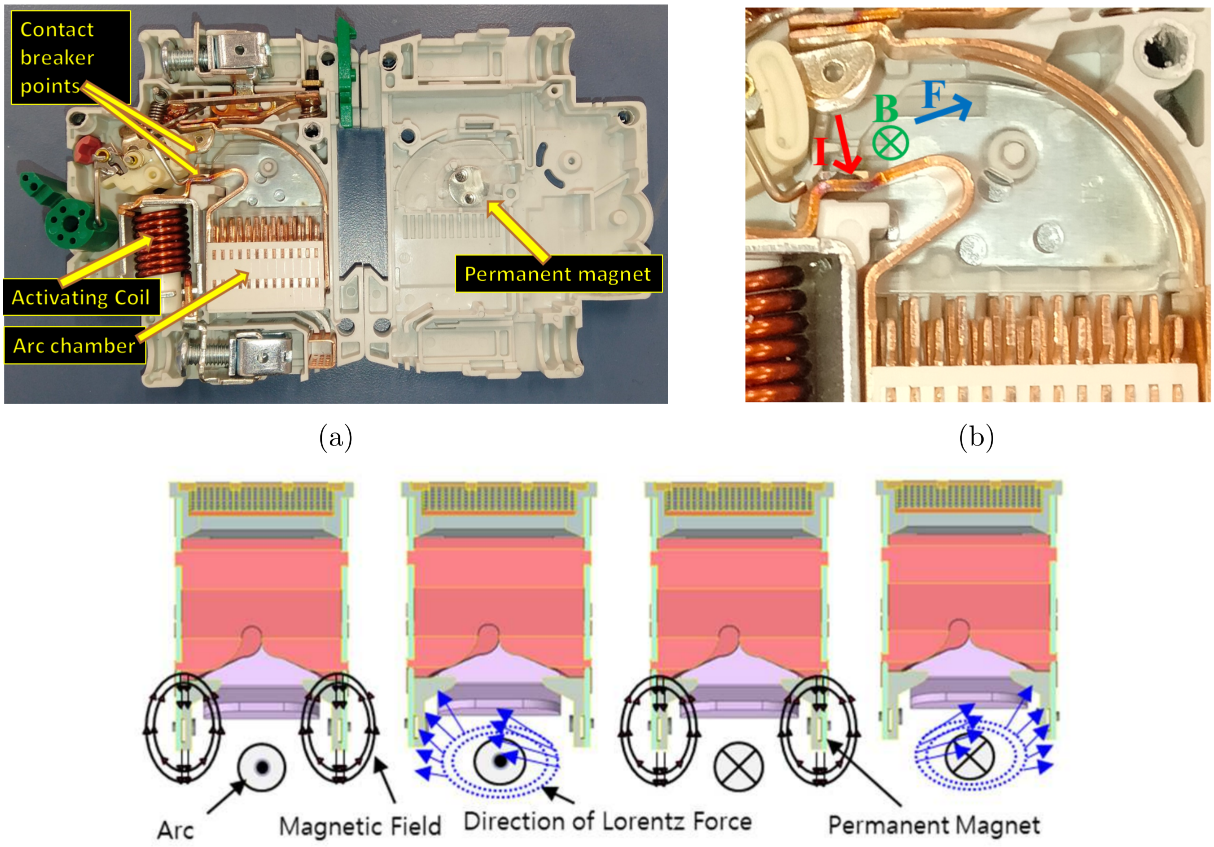


Figure 2.25: Arc resistance behaviour comparison for single-pole and three-pole circuit breaking

Figure 2.25 compares the arc resistance variation for single-pole and three-pole configurations. Arc resistance was calculated using Ohm's law based on instantaneous arc voltage and current data points.



(a)

(b)

(c)

Figure 2.26: Inbuilt permanent magnet inside a (a) 6-A rated Suntree DCCB, (b) Lorentz force, F acts on the arc current, I toward the arc chamber due to the applied magnetic field, B, (c) the Lorentz force drives the electric arc into the arc chamber [9].

2.4.3 Circuit Breaking using Magnetic Fields

The second approach to reducing arcing time involves using permanent magnets such as neodymium magnets within the CB, as shown in Fig. 2.26(a) [8–10]. Magnetic force applied on the electric arc helps to pull the arc away from the contacts as illustrated in Fig 2.26(b), and reduce the arc extinguishing time. Figure 2.26(c) further illustrates the Lorentz force acting on the electric arc, with two permanent magnets positioned near the arc.

The arc is driven into the splitter plates in the arc chamber by the Lorentz force. Figure 2.27 illustrates how the tripping time varies with distance between magnet and electric contact points for a given current and voltage condition.

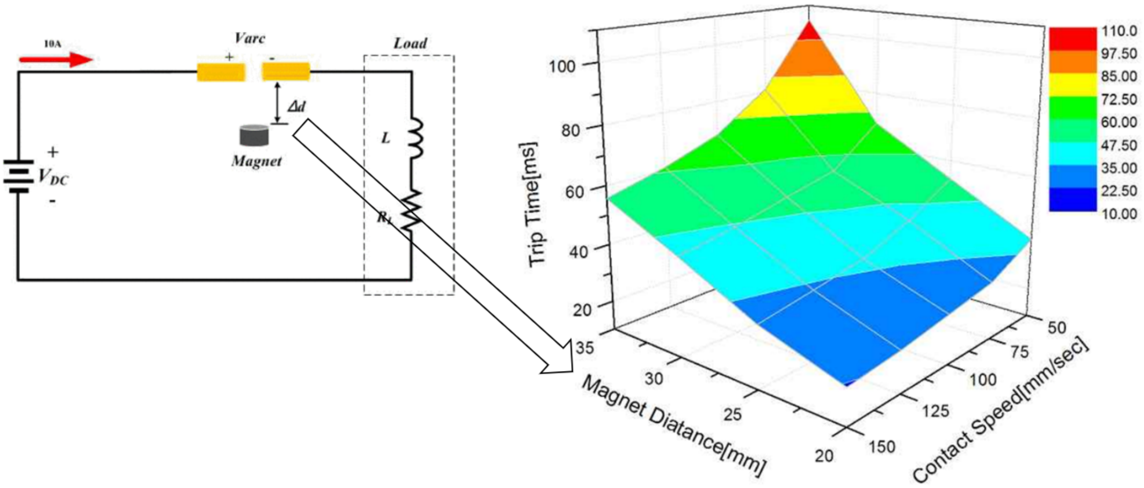


Figure 2.27: DC-breaking tripping times under externally applied magnetic force [8]

Tripping time decreased as the distance is reduced. However, reducing the distance below a certain value is not recommended, as the magnet may be damaged by the high arc current generated during the interruption of inductive loads [8].

2.4.4 Demonstration of Magnetic Field Effect on Arc Dynamics

Figure 2.28 illustrates the arc voltage and current characteristics under an externally applied magnetic field. A neodymium magnet is used for the test, with the distance between the magnet and the contact points adjusted manually to vary the applied magnetic field strength. Arc extinction time decreases as magnetic field strength increases.

The black, blue, and red oscillograms represent arc current waveforms, while the green, purple, and orange oscillograms represent arc voltage waveforms for the single-pole, two-pole, and three-pole cases, respectively. Arc interruption time decreases with increasing applied magnetic force. However, the peak arc voltage does not increase with magnetic force, unlike in the case of series-connected poles. Permanent magnet-based arc extinguishing is suitable for small sized DC breakers [8].

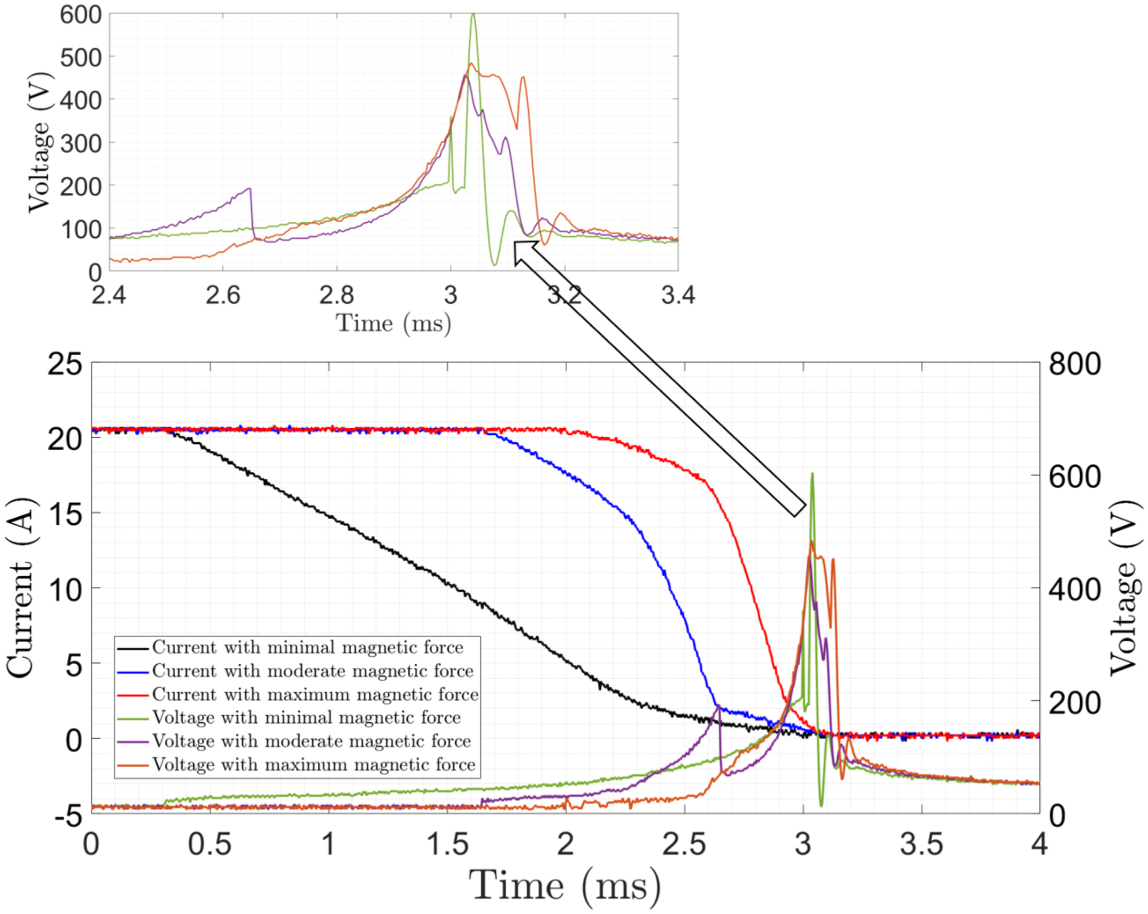


Figure 2.28: Arc extinguishing time decreases with externally applied magnetic force tested for a 2-A rated miniature circuit breaker.

2.5 Conclusion for the Chapter 2

This chapter analysed the types of DC faults, common DCCB configurations, and the processes of electric arcing and contact degradation based on preliminary experimental results. Two commercially available DCCB techniques were described and evaluated based on experimental results. The most straightforward contact protection technique, which uses a commutation path, will be presented and analysed in detail in the following chapter, based on preliminary experimental results from implementations using both passive and active components.

Chapter 3

Introducing a Commutation Path for the Fault Current

The formation of electric arcs and their consequences were discussed in the previous chapter. This section presents preliminary methods to reduce arc formation across the contacts using a commutation path, an additional current path typically connected in parallel with the CB, as briefly described in Section 2.3. The occurrence of the arc depends on the impedance of the commutation path. Impedance should be high in the steady state condition before the CB opens, and should be low during the transient condition as the CB opens to support arc extinguishing. Commutation path may include passive components such as inductors, capacitors, diodes, MOVs, and active components such as thyristors, MOSFETs and IGBTs. There are numerous ways to configure the commutation path. This chapter describes some of the simplest techniques, supported by preliminary experimental results.

3.1 Commutation Circuit Analysis with Passive Components

A commutation path can be implemented in different locations as shown in Fig. 3.1. During an overload fault, the commutation path may be connected across terminals ab, ac, or both. Under a short-circuit fault across the load R_{L}, connection is limited to ab as points b and c are effectively short-circuited.

The behaviour of the commutation path with passive components MOV, diode and capacitor is analysed in subsections 3.1.1.1, 3.1.2 and 3.1.3.1 respectively. In each case, the commutation component is connected in parallel with the CB across points a and b. The configuration with the commutation path between points a and c is discussed in subsection 3.2.2.

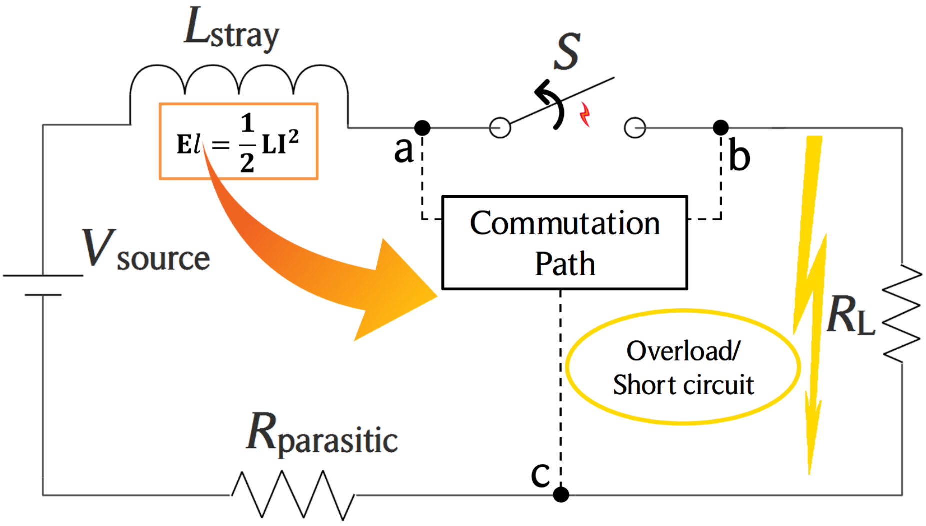


Figure 3.1: Possible locations (across terminals *ab* and *ac*) for a commutation path to assist arc extinction

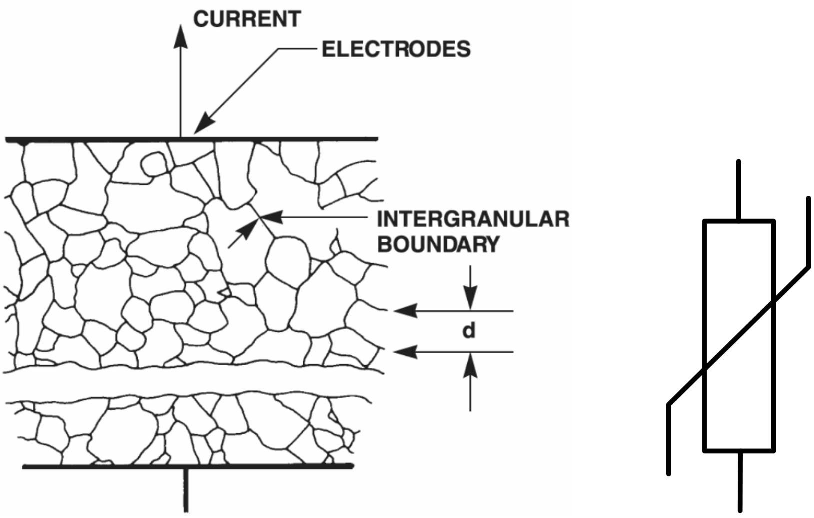
3.1.1 Metal Oxide Varistors

Metal oxide varistor (MOV) is a voltage dependent nonlinear resistor which is commonly used as a limited energy absorber in which energy is dissipated as heat.

MOVs are manufactured in disc, block, radial and axial shapes, as shown in Table 3.1. Surface-mounted variants are also commercially available [94].

Table 3.1: Metal oxide varistor shapes [95]

MOV type	**Image**
Disc	
Block	
Radial leaded	
Axial leaded	



(a) (b)

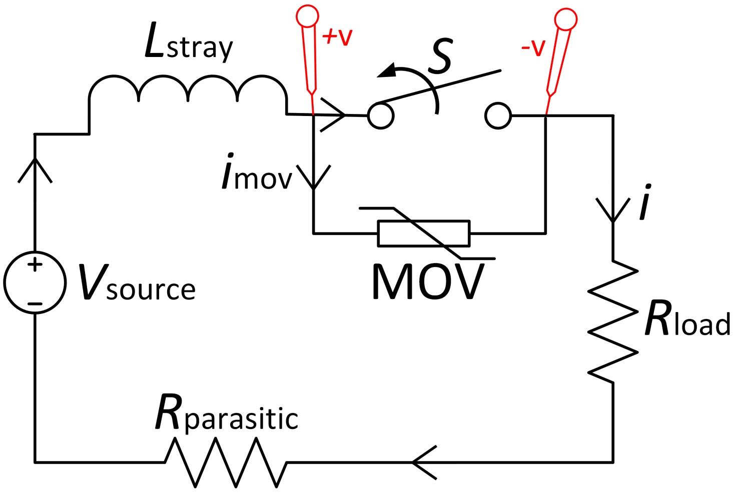
Figure 3.2: Metal oxide varistor: (a) cross-sectional view; (b) circuit symbol [96]

MOVs consist of two metal electrodes encapsulating a matrix of conductive zinc-oxide (ZnO) or other metal oxide grains, as illustrated in Fig. 3.2(a). The grains are separated by boundaries that exhibit p–n junction semiconductor characteristics, resulting in highly nonlinear voltage–current behaviour. Resulting from p–n junction characteristics, each inter-granular boundary has a defined voltage barrier. The collective effect of these barriers is referred to as the MOV breakdown voltage [97, 98].

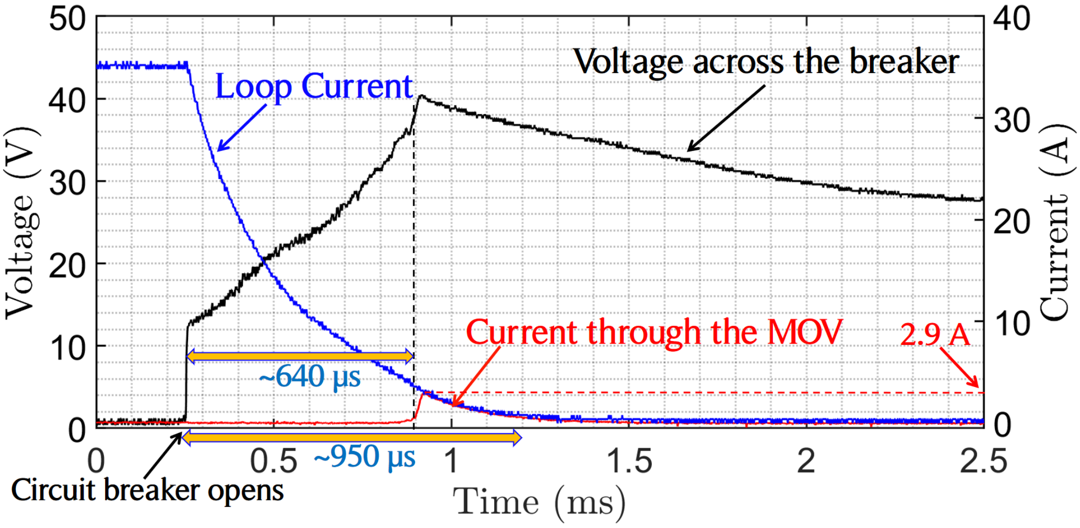
Under normal operating conditions, when the applied voltage is below breakdown threshold, the MOV exhibits high impedance and behaves nearly as an open circuit. During high-voltage transients, it rapidly switches to a low-impedance state, conducting substantial current while clamping the voltage to a safe level. However, each time the device fires, the absorbed energy produces localised heating within the MOV material, primarily across the ZnO grains and grain boundaries. Repeated thermal stress degrades these boundary regions, weakening the insulation. Consequently, the MOV undergoes gradual material deterioration, causing the clamp voltage to decrease progressively [39,99].

3.1.1.1 Commutation Path Using an MOV

This subsection presents experimental results for an MOV used as the commutation device. The test configuration consists of a 25-V DC source, 0.5-Ω load, 660-μH line inductance, and a B72214S0170K101 MOV (manufactured by TDK) connected parallel to a 10-A rated MCB. Figure 3.3(a) shows the corresponding circuit diagram with the MOV connected to the commutation path; voltage probes are indicated in red. Figure 3.3(b) presents three oscillograms: the blue, red, and black traces represent the DC loop current i, MOV current i_{mov}, and arc voltage, respectively. The DC loop current (blue trace) commutates to the MOV branch (red trace) following a 640-μs delay after CB opening. The MOV triggers when the arc voltage reaches approximately 37 V. Experimental results



(a)



(b)

Figure 3.3: Current commutation with an MOV: (a) circuit diagram; (b) characteristic waveforms

demonstrate that this method enables the MOV to absorb only a small amount of the arc current. Although the MOV current can be increased by using a MOV with a lower breakdown voltage, the breakdown voltage must still exceed the source voltage; otherwise, the MOV will conduct continuously and be destroyed.

3.1.2 Diodes

A diode is a p–n junction that exhibits nonlinear resistive behaviour depending on the applied voltage. Common types include rectifier diodes, Zener diodes, Schottky diodes, light-emitting diodes, photodiodes, fast-recovery diodes, and transient voltage suppressor (TVS) diodes. Although Zener diodes are specifically designed for reverse-biased operation, this investigation considers rectifier and fast-recovery diodes under reverse-bias conditions. These devices were subjected to high-voltage reverse pulses to examine their reverse energy absorption characteristics and breakdown behaviour. This evaluation assesses their suitability for arc absorption applications. A lightning surge simulator (LSS-6230) was used in this experiment—detailed in Appendix E—to apply consecutive artificial surges of 1.2/50 μs, conforming to IEEE standard, in the reverse direction. The results are summarised in Table 3.2.

Table 3.2: Reverse-biased performance of diodes

Diode type	**Maximum reverse voltage as per data sheet (V)**	**Voltage level causing damage during testing (V)**	**Reverse conduction capability**
Rectifier diodes: 1N4001, 1N4002... to 1N4007	50, 100... to 1000	1800	negligible (until applied voltage >1800 V)
Fast recovery diode: MUR410G	100	400	high (for applied voltage $\geq$ 300 V)
Fast recovery diodes: MUR220G, MUR420G	200	400	high (for applied voltage $\geq$ 300 V)

The tested rectifier diodes exhibit high reverse-voltage withstand capability, but their reverse conduction performance is poor. Column 4 of Table 3.2 indicates that reverse pulses of 300 V can readily pass through the tested fast-recovery diodes for a short duration. Figure 3.4 illustrates the voltage and current across the MUR410G diode when

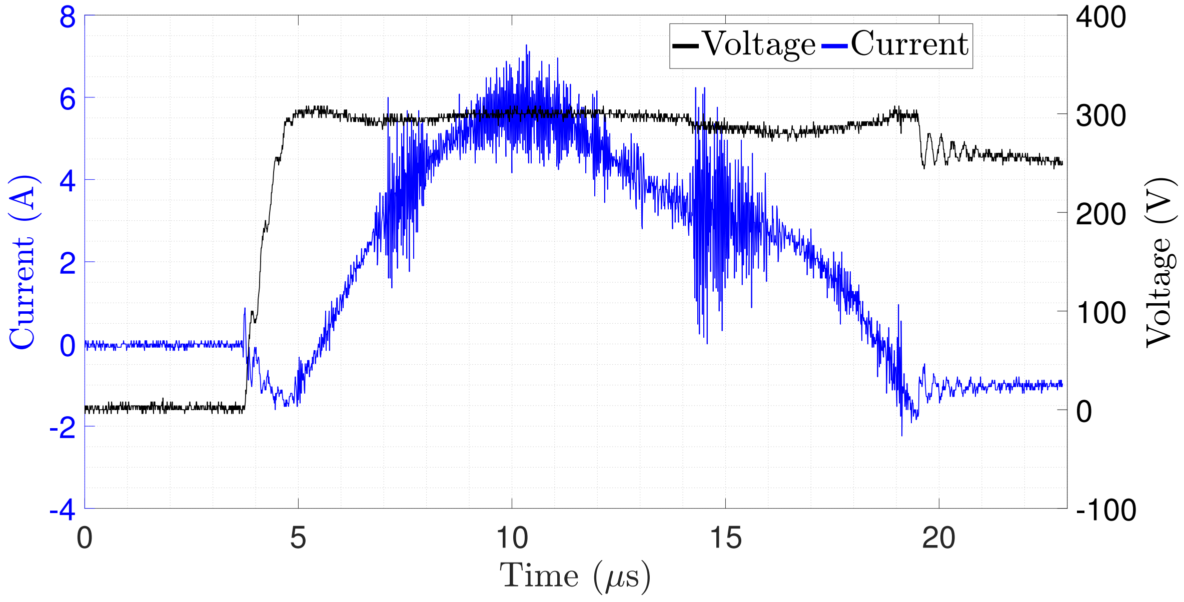


Figure 3.4: Reverse-biased characteristics of the fast-recovery diode MUR410G

subjected to a 300-V reverse-voltage pulse. This experiment applied 400 consecutive surges; the diode remained operational after 400 successive surges.

These results indicate that fast-recovery diodes can replace MOVs in the commutation path for limited energy absorption in low-power DC systems, provided the diode's joule rating is sufficient. However, further testing is required to confirm the suitability of reverse-biased diodes for arc absorption.

In addition to the diode types discussed, TVS diodes are well suited for arc absorption. A TVS diode is a Zener-based device optimised for fast response times typically in the picosecond to nanosecond range. It remains non-conductive under normal operating conditions and clamps transient over-voltages when the reverse voltage exceeds its breakdown voltage. An experimental case of arc absorption using TVS diodes will be presented in Section 3.2.2.

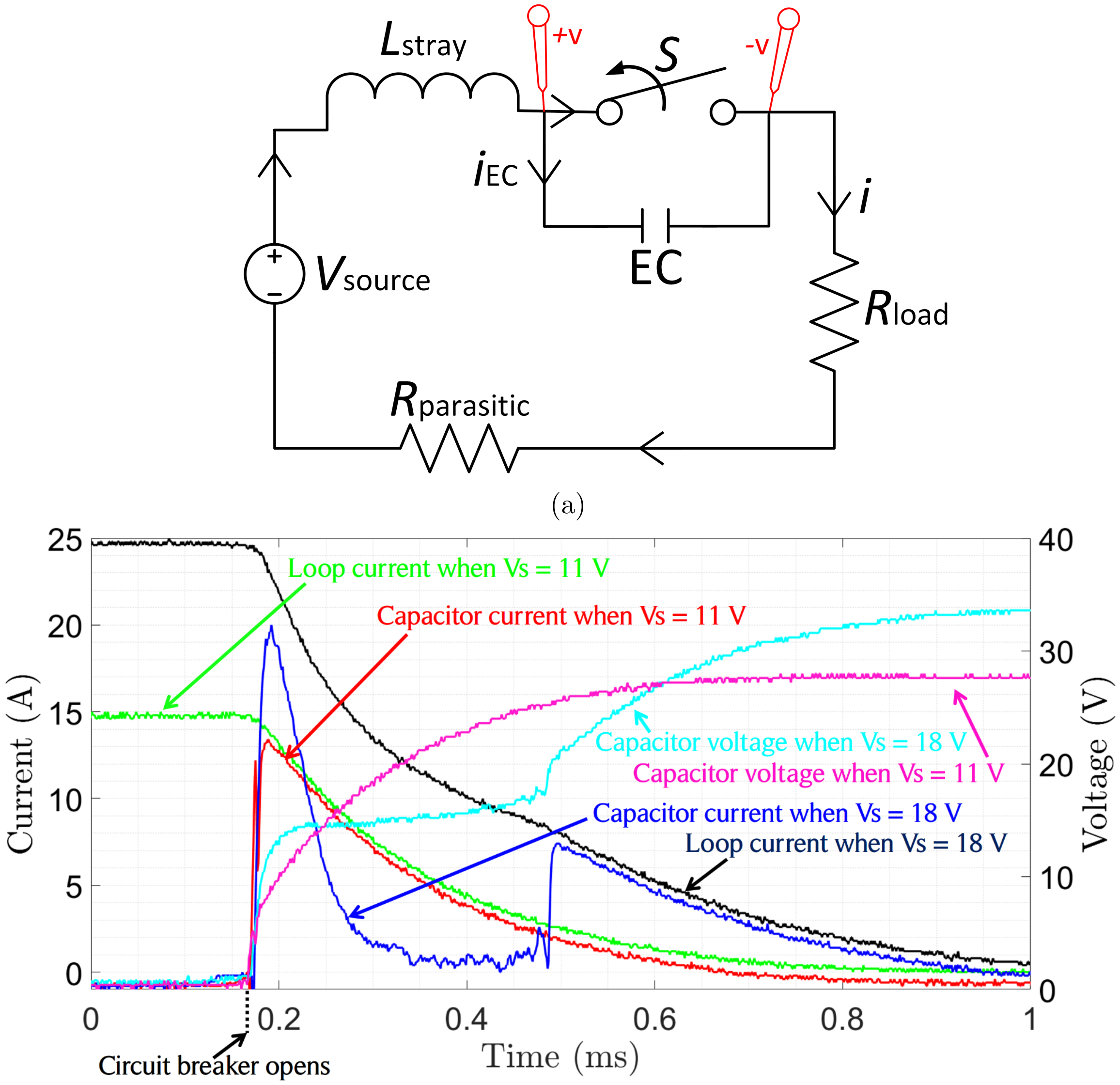
3.1.3 Capacitors and Supercapacitors

A capacitor is an electrostatic-based energy storage device whose stored energy $\frac{1}{2}CV^2$, is typically much lower than that of electrochemical batteries of comparable volume. Various types of capacitors, including electrolytic capacitors (EC), ceramic capacitors, and film capacitors, are available, offering high DC voltage ratings despite their lower energy rating due to microfarad-range capacitance. Supercapacitors (SC) are a special type of capacitor with capacitance values up to a million times higher than those of conventional capacitors for a given canister size. A detailed description of SCs will be provided in Chapter 4.

3.1.3.1 Commutation Path Using a Capacitor

To observe the current commutation behaviour, a 100-μF, 63-V EC was connected in parallel with the CB. The resulting voltage and current waveforms, together with the corresponding circuit diagram, recorded at source voltages of 11 V and 18 V, are shown in Fig. 3.5. The line inductance was maintained at 660 μH.

When the source voltage is 11 V and the loop current is 15 A, the red, green, and purple traces represent the capacitor current, loop current, and voltage across the EC, respectively. The EC absorbed the total current (red trace) from the contact pair during circuit opening. However, when the source voltage was increased to 18 V with a loop current of 25 A, the EC initially diverted 20 A (blue trace), with 5 A flowing through the arc. The capacitor current then progressively decreased relative to the loop current (black trace). When the second peak occurs in the EC current in blue trace, entire loop current is transferred into the EC with the arc in the contact pair diminishing. The EC cannot absorb all the energy stored in the line inductance during the circuit-breaking period at the loop current of 25 A; consequently, some energy is dissipated as an electric arc.



(a)

(b)

Figure 3.5: Current absorption capability of a 100-μF, 63-V EC at source voltages of 11 V and 18 V. (a) Circuit diagram, (b) corresponding waveforms.

Another experiment was conducted to compare the current commutation performance of SCs and ECs, with Fig. 3.6 comparing the performance of a 500-F, 3-V SC and a 100-μF, 63-V EC. The source voltage was set to 32 V.

The top traces show oscilloscope recordings from the experiment with the EC, and the bottom traces show those from the SC test. Both the EC and SC were used separately as commutation elements, connected in parallel with the CB in distinct experiments, with the loop current maintained at approximately 45 A.

When the EC is used, a sudden initial current of 18 A is absorbed from the EC, after which the current abruptly collapses and the remainder flows as the arc. Because the arc resistance is lower than the EC's ESR, current continues to flow through the arc. In the

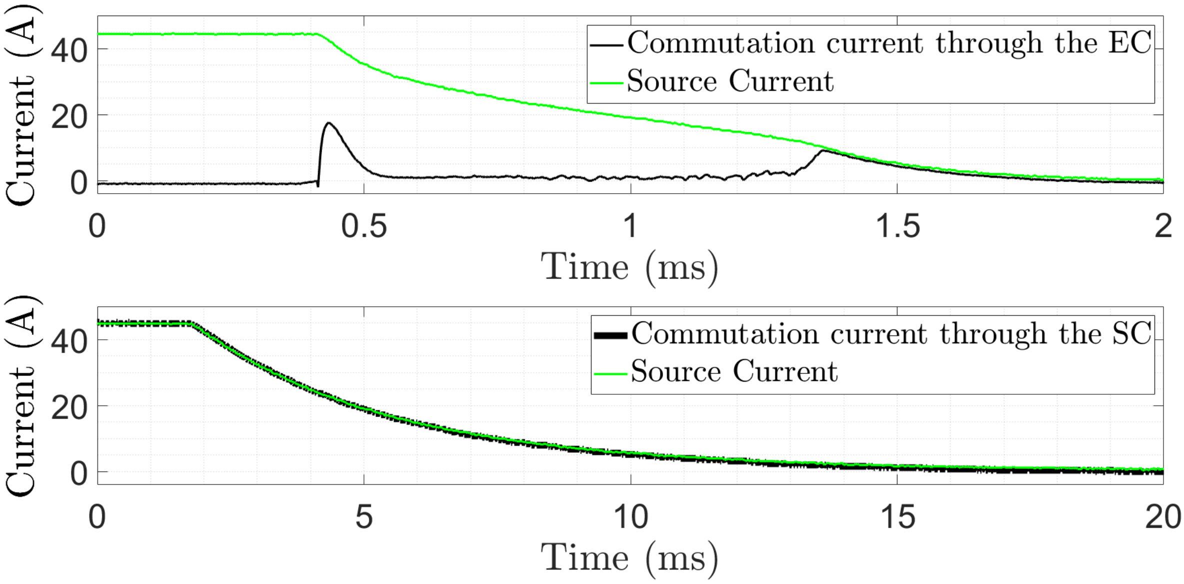


Figure 3.6: Current absorption performance comparison between a 500-F, 3-V SC (lower plot) and a 100-μF, 63-V EC (upper plot)

final stage (after 1.3 ms), as the arc resistance exceeds the EC's ESR, current is again absorbed by the EC.

When the SC is used, nearly the entire current flows through it under both steady-state and transient conditions, due to its very low ESR (3.2 mΩ) compared to the on-resistance of the CB (28 mΩ). As a result, the waveforms overlap closely in the lower trace. This indicates that the SC effectively diverts current from the contact pair, limiting arc formation. However, SCs have a key limitation: their low voltage ratings. Consequently, a SC cannot be directly connected in parallel with the CB, as it would be exposed to the source voltage and likely fail. The comparison in Fig. 3.6 illustrates the SC's superior current-handling capability during transients compared to the EC.

This subsection has discussed the use of a MOV, a diode, and a capacitor connected in parallel with the CB. In addition to passive components, active devices such as MOSFETs and IGBTs can also be used in the commutation path; their application will be addressed in Section 3.3.

3.2 Commutation Current Enhancing Techniques

This section presents three techniques for improving current commutation performance, based on experimental results.

3.2.1 Multiple Pole-based Current Commutation

Section 2.4 has described how the arc voltage rises rapidly with the addition of series-connected poles, contributing to reduced arc extinguishing time. This subsection examines

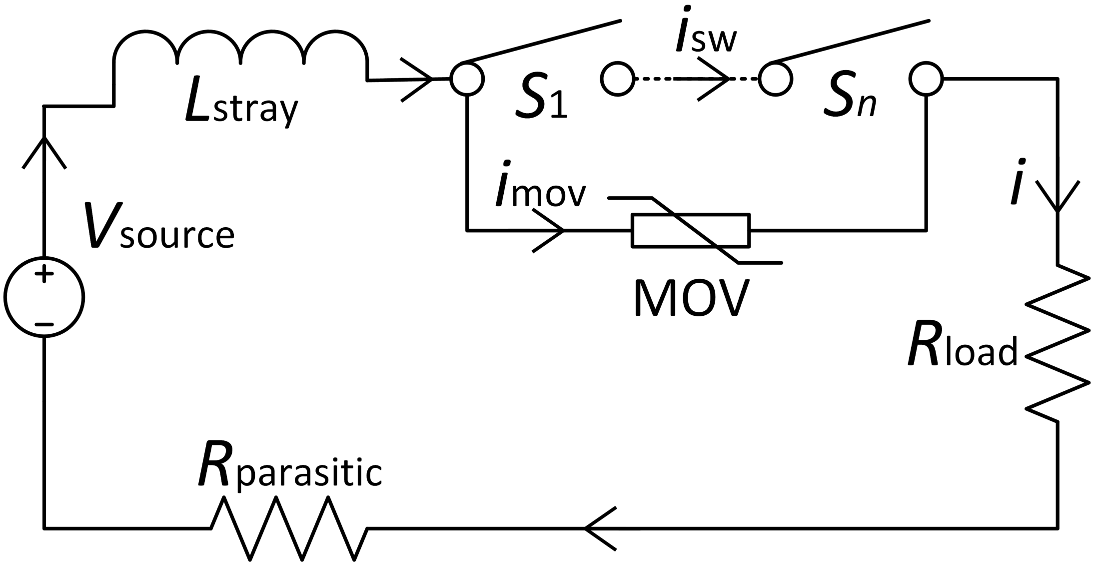


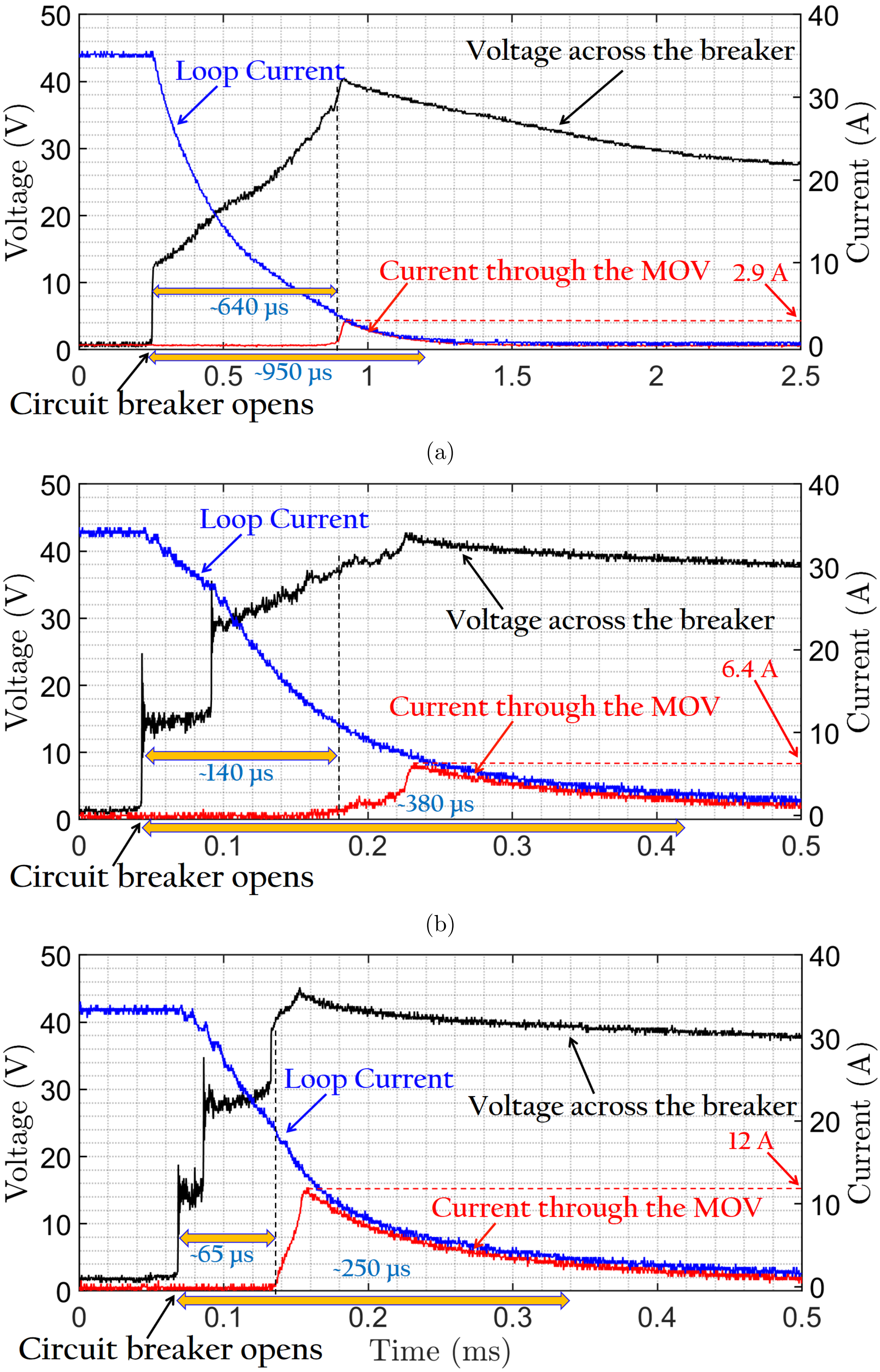
Figure 3.7: Current through the MOV increases with the number of poles connected in series.

the effect of such poles on the commutation current, based on experimental results. Figure 3.7 illustrates a simple DC circuit in which the total loop current is shared between the switches and the MOV, denoted by i_{sw} and i_{mov}, respectively.

If i_{mov} is increased, the arc current, i_{sw} can be reduced. The experiment was conducted using MOV B72214S0170K101. The source voltage, total loop current, stray inductance, and load resistance were maintained at the same levels as in the experiments described in subsection 3.1.1.1. Experimental results shown in Figure 3.8 (a), (b), and (c) correspond to single-pole, two-poles, and three-poles configurations, respectively. The waveforms demonstrate that increasing the number of poles diverts more arc current to the MOV path. The MOV triggers when the arc voltage reaches approximately 37 V, within 640 μs, 140 μs and 65 μs for the single-pole, two-poles and three-poles cases, respectively.

The peak current through the MOV in the single-pole configuration was 2.9 A and increased by 120% in the two-pole configuration and by 314% in the three-pole configuration.

The next technique, presented in Section 3.2.2, enhances the commutation current by relocating the commutation path from the conventional position in parallel with the CB to an alternative configuration, as described in Section 3.1.



(a)

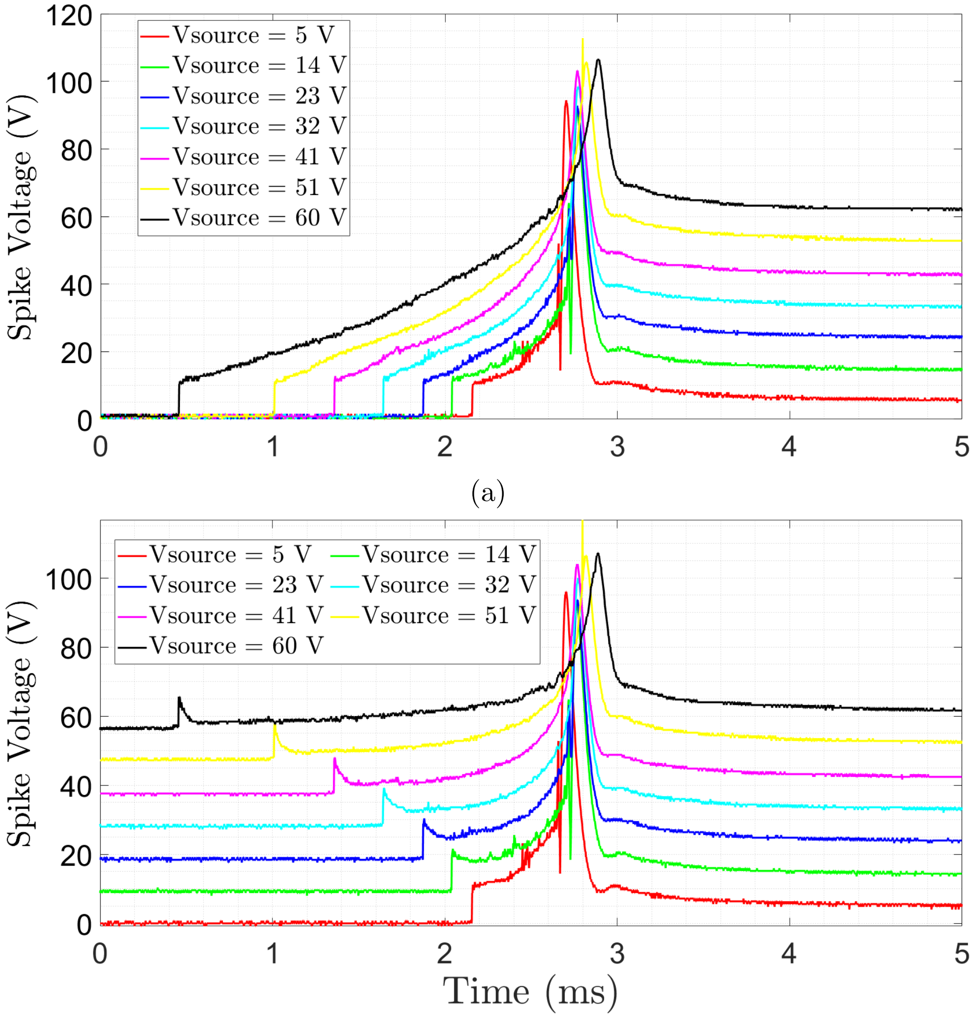
(b)

(c)

Figure 3.8: The MOV current (red trace) increases with the number of poles connected in series: (a) single-pole, (b) two-poles, (c) three-poles.

3.2.2 Optimal Placement of the Commutation Circuit

This subsection compares the transient voltage rise across *ab* and *ac* (shown in the circuit in Fig. 3.1) and demonstrates how relocating the commutation path affects the commutation current. The transient voltages across terminals *ab* and *ac* are illustrated in Fig. 3.9, where no commutation device is connected across either *ab* or *ac*. The experiment was conducted using incremental source voltage steps, based on a fixed loop current of 20 A.



(a)

(b)

Figure 3.9: Transient voltages across (a) *ab* (b) *ac* during circuit breaker opening

Figure 3.9(a) shows the voltage across the contact pair, which exhibits a transient waveform starting with a sudden rise of 13 V and peaking above the DC source voltage, regardless of the source voltage level.

Figure 3.9(b) shows the transient voltage across *a* and *c* is initially higher compared to the previous configuration. This demonstrates that a nonlinear device like a MOV/TVS-diode can be easily triggered when it is placed across *a* and *c* compared to across *a* and *b*. An example case using a TVS diode in the two different locations is presented in Fig. 3.10.

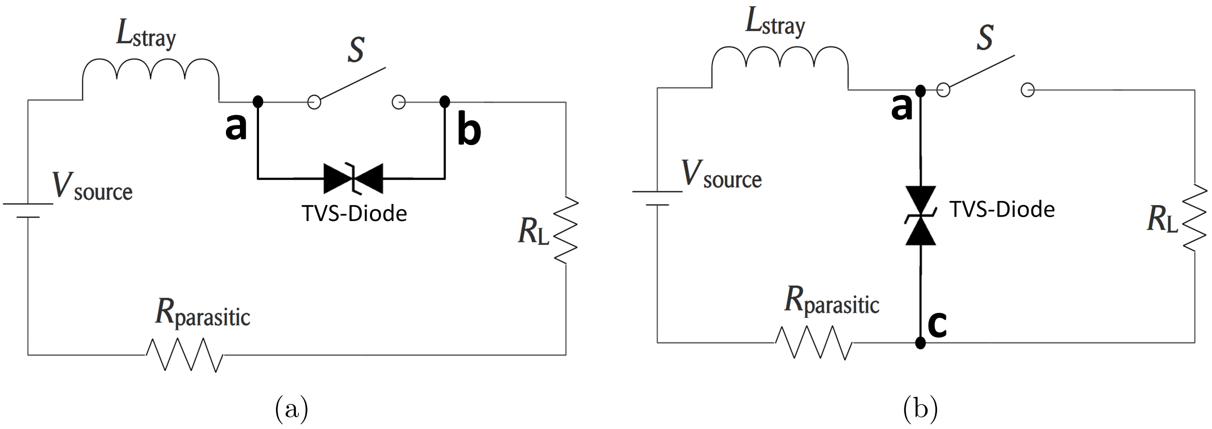


Figure 3.10: A TVS diode is connected across (a) *ab*, and (b) *ac* to compare the commutation current.

The TVS diode starts conducting when the voltage across it reaches its breakdown voltage. When connected across *ac*, as illustrated in Fig. 3.10(b), the transient voltage across the diode remains higher during the arcing period, enabling faster triggering compared to the configuration in Fig. 3.10(a).

Figure 3.11 shows two waveforms obtained using the TVS diode 1.5KE24CA for the circuits in Fig. 3.10 with a DC source voltage of 22 V and a loop current of 14.6 A. The diode current between a and c (black trace) exceeds that between a and b (blue trace) due to the higher voltage appearing across a and c.

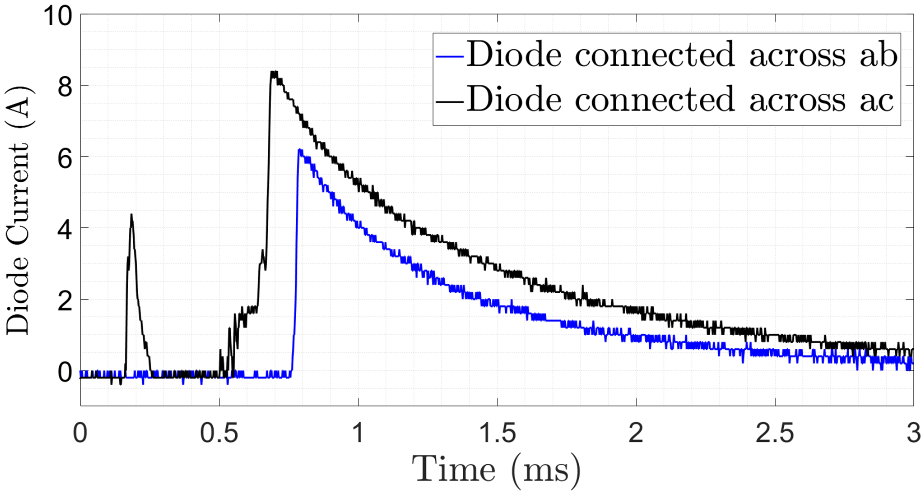


Figure 3.11: TVS-diode current increases when it is connected across a and c, compared to between a and b.

The third technique for increasing the commutation current using a parallel capacitor will be discussed in the following subsection.

3.2.3 Current Commutation with a Parallel Capacitor

In this subsection, a MOV is used as the commutation device, with an EC connected in parallel to increase the current through the MOV, as illustrated in Fig. 3.12.

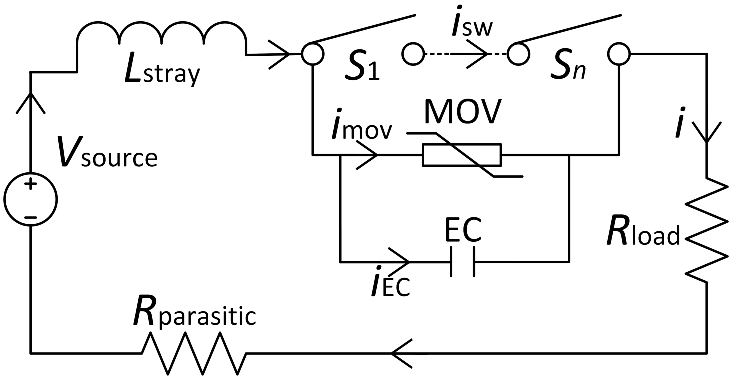
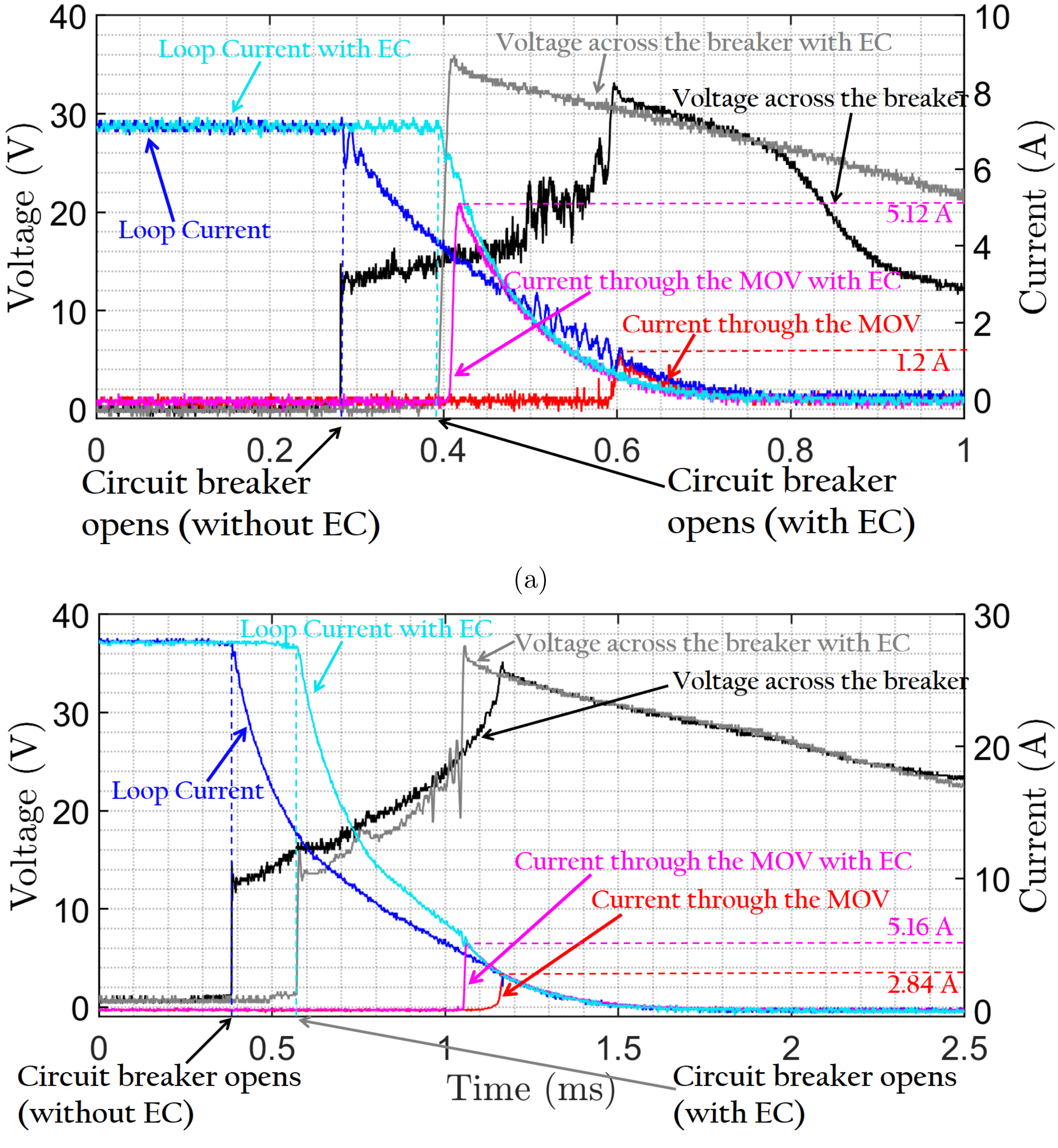


Figure 3.12: An EC is connected in parallel with the commutation path, which includes an MOV.



(a)

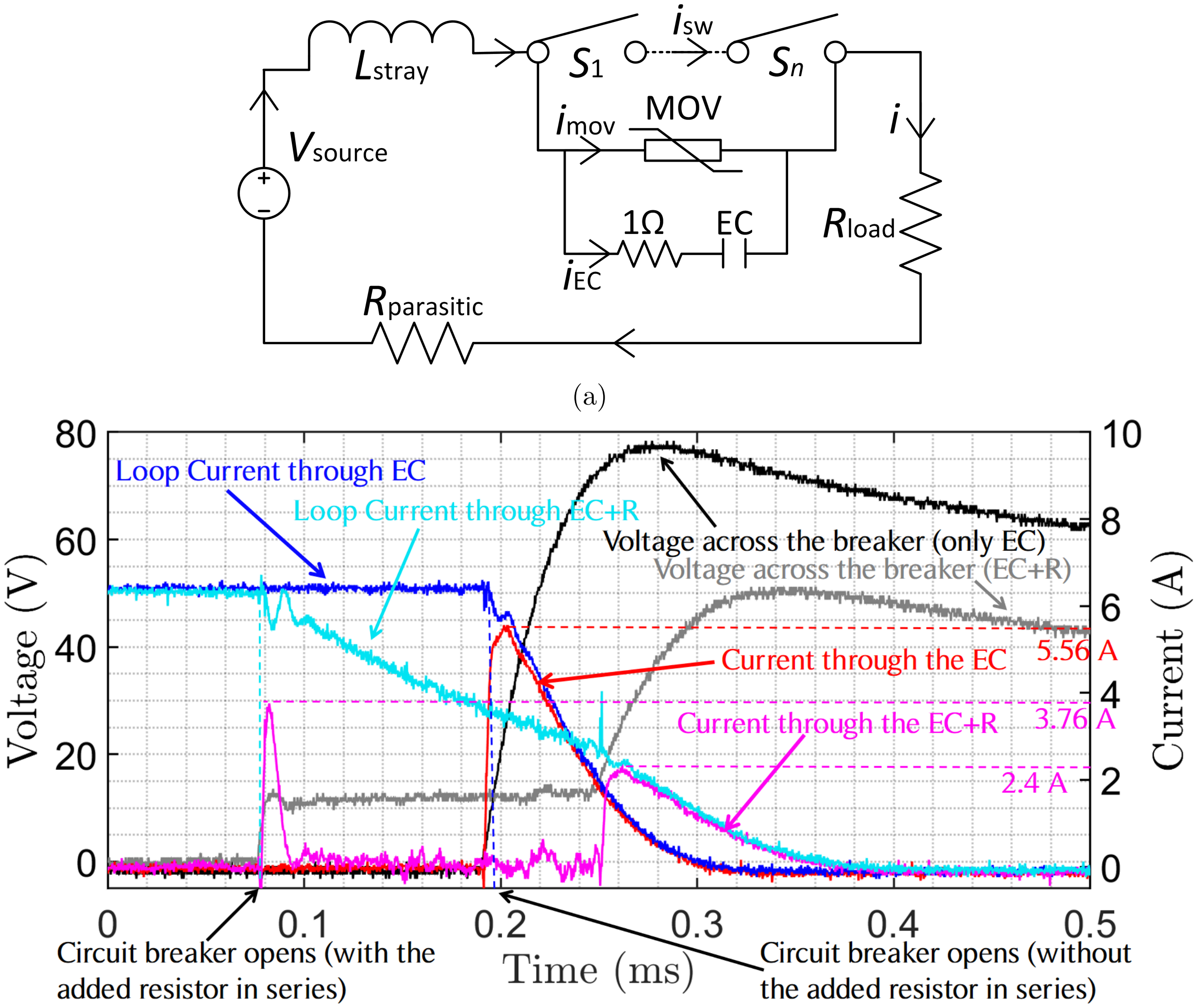
(b)

Figure 3.13: MOV commutation current increases with a parallel EC at source voltages of (a) 5 V and (b) 20 V.

Figure 3.13(a) shows the experimental results obtained with a source voltage of 5 V and a 2.2-μF, 63-V EC in parallel with the MOV. The peak MOV current increases by 326%, with the red trace representing the case without the EC and the purple trace the case with the EC. The MOV (B72214S0140K101) triggers when the arc voltage reaches approximately 35 V. The same experiment was repeated at a source voltage of 20 V and higher loop current, as shown in Fig. 3.13(b), where the peak MOV current increased by only 82%.

The MOV triggers rapidly when the arc voltage rises quickly. The current drawn by the EC increases the initial voltage across the MOV, facilitating faster MOV activation.

The aforementioned technique is effective only when the EC can rapidly absorb arc energy and develop a high voltage across its terminals. This behaviour depends critically on the capacitor's ESR. To investigate this dependence, a separate experiment was conducted with an additional resistor connected in series with the EC during current



(a)

(b)

Figure 3.14: Commutation current absorption performance with the ESR of the EC. (a) Circuit configuration, (b) Corresponding waveforms.

commutation, as illustrated in Fig. 3.14(a). The waveforms in Fig. 3.14(b) show that the series resistor limits the instantaneous current through the capacitor, thereby slowing the voltage build-up.

Figure 3.14(b) illustrates that the fault current was entirely absorbed by the 2.2-μF, 63-V EC, as shown by the red trace. However, arc absorption is discontinued when a 1-Ω resistor is connected in series with the capacitor, as indicated by the purple trace. Note that in this experiment, a 1-Ω resistor is connected in series with the EC to increase its effective ESR by adding to the EC's inherent resistance. This approach allows the same capacitor to be used in both high-ESR and low-ESR configurations.

Based on these preliminary results, this research work investigates the suitability of SCs in arc management, with initial observations presented from Chapter 4.

3.3 Commutation Circuit Analysis with Semiconductor Switches

This section analyses the use of semiconductor switches in the commutation path based on a novel hybrid DCCB topology designed and published by the author.

Semiconductor switch-based DCCBs are highly complex due to the requirement for auxiliary components such as DC power supplies and gate drivers. To address this, a simple, self-powered, self-controlled hybrid DCCB is proposed, in which the transistor acts as an instantaneous variable impedance. The commutation path, described previously, must exhibit high impedance before contact separation and low impedance once the contacts begin to open. Figure 3.15 shows experimental on-resistance data for three MOSFETs at varying gate-to-source voltages V_{gs}.

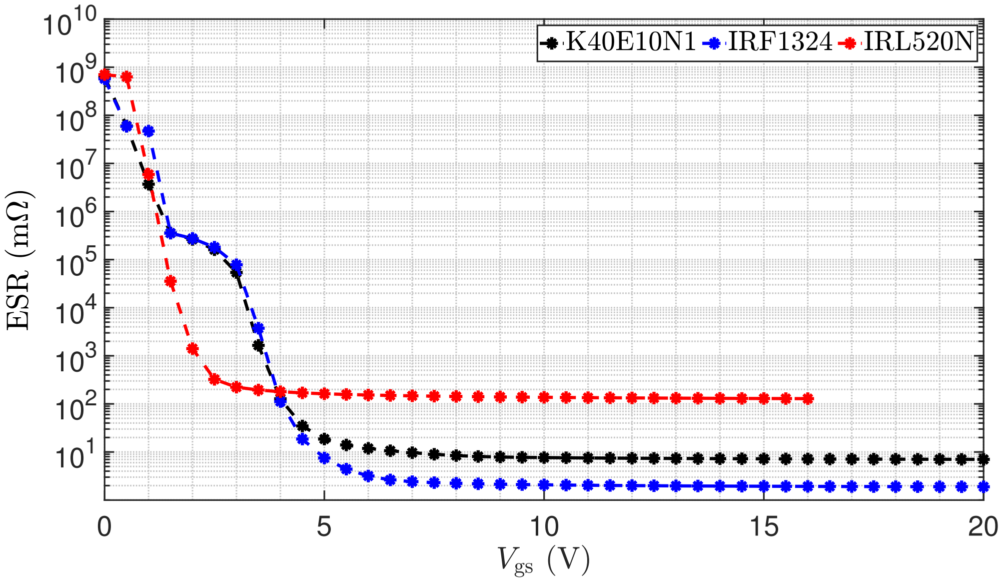


Figure 3.15: The MOSFET on-resistance decreases as the gate-to-source voltage increases.

The behaviour of any such transistor is similar: it functions as a nonlinear, gate-voltage-controlled resistor. This characteristic aligns precisely with the required properties of the commutation path. Based on this property, a new topology is proposed in which the MOSFET serves as the commutation device, as described in the following subsection.

3.3.1 Self-powered and Self-controlled Hybrid DCCB Topology

The proposed circuit is illustrated in Fig. 3.16. Usually, an additional control circuit and a DC power supply are required to activate the solid-state switches in hybrid DCCBs. However, the proposed topology utilises a simple passive controller circuit that makes use of the initial arc voltage generated during circuit opening. A TVS diode is used to absorb the residual energy stored in the line inductance.

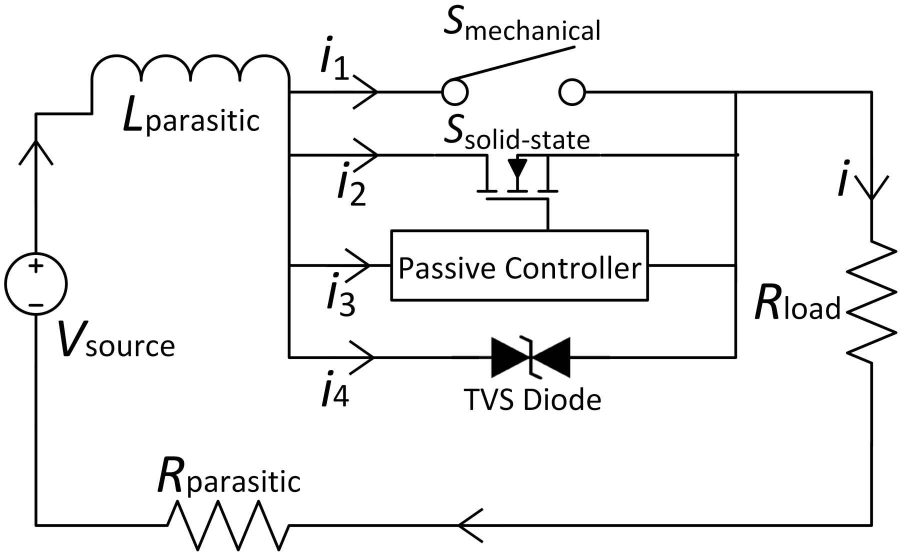


Figure 3.16: The proposed technique enables the passive controller to drive the solid-state switch.

3.3.1.1 Passive Controller Circuit

The passive controller circuit comprises only simple passive components: a toroidal transformer, capacitors, diodes, and resistors. The complete circuit diagram is shown in Fig. 3.17.

A small toroidal transformer is used with self-inductance values of L_1 and L_2 in its primary and secondary windings respectively. An EC, C_1, is placed in series with the primary winding to block the steady-state current. The list of components used is summarised in Table 3.3.

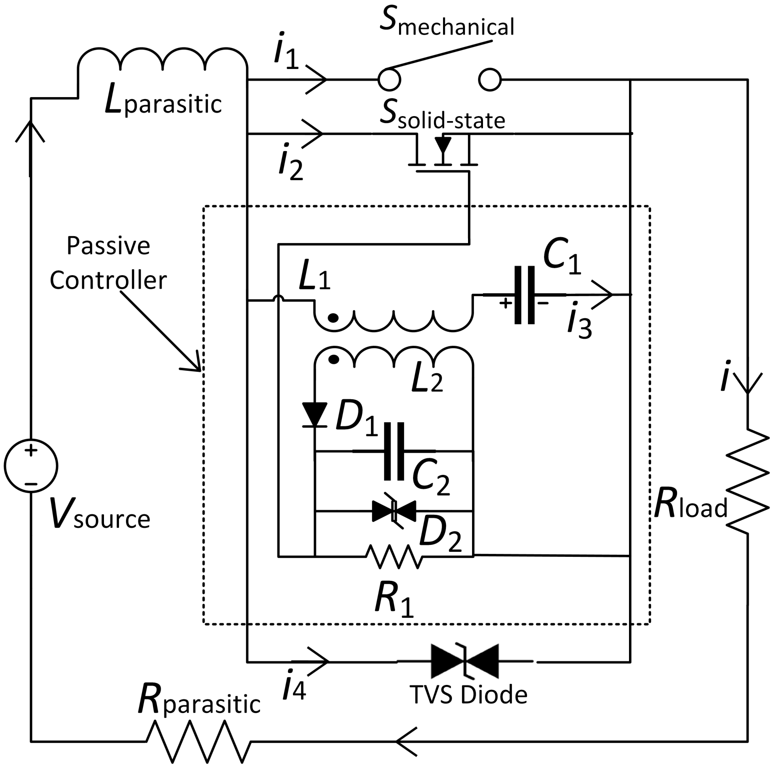


Figure 3.17: The passive controller circuit activates during circuit opening, commutating the current from the mechanical switch to the solid-state switch, and then turns off the solid-state switch autonomously.

The circuit operates when the mechanical switch, $S_{\text{mechanical}}$, opens during a fault condition. For the experimental prototype, a 6-kW DC power supply was used, with a source voltage of 60 V and a loop current of approximately 100 A achieved by adjusting the load, R_{load} with parasitic inductance of the loop of 660 μH. Two waveforms in Fig. 3.18 show the arc-voltage and arc-current characteristics during tripping for a ~100-A fault current, using a commercial AC MCB (6-A rated, Schneider Electric). The current decreases to zero within 3.25 ms, accompanied by a visible arc. The electric charge transferred during

Table 3.3: Components used in the passive controller

Component	**Sybmol**	**Model**	**Value**
Primary coil	L_1	-	310 μH
Secondary coil	L_2	-	2.1 mH
Electrolytic capacitor	C_1	-	100 μF, 63 V
Rectifier diode	D_1	1N4007	-
Electrolytic capacitor	C_2	-	4.4 μF, 50V
TVS diode	D_2	1.5KE56CA	-
Resistor	R_1	-	41 Ω

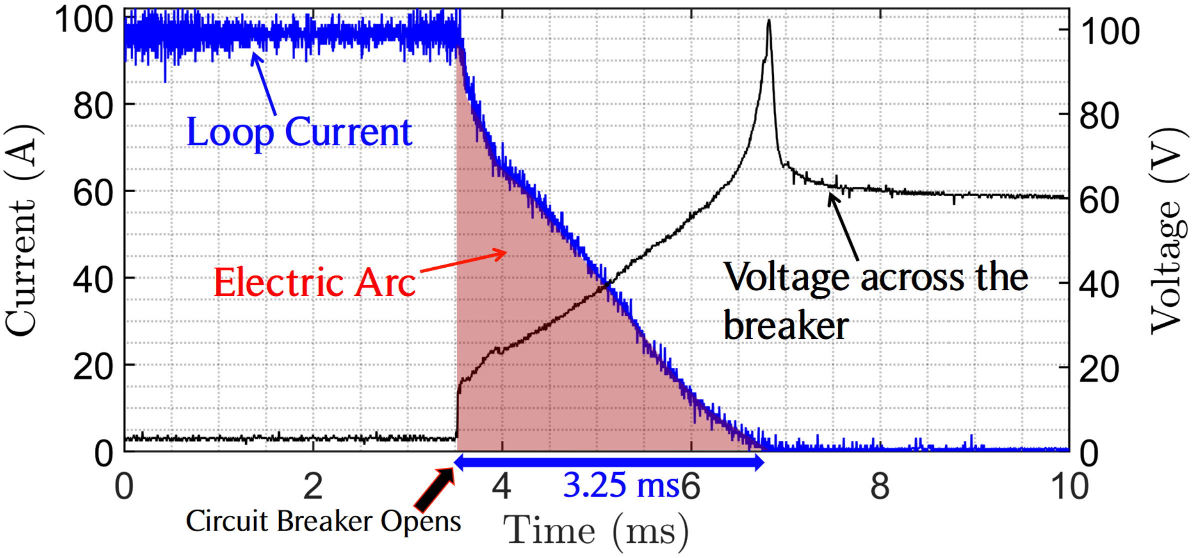


Figure 3.18: Interruption of a 100-A fault current using a commercial AC miniature circuit breaker

the arc event is highlighted in red in Fig. 3.18. Experimental results for the proposed technique are shown in Fig. 3.19 where the fault current is interrupted within 2 ms (blue trace).

For the experiment, four IRFB3206PbF MOSFETs were connected in parallel to increase the current rating of the solid-state path. The initial arc voltage during breaker opening is conditioned by the passive controller, and the resulting signal is used to drive the MOSFETs. The conditioned gate-to-source voltage, V_{gs} (red trace) rises to 13 V, then suddenly drops to nearly 6 V, decreases gradually, and finally falls to zero. The fault current (blue trace) is naturally transferred to the MOSFETs path (green trace) with negligible arc. The electric arc is significantly reduced, and the fault extinguishing time is reduced by approximately 40% in the hybrid topology compared to the traditional AC

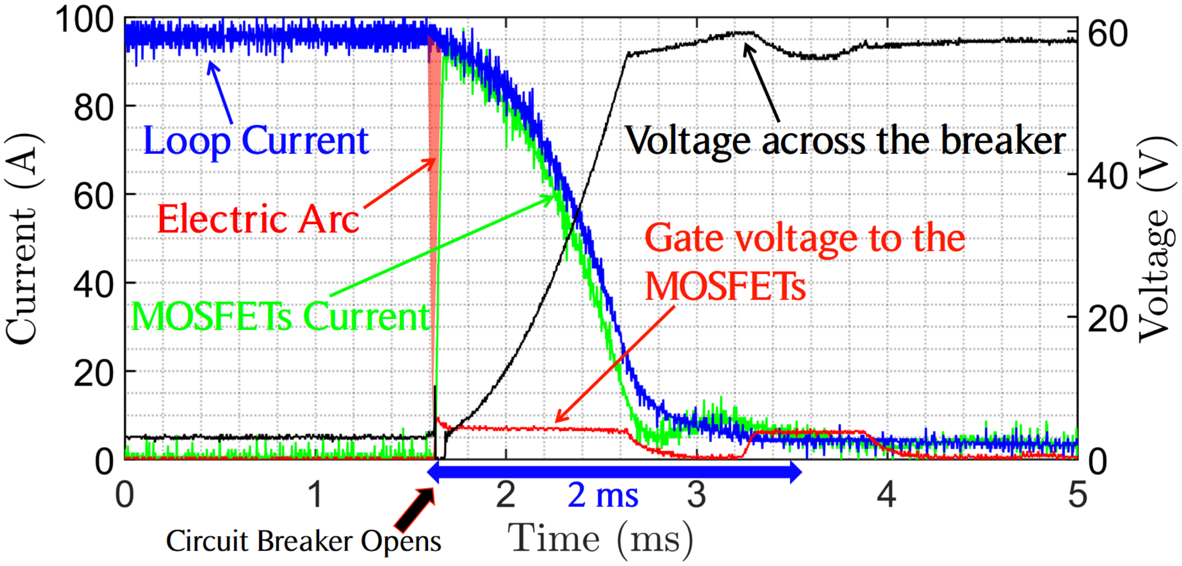


Figure 3.19: Interruption of a 100-A fault current using the novel hybrid topology

breaker. The TVS diode limits the transient voltage spike (black trace) generated when the MOSFETs are turned off and protects them from damage. The experimental setup is shown in Fig. 3.20. The 100-A fault current was interrupted within 2 ms using the proposed technique, whereas the conventional approach required 3.25 ms.

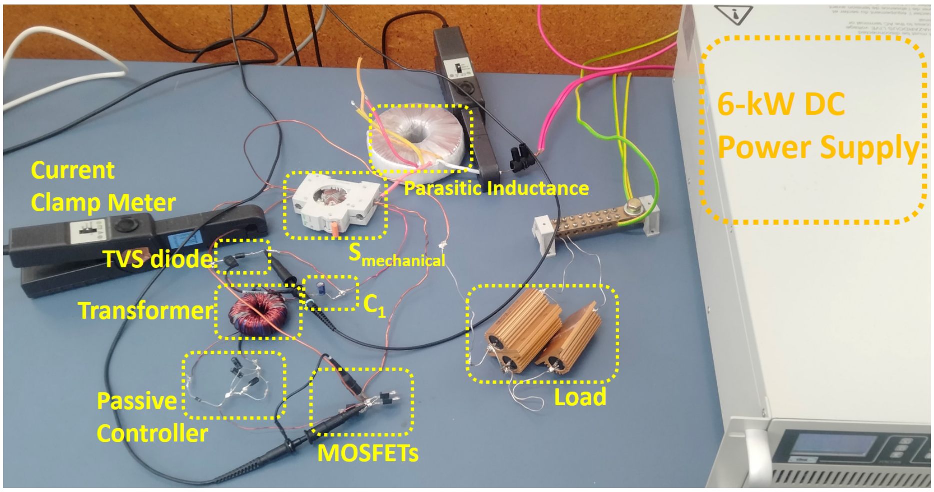


Figure 3.20: Experimental setup of the proposed hybrid DCCB

3.4 Conclusion for the Chapter 3

This chapter presented a commutation path using simple passive components (MOV, diode, and capacitor) and an active component (MOSFET) to assist in arc extinction during DC circuit breaking. Three techniques for enhancing the commutation current were also presented, based on experimental results. In Section 3.1.3, the SC is briefly introduced to this research, with a detailed discussion provided in the following chapter.

Chapter 4

Introducing Supercapacitors for DC Circuit Breaking

4.1 Supercapacitor Technology

Electrochemical double-layer capacitors (EDLC), commonly referred to as supercapacitors (SC) or ultracapacitors represent a relatively recent class of capacitors that have been available commercially since the late 1980s [100]. SCs have comparatively higher energy storage capability with one million times of capacitance compared to electrolytic or other conventional capacitor types for similar canister size. Figure 4.1 shows that a small SC canister (5 F/3 V) has three times of energy storage capability (22.5 J) compared to a relatively high-voltage-rated EC (100 μF/400 V/8 J).

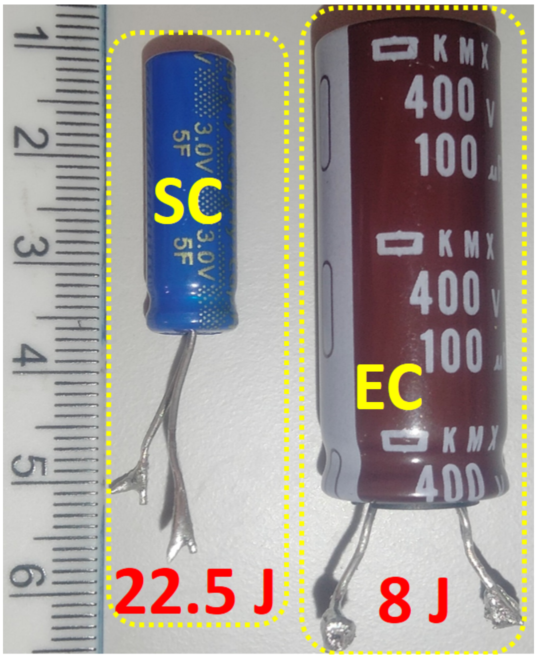


Figure 4.1: Canister size comparison between a low-voltage SC and a high-voltage EC

The other two special properties of SCs are their very low voltage rating (3 to 4 V per cell) and very low ESR. A comparison of ESR between SCs and ECs is shown in Fig. 4.2. The corresponding ESR values were obtained from the manufacturer, Würth Elektronik [101].

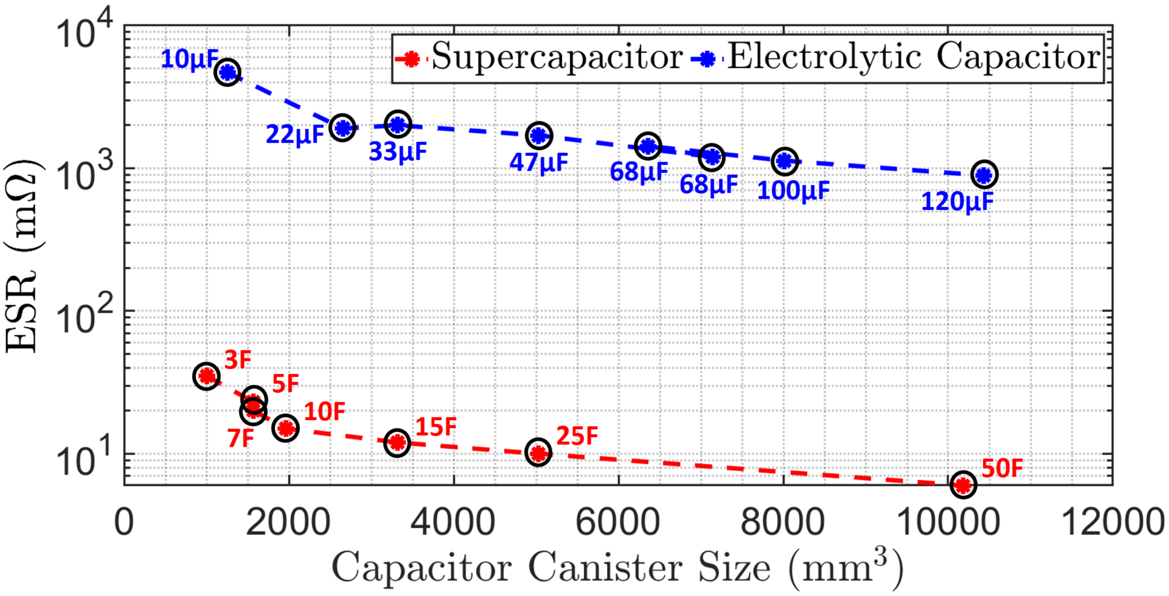


Figure 4.2: Electrolytic capacitors of the same canister size have approximately one to two orders higher ESR compared to supercapacitors [58].

Table 4.1 lists seven electrical properties: capacitance, rated DC voltage, ESR, joule rating, maximum power, short-circuit current, and canister size for selected commercial SCs from a single manufacturer. It shows that ESR decreases with increasing capacitance and volume.

Table 4.1: Supercapacitor information

C(F)	V(V)	ESR (mΩ)	E_C (J)	P_{max} (W)	I_s (A)	Size D×L(mm)
1	3	215	4.5	10	14	8×13
5	3	85	23	26	35	8×25
10	3	45	45	50	67	10×30
50	3	20	225	113	150	18×40
100	3	8	450	281	375	22×45
220	3	7.5	990	300	400	25×70
360	3	3.2	1620	703	938	35×62

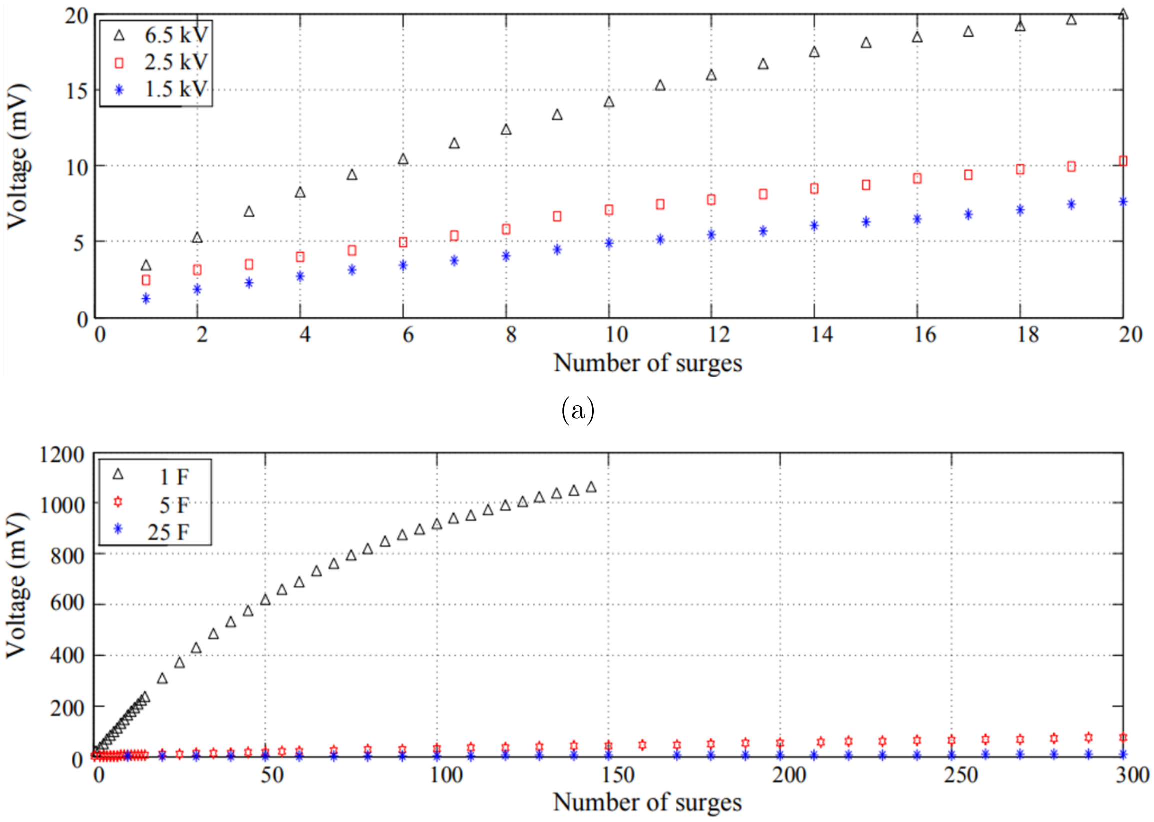
The maximum energy storable in a SC based on $\frac{1}{2}CV^2$ is given in column 4. Column 5 shows the maximum power delivery capability, $P_{\max}=\frac{V^2}{4*\mathrm{ESR}}$ [102] indicating that SCs are superior in short term power delivery compared to rechargeable batteries. Column 6 provides the short-circuit current, $I_\mathrm{s}=\frac{V}{\mathrm{ESR}}$, which demonstrates their high charge and discharge current capability. As shown in the table, larger SCs exhibit higher short-circuit current.

Given that the inductive energy in a DC loop is $\frac{1}{2}LI^2$, a SC can be used in the commutation path if the loop current I is less than the SC's short-circuit current I_s. Table 4.2 compares the inductive energy in a DC loop with a single SC's energy storage capability. However, a single-cell SC has a much lower DC voltage rating than the source voltage—unlike electrolytic, film, or ceramic capacitors—making it impractical to connect the SC directly across the switch after circuit interruption. In the development of a practical DCCB topology based on a SC, this presents a significant research challenge.

Table 4.2: Stored energy in different parasitic inductive elements compared to the energy storage capability of different SCs

$\boldsymbol{L}$ ($\boldsymbol{\mu}$**H**)	$\boldsymbol{\frac{1}{2}LI^2}$ **at 100 A (J)**	C**(F)**	$\boldsymbol{\frac{1}{2}CV^2}$ **at V = 3 V (J)**
1	0.005	1	4.5
10	0.05	1	4.5
100	0.5	1	4.5
1000	5	5	23
$\boldsymbol{L}$ ($\boldsymbol{\mu}$**H**)	$\boldsymbol{\frac{1}{2}LI^2}$ **at 1000 A (J)**	C**(F)**	$\boldsymbol{\frac{1}{2}CV^2}$ **at V = 3 V (J)**
1	0.5	1	4.5
10	5	5	23
100	50	50	225
1000	500	220	990

Another important characteristic of SCs is their longevity, with excellent reliability under frequent charge and discharge cycles, particularly when subjected to high-voltage, high-current transients. Although SCs are rated for very low operating voltages, short-duration high-voltage or high-current surges do not cause damage provided the stored energy remains below their rated limit. Due to their high energy storage capacity, SCs exhibit minimal terminal voltage rise during surge events. Figure 4.3(a) shows the terminal voltage of a 5-F SC under consecutive high-voltage (peak voltages of 1.5 kV, 2.5 kV



(a)

(b)

Figure 4.3: Build-up of SC terminal voltage under (a) different surge voltages applied to a 5-F capacitor, and (b) 6-kV peak surges applied to different SCs [103]

and 6.5 kV) surges applied using the LSS 6110 surge simulator. Figure 4.3(b) compares the voltage build-up across three different SCs (1 F, 5 F and 25 F) subjected to repeated 6-kV pulses.

As shown in Fig. 4.3(b), the rise in SC terminal voltage remains negligible even after hundreds of consecutive surges, when compared to the applied surge voltage. Table 4.3 summarises the performance of the SCs under high-voltage and high-current surge conditions.

The lightning surge simulator LSS 6110, with its peak output voltage of 6.6 kV, was used to obtain these results. The pre-charge voltage was adjusted to multiple levels to represent different operating conditions.

This subsection highlighted the superior performance of SCs. The next subsection presents a novel galvanic isolation technique for CBs, developed by the author, which exploits the exceptionally low ESR of SCs.

Table 4.3: A summary of test results applicable to the three SC families used in the surge capability testing [104]

Capacitor data	**Pre-charged voltage (mV)**	**Number of consecutive surges to destroy the device**
Cap-xx, 0.18 F, 2.3 V	0	220 to over 250
	250	over 220
	500	over 180
	1800	over 160
Maxwell, 230 F, 2.5 V	0	did not fail after 1000
	200	did not fail after 600
	1000	did not fail after 600
	2500	did not fail after 600
Maxwell, 90 F, 2.7 V	0	did not fail after 1000
	500	did not fail after 600
	1000	did not fail after 600
	2000	did not fail after 600

4.2 Self-operated Supercapacitor-assisted Galvanic Isolation Switch for Hybrid DCCBs

Galvanic isolation is essential for a CB in the open position, particularly in solid-state and hybrid DCCBs, since the semiconductor switch does not provide galvanic isolation. Although this aspect has been mentioned in much of the existing literature, there is limited research on the design of such isolation with proper synchronisation of fault detection and clearing. To address the aforementioned issue, the author proposed a novel circuit topology, shown in Fig. 4.4, in addition to the development of the SCA-DCCB.

This topology is designed for a hybrid DCCB, in which the proposed passive controller activates a galvanic isolation switch using the SCA technique. S_{m1} is the main mechanical switch of the hybrid DCCB and S_{m2} is the second mechanical switch (galvanic isolation switch) proposed to disconnect the MOSFET path after fault clearance. The SCA-passive controller forms a separate DC circuit loop composed of simple passive components, capable of opening S_{m2} immediately upon fault clearance with precise synchronisation.

Figure 4.5 shows the detailed circuit diagram of the hybrid DCCB. During fault initiation, the fault current is diverted through MOSFET-1, which is subsequently turned

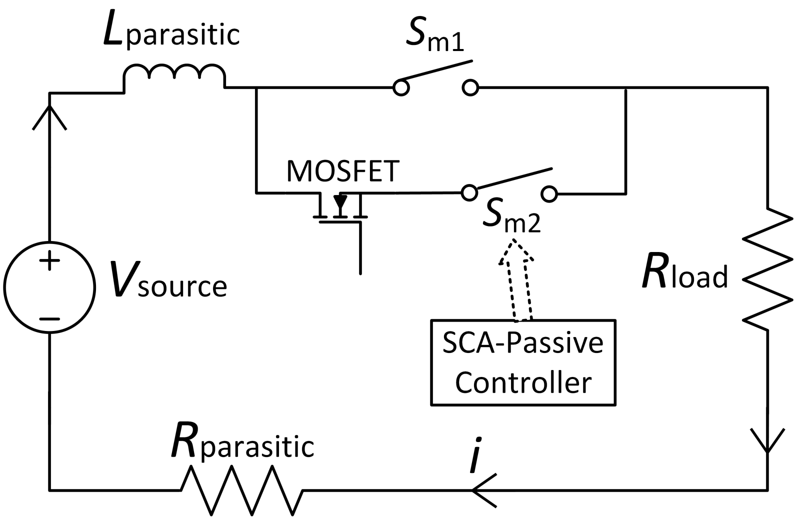


Figure 4.4: Supercapacitor-assisted passive controller is used to activate the galvanic isolation switch-S_{m2}.

off. The generation and application of the control signal for MOSFET-1 are described in Section 3.3.1. The dotted rectangle in the figure highlights the placement of a small toroidal transformer in series with MOSFET-1, which enables the proposed galvanic isolation technique.

The secondary winding of the transformer and the supplementary circuit detect the fault extinguishing moment and generate a control signal to activate the SC circuit loop by applying the required gate-to-source voltage to MOSFET-2. S_{m2} and $S_{\text{m2}'}$ are two mechanical switches that are mechanically and electrically synchronised, representing two series-connected poles in a commercially available 3-phase ACCB. When MOSFET-2

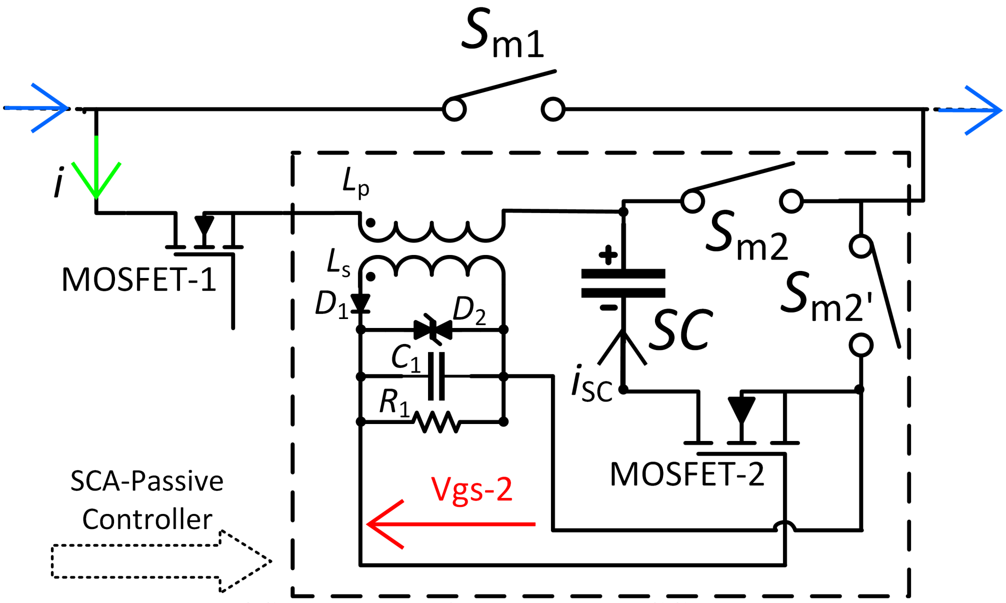
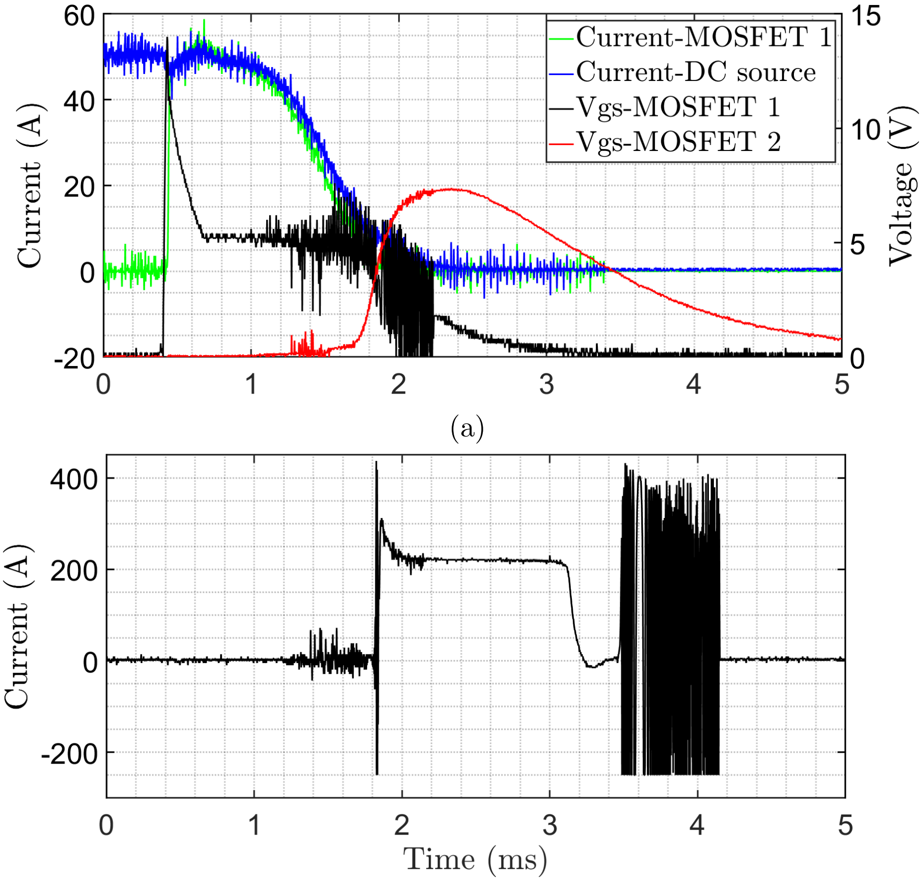


Figure 4.5: The main MOSFET path of the hybrid DCCB is disconnected shortly after the fault is cleared using the SCA-passive controller circuit.

begins conducting, both S_{m2} and $S_{\mathrm{m2'}}$ trip instantaneously, galvanically isolating the MOSFET-1 path in response to the high transient current through the switches. The threshold tripping current for S_{m2} and $S_{\mathrm{m2'}}$ is readily achieved due to the high discharge current from the SC, as both the loop resistance and SC's ESR are low despite the SC's lower voltage rating. The rated current of S_{m2} and $S_{\mathrm{m2'}}$ is selected to be higher than that of the main mechanical switch S_{m1}, ensuring S_{m2} does not trip before fault clearing. The loop inductance of the SC subcircuit is negligible due to the short length of the SC loop path. Consequently, the electric arc across S_{m2} and $S_{\mathrm{m2'}}$ is negligible during circuit isolation, even at high SC current i_{SC}. Figure 4.6 illustrates the experimental observations for the built prototype shown in Fig. 4.7.

The red trace (V_{gs2}) is generated by the passive elements shown in the Fig. 4.5 and is applied to MOSFET-2 in the SC circuit loop immediately after the current through MOSFET-1 reduces to near zero. The current through the MOSFET-1 is shown in green, and the source current is shown in blue. The gate-to-source voltage applied to MOSFET-1 is shown in black. A 6-A rated AC MCB is used as the main mechanical switch S_{m1}, and two poles from a 10-A rated 3-phase MCB are used for S_{m2} and $S_{\mathrm{m2'}}$. The current through



(a)

(b)

Figure 4.6: Proposed passive controller characteristic curves: (a) source current (blue trace), MOSFET-1 current (green trace), $v_{\mathrm{gs_1}}$ (black trace), $v_{\mathrm{gs_2}}$ (red trace), and (b) SC current

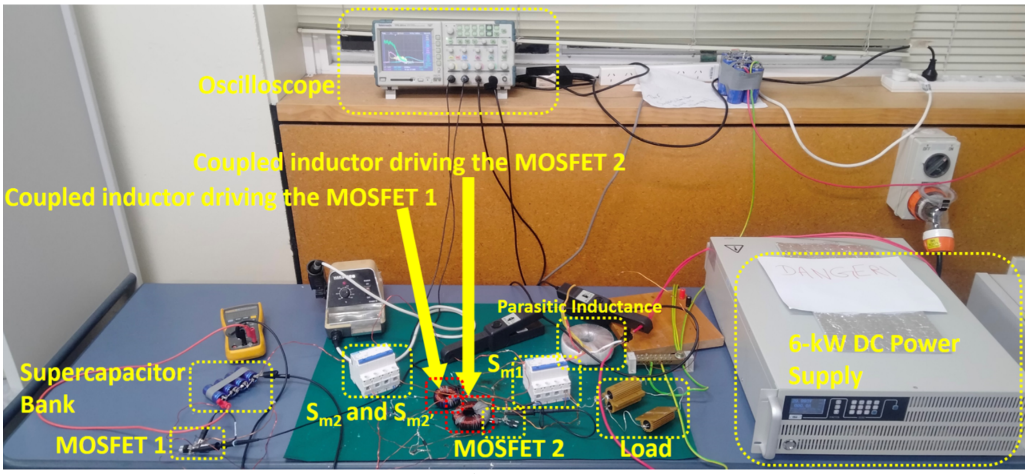


Figure 4.7: Experimental setup of the proposed isolation switch activator

the SC and MOSFET-2 reaches approximately 220 A during the isolation. The circuit achieves galvanic isolation within 1 ms, as shown in Fig. 4.6(b), where the SC current persists for approximately 1 ms. The SC current is measured using a series resistor by measuring the voltage across the resistor. The noise observed in the oscillogram after galvanic isolation arises from measurement error and from noise generated by the power supply and the current-measuring resistor used.

This subsection discussed previously published work based on high discharge current capability of SCs enabled by their extremely low ESR. The next subsection presents a patented supercapacitor-assisted surge absorber (SCASA) technique that provides the primary motivation for the current SCA-DCCB research.

Up to now, the author has presented two circuit topologies in Section 3.3.1 and Section 4.2, along with preliminary work on DCCB arc extinction using solid-state switches for circuit interruption. These results are auxiliary outcomes obtained during the development of a supercapacitor-based arc energy management technique. However, the author did not pursue further research involving semiconductor switches in the main circuit-breaking path due to increased circuit complexity, the need for a greater number of semiconductor switches, and higher cost, and instead adopted a mechanical-contact-based approach. In this approach, solid-state switches are used only in auxiliary circuits, not directly in the main current interruption path.

Most findings from this research have been published across nine peer-reviewed conference papers and one journal article. This thesis provides a detailed and organised compilation of the published material, offering a comprehensive overview of the research and its outcomes.

The following chapters present the novel supercapacitor-assisted (SCA) arc management technique—the primary focus of this research—based on a current reduction approach using a precharged SC.

4.3 Patented Supercapacitor-assisted Surge Absorber (SCASA) Technique

SCASA technique utilises the low ESR of a SC to absorb transient energy in a high-voltage impulse superimposed on a 230-V AC power line. The patented SCASA circuit topology is shown in Fig. 4.8 where the transient energy is distributed among the SC, inductive loop and the MOV, which helps minimise stress on the MOV compared to that typically seen in traditional surge protectors based on MOVs, *LC* filters, and bidirectional breakover devices.

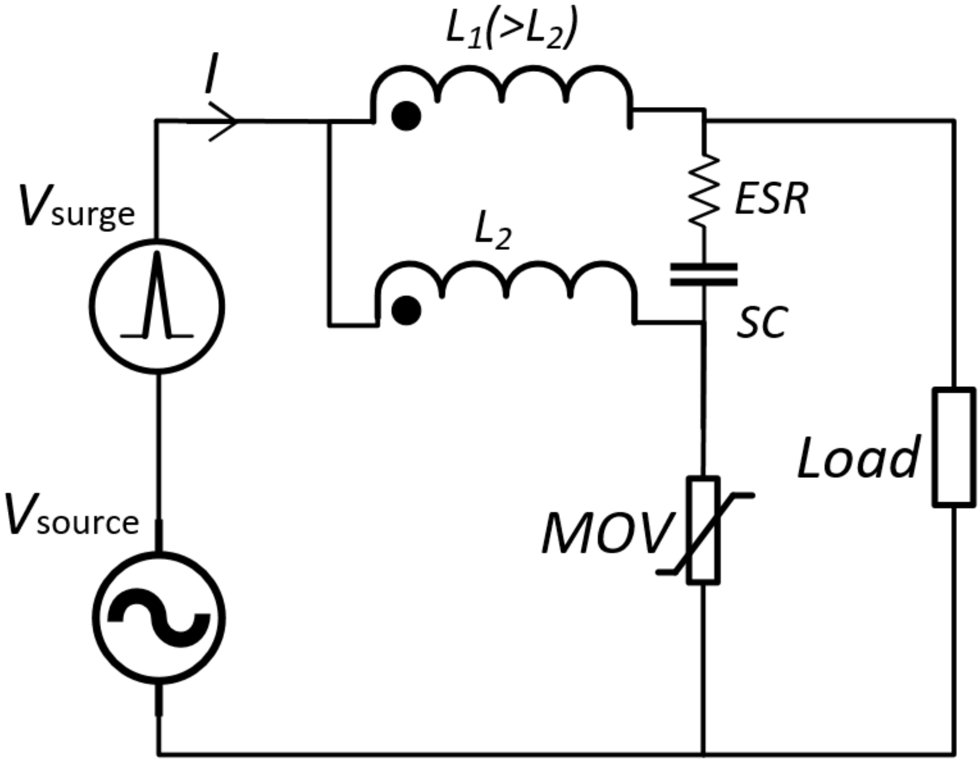


Figure 4.8: Patented supercapacitor-assisted surge absorber (SCASA) circuit [12]

A significant challenge in the SCASA design was the low DC voltage rating of the SC, which makes it impossible to place a SC across the live and neutral lines of the 230-V AC power rail, as is done in with an MOV in a generic surge absorber. In SCASA, high-voltage transients are mitigated using the low ESR of SCs. In the new SCA-DCCB design, the focus is on high-current transients; this motivated the development of the novel concept. Based on the duality of current and voltage in electrical circuits, the author concluded that an SC can be effectively used to overcome the arcing issue in a DCCB. The duality between SCASA and the new DCCB technique remains conceptual and has not been theoretically and experimentally validated; this aspect requires further investigation in future work. Based on this fundamental thinking, we investigate the concept of a current reduction technique based on SC energy storage.

4.4 Comparison of Energy Absorption-based and Energy Delivery-based Supercapacitor Subcircuits for DC Circuit Breaking

Motivated by the success of the SCASA technique, new arc-energy absorption methods were investigated, based on the high-current charge/discharge capability of SCs. A major limitation, however, is the very low DC voltage rating of SCs, which makes them unsuitable for placement across the open-circuited contacts of a DCCB. Numerous circuits were tested with the SC placed across the CB, along with additional supporting circuitry. However, these configurations were ultimately abandoned due to the low-voltage rating of SCs. Preliminary results based on arc energy absorption by the SCs are presented in [31, 59, 60, 105]. Given the low-voltage rating of SCs, instead of attempting to absorb arc energy into a SC subcircuit, an energy delivery-based approach was used to develop an arc management approach that momentarily applied a reverse voltage to the DC loop, thereby reducing the loop current.

4.5 Supercapacitor-based Transient Energy Management in DCCBs: A Conceptual Approach

A pre-charged SC can deliver a high-current pulse due to the extremely low ESR, as discussed in section 4.1. Based on the high current capability of SCs, reverse energy pumping has been identified as a potential method for arc management for DCCBs. The proposed SC-based technique is illustrated using the block diagram shown in Fig. 4.9. A SC is connected in series with a high-current, low-voltage MOSFET and the primary winding of a transformer. Secondary winding of the transformer is connected in series with the mechanical CB in the main DC loop.

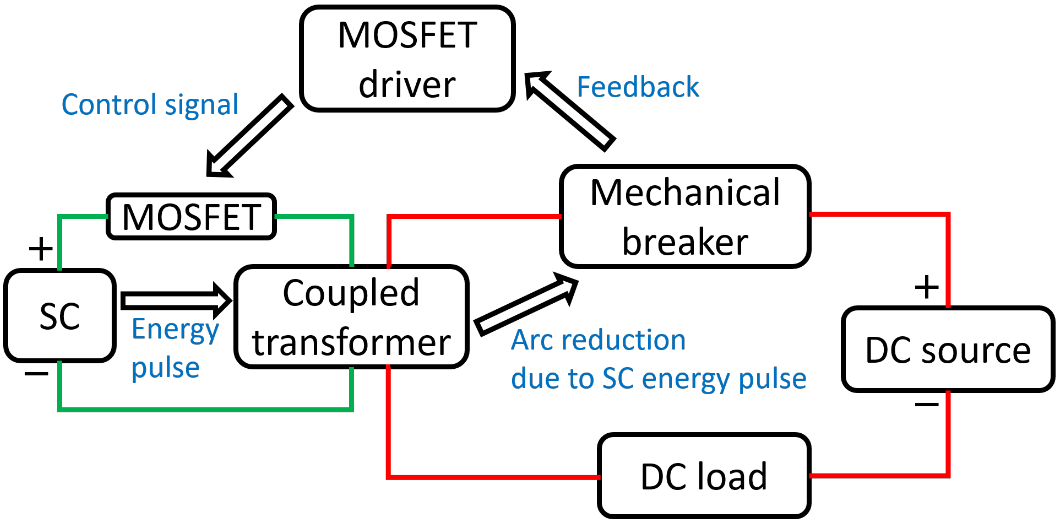


Figure 4.9: Simplified block diagram of the proposed topology

Control signal for the MOSFET is generated by a simple driver circuit, with feedback taken from the contact-opening phase of the mechanical breaker. The MOSFET is turned on with a delay of a few microseconds after the mechanical breaker begins to open. A sudden high-current pulse is pumped from the SC to the primary winding of the transformer. Part of the SC's energy is then delivered to the DC circuit loop via the coupled transformer, reducing the arc energy and thereby reducing the electric arc.

4.6 Conclusion for the Chapter 4

This chapter discussed the properties of SCs and illustrated their low ESR characteristic using the author's published work. Furthermore, the SCASA technique was summarised, as it provides the primary motivation for this research. A detailed discussion of the novel approach, including analytical, simulation, and experimental results, will be presented in the next chapter.

Chapter 5

Supercapacitor-assisted Arc Management Technique (SCA^{2}M)

After analysing numerous existing DCCB techniques—including solid-state and hybrid variants—we found that each approach has its own limitations for commercial-scale implementation, as discussed in earlier chapters. Significant research efforts are currently underway to address these challenges. However, recognising the superior current-pumping capability of SCs due to their very low ESR, we developed a novel DCCB arc-extinguishing method. This approach generates a very high current pulse in a loop that is completely isolated from the main DC loop during the circuit-breaking instant and magnetically transfers that pulse energy to the main DC loop using a coupled transformer, thereby substantially reducing the arc, as briefly introduced in the previous chapter. This method is termed the supercapacitor-assisted arc management technique (SCA^{2}M) and is presented in detail from this chapter onward, with simulated and experimental results shown sequentially. Additional results, including arc visualisation, are provided in Chapter 6. MATLAB is used for simulation. The analysis begins with the pumped SC current. Subsequently, an electric arc is modelled at the simplest level with optimised arc modelling being deferred to future work.

The SCA^{2}M technique comprises three main elements illustrated in Fig. 5.1: (i) an SC-based high-current pulse generator, termed the supercapacitor-assisted transient energy pump (SCATEP), (ii) a coupled transformer, and (iii) a MOSFET driver.

The SCATEP is developed using a SC and a MOSFET, connected in series with the primary winding of a transformer. The transformer couples the part of SC's energy pulse to the secondary winding, where a mechanical breaker is connected in series. A typical CB—mechanical, solid-state, or hybrid—includes a current-sensing mechanism for fault detection. However, no additional sensors or regulated DC power supplies are required to detect the fault current or trigger the breaker with this arc management technique, as it relies on mechanisms already built into the device and is compatible with any mechanical CB. Future work will extend the technique to operate with any DCCB, including solid-state and hybrid DCCBs. The mechanical breaker trips automatically via one of two mechanisms: (a) electromagnetic tripping for short-circuit faults and (b) thermal overload

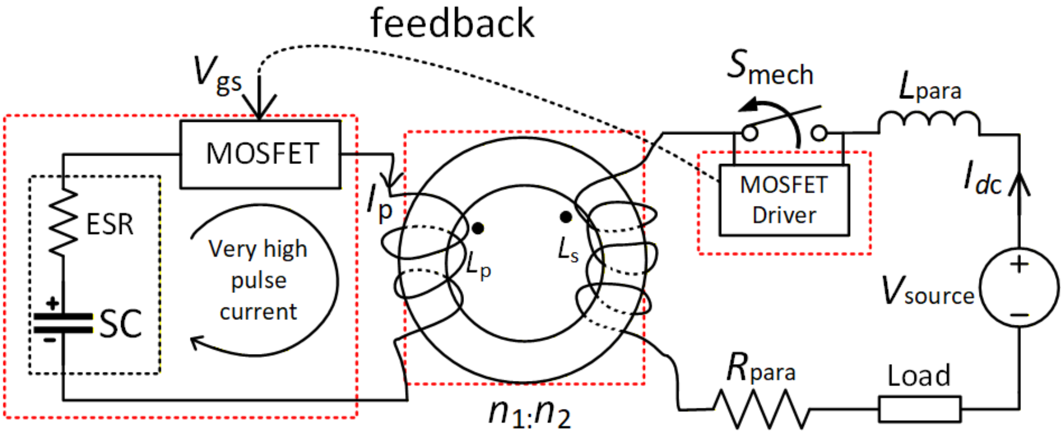


Figure 5.1: Proposed SC-based circuit for arc reduction using SC pulse energy

tripping for overload faults. When the breaker begins to open, the MOSFET driver detects the initiation of contact separation by the sudden 13-V voltage rise, which is the initial arc voltage described in earlier chapters. Using this voltage, the MOSFET driver generates a clean gate-to-source voltage pulse and synchronises MOSFET activation with mechanical breaker opening within a microsecond order time delay. The working principle of the MOSFET driver is explained in Section 5.1.6. The key stages of the SCA^{2}M technique are analysed in the following subsections based on simulated and experimental results.

5.1 SCA^{2}M Circuit Topology

The initial prototype was designed and tested for a 2-kW/80-A/25-V DC system, and additional tests under higher power conditions were conducted to validate the technique's scalability, which will be discussed in Chapter 6.

Figure 5.2 illustrates a transformer circuit where the secondary winding is connected in series with the mechanical switch, DC source, and load. When the mechanical contact opens, an electric arc is initiated.

The transformer-induced secondary voltage $e_s(t)$, which opposes the DC source voltage, reduces the DC loop current $i_{dc}(t)$ supplied by the source. The arc generated during circuit opening depends on the stored energy in the inductive elements of the main DC loop. As inductance increases, the arc intensifies. In a real industry-based DC system, lengthy wires introduce line inductance. However, in this prototype, short wire lengths were used, resulting in very low line inductance (7 μH) and an insufficient arc for the experiment. To address this, the loop inductance was increased by adding an air-core inductor with 50-μH inductance, constructed using 8-AWG gauge wire. An air-core inductor was chosen because the inductance of a magnetic-core inductor decreases under DC current flow due to core saturation.

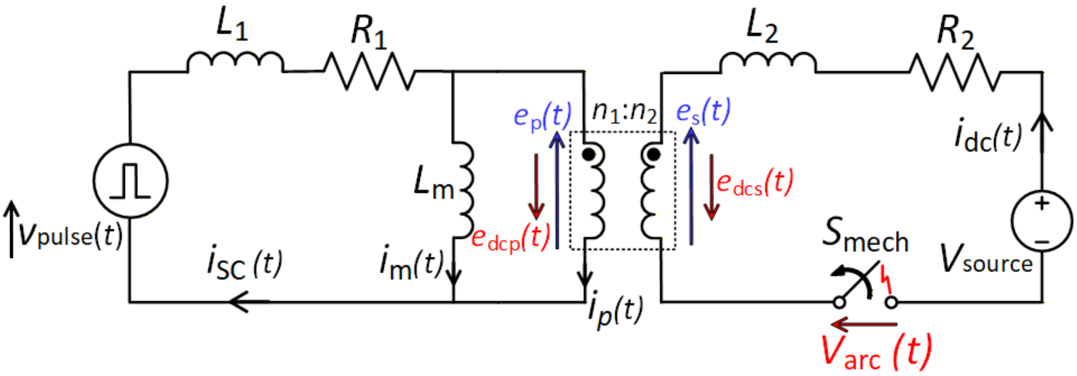


Figure 5.2: SC pulse energy is transferred from the primary winding to the secondary winding.

In Fig. 5.2, L_2 represents the total DC loop line inductance, including the transformer secondary winding's leakage inductance. The parameters R_2, R_1, and L_1 denote the total DC loop resistance (including load resistance), the transformer primary winding's total loop resistance (encompassing the ESR of the SC, MOSFET on-resistance, transformer winding resistance, and other remaining wiring resistance), and the total loop inductance of the primary winding, respectively. The magnetising inductance of the transformer, referred to the primary circuit, is denoted by L_{m}, where $i_{\mathrm{m}}(t)$ and $i_{\mathrm{p}}(t)$ represent the magnetising current and transformer primary current, respectively, summing to the SC current $i_{\mathrm{SC}}(t)$. Transformer core loss resistance is neglected; the reason is explained in subsection 5.1.2.

For analysis, the SC–MOSFET combination is modelled as a single-pulsed voltage source $v_{\mathrm{pulse}}(t)$, with a peak value equal to the SC voltage. The activation sequence of the DCCB is summarised below:

- Mechanical switch S_{mech} begins to open under a fault condition (overload, short circuit, or manual tripping)
- Loop current $i_{\mathrm{dc}}(t)$ begins to decrease as the CB opens. Due to this current reduction, voltage $e_{\mathrm{dcs}}(t)$ is induced in the transformer's secondary winding, as shown in Fig. 5.2, and the corresponding primary voltage $e_{\mathrm{dcp}}(t)$ appears across the primary winding.
- After a short delay, $v_{\mathrm{pulse}}(t)$ is applied by turning on the MOSFET with feedback, as illustrated in Fig. 5.1.
- High current pulse $i_{\mathrm{SC}}(t)$ flows through the SC–MOSFET path, and $e_{\mathrm{p}}(t)$ is induced in the primary transformer winding, as shown in Fig. 5.2. The corresponding secondary voltage $e_{\mathrm{s}}(t)$ is induced in the secondary winding, which opposes the source voltage and helps reduce the DC loop current $i_{\mathrm{dc}}(t)$ rapidly.
- The secondary induced voltage $e_{\mathrm{s}}(t) - e_{\mathrm{dcs}}(t)$ is the key parameter for extinguishing the arc quickly which forces $i_{\mathrm{dc}}(t)$ to zero.

The 2-kW prototype was built with low values of L_1 and R_1 to increase $e_\mathrm{p}(t)$, thereby increasing $e_\mathrm{s}(t)$. The value of $e_\mathrm{dcs}(t)$ is usually small compared with $e_\mathrm{s}(t)$, because the rate of change of $i_\mathrm{dc}(t)$ is low compared with that of $i_\mathrm{SC}(t)$, where the induced voltages are proportional to the rate of change of current. Since the arc voltage $v_\mathrm{arc}(t)$ also affects $e_\mathrm{s}(t) - e_\mathrm{dcs}(t)$, the analysis becomes complex, and must be examined using plasma physics. Therefore, for the initial current reduction analysis, the circuit is simplified as shown in Fig. 5.3, where DC current reduction and the corresponding electric arc are not considered. The current $i_\mathrm{s}(t)$ is generated due to the induced secondary voltage $e_\mathrm{s}(t)$.

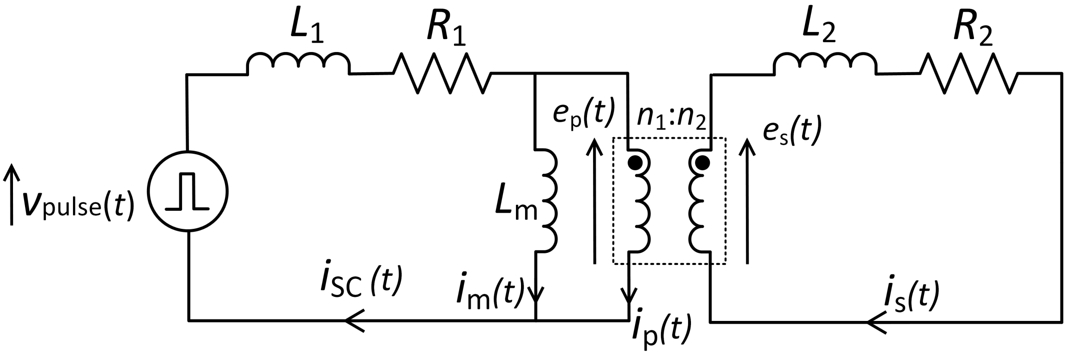


Figure 5.3: Simplified transformer equivalent circuit for the current reduction technique

After completing this analysis, the author developed a simplified arc model to account for the effects of the decaying DC current, which will be discussed in subsection 5.1.3.

5.1.1 Supercapacitor-assisted Transient Energy Pump (SCATEP)

The energy pump comprises two main elements: the SC bank and the MOSFET. The SC is connected in series with a high-current, low-voltage MOSFET to generate a high-current pulse, facilitated by the low ESR of both the SC and the MOSFET. The primary side of the circuit connects to the primary winding of the transformer, while the secondary winding links in series with the main DC loop. The SC–MOSFET loop is galvanically isolated from the main DC loop by the transformer. As shown in Fig. 4.2 in Section 4.1, SCs can exhibit ESR values up to approximately one to two orders of magnitude lower than those of electrolytic capacitors. Additionally, since high-current, low-voltage MOSFETs feature on-resistances in the milliohm range, the SC–MOSFET loop can be engineered with minimal resistance (R_1) and inductance (L_1), enabling higher current delivery.

5.1.1.1 SC Bank

For the 2-kW prototype circuit, five Green-Cap SCs rated at 3000-F, 3-V (Technical specifications are in Appendix F) are connected in series to generate 14 V. The SC voltage is first defined, and based on this, the other parameters are calculated as discussed in the following subsections.

5.1.1.2 MOSFET Switch

For the MOSFET, IXFX520N075T2 power MOSFETs (Appendix B.3) were used, with a maximum pulse current rating of 1350 A, a voltage rating of 75 V, and a maximum pulse energy rating of 3 J, with an on-resistance of less than 2.2 mΩ. The detailed design information of the MOSFET is discussed later in this chapter, as the coupled transformer must be designed first. Since the SCs are comparatively low-voltage devices, a low-voltage MOSFET can be used, which reduces cost in the DCCB.

5.1.2 Coupled Transformer

The transformer is used in the SCA^{2}M technique for two main reasons: to place the low-voltage SC without exposing it to the DC source voltage, and to isolate the SC–MOSFET loop from the main DC loop. A simple toroidal transformer is designed to transfer the maximum percentage of primary winding's energy to the secondary winding, thereby reducing the main DC loop current during circuit interruption. Two critical design steps are identified: transformer core selection, and determination of the number of turns in the primary and secondary windings.

The coupled transformer is used in this SCA^{2}M technique as a pulse transformer, delivering only a single pulse over a period of hundreds of microseconds. Core losses—hysteresis and eddy currents—are generally negligible because excitation occurs briefly and does not produce significant heating. However, winding resistance remains critical even for a single pulse. Higher resistance reduces energy transfer efficiency, introduces voltage drops, and distorts the pulse shape, especially when fast rise times are required. Leakage inductance is often more significant than core losses, as it directly affects pulse fidelity. Leakage inductance arises from the uncoupled self-inductance of the transformer windings. Therefore, in the transformer design, the author minimised both winding resistance and leakage inductance.

In order to analyse the transient secondary current, $i_{\mathrm{s}}(t)$, it is appropriate to begin with calculation $e_{\mathrm{p}}(t)$, followed by $i_{\mathrm{p}}(t)$. Figure 5.3 is further simplified to Fig. 5.4 by considering the transformer equivalent referred to the primary side, where the turns ratio is $n = \frac{n_2}{n_1}$.

To analyse the above circuit, a unit-step function:

$$u(t) = \begin{cases} 0, & t < 0 \\ 1, & t \geq 0 \end{cases}$$

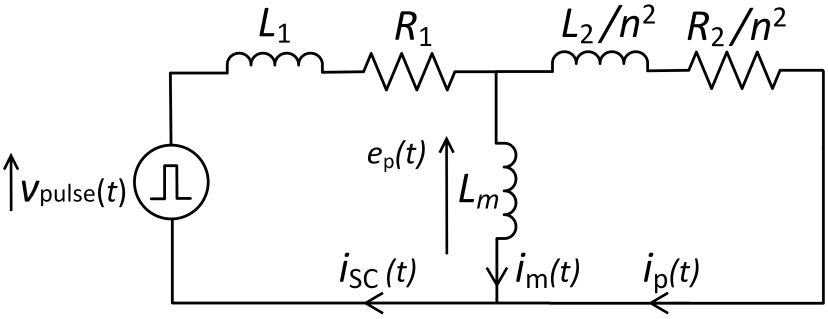


Figure 5.4: Referred to the primary-side equivalent circuit of the transformer

is used with a magnitude equal to the maximum value of $v_{\text{pulse}}(t)$, which corresponds to the SC voltage. Figure 5.5 illustrate the Laplace transform parameters in the circuit.

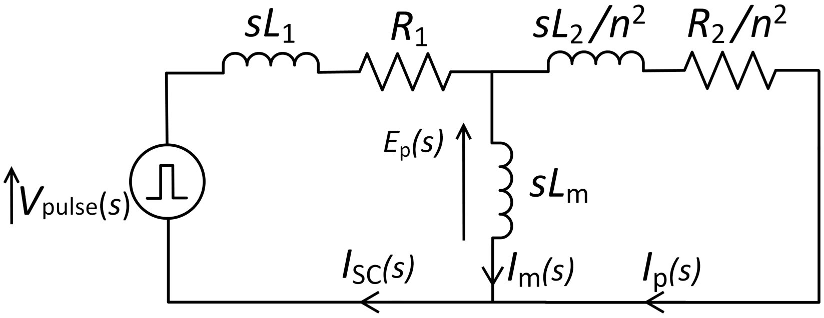


Figure 5.5: Equivalent circuit representation in the Laplace domain

The expression for $E_{\text{p}}(s)$ in Eq. 5.1 is obtained using the voltage division rule. The primary current of the transformer, $I_{\text{p}}(s)$ is given by Eq. 5.2, and the secondary current, $I_{\text{s}}(s)$, is given by Eq. 5.3. For improved circuit performance, the peak of $I_{\text{s}}(s)$ should be maximised and its associated time constant should be minimised to achieve a rapid current zero crossing in the primary DC loop. The time-constant of the SC circuit determines the duration required to extinguish the DC loop current.

$$E_{\text{p}}(s) = \left(\frac{L_{\text{m}}}{L_1 + L_{\text{m}} + \frac{R_1}{s}} \right) \times V_{\text{pulse}}(s) \tag{5.1}$$

$$I_{\text{p}}(s) = \frac{E_{\text{p}}(s)}{\frac{sL_2}{n^2} + \frac{R_2}{n^2}} \tag{5.2}$$

$$I_{\text{s}}(s) = \frac{I_{\text{p}}(s)}{n} \tag{5.3}$$

5.1.2.1 Transformer Type Selection

Figure 5.4 is further simplified and shown in Fig. 5.6 to mathematically justify the selection of the appropriate transformer type. For this analysis, the initial DC loop current I_{dc} is considered. The simplified circuit represents the primary-referred equivalent with loop resistance and loop inductance neglected, and the load is represented as Z.

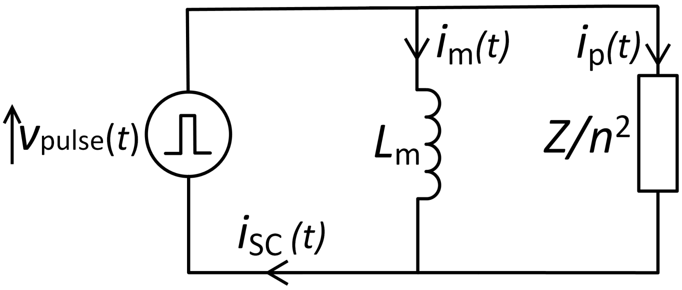


Figure 5.6: Simplified transformer circuit referred to the primary side

The DC current in the main loop is,

$$I_{\text{dc}} = \frac{V_{\text{dc}}}{Z} \tag{5.4}$$

where V_{dc} is the DC source voltage. The primary winding current in the transformer loop $i_{\text{p}}(t) = \frac{V_{\text{pulse}}(t)}{Z/n^2} = \frac{V_{\text{SC}}(t)}{Z/n^2}$, where the turns ratio $n > 1$ for a step–up transformer and $n < 1$ for a step–down configuration. The corresponding secondary current transferred to the DC loop is,

$$i_{\text{s}}(t) = \frac{i_{\text{p}}(t)}{n} = \frac{V_{\text{SC}}(t)/n}{Z/n^2} = \frac{V_{\text{SC}}(t) \times n}{Z} \tag{5.5}$$

To zero the current in the main DC loop, the transferred secondary current $i_{\text{s}}(t)$ must equal or exceed the main DC loop current,

$$i_{\text{s}}(t) \geq I_{\text{dc}} \tag{5.6}$$

Thus the relationship between $V_{\text{SC}}(t)$ and V_{dc} can be obtained by substituting for I_{dc} and $i_{\text{s}}(t)$ from equations 5.4 and 5.5 respectively.

$$V_{\text{SC}}(t) \geq \frac{V_{\text{dc}}}{n} \tag{5.7}$$

Equation 5.7 shows that, for a step-down transformer ($n < 1$), the SC voltage must be higher than the DC source voltage, which is unsuitable. In contrast, a step-up ($n > 1$) configuration allows the use of a low-voltage SC. Therefore, to effectively integrate SCs in this novel approach, only a step-up transformer is appropriate. For a 14-V SC voltage and a 25-V DC voltage, the minimum transformer ratio should be greater than or equal to 1.8 according to Eq. 5.7.

5.1.2.2 Magnetic Core Selection

Transformer core selection must be performed carefully because the secondary winding carries continuous DC current during normal operation, which may cause magnetic core saturation. Initially, a ferrite magnetic core, 5975011121 from the manufacturer Fair-Rite,

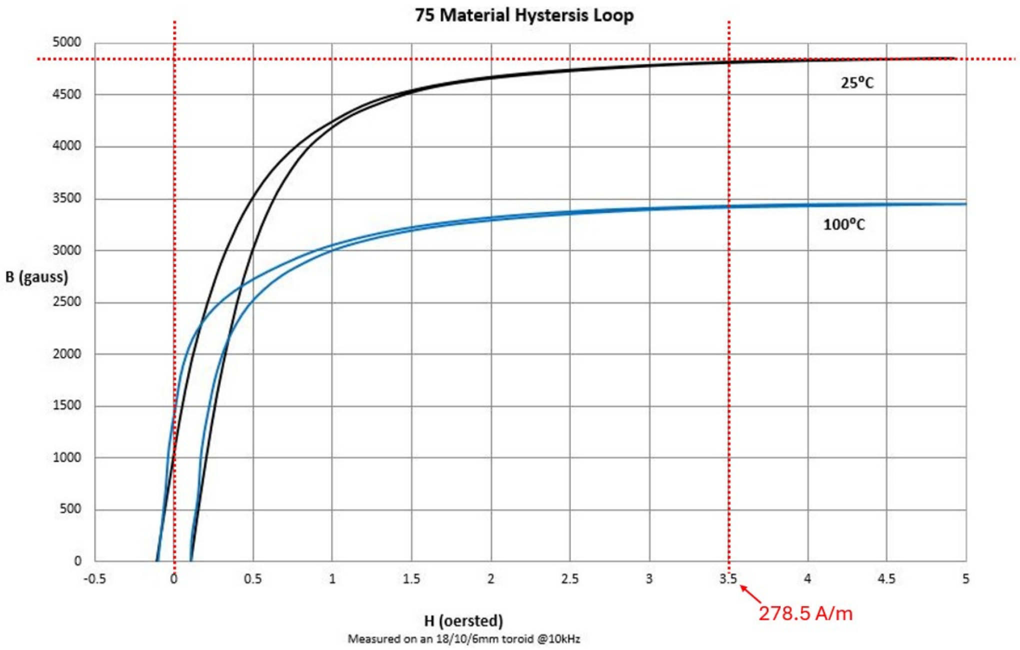


Figure 5.7: B–H curve of ferrite magnetic core 5975011121

is considered, and Fig. 5.7 illustrates the B–H curve of the material. The corresponding datasheet is provided in Appendix D.1.

According to Fig. 5.7, the core fully saturates when the ampere–turn value reaches 278.5 per unit effective path length. For this core (5975011121), the effective path length is 16.5 cm, giving an ampere–turn value of 46 A ($278.5 \times 16.5 \times 10^{-2}$). This indicates that a single-turn wound core saturates at 46 A; for two turns, the saturation current is 23 A, and so on. Therefore, such ferrite cores are unsuitable, and a powdered iron core with high DC bias capability was used instead. Figure 5.8 illustrates the DC-biased performance curve for a low-permeability, powdered iron core, 0078773A7 from the manufacturer Magnetics, showing superior DC biasing performance compared with the ferrite core. The corresponding datasheet is provided in Appendix D.2.

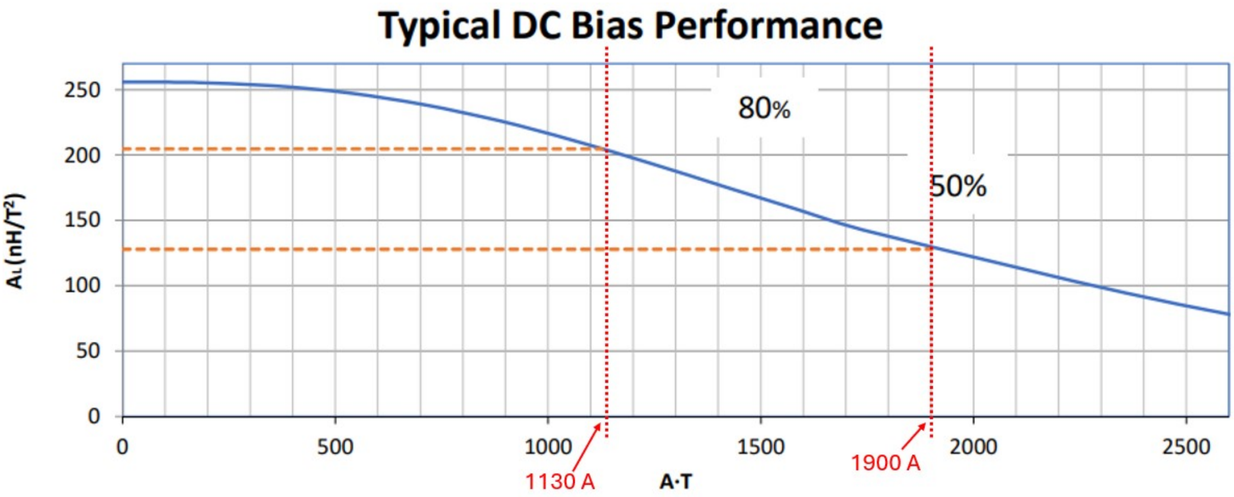


Figure 5.8: DC bias performance of powdered iron core 0078773A7

For the prototype circuit, an 80-A DC system is used. If 10 secondary turns are assumed, the total ampere–turns are 80 × 10 = 800, thus A_{L} (permeance) is set to 230 nH/T^2. According to the DC-bias characteristic curve, the A_{L} value of the core decreases from 256 to approximately 230 nH/T^2, representing only a 10% reduction for 10 secondary turns. The actual number of secondary turns is 11, and the design details are provided in the next subsection.

5.1.2.3 Number of Turns Selection

In this subsection, the reflected current on the secondary side is analysed, accounting for DC biasing as the transformer core is subjected to a continuous DC current. Given the need to consider multiple transformer winding parameters, the following method is adopted. Adding the coupled transformer to the circuit loop increases the effective line inductance. The DC loop inductance before inserting the transformer is 57 μH. A condition is defined such that the added self-inductance does not increase the existing line inductance by more than 50% (equivalent to 28.5 μH), and the added total inductance—comprising self-inductance and other leakage inductances—does not increase the existing line inductance by more than 60%.

Figure 5.9 shows MATLAB simulation results for the effective DC loop current under different transformer winding configurations: varying primary winding turns (n_1) and transformer turns ratios (n=n_2/n_1).

From the possibilities presented in Fig. 5.9, $n_1 = 4$ and $n = 2.75$ are selected, giving $n_2 = 11$ for the design. According to the magnetic core's DC biasing performance curve

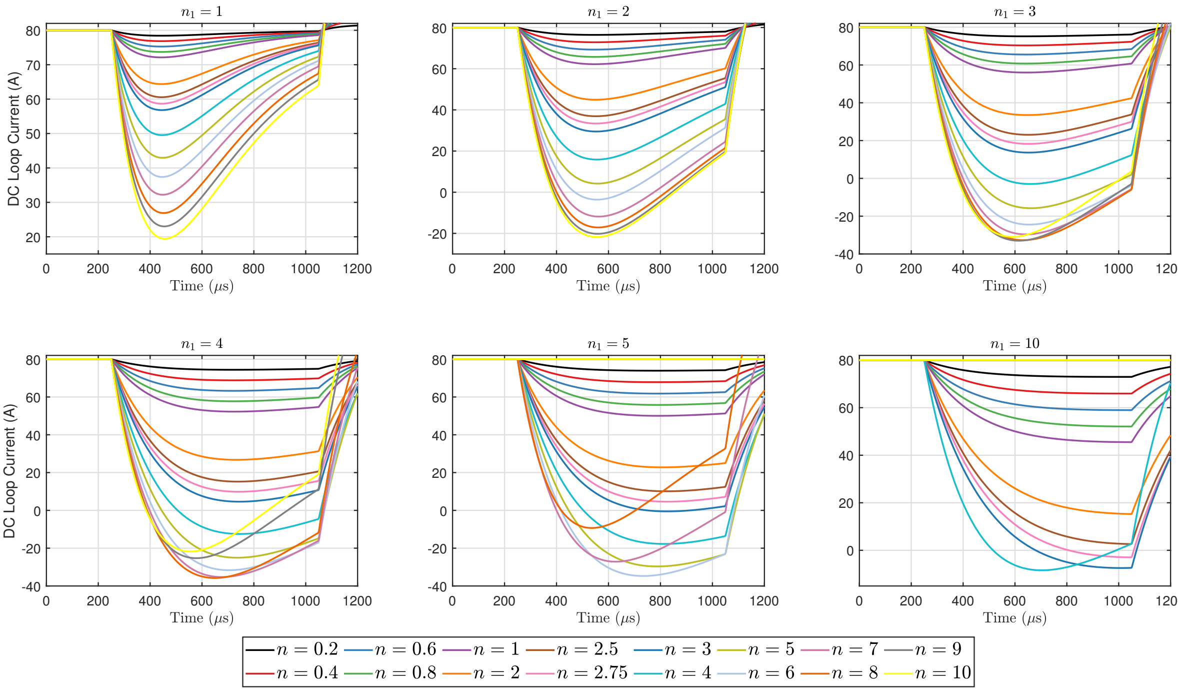


Figure 5.9: Simulated DC loop current reduction for various transformer-winding configurations

in Fig. 5.8, the A_{L} value is 225 nH/T^2, satisfying the defined restriction, with the added inductance due to the secondary winding now $L_{\mathrm{s}} < 28.5\ \mu$H. The primary and secondary inductances can thus be calculated as:

$$L_{\mathrm{p}} = 225 \times 4^2 = 3.6\ \mu H \tag{5.8}$$

$$L_{\mathrm{s}} = 225 \times 11^2 = 27.2\ \mu H \tag{5.9}$$

5.1.2.4 Transformer Measurements

The transformer self-inductance values were determined in the previous subsection. To determine the leakage inductance, the coupling coefficient K is first calculated. Figure 5.10 shows the series and inverse series inductor connection arrangements used to obtain the transformer mutual inductance and coupling coefficient.

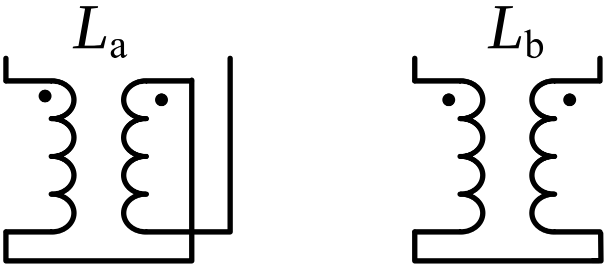


Figure 5.10: Measurement of transformer inductances: series connection inductance L_{a}, and inverse series connection inductance L_{b}

For the series and inverse series configurations, the following expressions are derived, where L_{p} and L_{s} represent the self-inductance values of the transformer's primary and secondary windings, respectively.

$$\begin{aligned} L_{\mathrm{a}} &= L_{\mathrm{p}} + L_{\mathrm{s}} + 2M, & (5.10)\\ L_{\mathrm{b}} &= L_{\mathrm{p}} - L_{\mathrm{s}} - 2M. & (5.11) \end{aligned}$$

The mutual inductance and coupling coefficient of the transformer are calculated using,

$$M = \frac{L_{\mathrm{a}} - L_{\mathrm{b}}}{4} \tag{5.12}$$

$$K = \sqrt{\frac{M^2}{L_{\mathrm{p}} L_{\mathrm{s}}}} \tag{5.13}$$

Tests were conducted using an LCR meter at 1 kHz for the designed transformer, as the SC pulse applied to the transformer has a duration of approximately one millisecond, yielding $L_\mathrm{a} = 48.44$ μH and $L_\mathrm{b} = 15.87$ μH, resulting in a mutual inductance of $M = 8.14$ μH. The coupling coefficient is calculated as $K = \sqrt{\frac{8.14^2}{3.6 \times 27.2}} = 0.823$. The leakage inductance ℓ is determined from the self-inductance L and coupling coefficient K,

$$\ell = (1 - K) \times L \tag{5.14}$$

Therefore, the primary winding leakage inductance is $\ell_\mathrm{a} = 0.64$ μH, and the secondary winding leakage inductance is $\ell_\mathrm{b} = 4.81$ μH. Transformer parameter values useful for the analysis are summarised in the Table. 5.1.

Table 5.1: Transformer parameters

Parameter	**Value**
n_1	4
n_2	11
L_p	3.6 μH
L_s	27.2 μH
ℓ_a	0.64 μH
ℓ_b	4.81 μH

5.1.2.5 Current Transfer Analysis

For the analysis of the 80-A/25-V/2-kW DC loop, the parameters used in the prototype are listed in Table. 5.2. These are the values used in the MATLAB simulations.

The preliminary equations (5.1, 5.2, and 5.3) are derived using the Laplace transform in Section 5.1.2. These equations are now used with substituted parameter values to formulate the simulation equations. The SC voltage amplitude is set to 14 V for a duration of 800 μs, with the step function defined in Eq. 5.15. The 800-μs duration is chosen to match with the arc duration of 700 μs for an 80-A current, as presented in subsection 5.1.3.

$$v_\mathrm{pulse}(t) = 14(u(t) - u(t - 0.0008)) \tag{5.15}$$

The values from Table 5.2 are substituted into Eq. 5.1 to derive Eq. 5.16. By applying the inverse Laplace transform to Eq. 5.16, the induced voltage in the primary winding, $e_\mathrm{p}(t)$, is obtained as shown in Eq. 5.17.

$$E_\mathrm{p}(s) = \left(\frac{225 \times 10^{-9} \times 4^2}{(0.9 \times 10^{-6}) + (225 \times 10^{-9} \times 4^2) + \frac{(2.8 \times 10^{-3})}{S}} \right) \times \frac{14}{s} \times (1 - e^{-800 \times 10^{-6} s}) \tag{5.16}$$

Table 5.2: Parameters used in the circuit prototype and simulations

Parameter	**Description**	**Value**
A_L	permeance value	225 nH/T^2
R_1	includes ESR of the SC bank, primary winding resistance, and MOSFET on-resistance	2.8 mΩ
L_1	includes transformer primary winding leakage inductance (0.64 μH) and remaining primary loop inductance (0.26 μH) due to wiring	0.9 μH
R_2	includes load resistance (200 mΩ), secondary winding resistance, CB on resistance (47 mΩ), and remaining loop resistance (65.5 mΩ) due to wiring	312.5 mΩ
L_2	includes the transformer secondary winding leakage indutance (4.81 μH), added air core inductor (50 μH), and remaining secondary loop inductance (7 μH) due to wiring	61.8 μH
Duration of V_pulse	pulse duration corresponds to MOSFET ON time set by the MOSFET driver (subsection 5.1.6).	800 μs
Amplitude of V_pulse	voltage of the SC bank	14 V
DC source voltage, V_source	-	25 V

$$e_\mathrm{p}(t) = 11.2e^{-622.22t}(1 - 1.65u(t - 0.0008)) \tag{5.17}$$

Substituting the values into Eq. 5.2 and applying the inverse Laplace transform yields the time-domain equation for the primary winding current,

$$i_\mathrm{p}(t) = 309.1\left(e^{-622.22\,t} - e^{-5056.63\,t}\right) + u(t - 0.0008)\left(17656.9\,e^{-5056.63\,t} - 508.44\,e^{-622.22\,t}\right) \tag{5.18}$$

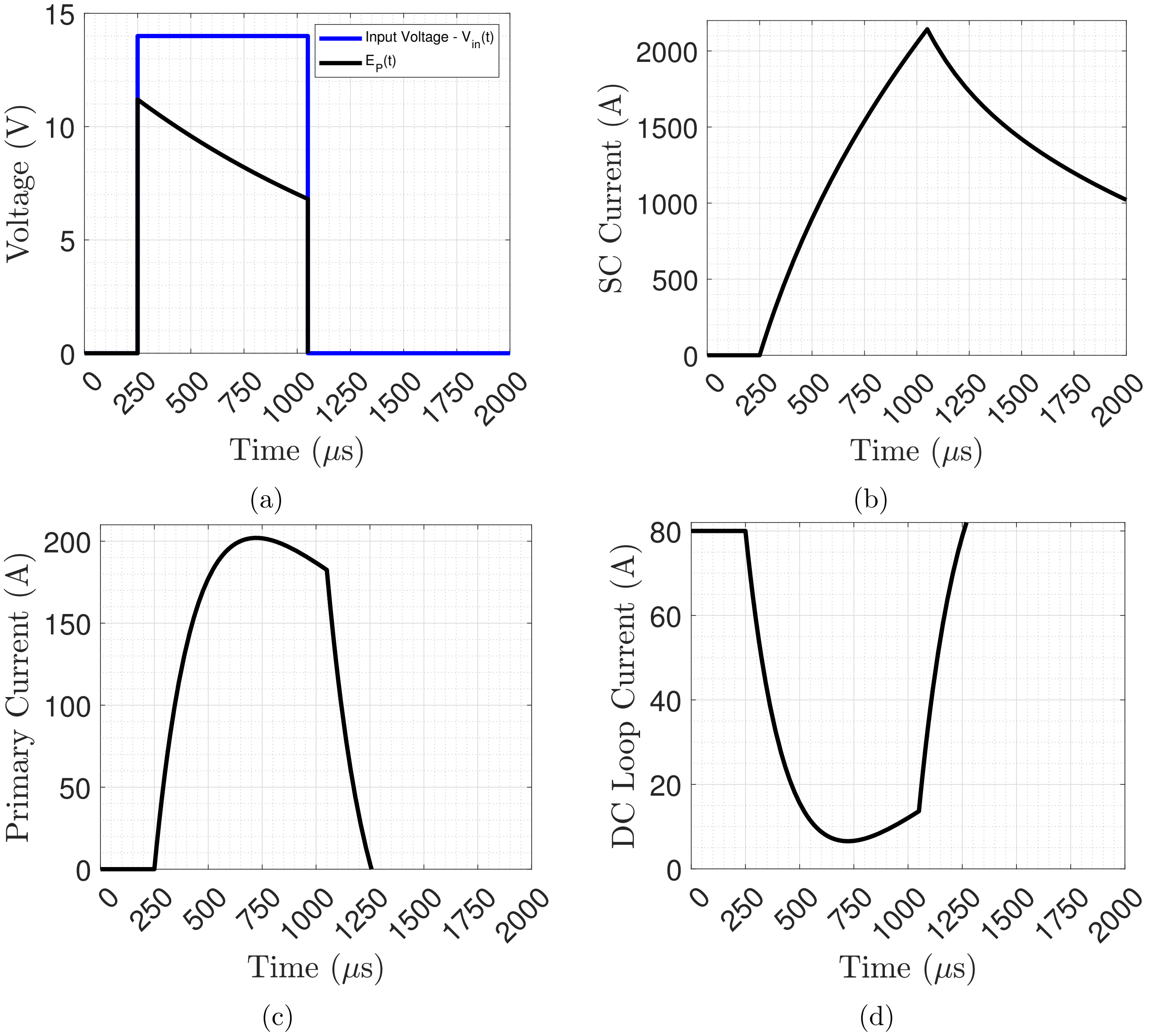
The secondary current, $i_\mathrm{s}(t)$, is obtained by dividing the primary current by the turns ratio,

$$i_\mathrm{s}(t) = 112.4\left(e^{-622.22\,t} - e^{-5056.63\,t}\right) + u(t - 0.0008)\left(6420.68\,e^{-5056.63\,t} - 184.88\,e^{-622.22\,t}\right) \tag{5.19}$$

The effective DC loop current has an initial DC current of 80 A,

$$i_\mathrm{dc}(t) = 80 - i_s(t) \tag{5.20}$$

Figure 5.11 illustrates four different parameter variations for the designed transformer. Fig. 5.11(a) shows the voltage $e_\mathrm{p}(t)$ (black trace) across the magnetising inductance L_m, as given by equation 5.17, while the blue trace represents the SC voltage during the applied pulse duration. Figure 5.11(b) shows the current through the SC–MOSFET loop, plotted as the sum of the primary current and the magnetising current, where the magnetising current is obtained in the same manner as the primary current. Figure 5.11(c) shows the current through the primary winding of the transformer, and Fig. 5.11(d) shows the effective DC loop current, where the steady 80-A DC current is suppressed by the secondary reflected current.



(a) (b)

(c) (d)

Figure 5.11: Simulated waveforms. (a) SC input voltage and voltage induced in the primary winding; (b) SC current; (c) primary winding current; (d) DC loop current under the current reduction technique.

Up to this point, the modeling has ignored the electric arc in the secondary loop. A comprehensive model is not developed in this work due to its complexity and because it is outside the scope of this study; the focus is on introducing the SCA^{2}M technique, with full modelling reserved for future work. However, to finalise and present the study, a simplified arc model has been developed to simulate the complete circuit, as described in the following subsection.

5.1.3 DC Arc Model

Figure 5.12 depicts a simplified circuit representing the DC loop behaviour during opening of the CB, S_{mech} with voltages across the elements indicated immediately after opening commences. The DC loop current is I before the CB opens and $i_{\mathrm{dc}}(t)$ thereafter. Applying Kirchhoff's voltage law to the DC loop yields Eq. 5.21. The challenging task is to develop an accurate model for the arc voltage, $v_{\mathrm{arc}}(t)$, and the arc current, $i_{\mathrm{dc}}(t)$.

$$v_{\mathrm{arc}}(t) = V_{\mathrm{dc}} + v_{\mathrm{lpara}}(t) - v_{\mathrm{rpara}}(t) - v_{\mathrm{load}}(t) \tag{5.21}$$

The behaviour of the arc is difficult to model due to the erratic and unpredictable nature of arc faults [106–109]. Two classical dynamic DC arc models are widely used: (i) the Mayr arc model [110] and (ii) the Cassie arc model [111], both derived from arc energy-balance principles. The Mayr model is best suited for lower-current arcs, whereas the Cassie model is more appropriate for higher-current arcs [106–109, 112, 113].

The Mayr model describes the dynamics of arc conductance under the assumption of constant cooling power P_0:

$$\frac{1}{g}\frac{\mathrm{d}g}{\mathrm{d}t} = \frac{1}{\tau_{\mathrm{m}}}\left(\frac{v_{\mathrm{arc}}i}{P_0} - 1\right) \tag{5.22}$$

where:

g is the arc conductance (S),
i is the arc current (A),

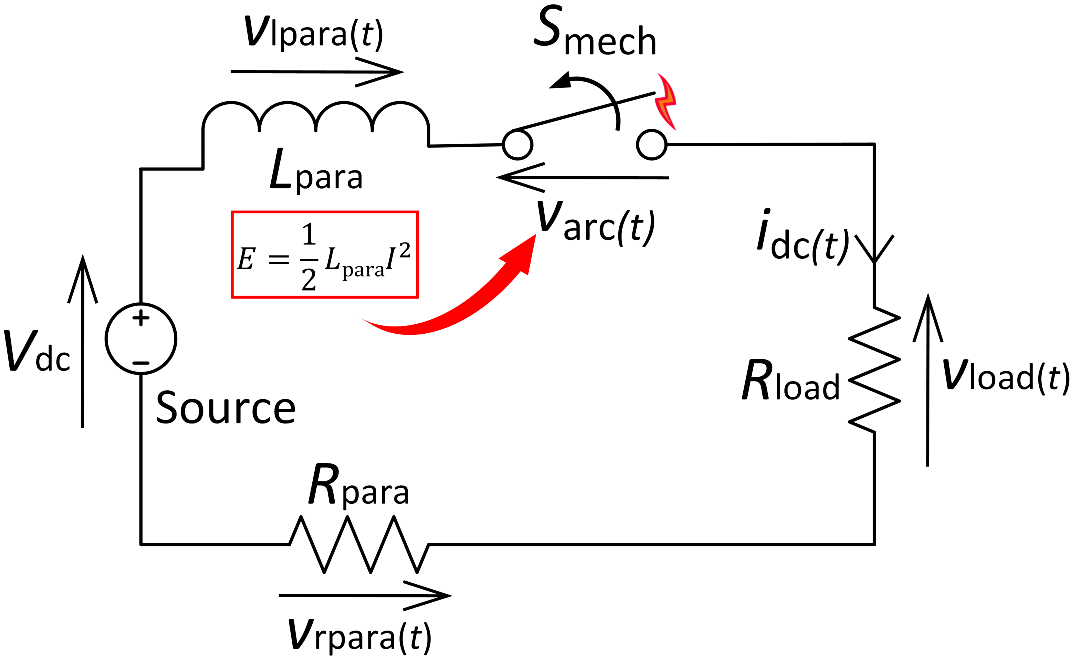


Figure 5.12: Simple DC circuit illustrating the generation of an electric arc during circuit opening

v_{arc} is the arc voltage (V),
P_0 is the constant cooling power (W),
τ_{m} is the Mayr time constant (s).

The Cassie model assumes a constant arc voltage V_c and is more suitable for high-current arcs sustained over a longer duration—typically several tens of milliseconds:

$$\frac{1}{g}\frac{\mathrm{d}g}{\mathrm{d}t} = \frac{1}{\tau_{\mathrm{c}}}\left(\frac{v_{\mathrm{arc}}}{V_{\mathrm{c}}} - 1\right) \tag{5.23}$$

where:

g is the arc conductance (S),
v_{arc} is the arc voltage (V),
τ_{c} is the Cassie time constant (s),
V_{c} is the reference arc voltage (V),

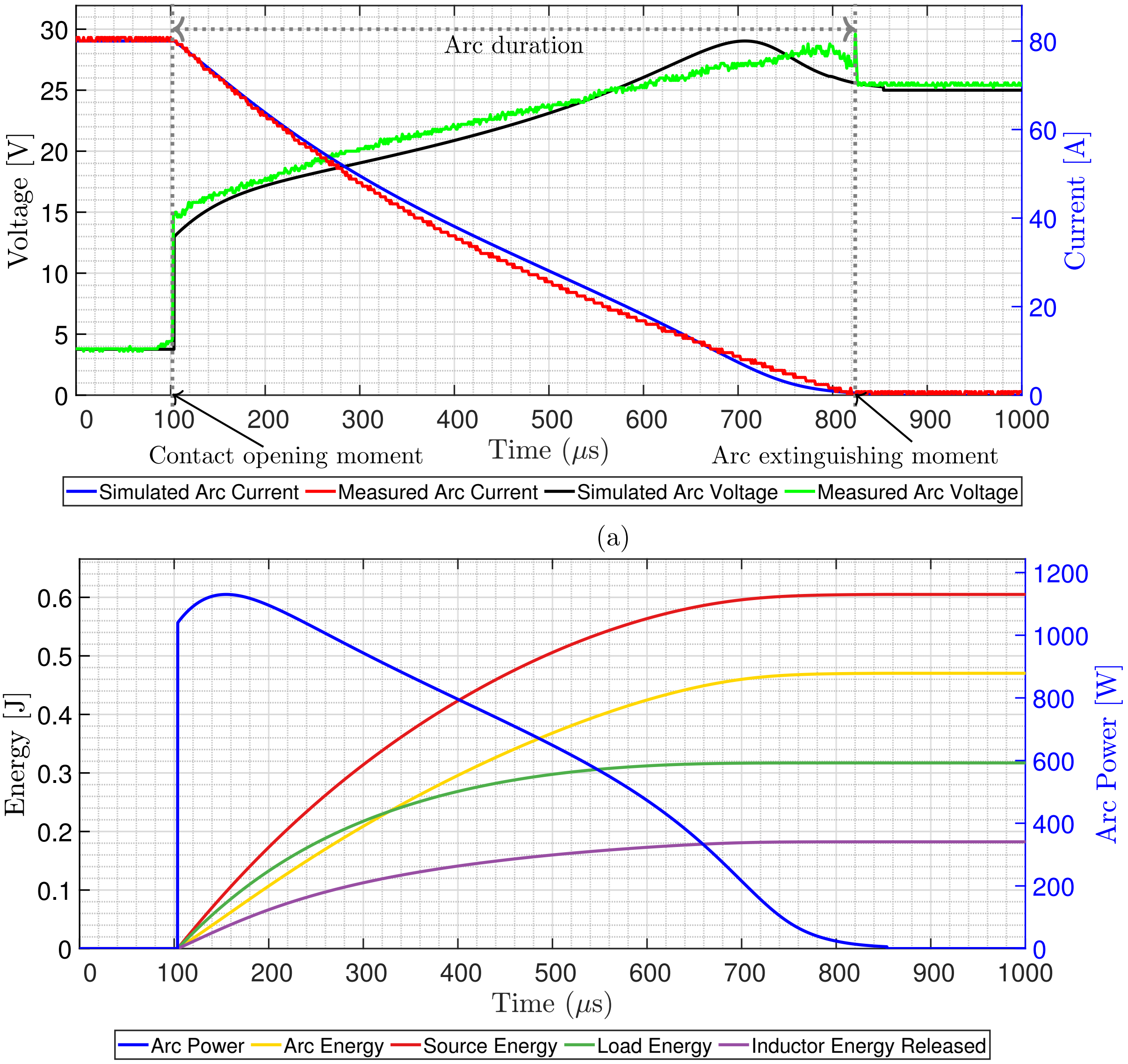
However, these models describe the arc only after its generation, and do not account for the initial characteristics of arc formation.

The Mayr model is selected for this research, as it closely aligns with most experimental results. The parameters P_0 and τ_{m} are determined based on experimental observations. In the original Mayr model, P_0 is assumed constant, as the model was developed for low currents. However, for an 80-A arc, this assumption does not hold, and the cooling power constant—the rate at which the arc dissipates energy to its surroundings—is modified as shown in the following equation, with cooling power expressed in watts. And the Mayr time constant is defined as 40 μs. Cooling power and the arcing time constant were obtained from limited experimental arc voltage and current values.

$$P_0 = 400 + 14\, i_{\mathrm{dc}}(t) \tag{5.24}$$

The initial arc voltage (approximately 13 V) is not predicted by the Mayr model, as the model describes the arc only after it is generated. Therefore, it is manually added to the simulated waveforms. An attempt was made to modify Mayr's equation to represent this initial arc voltage; however, this adversely affected the original equation and disrupted its energy balance property. Consequently, the value is manually inserted into the simulation. Figure 5.13(a) shows the simulated arc-current (blue trace) and voltage (black trace) alongside the experimental waveforms (in red and green). The MATLAB code will be provided in Appendix A.

Figure 5.13(b) illustrates the variation of arc power with time and the energy distribution in the DC circuit. The red trace represents the energy supplied by the DC source during the arc duration, and the purple trace represents the energy released from the line inductance. The yellow and green traces depict the energy dissipated through the arc and



(a)

(b)

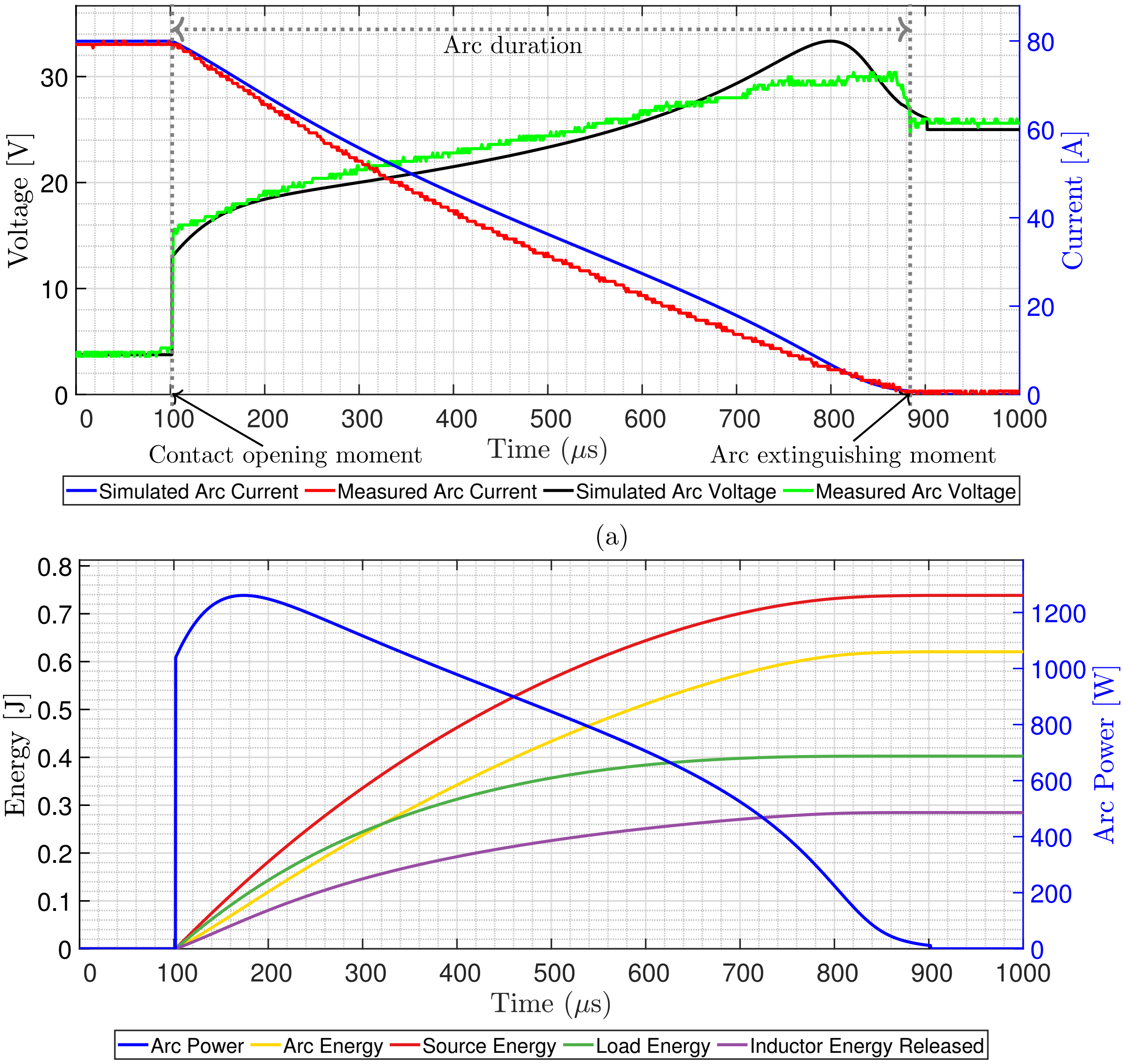
Figure 5.13: Arc characteristics without SCA^{2}M. (a) Comparison of arc current and voltage characteristics between simulation and experimental observations; (b) arc power and energy distribution across the circuit elements during the arcing period.

the energy dissipated through the load, including parasitic resistance, during the arcing period. The energy supplied by the source and the stored energy in the line inductance are dissipated through the arc and the resistive elements in the DC loop.

The simulated and experimental results show that the arc current persists for approximately 700 μs during normal arcing operation without SCA^{2}M. The arc current exhibits a nearly exponential decay, as shown in Fig 5.13(a). This behaviour depends on the type of load. For inductive loads, the waveform may exhibit an exponential growth shape. A detailed discussion of the arc current and voltage characteristics based on Mayr's arc model with respect to different load types and cooling power, can be found in [113].

The normal arc was described earlier. After connecting the coupled transformer, whose primary and secondary windings have self-inductance of 3.6 μH and 27.2 μH respectively, the SCA^{2}M technique is integrated with the arc model to obtain simulation results. Inserting the coupled transformer increases the total DC loop inductance from 57 μH to 89 μH (57 μH + 27.2 μH + 4.8 μH), a 56% (< 60%) increase, where 4.8 μH represents the secondary leakage inductance of the transformer winding. This additional inductance prolongs the arc, as shown by the simulated and experimental results in Fig. 5.14. The SC voltage is maintained at zero to highlight the increase in arcing time.

The cooling power constant is slightly increased in this case, as shown in the following equation, and the arcing time constant is reduced from 40 μs to 35 μs.



(a)

(b)

Figure 5.14: Arc characteristics with the coupled transformer connected and the SC subcircuit deactivated ($V_{\mathrm{SC}} = 0$). (a) Comparison of arc current and voltage characteristics between simulation and experimental observations; (b) arc power and energy distribution across the circuit elements during the arcing period.

$$P_0 = 450 + 14\, i_{\mathrm{dc}}(t) \tag{5.25}$$

The increase in inductance due to the added transformer raises the arcing time by approximately 80 μs. This arcing time difference does not scale linearly with inductance, as numerous other factors—such as contact surface condition—affect the results. Further research is required to establish a precise relationship between arcing time and line inductance.

In SCA^{2}M technique, increasing the SC voltage reduces the arcing time. The arc characteristics are illustrated with a 14-V SC pulse applied, activating the SC subcircuit. The corresponding results are shown in Fig. 5.15, where the red and green traces represent the experimental arc current and SC path current, respectively, and the blue and black traces represent the corresponding simulation results.

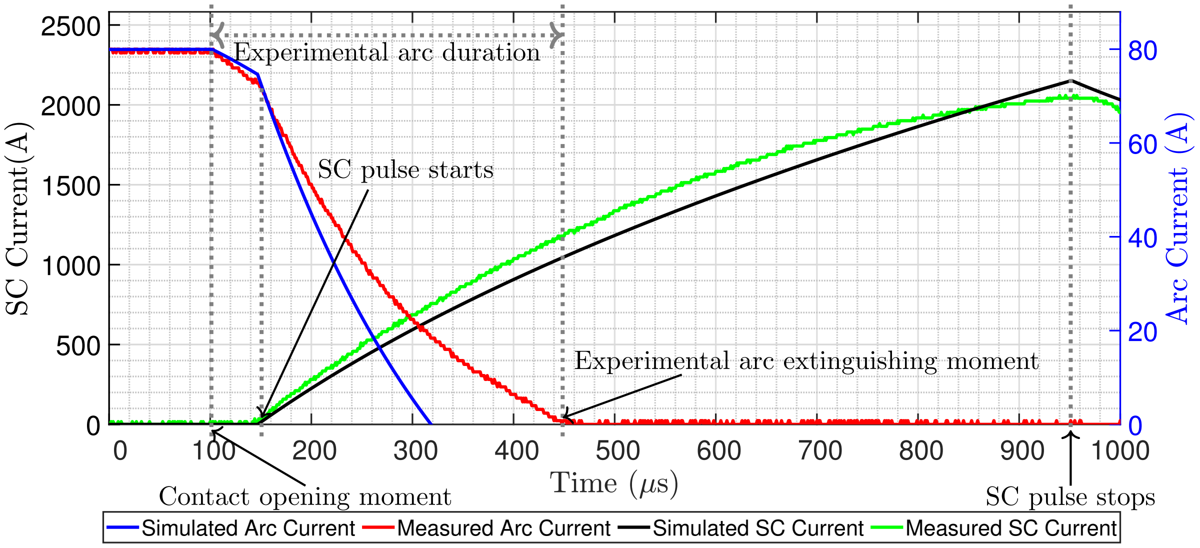


Figure 5.15: Arc-current and SC-current waveforms with the SC subcircuit activated with V_{SC}=14 V

The arc current is extinguished within 350 μs according to the experimental results, representing a 50% reduction from 700 μs. The corresponding arc energy reduction is calculated as 55% based on experimental values. It should be noted that a delay of approximately 50 μs occurs before the SC current is initiated after the arc forms (when the CB begins to open). This delay can be adjusted by controlling the circuit parameters associated with the MOSFET driver circuit, as discussed in subsection 5.1.6.

The simulation results differ from the experimental observations throughout Figs. 5.13, 5.14, and 5.15 due to the following reasons:

- The arc model assumes uniform plasma, fixed geometry, and constant cooling and arcing time. However, these parameters vary during the arc, and specifically near extinction, the arc becomes unstable (transitions from a thermally sustained plasma to rapid deionisation), the plasma narrows and becomes non-uniform, and the conductance drops in a non-exponential way
- The arc model was originally formulated with two constants - cooling power and arcing time constant - for arcs near, but not at, the moment of extinction or ignition. Here it is modified by treating cooling power as a variable and arcing time as a constant (though in reality it changes dynamically), with both derived from a limited set of experimentally measured arc voltage and current values for the 80 A prototype
- Additionally, the internal characteristics of the breaker, such as contact surface condition, erosion, and oxidation, affect the arc parameters, none of which are accounted for in the model.

Specifically, the discrepancies between the simulation and experimental results shown in Fig. 5.15 can be attributed to the following reasons, in addition to those mentioned earlier:

- The difference between the red and blue curves is mainly due to the varying arc resistance, which is assumed to be fixed in the simulation
- The difference during the arcing period between the green and black curves is mainly because the voltage $e_{\mathrm{dcp}}(t)$ was neglected, which if included, would increase the total SC current
- The difference at the final stage between the green and black curves is mainly due to the assumed constant inductance factor of 225 nH/T^2 for the powdered iron core, whereas in reality it varies from 225 ± 8% to 256 ± 8% with reducing DC bias
- The arc voltages with and without the SCA^{2}M technique are assumed to be identical during the arcing period, as further explained with reference to Fig. 5.16.

Figure 5.16 demonstrates that the assumption mentioned above is reasonable: the figure compares experimental arc-voltage waveforms with (blue trace) and without (black trace) the SCA^{2}M, showing that the arc voltage is closely similar during the arcing period with the SCA^{2}M. Note that the coupled transformer is connected in both cases where $V_{\mathrm{SC}} = 0$ for the black trace and $V_{\mathrm{SC}} = 14$ V for the blue trace. For the experiment, the MOSFET in the primary loop was turned on approximately for $800\,\mu$s. As shown in Fig. 5.16, the MOSFET turns off at approximately $950\,\mu$s, having been turned on at $150\,\mu$s. When the MOSFET turns off, the SC energy pulse starts disappearing from the primary winding, which consequently affects the arc voltage as shown in the Fig. 5.16.

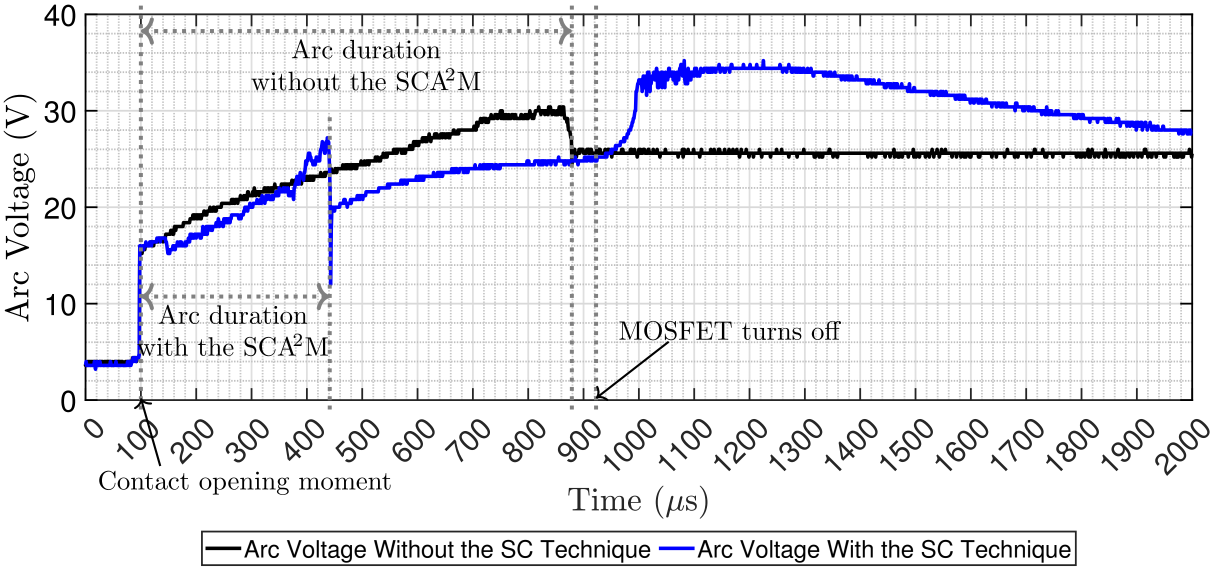


Figure 5.16: Experimental arc voltages without and with the SCA²M technique

As described earlier, the SC subcircuit is activated simultaneously with CB opening, subject to a slight delay. The MOSFET that connects the SC is driven by a self-driven gate driver. The selection of the MOSFET and the gate driver design are explained in the following subsections.

5.1.4 MOSFET Switch Selection

Figure 5.17 shows the LR circuit where L_1 and R_1 denote the total loop inductance and resistance seen by the SC pulse source, respectively. The corresponding values are $L_1 = (0.9{+}3.6)\ \mu\text{H}$ and $R_1 = 2.8\ \text{m}\Omega$ as given in the Table 5.2. Therefore the time-constant τ of the LR circuit is 1.6 ms.

The SC loop current-pulse duration is assumed to be 1 ms for the worst case, as the experimental arcing time is 700 μs. The SC current $i_{\text{sc}}(t)$ is calculated as 2324 A

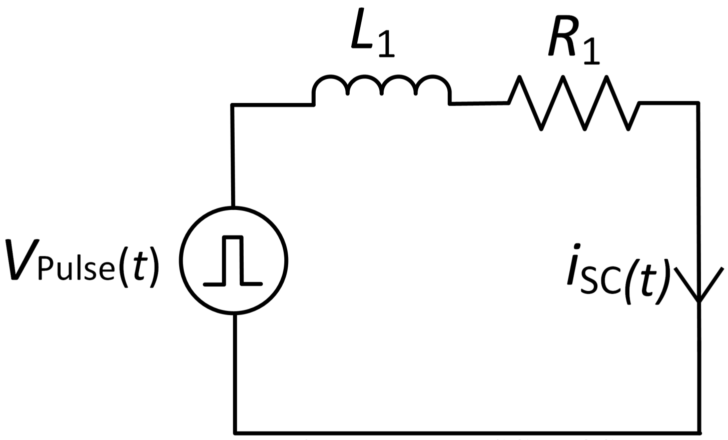


Figure 5.17: LR circuit referring to the SC–MOSFET loop

at 1 ms. Consequently, a high-pulse-current-capable MOSFET, IXFX520N075T2, is selected, as briefly discussed in Subsection 5.1.1.2. Given the MOSFET's peak current rating of 1350 A, at least two MOSFETs must be connected in parallel to share the current. With two MOSFETs in parallel, each handles a peak current of $2324/2 = 1162$ A. For a 1-ms peak current duration, the energy dissipated through each MOSFET is $1162^2 \times 2.2 \times 10^{-3} \times 10^{-3} = 2.97$ J, which is slightly below the MOSFET's maximum pulse energy rating of 3 J. Therefore, two MOSFETs are connected in parallel. Additionally, during MOSFET turn-off, the energy must be carefully absorbed, so four TVS diodes (1.5KE15CA) (AppendixB.4) are connected in parallel with each MOSFET.
A printed circuit board (PCB) is designed using the software EasyEDA, where the schematic and PCB layout provided in Appendix B.1 and Appendix B.2, respectively.

5.1.5 TVS Diode Selection

Since the SC voltage is maintained at 14 V, the selected TVS diode must have a breakdown voltage higher than 14 V, but not excessively so, as a much higher rating would delay its triggering. Therefore, the 1.5KE15CA TVS diode is used, which has a trigger voltage of 15 V. Four diodes are used per MOSFET, based on the maximum pulse energy absorption capability of a diode.

5.1.6 MOSFET Driver Circuit

The initial arc voltage during CB opening is used to generate the MOSFET driver control signal. The circuit diagram of the MOSFET driver prototype is shown in Fig. 5.18, where Q_1 is the main MOSFET, connected in series with the SC bank.

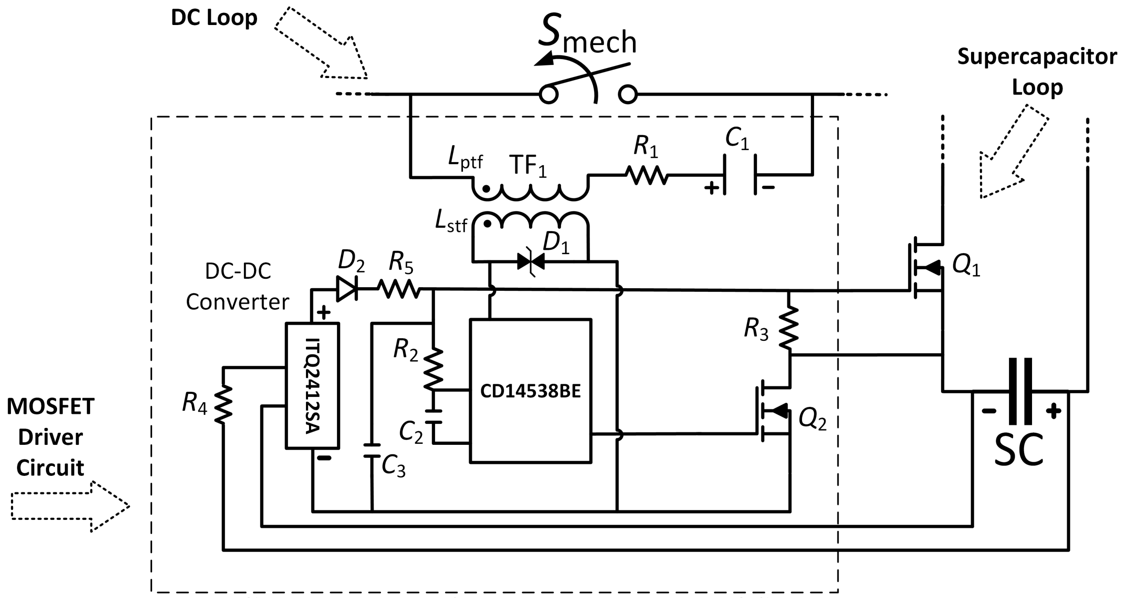


Figure 5.18: Control circuit for generating the MOSFET gate drive signal

An RLC branch, comprising the primary winding inductance L_{ptf} of a 48/230 V small power transformer TF_1, connected in parallel with the CB, S_{mech}. An electrolytic capacitor C_1 prevents short-circuiting of the CB. The resistance R_1 in the RLC branch influences the delay time for generating the SC current after the CB begins to open; reducing R_1 decreases this delay.

For low-rated CBs, such as the 6-A MCB used in this research, the resistance R_1 must be relatively high (2.7 kΩ). Otherwise, the circuit becomes overly sensitive to the rising fault current, as a larger portion of the initial fault current enters the RLC branch and charges C_1 quickly compared to the current flowing through the CB. This causes the main MOSFET to activate and trigger the SC pulse before the CB opens, which is an undesirable outcome. For higher-rated CBs, R_1 can be reduced because the lower on-resistance of the CB ensures that the initial fault current entering the RLC branch remains smaller than the current through the CB, thereby maintaining proper coordination.

Alternatively, this behaviour presents a promising direction for future research toward an enhanced version of SCA^{2}M technique, as it enables MOSFET activation based solely on fault current rise rather than arc-voltage detection across the CB. However, in such a scenario, the CB may not trip properly due to current reduction caused by SCA^{2}M. This approach warrants further investigation.

The secondary winding of the transformer, with inductance L_{stf}, is connected in parallel with a TVS diode (1.5KE6.8CA). During CB opening, the initial arc voltage of approximately 13 V drives TF_1 and triggers the TVS diode. Due to the high impedance and thus limited power transfer capability of TF_1, the voltage clamped by the TVS diode is insufficient to directly drive high-power MOSFETs. The duration of the voltage pulse generated by the TVS diode also depends on the arcing time, as the arc voltage is directly linked to the transformer primary winding voltage. To address these issues and precisely control the gate drive pulse duration, an additional secondary MOSFET, Q_2 (as shown in Fig. 5.18), and a monostable multivibrator (CD14538BE) are used. By adjusting the resistor R_2 and capacitor C_2, the pulse duration Δt can be tuned according to equation 5.26, where R_{x} represents the effective path resistance from the DC-DC converter to R_2 as shown in Fig. 5.18. The DC-DC converter module, ITQ2412SA is used (Appendix C.3) to power the auxiliary MOSFET (Q_2) and the multivibrator. The DC input to the converter is taken from the main SC, as illustrated in Fig. 5.18. The voltage across resistor R_3 drives the main MOSFET, Q_1. This driver circuit provides a clean gate-to-source voltage of approximately 12 V (the converter output) to Q_2 for a duration of Δt.

$$\Delta t = (R_2 + R_{\mathrm{x}}) \times C_2 \tag{5.26}$$

The parameter values used in the gate driver circuit are listed in Table 5.3. The value of Δt is set approximately 800 μs for the prototype circuit.

Table 5.3: Parameters used for the MOSFET driver circuit

Parameter	**Value**
R_1	2.7 kΩ
R_2	6.7 kΩ
R_3	1 kΩ
$R_4 = R_5$	22 Ω
C_1	275 μF
C_2	100 nF
C_3	100 μF

A PCB for the MOSFET driver circuit was designed using the software EasyEDA. The schematic and PCB layout are provided in Appendix C.1 and C.2, respectively.

5.2 Introducing Multiple Transformers to the SCA^{2}M Topology

The effectiveness of the current-reduction technique is further improved by using multiple transformers. Two-transformer configuration is described in this section and can be extended to a greater number of transformers; however, further research is required.

Two configurations are possible for connecting two transformers, as shown in Figs. 5.19 and 5.20. In both cases, the primary windings of the transformers are connected in parallel to absorb more energy from the SC, leveraging its high energy density as discussed in Chapter 4. The secondary windings are connected in parallel in the first configuration and in series in the second. For the analysis, the two transformers are assumed to be identical, and the DC source voltage is not considered.

In the first configuration, shown in Fig. 5.19, the secondary induced voltages $e_{\mathrm{s}}(t)$ are identical for both windings. With the two secondary windings connected in parallel, the total loop resistance and inductance are halved.

The induced current through the load, $i'_{\mathrm{s}}(t)$, is expressed in Eq. 5.27. For overload faults, the load dominates over parasitic elements, enabling simplification (Eq. 5.27) of the equation by neglecting the parasitic resistance and inductance in the DC loop. For a short-circuit fault, where the load is short-circuited, parasitic elements dominate, and the equation can be simplified as shown in Eq. 5.28. This configuration is more effective for short-circuit faults, as it allows the induced current to be doubled.

$$i'_{\mathrm{s}}(t) = \frac{e_{\mathrm{s}}(t)}{(\frac{R_2+jL_2}{2}) + Z} = \frac{2e_{\mathrm{s}}(t)}{(R_2+jL_2)+2Z} \approx \frac{e_{\mathrm{s}}(t)}{Z} \tag{5.27}$$

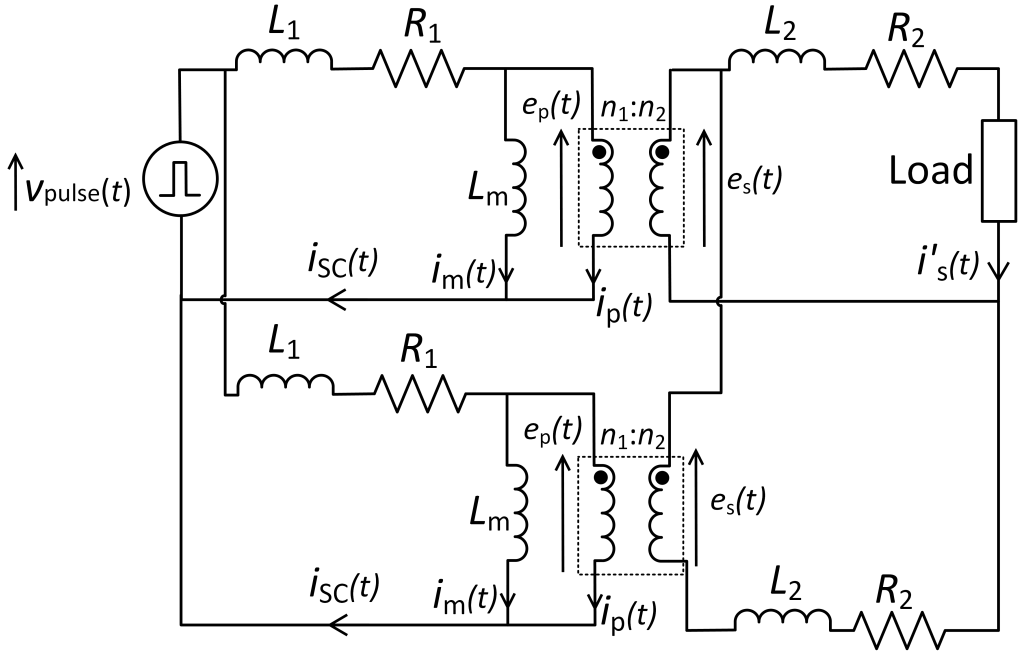


Figure 5.19: Two-transformer-based SCA^{2}M configuration with secondary windings connected in parallel

$$i'_{\text{s}}(t) = \frac{2e_{\text{s}}(t)}{(R_2 + jL_2) + 2Z} \approx \frac{2e_{\text{s}}(t)}{(R_2 + jL_2)} \tag{5.28}$$

The induced current associated with the series-connected transformer configuration, $i''_{\text{s}}(t)$ is given in Eq. 5.29. For overload faults (with the load present), the equation simplifies as shown in Eq. 5.29. For short-circuit faults (with the load short-circuited), the expression simplifies as given in Eq. 5.30. This configuration is therefore suitable for overload faults, as it increases the induced current.

$$i''_{\text{s}}(t) = \frac{2e_{\text{s}}(t)}{2(R_2 + jL_2) + Z} \approx \frac{2e_{\text{s}}(t)}{Z} \tag{5.29}$$

$$i''_{\text{s}}(t) = \frac{2e_{\text{s}}(t)}{2(R_2 + jL_2) + Z} \approx \frac{e_{\text{s}}(t)}{(R_2 + jL_2)} \tag{5.30}$$

As the experimental work in this research is based on a fault scenario that includes the load, the series-connected transformer configuration is the preferred choice.

A separate experiment was conducted to validate this modification strategy. Figure 5.21 presents the experimental arc voltages and arc currents for all scenarios. The top figure shows the arc currents: the green trace corresponds to the case without a coupled transformer; the blue trace represents a single transformer with the SC subcircuit deactivated, where the arcing time increases slightly; the brown trace shows the reduced arcing time with a single transformer when the SC subcircuit is activated using a 14-V

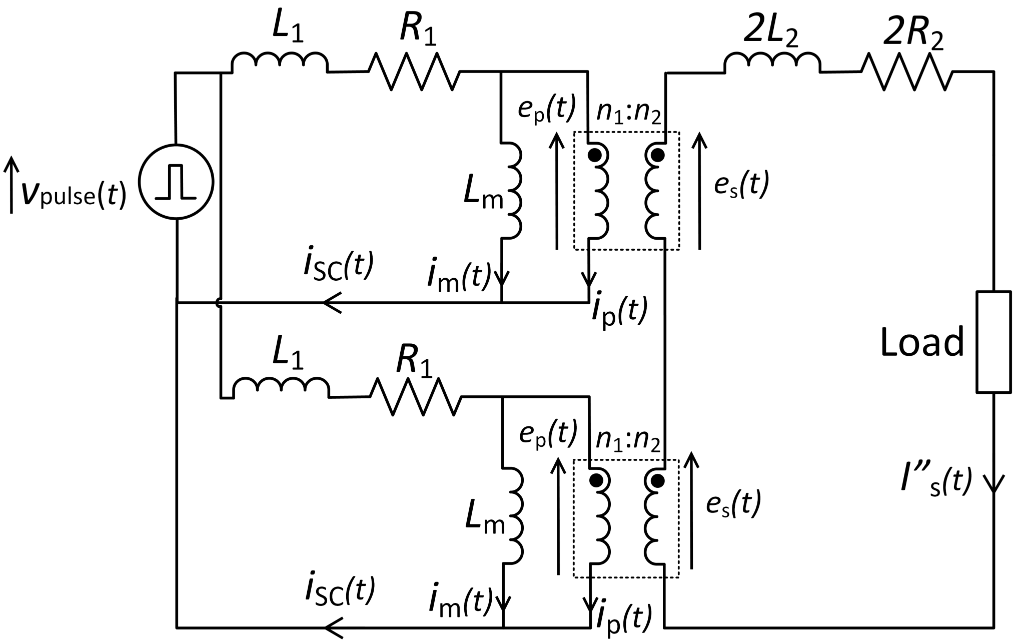


Figure 5.20: Two-transformer-based SCA^{2}M configuration with secondary windings connected in series

SC voltage pulse; the black trace corresponds to two transformers with the SC subcircuit deactivated; and the red trace shows a significant reduction in arcing time when the SC subcircuit is activated for the two-transformer configuration with a 14-V SC voltage pulse. The bottom figure illustrates the corresponding arc voltages using the same colour

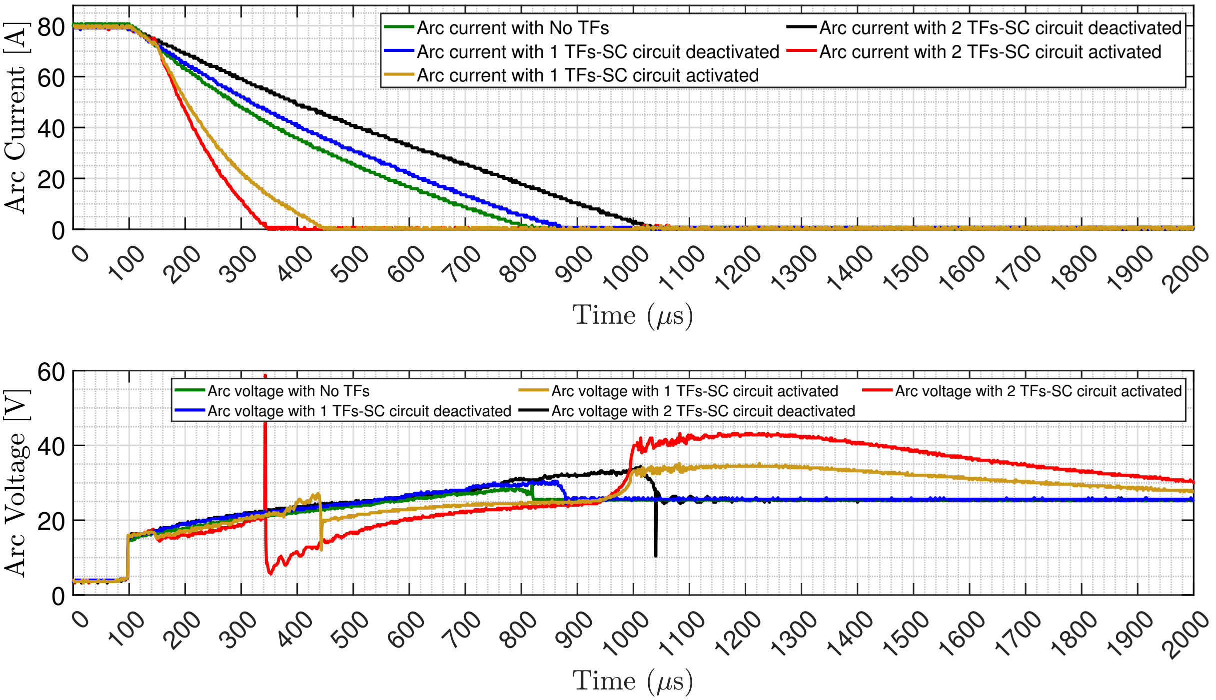


Figure 5.21: Arc current (top figure) and arc voltage (bottom figure) characteristics for all scenarios

scheme.

By using two transformers, the arcing time is further reduced from 700 μs (no transformer connected) to 250 μs, compared with 350 μs in the single-transformer case. This corresponds to a 50% arcing time reduction with a single transformer and a 64% reduction with two transformers. The corresponding arc energy reduction is calculated as 67% for the two-transformer-based implementation, based on experimental values.

5.3 Conclusion for the Chapter 5

The new SCA^{2}M technique is presented, and analytical and simulation exercises were carried out. The results are compared with experimental observations from the 2-kW prototype circuit. The analysis and experimental work are further extended to the two-transformer case—a modification that increases the induced current, as detailed in this chapter. The arc was visually captured by the author and subsequently analysed for incremental SC voltage steps from 0 V to 14 V; these results will be presented in the next chapter. Additionally, the SCA^{2}M technique is implemented in higher-power DC systems up to 21 kW to verify its scalability, with those results will also be reported in the next chapter.

Chapter 6

SCA^{2}M Operation: Arc Visualisation and Further Results

This chapter presents further experimental results of the SCA^{2}M technique, including arc visualisation for the 2-kW prototype under different SC voltages, and extends the evaluation to high-power-rated DC systems up to 21 kW, concluding the work.

6.1 2-kW Circuit Prototype

The prototype circuit for demonstrating the SCA^{2}M approach is shown in Fig. 6.1, and a zoomed-in view of the CB is shown in Fig. 6.2 for clarity. In addition to the main SC bank associated with the SCATEP, another SC bank is used as the DC source, as shown in the Fig. 6.1. A SC bank is chosen as the DC source instead of a switched-mode DC power supply because it provides a high DC current at low voltage, and it delivers a clean DC voltage and current without noise that could interfere with the oscillograms. Initially,

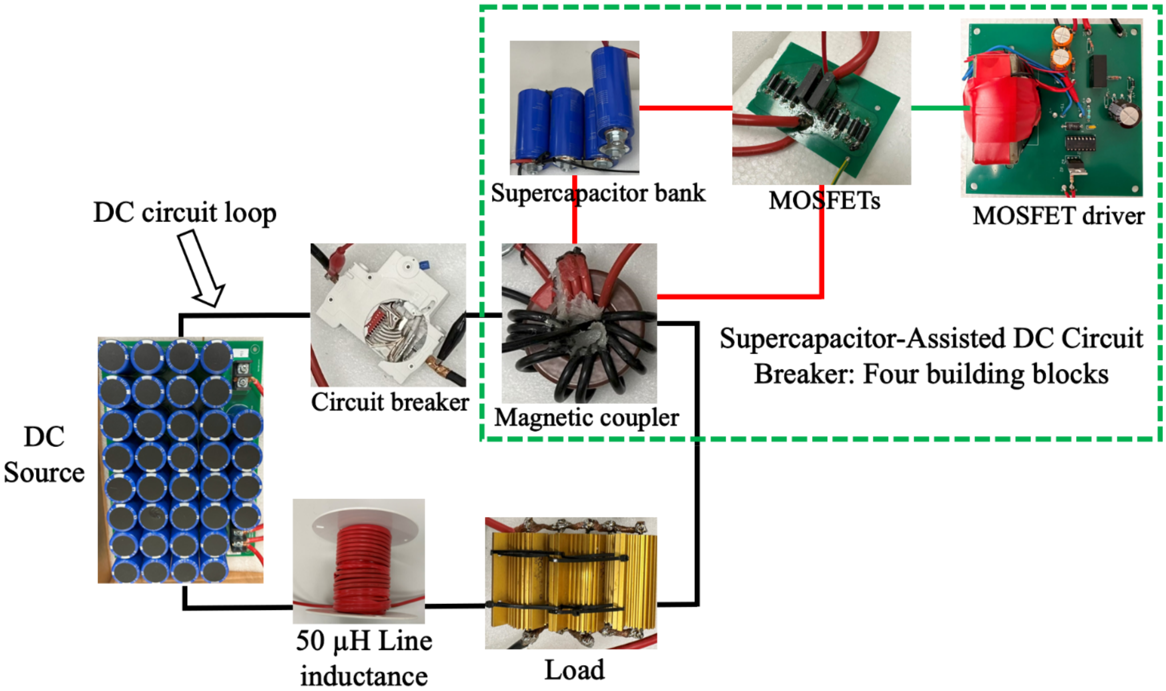


Figure 6.1: Laboratory prototype for the 80-A/25-V/2-kW SCA^{2}M implementation

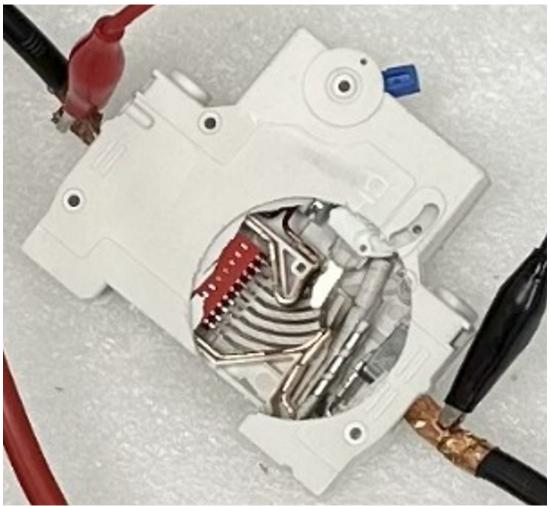


Figure 6.2: Circuit breaker used in the SCA^{2}M implementation

a 6-kW DC power supply was used for this purpose. However, due to severe noise that significantly distorted the oscillograms, its use was discontinued. A 6-A MCB is used for the main breaker, with its plastic cover modified to allow visualisation of the arc as illustrated in Fig. 6.2. The same experiment was also conducted with different types of CBs, and it was observed that the condition of the contact points—used or brand new—affects the operation of the SCA^{2}M prototype, as the on-resistance of a CB changes with use. Results associated with this are provided in subsection 6.2, and this aspect should be further analysed in future work.

For the current measurements, a Tektronix-A622 current probe was used, capable of measuring DC currents up to 100 A. However, in the SC–MOSFET path (loop creating the SCATEP operation), the DC current reaches the kiloampere range. To address this, a current divider was implemented in which the 8-AWG wire was split into identical strands arranged symmetrically to avoid introducing unwanted inductance. The current divider is illustrated in Fig. 6.3. This approach is applicable to both AC and DC to high-current

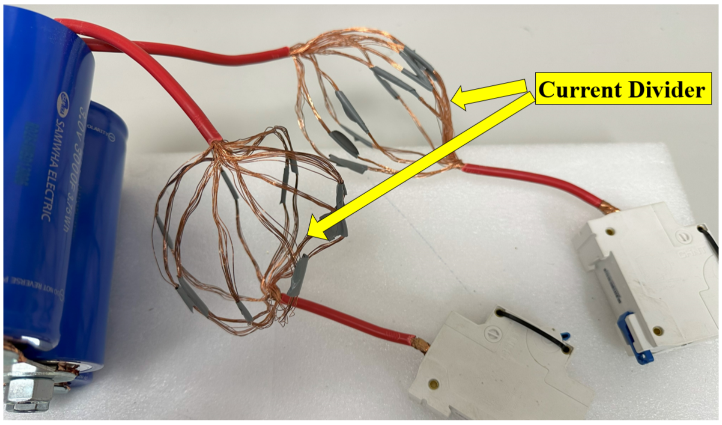


Figure 6.3: Current divider arrangement used for high-current measurement in the SCA^{2}M prototype.

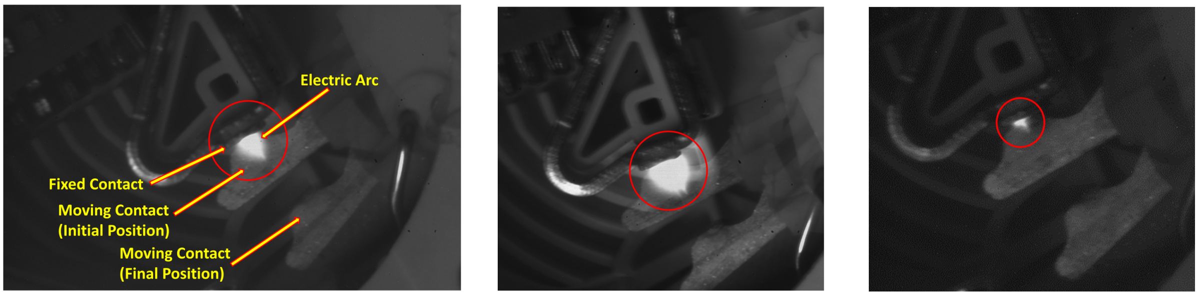
measurement scenarios, and can be tuned for high-precision measurements, potentially eliminating the need for costly current measurement instrumentation.

Two separate wires are used for the two MOSFETs to reduce loop resistance, and two safety breakers are placed in these paths, as illustrated in Fig. 6.3.

6.2 SCA^{2}M Arc Visualisation

Experiments were conducted with different CBs, including used and new MCBs rated at 6 A. The results in Chapter 5 are based on a used 6-A MCB, achieving a 50% arcing time reduction with a single transformer and a 64% arcing time reduction with two transformers. Using a different and used 6-A MCB with a 600-μs, 14-V pulse applied to the MOSFET under similar conditions, the following results are presented. The visible electric arcs were captured using a BASLER acA1920-150μm camera. By using a higher exposure time, the cumulative arc intensity is recorded for each scenario, as shown in the arc figures throughout this chapter.

Three images in Fig. 6.4 illustrate the variation in the visible arc with and without the SCA^{2}M technique applied. Figure 6.4(a) shows the visible arc when a 6-A MCB trips under an 80-A fault current, with a corresponding arcing time of 680 μs.



(a) (b) (c)

Figure 6.4: Electric arc generated during CB opening in an 80-A/25-V/2-kW DC system using a generic 6-A MCB. (a) Pure arc; (b) arc with a coupled transformer at zero SC voltage; (c) arc with a coupled transformer at 14-V SC voltage.

Panel(b) illustrates the arc when the coupled transformer is inserted with zero SC voltage. The arc duration and visibility increase due to the additional inductance from the transformer winding, with the arcing time extending from 680 to 850 μs. Panel(c) shows reduced arc intensity when the SC voltage is increased to 14 V. The corresponding arcing time decreases from 680 to 360 μs, representing a 47% reduction in arc duration.

Figure 6.5 illustrates the visible arcs as the SC voltage increases from 0 to 14 V in 1 V increments. Corresponding arcing times are shown above each arc image, with the percentage change relative to the reference indicated below.

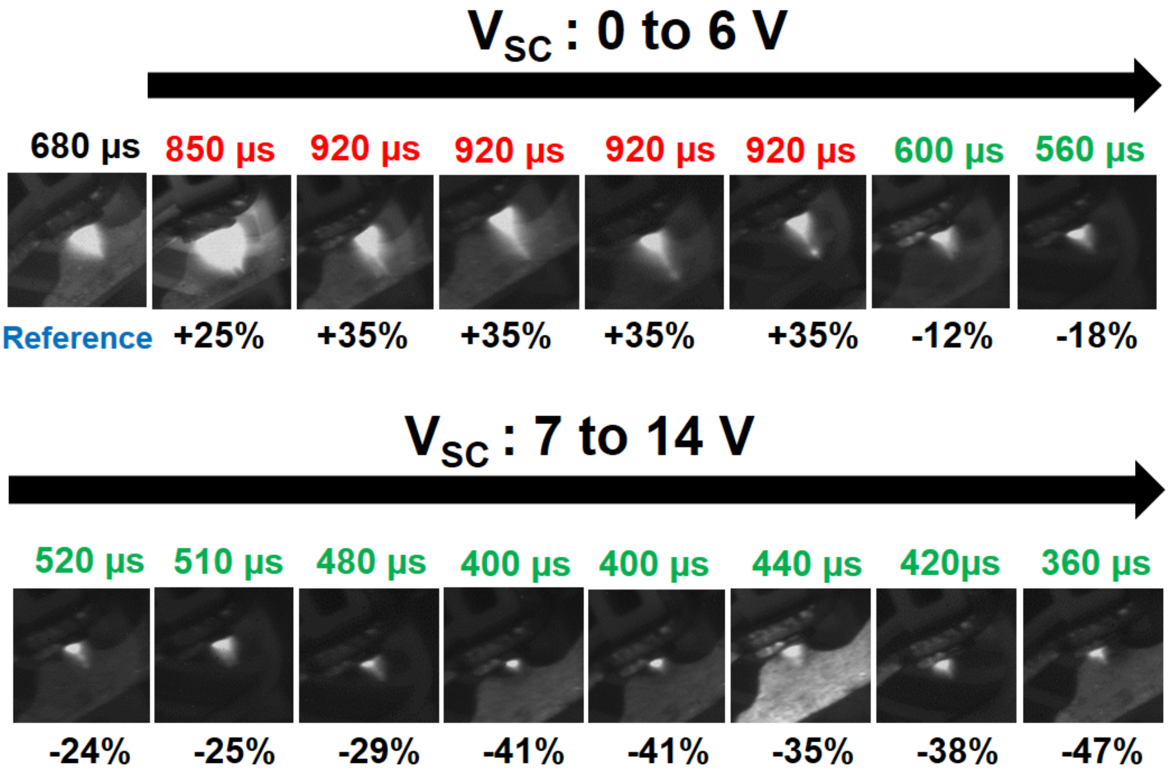


Figure 6.5: Changes in arc intensity as the SC voltage increases from 0 V to 14 V. Arc duration deviations from the reference are indicated: red denotes increased arcing time, green denotes reduced arcing time. Percentage changes are shown below each image.

Arc images with red duration values indicate an increase in arcing time relative to the reference of 680 μs—the arcing time without the SC subcircuit, shown in the top left corner of Fig. 6.5. Those with green values denote a reduction compared to this reference. When the coupled inductor-based subcircuit is connected to the DC loop without triggering the SC ($V_{\mathrm{SC}} = 0$), the arcing time increases by 25% to 850 μs, as depicted in the second image from the top left in Fig. 6.5. For SC voltages between 0 V and 4 V, the arcing time exceeds the reference due to the increased total loop inductance introduced by the coupled transformer, which is not sufficiently compensated by these low SC voltages. A slight discrepancy can be observed between measured arcing times and arc visibility when comparing the reference image with the sequence of four images corresponding to SC voltages of 1–4 V. This occurs because, at low SC voltages, arcing time is extended due to arc current rebound: the arc initially diminishes and then intensifies again as the SC provides insufficient pulse energy, as illustrated in Fig. 6.6. Although the arcing time increases due to this arc current rebound, the corresponding charges associated with the arc are low compared to the zero SC voltage scenario. The area under the arc current–time graph for zero SC voltage in Fig. 6.6 is higher than the corresponding area under the arc current curve associated with SC voltages of 1 V to 4 V. Therefore, the captured image of this behaviour over time results in the arc intensity observed at zero SC voltage appearing more energetic than the longer-lasting arcs recorded for V_{SC} values

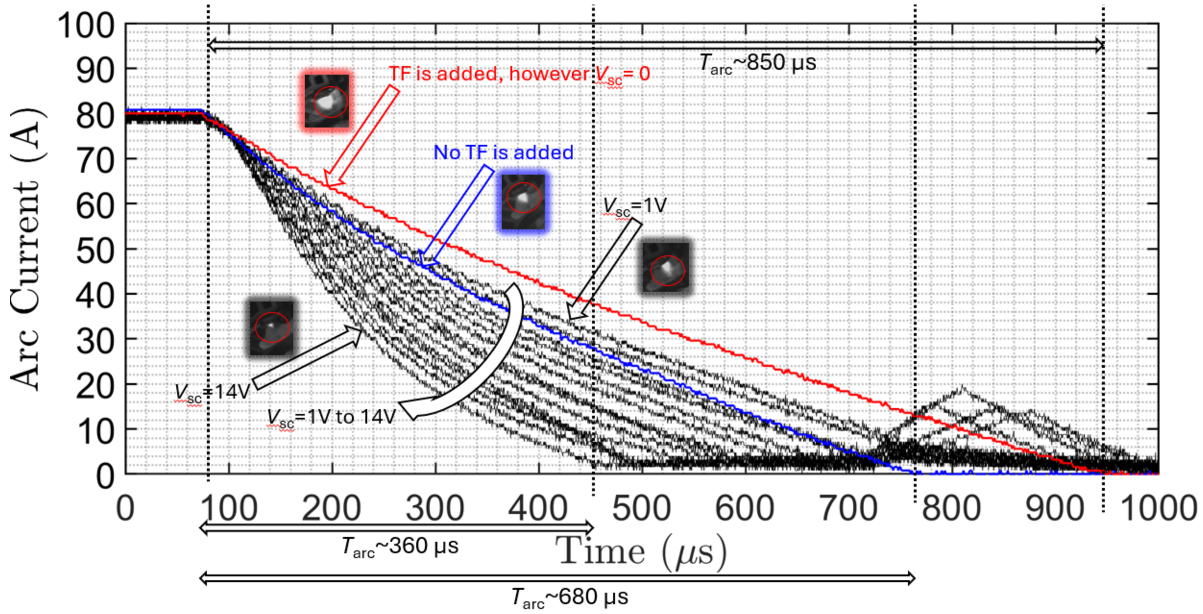


Figure 6.6: Experimental arc-current waveforms for the single-transformer configuration

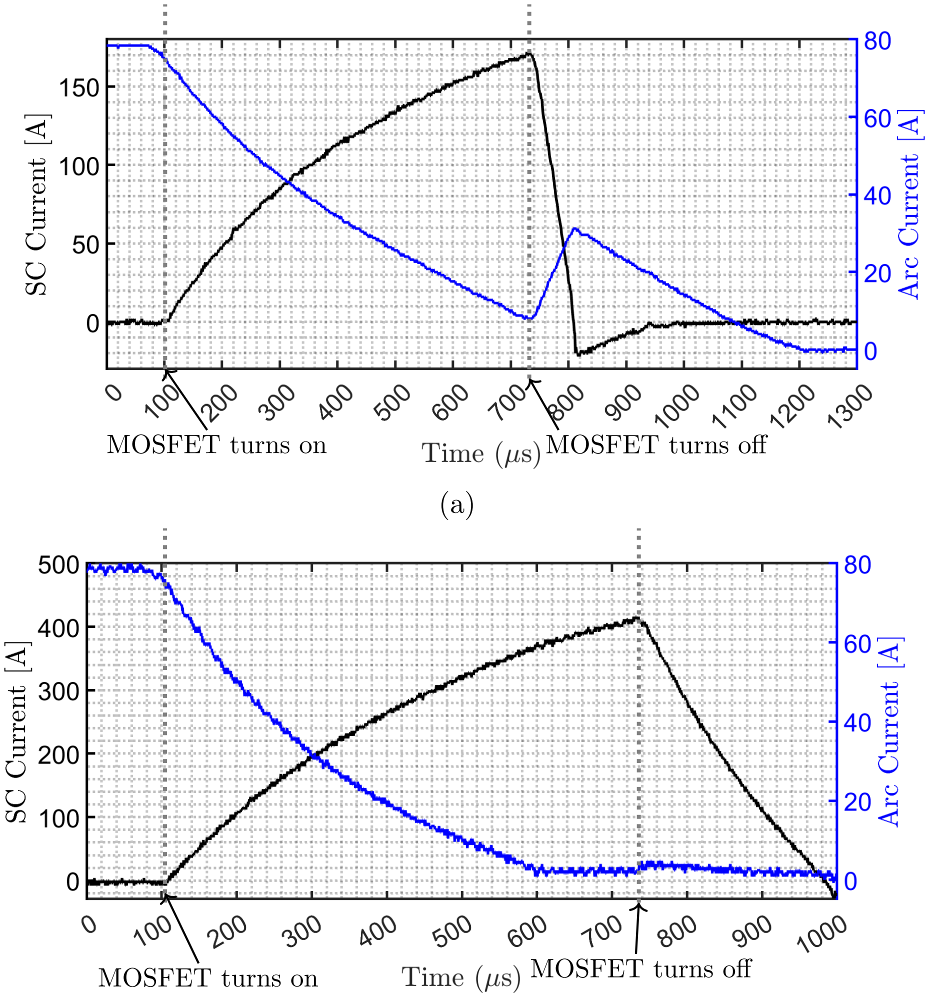
between 1 V and 4 V. At a SC voltage of 5 V, the arcing time decreases relative to the reference, with further reductions as the voltage increases from 5 V to 14 V.

Figure 6.6 presents experimental arc-current waveforms corresponding to the visible arcs shown in Fig. 6.5. The blue trace represents the arc-current waveform without the coupled transformer connected, giving an arcing time of 680 μs. The red trace shows the arc-current when the coupled transformer is added but the SC loop is inactive; arcing time increases to 850 μs due to the added inductance. Fourteen black traces depict the arc currents for SC voltages ranging from 1 V to 14 V. At lower SC voltages, the arc current reappears after approaching near zero, indicating arc rebound. Arcing time decreases with increasing SC voltage.

The arc rebounds because, at lower SC voltages, the applied SC pulse stops before the arc is extinguished. This is a consequence of the fixed SC pumping time, where the MOSFET on-time was set to 600 μs for the experiments associated with figures 6.4–6.10.

Fig. 6.7 presents the experimental results for SC voltages of 2 V (top) and 6 V (bottom). At an SC voltage of 2 V, the SC current ceases to flow during the arc interruption process. Specifically, the MOSFET is switched off at approximately 740 μs, after which the SC current decays through the TVS diode connected in parallel with the MOSFET. As the SC current decays, the voltage induced in the secondary winding reverses polarity, becoming the same polarity as the source voltage, and consequently acts to sustain the remaining arc. Under these conditions, the arc can no longer be suppressed and instead begins to rebound. The behaviour of the remaining arc is governed by the combined influence of the source voltage and the induced voltage generated by the decaying SC current.

However, when the SC voltage is 6 V, the SC current continues to be pumped until the arc is fully extinguished; therefore, the arc does not rebound.

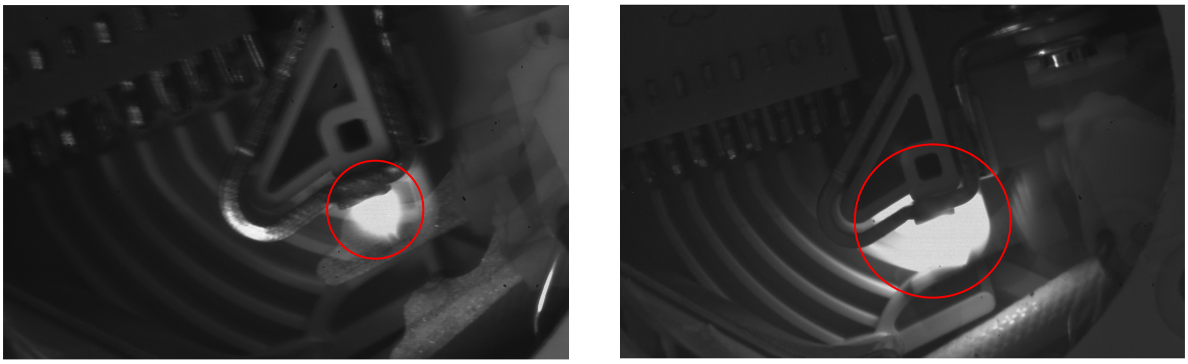


(a)

(b)

Figure 6.7: Arc current and SC current behaviour for SC voltages of (a) 2 V and (b) 6 V

Two images shown in Fig. 6.8 compare the visible arcs for the single-transformer and two-transformer cases with the SC subcircuit inactivate ($V_{\mathrm{SC}} = 0$). Figure 6.9 illustrates the visible arc for the two-transformer case as the SC voltage varies from 1 V to 14 V.



(a) (b)

Figure 6.8: Electric arc generated during CB opening at zero SC voltage. (a) With one coupled transformer inserted; (b) with two coupled transformers inserted.

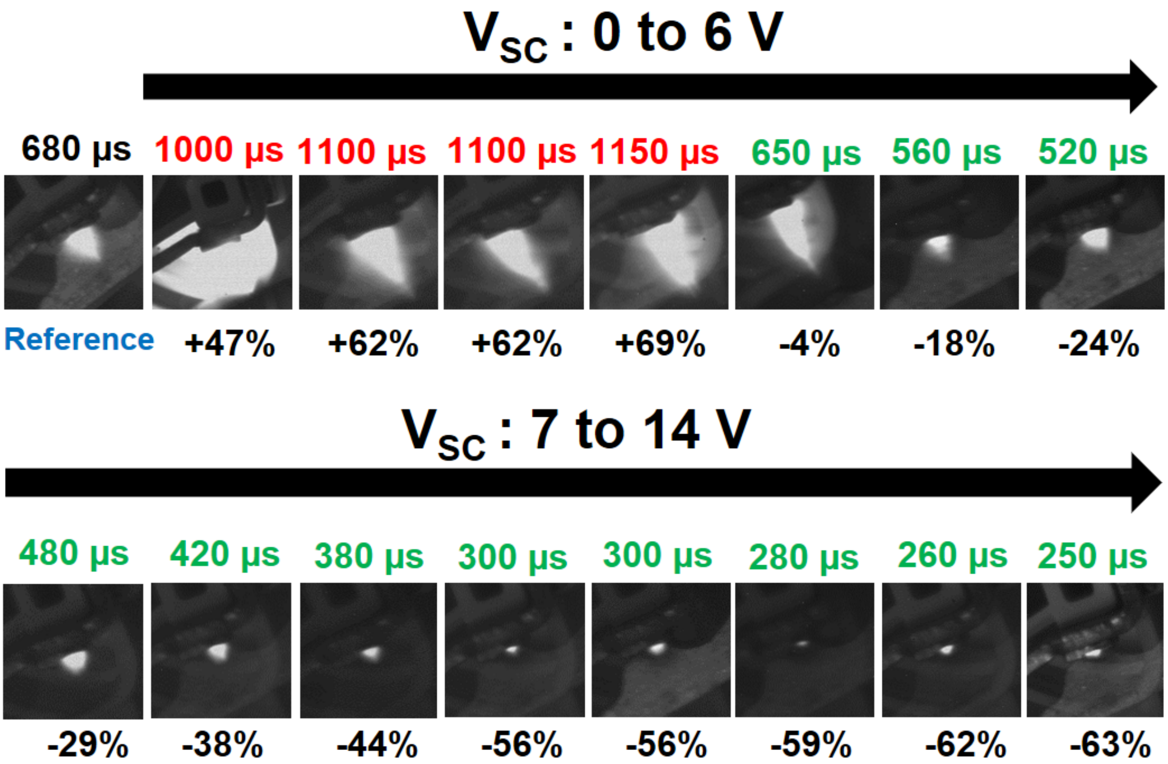


Figure 6.9: Arc variation as the SC voltage increases from 0 V to 14 V in the two-transformer case where arc duration deviations from the reference are indicated: red denotes increased arcing time, green denotes reduced arcing time. Percentage changes are shown below each image.

The arcing time reduction is 63% for the two-transformer configuration. Figure 6.10 presents experimental arc-current waveforms corresponding to the visible arcs in Fig. 6.9 for the two-transformer configuration.

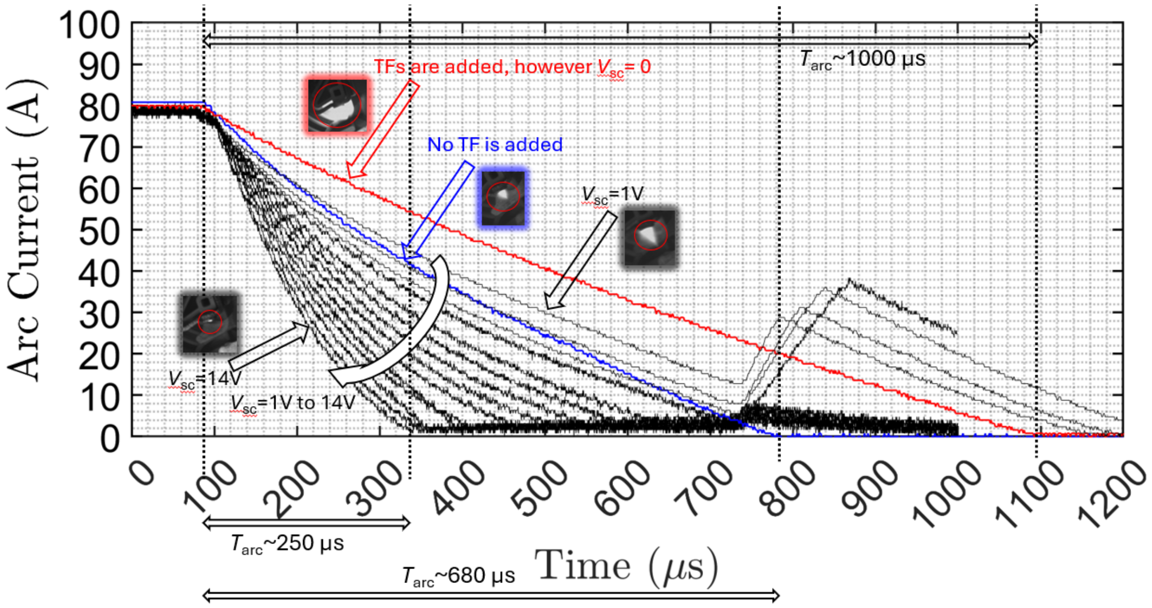


Figure 6.10: Experimental arc-current waveforms for the two-transformer configuration

The blue trace shows the arc current without the coupled transformer connected, with an arcing time of 680 μs. The red trace shows the arc current when the two coupled transformers are added but the SC loop is inactive; arcing time increases to 1000 μs due to the added inductance. Fourteen black traces depict the arc currents for SC voltages ranging from 1 V to 14 V. At lower SC voltages, the arc current reappears after approaching near zero, indicating arc rebound. Arcing time decreases with increasing SC voltage.

When a new 6-A MCB was used, arcing times were significantly reduced, as summarised in Table 6.1. Condition indicates usage status (new or used). The column titles are defined below.

- t_{arc}: original system without SCA^{2}M
- t_{arc1}: one transformer but without activating SC subcircuit
- t_{arc1SC}: one transformer; SC subcircuit activated at 14 V
- p_1: percentage reduction with one transformer and $V_{\text{SC}} = 14$ V
- t_{arc2}: two transformers but without activating SC subcircuit
- t_{arc2SC}: two transformers; SC subcircuit activated at 14 V
- p_2: percentage reduction with two transformers and $V_{\text{SC}} = 14$ V

When comparing the results in Table 6.1, the condition of the CB's contact points—such as contact resistance and mechanical wear—is a significant factor influencing arcing times. However, arcing time reduction percentages are consistent for the SCA^{2}M in both the single and two-transformer cases. This analysis could be strengthened through further research on CBs of different ratings and types. In the next subsection, the author presents summarised results of applying SCA^{2}M to higher DC voltage and current systems to demonstrate scalability for the single-transformer case.

Table 6.1: Summary of results for three 6-A MCBs

Condition	$t_{\textbf{arc}}$ (μs)	$t_{\textbf{arc1}}$ (μs)	$t_{\textbf{arc1SC}}$ (μs)	p_1	$t_{\textbf{arc2}}$ (μs)	$t_{\textbf{arc2SC}}$ (μs)	p_2
Worn MCB #1 (chapter 5)	700	780	350	50%	940	250	64%
Worn MCB #2 (chapter 6)	680	850	360	47%	1000	250	63%
New MCB (chapter 6)	520	650	260	50%	750	220	58%

6.3 Arc Extinguishing Performance of SCA^{2}M for Different DC Power Systems

Initial validation of SCA^{2}M was conducted on an 80-A/25-V/2-kW DC system to establish proof of concept. Subsequent tests, performed under low and extended operating conditions as presented in Table 6.2, evaluate the scalability of SCA^{2}M to higher-power systems.

Table 6.2: Arc quenching capability results for SCA^{2}M from experimental data using the single-transformer configuration

Tested DC system	**Arcing time without SC suppression (µs)**	**Arcing time with SC suppression (µs)**	**Durations reduction (%)**
48 A/12 V/576 W	220	130	41
80 A/25 V/2 kW	680	360	47
120 A/35 V/4.2 kW	1100	750	32
170 A/50 V/8.5 kW	1500	1000	33
210 A/100 V/21 kW	4000	3600	10

These results show that SCA^{2}M performance decreases with increasing DC system voltage and current ratings. This is because, as the system rating increases, SCA^{2}M parameters must also be scaled. This can be achieved by: (i) increasing the SC bank voltage, (ii) improving the magnetic properties of the transformer or using multiple transformers, and (iii) reducing the parasitic resistance and inductance in the primary SC loop. These three approaches will be further discussed in the Future Directions chapter.

In the presented work, the primary SC current reaches nearly 2 kA using five 3000-F/3-V SCs connected in series. Generally, a single short-circuited 3000-F/3-V SC can deliver up to approximately 10 kA due to its very low ESR of 0.23 mΩ. Therefore, with proper design and fine tuning, the SCA^{2}M technique has strong potential to become a superior arc extinguishing method, owing to the high current delivery capability of SCs.

6.4 Conclusion

The novel supercapacitor-assisted arc management (SCA^{2}M) proposed in this thesis was inspired by the patented supercapacitor-assisted surge absorber (SCASA). The success of the method relies on the non-invasive injection of a momentary pulse energy into the DC loop via a transformer. This approach demonstrates that low-voltage SCs can be used effectively to extinguish arcs in DCCBs, thereby enhancing the lifetime of mechanical CBs in DC applications.

Experimental SCA^{2}M results were analysed using images of the electric arc obtained from a 2-kW DC prototype circuit. Additional experiments were conducted at higher voltages and currents to assess the scalability of SCA^{2}M. The achievements of this research and the directions for future work will be presented in the final chapter.

Chapter 7

Achievements and Future Research Directions

This research introduces a novel application of SCs in DCCBs. The results demonstrate that SCs can effectively control electric arcs and manage arcing duration during circuit interruption. Researchers and manufacturers are encouraged to further investigate this approach. Future work should focus on testing SCs in higher-voltage and higher-current DC systems and integrating them with existing breaker technologies. Ultimately, this SC-based method has the potential to enable more reliable and efficient DCCBs for applications in renewable energy, electric vehicles, and power grids.

7.1 International Research Collaborations

The successful demonstration of the SCA^{2}M prototype was observed by the Head of the Research and Development team at Sécheron Hasler in Geneva, Switzerland—a pioneering DCCB manufacturer for DC railway systems. During his visit to the University of Waikato, an opportunity arose for a five-week research visit to Sécheron from 1 May to 8 June 2025. This visit proved to be one of the most valuable experiences of my academic journey. During this period, I designed a fast fault-current detection circuit for their upcoming DCCB. Additionally, I had the opportunity to visit the Fraunhofer Research Institute in Germany by invitation—one of the world's largest applied research organisations. During the same visit, I presented part of a tutorial on supercapacitor techniques for protecting DC systems, appliances, and microgrids, and also presented my ninth conference paper at the 7th IEEE International Conference on DC Microgrids (IEEE-ICDCM) in Estonia.

7.2 Future Research Directions

This research, conducted over nearly three and a half years as a PhD project, has investigated the suitability of SCs for arc management in DCCBs. A second PhD project has already commenced, building on this foundation to enhance the performance of the current implementation and develop a functional prototype for higher-voltage DC systems. Several unexplored aspects of SCA^{2}M technique have been identified for further investigation, as listed below.

- With regard to increasing the SC bank voltage, designing a boost converter into the SC stage to increase its DC voltage could be explored in future research.
- SCs are an excellent source for producing very high currents. Even with a 3-V, 3000-F SC, it is possible to generate approximately 10 kA. If a technique can be developed to pass this large current through an inductive loop and then abruptly disconnect it using high-current (very low voltage) rated MOSFETs just before the circuit breaker opens, very high voltages could potentially be generated. This could serve as a promising starting point for developing a simple yet powerful voltage-boosting technique, as an alternative to complex high-power boost converters.
- Also the SCs are becoming increasingly popular and are attracting growing research interest. The future development of higher-voltage-capable SCs would allow this approach to perform considerably better than current implementations permit.
- With regard to the enhancement of magnetic properties, the SCA^{2}M technique can be improved by increasing the magnetising inductance. The author initially attempted to use ferrite cores with higher permeability, which provides a higher magnetising inductance and thereby limits the magnetising current. A separate degaussing coil was also explored to avoid magnetic saturation of the core; however, this approach was unsuccessful. Further research is warranted to properly optimise the magnetic design, with the aim of increasing the magnetising inductance without going into saturation, so that more energy drawn from the SC bank can be efficiently delivered to the secondary side.
- With regard to reducing the resistance in the primary SC loop, the performance depends on how much voltage can be transferred to the primary winding of the transformer from the SC terminal voltage. This is limited by the $2.8\,\text{m}\Omega$ primary winding resistance and $0.9\,\mu\text{H}$ primary winding inductance in the proposed $2\,\text{kW}$ prototype. Since the ESR of the SC bank is $1.15\,\text{m}\Omega$ (0.23×5) and the MOSFET on-resistance is in the range of a few milliohms, careful design could reduce the $2.8\,\text{m}\Omega$ resistance to nearly the ESR of the SC bank by connecting MOSFETs in parallel. This would enable more voltage to be transferred to the primary winding and allow higher currents to be drawn from the SC bank.
- The duality between SCASA and the new SCA^{2}M technique remains conceptual and has not been validated theoretically or experimentally; this aspect requires further investigation.
- A dedicated charging unit and voltage monitoring system are required to maintain the SC bank's voltage.

- The relationship between the electric arc and the DC loop parameters—such as source voltage, line inductance, line current, and arcing time—requires further analysis, as the precise dependencies have not been established.
- The same experiment was also conducted with similar types of older and newer circuit breakers, and it was observed that the breaker's properties—such as on-resistance and wear and tear of the internal mechanical actuators—affect the arcing times. This influence should be further investigated using a wider range of CB types.
- Initial arc voltage is used to trigger the SC path in the SCA^{2}M technique. However, a current-feedback mechanism detecting the fault current could also be used to activate the SC path, potentially offering faster response times.
- Authors identified two operational modes for the SCA^{2}M technique: (i) forward-mode operation and (ii) flyback-mode operation. The first mode is analysed in this thesis, although it is not explicitly referred to as "forward–mode". In forward-mode operation, part of the SC's energy is directly fed into the primary transformer winding and transferred to the secondary winding. In flyback-mode operation, part of the SC's energy is first stored in the magnetising inductance of the transformer and subsequently returned to the main DC loop. This flyback-mode warrants further analysis.
- SCA^{2}M uses a pre-charged SC to inject pulse energy into the DC loop. However, an alternative approach—using a fully discharged SC to absorb arc energy—may also be feasible. This method was attempted by the author but did not yield a viable solution due to the SC's very low DC rated voltage, which does not permit leaving connected across the CB contact pair.
- The two-transformer configuration was implemented and yielded successful results in this research; however, further investigation with proper tuning is required to assess its scalability as the number of connected transformers increases.
- SCA^{2}M was developed primarily for mechanical circuit breakers; however, the technique can be further extended to solid-state and hybrid DCCB variants.

Appendix A

MATLAB Code

The important sections of the MATLAB simulation code are included in this appendix.

A.1 MATLAB Code for the Transformer Turns Ratio Selection

The following code was used to generate Fig. 5.9.

```
clear all; close all; clc;

% Define symbolic variables
syms s t real
assume(t >= 0);

% Parameters
x1 = 0;
x2 = 1200e-6;

% Font size
f = 20;

% Transformer primary turn values
n1_values = [1, 2, 3, 4, 5, 10];
num_n1 = length(n1_values);

% Primary loop resistance
r = 2.8e-3;

% Primary loop leakage inductance matrix
l_primary_leak =[
[0.05, 0.05, 0.05, 0.05, 0.05, 0.05, 0.05, 0.05, 0.05, 0.05, 0.05,
    0.04, 0.04, 0.04, 0.04, 0.04]*(10^-6);
[0.18, 0.18, 0.18, 0.18, 0.18, 0.18, 0.18, 0.18, 0.18, 0.17, 0.16,
    0.15, 0.15, 0.13, 0.12, 0.11]*(10^-6);
[0.41, 0.41, 0.41, 0.41, 0.41, 0.40, 0.39, 0.38, 0.37, 0.35, 0.32,
    0.28, 0.24, 0.21, 0.18, 0.14]*(10^-6);
[0.73, 0.73, 0.73, 0.73, 0.73, 0.68, 0.65, 0.64, 0.62, 0.54, 0.45,
    0.35, 0.28, 0.23, 0.14, 0.11]*(10^-6);
[1.14, 1.14, 1.14, 1.14, 1.11, 1.00, 0.97, 0.93, 0.89, 0.71, 0.55,
    0.40, 0.22, 0.11, 0.00, 0.00]*(10^-6);
[4.57, 4.57, 4.57, 4.57, 4.07, 2.83, 2.21, 1.95, 1.59, 0.44, 0.00,
    0.00, 0.00, 0.00, 0.00, 0.00]*(10^-6);
];

% Define MOSFET's OFF time
a = 1050e-6;

% SC pulse
Vin(t) = 14 * (heaviside(t - 250e-6) - heaviside(t - a));
```

```
% SC pulse from Laplace domain
Vin_s = laplace(Vin(t), t, s);

% n_values = turns ratio values
n_values = [0.2, 0.4, 0.6, 0.8, 1, 2, 2.5, 2.75, 3, 4, 5, 6, 7, 8,
   9, 10];
num_n = length(n_values);

% Defined colours for the plots
cmap = [
0 0 0;             % black
0.894 0.102 0.110; % red
0.216 0.494 0.722; % blue
0.302 0.686 0.290; % green
0.596 0.306 0.639; % purple
1.000 0.498 0.000; % orange
0.651 0.337 0.157; % brown
0.968 0.505 0.749; % pink
0.121 0.466 0.705; % sky blue
0.090 0.745 0.811; % teal
0.737 0.741 0.133; % olive
0.682 0.780 0.909; % light blue
0.800 0.475 0.655; % violet
0.933 0.400 0.000; % dark orange
0.5 0.5 0.5;       % grey
1 1 0              % bright yellow
];

% Inductance factor values (Permeance values)
Al_base = [
[258, 258, 258, 258, 258, 258, 258, 258, 258, 258, 255, 245, 240,
   240, 235, 230]*(10^-9);
[258, 258, 258, 258, 258, 258, 255, 250, 250, 240, 230, 210, 205,
   190, 175, 160]*(10^-9);
[258, 258, 258, 258, 258, 250,245 ,240 , 235, 220, 200, 175, 150,
   130, 110, 90]*(10^-9);
[258, 258, 258, 258, 258, 240,230 ,225 , 220, 190, 160, 125, 100,
   80, 50, 40]*(10^-9);
[258, 258, 258, 258, 250, 225,220 ,210 , 200, 160, 125, 90, 50,
   25, 0, 0]*(10^-9);
[258, 258, 258, 258, 230, 160, 125 ,110 , 90, 25, 0, 0, 0, 0, 0,
   0]*(10^-9);
];

% Secondary DC loop leakage indutance values
l2_values_leak = [
[0, 0.01, 0.02, 0.03, 0.05, 0.18, 0.29, 0.35, 0.41, 0.73, 1.13,
   1.56, 2.08, 2.72, 3.73, 4.07]*(10^-6);
[0.01, 0.03, 0.07, 0.12, 0.18, 0.73, 1.13, 1.34, 1.59, 2.72, 4.07,
   5.35, 7.11, 8.61, 10.04, 11.33]*(10^-6);
[0.02, 0.07, 0.15, 0.26, 0.41, 1.59, 2.44, 2.89, 3.37, 5.61, 7.97,
   10.04, 11.71, 13.25, 14.19, 14.34]*(10^-6);
[0.03, 0.12, 0.26, 0.47, 0.73, 2.72, 4.07, 4.82, 5.61, 8.61,
   11.33, 12.74, 13.88, 14.50, 11.47, 11.33]*(10^-6);
[0.05, 0.18, 0.41, 0.73, 1.11, 3.98, 6.08, 7.03, 7.97, 11.33,
   13.83, 14.34, 10.84, 7.08, 0.00, 0.00]*(10^-6);
[0.18, 0.73, 1.64, 2.92, 4.07, 11.33, 13.83, 14.72, 14.34, 7.08,
   0.00, 0.00, 0.00, 0.00, 0.00, 0.00]*(10^-6);
];

% Define time vector
t_vec = linspace(x1, x2, 500);

% Y-Axis of the plot
ylabel_str = 'DC Loop Current (A)';
```

```
% Define Y-Axis limits
ylims_all = { [15 82], [-30 82], [-40 82], [-40 82], [-40 82],
   [-15 82]};

figure('Position', [1950, -240, 1890, 1034], 'Color', 'w');

% plot all the graphs
for i_n1 = 1:num_n1
    ax(i_n1) = nexttile;
    hold on;
    grid on;
    box on;

    n1 = n1_values(i_n1);

    for i_n = 1:num_n
        n = n_values(i_n);
        color = cmap(i_n, :);

        % ---------- Compute Transformer parameters ----------

        % Primary loop inductance
        l = 0.26e-6 + l_primary_leak(i_n1, i_n);

        % Inductance factor
        Al = Al_base(i_n1, i_n);

        % Magnetising inductance
        Lm = Al * n1^2;

        % Secondary loop inductance
        l2 = 50e-6 + 7e-6 + l2_values_leak(i_n1, i_n);

        % Secondary loop resistance
        r2 = (312.5e-3);

        % Referred to primary secondary impedance
        Z_s = (r2 / n^2) + (l2 / n^2) * s;
        Z3_s = (Lm * s * Z_s) / (Lm * s + Z_s);

        % Total impedance referred to primary side
        Zt_s = Z3_s + l * s + r;

        % Primary winding current
        Ip_s = (Vin_s / Zt_s) * (Lm * s / (Lm * s + Z_s));

        % Primary winding current in time domain
        Ip(t) = ilaplace(Ip_s, s, t);

        % DC Loop parameters
        Vdc = 25;
        Idc = Vdc / r2;

        % Plot data
        y_data = Idc - double(subs(Ip(t), t, t_vec)) / n;

        plot(t_vec * 1e6, y_data, 'LineWidth', 1.8, 'Color',
           color);
    end

    xlabel('Time ($\mu$s)', 'Interpreter', 'latex');

    % Label Y-Axis only the leftmost column subplots
    if mod(i_n1, 3) == 1
        ylabel(ylabel_str, 'Interpreter', 'none');
    end

    % Plot Titles
```

```
    title(['$n_1 = ' num2str(n1) '$'], 'Interpreter', 'latex',
       'FontSize', f);

    ax(i_n1).FontSize = 14;
    ax(i_n1).LineWidth = 1.2;

    ylim(ax(i_n1), ylims_all{i_n1});
end

% Shared legend
lgd = legend(arrayfun(@(n) ['$n=' num2str(n) '$'], n_values,
   'UniformOutput', false), ...
'Interpreter', 'latex', 'FontSize', 20, 'NumColumns', 8);
lgd.Layout.Tile = 'south';
lgd.Box = 'on';

% Export to EPS image
set(gcf,'Renderer','painters');
print(gcf,'-depsc2','-r600','subplot_results.eps');
```

The following part of the code was used to generate the supercapacitor current illustrated in Fig. 5.11, with the turns ratio n=2.75 and primary winding turns n_1=4. The other three plots were generated using the equations already presented in the preceding code.

A.2 MATLAB Code for the SC current

```

% Magnetising current
Im_s = (Vth_s / (Lm * s));

% Convert to time domain

% Primary current
Ip(t) = ilaplace(Ip_s, s, t);

% Magnetising current
Im(t) = ilaplace(Im_s, s, t);

% Supercapacitor current
It(t) = Ip(t) + Im(t);
```

A.3 MATLAB Code for the Circuit Breaking

The following code simulates a fault condition to demonstrate circuit breaker opening.

```

%% ---------- Circuit Parameters ----------

% Source voltage (25 V)
Vdc_breaker = 25;

% Loop resistance excluding the CB's on-resistance = 265.5 milliohm
R_load = (265.5e-3);

% On resistance of the circuit breaker contacts (47 milliohm )
Ron = 47e-3;
```

```
% Parasitic inductance in the DC loop (57 microhenry)
Ls = 57e-6;

%% ----- Circuit Breaker and Simulation Parameters -----

% Rated current of breaker (6 A)
I_rated = 6;

% Time when load is switched ON (s)
t_on = 0.00098 - 0.000012;

% Total simulation time (6 ms)
t_sim = 0.006;

%% ---------- Magnetic trip settings ----------

% Threshold current to initiate magnetic trip (30 A)
I_magnetic_threshold = 5 * I_rated;

%% ---------- Simulation ----------

% Number of time steps in simulation
N = 25000;

% Time step size (simulation duration divided into N-1 intervals)
dt = t_sim / (N - 1);

% Anonymous function to compute time at step k
t_breaker = @(k) (k-1)*dt;

%% ----- Preallocated Circuit Breaker Simulation Variables -----

% Circuit breaker current over time
I_breaker_vals        = zeros(1,N);

% Terminal voltage across the circuit breaker
Varc_vals             = zeros(1,N);

% Initial terminal voltage = Source voltage
Varc_vals(1)          = Vdc_breaker;

% Breaker resistance state over time
R_breaker_state_vals = ones(1,N)*1e-6;

% Arc conductance over time (S)
g_vals                = zeros(1,N);

% Time vector for each step
t_breaker_vals        = zeros(1,N);

% Time derivative of current (dI/dt) for numerical integration
dIdt_vals = zeros(1, N, 'double');

%% ---------- Trip Variables ----------

% Time when mechanical opening begins
breaker_opening_start_time = 0;

% Flag: true once any trip condition is met
trip_initiated = false;

% Flag: true while trip is being processed
tripping = false;

% Flag: true during mechanical opening phase
breaker_opening = false;
```

The following code was used to model the arc-voltage, arc-current, arc-power, and energy-related waveforms shown in Fig. 5.13.

A.4 MATLAB Code for the Electric Arc

```
%% ---------- Arc Parameters ----------

% Arc time constant (40 microseconds)
tau = 0.040e-3;

% Minimum current below which arc is considered extinguished
Iarc_min = 0;

%% ---------- Arc Function ----------

function [Varc, g_new] = computeArcVoltage(t,...
breaker_opening_start_time, t_breaker_opening_time, Vdc,
breaker_opening, I_breaker, g_prev, dt, tau, ~, Iarc_min)


 % ---------- Persistent variables ----------

 % Was the arc active in the previous time step?
 persistent arc_active_prev;

 % Has the arc ignited for the first time in this opening event?
 persistent first_ignition;

 % ----- Initialize persistent variables on the first call -----

 if isempty(arc_active_prev)

 % Start with no arc
 arc_active_prev = false;

 % No ignition has happened yet
 first_ignition = false;
 end

 % ---------- Time window of physical breaker opening ----------

 % Opening starts here
 t_open_start = breaker_opening_start_time;

 % Opening ends here
 t_open_end   = breaker_opening_start_time +
    t_breaker_opening_time;

 % ---------- Check if the arc should be active now ----------

 % The arc can only exist if the breaker is in the process of
    opening (breaker_opening == true) AND the current time is
    within the opening window

 arc_active_now = breaker_opening && (t >= t_open_start) && (t <
    t_open_end);

 % ---------- Case 1: Before the breaker starts opening ----------

 if ~arc_active_now && t < t_open_start

 % No arc thus, arc voltage is zero
 Varc = 0;
```

```
% Conductance stays the same (no arc to change it)
g_new = g_prev;

% Reset ignition flag (not needed yet)
first_ignition = false;

% Arc is not generated
arc_active_prev = false;

% ---------- Case 2: After the breaker has fully opened ----------

elseif t >= t_open_end

% Arc is gone thus, full supply voltage appears across breaker
Varc = Vdc;

% No conductive path thus, conductance is zero
g_new = 0;

% Reset for next possible opening event
first_ignition = false;

% Arc is extinguished
arc_active_prev = false;

% ---------- Case 3: During the breaker opening window ----------

else

 % Arc is now active
 arc_active_prev = true;

 % ---------- Subcase 3a: First moment the arc ignites ----------

 if ~first_ignition

  % When arc first forms, it jumps to ~13 volts
  V_arc_initial_jump = 13;

  % Check if there's meaningful current
  if I_breaker > 1e-6

  % Set initial conductance using Ohm's law
  g_new = I_breaker / V_arc_initial_jump;
  else

  % Tiny default conductance ia aet if current is nearly zero
     (avoid division by zero)
  g_new = 1e-6;
  end

  % Output the initial arc voltage
  Varc = V_arc_initial_jump;

  % Mark that ignition has happened (only once per opening)
  first_ignition = true;

 % -- Subcase 3b: Arc is already burning (after first ignition) --
 else

  % Determine the cooling power (P0):

  P0 = 400 + 14 * I_breaker;

  % Update arc conductance using the Mayr's Arc model: dg/dt =
     (i^2 / P0 - g) / tau
  dg_dt = (1/tau) * ((I_breaker^2 / P0) - g_prev);

  % Euler method: step forward in time
  g_new = g_prev + dg_dt * dt;
```

```
   % Never let conductance drop below a tiny minimum
   g_new = max(g_new, 1e-6);

   % Compute arc voltage:
   if I_breaker > Iarc_min

   % If current is above minimum needed to sustain arc:

   % Ohm's law: V = I / g
   Varc = I_breaker / g_new;

   else

   % If current is too low, arc can't be sustained:

   % Arc voltage becomes the source voltage (open circuit)
   Varc = Vdc;

   % Arc extinguishes thus, conductance reset to zero
   g_new = 0;
   end
  end
 end
end

%% ---------- Main Simulation Loop ----------

% Loop over each time step from 1 to N
for k = 1:N

 % Save current simulation time
 t_breaker_vals(k) = t_breaker(k);

 % Skip calculations at first time step (k=1) because we need
    previous values
 if k > 1

  %% --- Compute Arc Current, Arc Voltage and Rate of Change of
     Current (di/dt) ---

  % Case 1: Before the (circuit breaker) CB is turned ON (t < t_on)
  if t_breaker_vals(k) < t_on

  % No current flows yet
  I_breaker_vals(k) = 0;
  dIdt_vals(k) = 0;

  % Voltage at breaker terminals equals source voltage (open
     circuit)
  Varc_vals(k) = Vdc_breaker;

  % Case 2: CB is conducting (no trip initiated OR not yet opening)
  elseif ~tripping || ~breaker_opening

  % Use CB's on-resistance (47 milliohms) for closed contacts
  R_breaker_state_vals(k) = Ron;

  % Total circuit resistance = load resistance + breaker resistance
  R_total = R_load + R_breaker_state_vals(k);

  % Use circuit equation: V = L * dI/dt + I * R  -->  dI/dt = (V -
     I*R) / L
  dIdt_vals(k) = (Vdc_breaker - I_breaker_vals(k-1) * R_total) /
     Ls;

  % Update current using Euler integration: I_new = I_old + dI/dt
     * dt
  I_breaker_vals(k) = I_breaker_vals(k-1) + dIdt_vals(k) * dt;
```

```
% Voltage across the CB is just the resistive drop across closed
   contacts
Varc_vals(k) = I_breaker_vals(k) * Ron;

% Case 3: CB is opening (arc is active)
elseif breaker_opening && t_breaker_vals(k) <
   breaker_opening_start_time + t_breaker_opening_time

% Convert previous arc conductance to resistance (avoid division
   by zero)
R_arc = 1 / max(g_vals(k-1), 1e-6);
R_total = R_load + R_arc;

% Compute di/dt
dIdt_vals(k) = (Vdc_breaker - I_breaker_vals(k-1) * R_total) /
   Ls;
I_breaker_vals(k) = I_breaker_vals(k-1) + dIdt_vals(k) * dt;

% Ensure current does not drop below minimum needed to sustain
   arc
I_breaker_vals(k) = max(I_breaker_vals(k), Iarc_min);

% Call arc model to compute arc voltage and new conductance
[Varc_temp, g_new] = computeArcVoltage(...
t_breaker_vals(k), breaker_opening_start_time,
   t_breaker_opening_time, ...
Vdc_breaker, breaker_opening, I_breaker_vals(k), g_vals(k-1),
   dt, tau, [], Iarc_min);

% Save results from arc model
Varc_vals(k) = Varc_temp;
g_vals(k) = g_new;

% Update breaker resistance based on new arc conductance
R_breaker_state_vals(k) = 1 / max(g_vals(k), 1e-6);

% Case 4: After the CB has opened
else

% No current can flow
I_breaker_vals(k) = 0;
dIdt_vals(k) = 0;

% Source voltage appears across open terminals
Varc_vals(k) = Vdc_breaker;

% Set resistance to a very high value (open circuit)
R_breaker_state_vals(k) = 1e6;

% Arc is finished, thus conductance = 0
g_vals(k) = 0;
end

%% ---------- Magnetic Trip Detection ----------

% If CB is not tripped yet AND current exceeds magnetic threshold
if ~trip_initiated && I_breaker_vals(k) > I_magnetic_threshold

% Mark that trip condition was met
trip_initiated = true;

% Begin trip sequence
tripping = true;

% Schedule CB opening to start after a small delay
breaker_opening_start_time = t_breaker_vals(k) +
   t_breaker_open_start_delay;
```

```
end

%% ---------- Handle Breaker Opening and Arc Behavior ----------
if tripping

 % Sub-case A: Time to Initiate CB opening
 if t_breaker_vals(k) >= breaker_opening_start_time &&
    ~breaker_opening

  % Mark that opening has begun
  breaker_opening = true;

  % Initialise arc model at the very first moment of opening
  [Varc_vals(k), g_vals(k)] = computeArcVoltage(...
  t_breaker_vals(k), breaker_opening_start_time,
     t_breaker_opening_time, ...
  Vdc_breaker, breaker_opening, I_breaker_vals(k), g_vals(k-1),
     dt, tau, [], Iarc_min);

 % Sub-case B: CB is opening - continue updating arc
 elseif breaker_opening

  % Update arc voltage and conductance using arc model
  [Varc_vals(k), g_vals(k)] = computeArcVoltage(...
  t_breaker_vals(k), breaker_opening_start_time,
     t_breaker_opening_time, ...
  Vdc_breaker, breaker_opening, I_breaker_vals(k), g_vals(k-1),
     dt, tau, [], Iarc_min);

  % If current is high enough to sustain arc, use arc resistance
  if I_breaker_vals(k) > Iarc_min
  R_breaker_state_vals(k) = 1 / max(g_vals(k), 1e-6);
  else

  % Otherwise, arc is extinguished (open circuit)
  R_breaker_state_vals(k) = 1e6;
  g_vals(k) = 0;
  end

 % Sub-case C: Tripping has started, but opening hasn't begun
    yet (waiting for delay)
 else

 % Keep previous resistance (contacts still closed)
 R_breaker_state_vals(k) = R_breaker_state_vals(k-1);

 % Terminal voltage is just I * Ron (since contacts are still
    closed)
 Varc_vals(k) = I_breaker_vals(k) * Ron;

 % Arc conductance remains unchanged (no arc yet)
 g_vals(k) = g_vals(k-1);
 end

% No trip has occurred, thus CB remains closed
else

 % Only apply closed-breaker behavior after the main switch
    turns on
 if t_breaker_vals(k) >= t_on

 % Low contact resistance
 R_breaker_state_vals(k) = Ron;

 % Voltage drop across contacts
 Varc_vals(k) = I_breaker_vals(k) * Ron;

 % No arc, thus zero conductance
```

```
   g_vals(k) = 0;
   end
  end
 end
end

%% ---------- Arc Power & Energy Analysis ----------

% Compute arc power = Varc * I_breaker
P_arc_vals = Varc_vals .* I_breaker_vals;

% Create mask: 1 during arcing, 0 otherwise
arc_mask = zeros(1, N);
for k = 1:N
 if breaker_opening && ...
  t_breaker_vals(k) >= breaker_opening_start_time && ...
  t_breaker_vals(k) < breaker_opening_start_time +
     t_breaker_opening_time && ...
  I_breaker_vals(k) > Iarc_min
  arc_mask(k) = 1;
 end
end

% Apply mask: only keep power during arcing
P_arc_vals = P_arc_vals .* arc_mask;

% Compute arc energy (Joules) using cumulative trapezoidal
   integration
E_arc_vals = cumtrapz(t_breaker_vals, P_arc_vals);

%% ---------- Analysis for the Energy Balance ----------

% Source power during the arcing time
P_source_during_arc = Vdc_breaker * I_breaker_vals .* arc_mask;

% Total energy supplied by the source during arcing
E_source_arc_total = cumtrapz(t_breaker_vals, P_source_during_arc);

% Power dissipated in load resistor during arcing
P_load_during_arc = (I_breaker_vals.^2 .* R_load) .* arc_mask;

% Energy dissipated in load resistor during arcing
E_load_total = cumtrapz(t_breaker_vals, P_load_during_arc);

%Compute Cumulative Inductive Energy Released During Arcing

% Find indices where arcing occurs
arc_indices = find(arc_mask == 1);

% First index of arcing
k_start_arc = arc_indices(1);

% Last index of arcing
k_end_arc    = arc_indices(end);

%Starting time of the arc
t_start_arc = t_breaker_vals(k_start_arc);

%End time of the arc
t_end_arc    = t_breaker_vals(k_end_arc);

% Initial inductor energy at start of arcing
E_L_initial_val = 0.5 * Ls * I_breaker_vals(k_start_arc)^2;

% Compute inductor energy at each time step: 0.5*Ls*I(t)^2
E_L_instant = 0.5 * Ls * I_breaker_vals.^2;

% Cumulative energy released from inductor at each time t:
E_L_released_cumulative = E_L_initial_val - E_L_instant;
```

```
% Clamp to zero ( to ensure that inductor does not absorb energy)
E_L_released_cumulative = max(E_L_released_cumulative, 0);
```

A.5 MATLAB Code for the Transformer Current Reduction Technique

The following part of the code was used to simulates the SCA^{2}M technique with the defined parameters.

```
%% ---------- TRANSFORMER MODEL ----------

% Define symbolic variables for frequency (s) and time (t)
syms s t;

% Timing parameters for MOSFET switching

% Time when MOSFET turns off (pulse ends)
a = breaker_open_time + 850e-6;

% Core and winding parameters of the transformer

% Inductance per turn squared (Al value)
Al = 225e-9;

% Number of primary turns
n1 = 4;

% Magnetizing inductance of primary
Lm = Al * n1^2;

% Primary loop winding resistance
r = 2.8e-3;

% Primary loop leakage inductance
l = 0.9e-6;

% Turns ratio: secondary / primary
n = 2.75;

%Secondary total loop resistance
r2 = (312.5e-3);

% Secondary winding loop inductance
l2 = 50e-6 + 7e-6 + 4.81e-6;

% Steady-state DC loop current
Idc = Vdc_breaker / R_load;

% Input SC voltage: rectangular pulse from breaker open time
Vin = @(t) 14 * (heaviside(t - breaker_open_time-(45e-6)) -
   heaviside(t - a));


%% -------- Transformer Current Reduction Circuit Analysis --------

% Uses Laplace domain to compute voltages and currents

% Laplace transform of input voltage pulse
Vin_s = @(s) laplace(Vin(t));
```

```
% Referred secondary load impedance to primary side
Z = @(s) (r2 / (n^2)) + (l2 / (n^2)) * s;

% Total impedance calculations in Laplace domain

% Parallel combination of Lm and Z
Z3_s = @(s) (Lm * s * Z(s)) / (Lm * s + Z(s));

% Total impedance referred to the primary loop
Zt_s = @(s) Z3_s(s) + l*s + r;

% Voltage across the magnetizing inductance branch
Ep_s = @(s) (Lm / (l + Lm + r/s)) * Vin_s(s);

% Inverse Laplace to obtain the time domain
Ep_t = @(t) ilaplace(Ep_s(s));

% Convert Ep_t and Es_t (secondary windings' voltage) to a
   numerical function

% Numerical version
Ep_t_num = matlabFunction(Ep_t(t), 'Vars', t);

% Numerical version
Es_t_num = matlabFunction(n*Ep_t(t), 'Vars', t);

% Define a time vector: 1x25000
tvec = linspace(0, t_sim, 25000);

% Evaluate
Ep_t_num_values = Ep_t_num(tvec);
Es_t_num__values = Es_t_num(tvec);
```

A.6 MATLAB Code for the SC Current with the Arc Model and the Arc Management Technique

The following part of the code was used to obtain the supercapacitor current with the SCA^{2}M technique activated, as illustrated in Fig. 5.15.

```

%Primary winding current
Ip_s = @(s) ((Ep_s(s)) / Z(s));

%Magnetising current
Im_s = @(s) ((Ep_s(s)) / (Lm * s));

% Inverse Laplace to get time-domain expressions
Ip_t = @(t) ilaplace(Ip_s(s));
Im_t = @(t) ilaplace(Im_s(s));

% Total input current = primary + magnetizing
It_t = @(t) Ip_t(t) + Im_t(t);

% Convert symbolic time-domain currents to numerical functions
Ip_t_num = matlabFunction(Ip_t(t), 'Vars', t);
Im_t_num = matlabFunction(Im_t(t), 'Vars', t);
It_t_num = matlabFunction(It_t(t), 'Vars', t);

% primary current values at all 25000 time points
Ip_vals = Ip_t_num(tvec);
```

```
% magnetising current values at all 25000 time points
Im_vals = Im_t_num(tvec);

% total current values at all 25000 time points
It_vals = It_t_num(tvec);
```

Appendix B

Power Circuit

B.1 PCB Schematic Layout

Schematic diagram of the power circuit PCB for the SCA^{2}M prototype design.

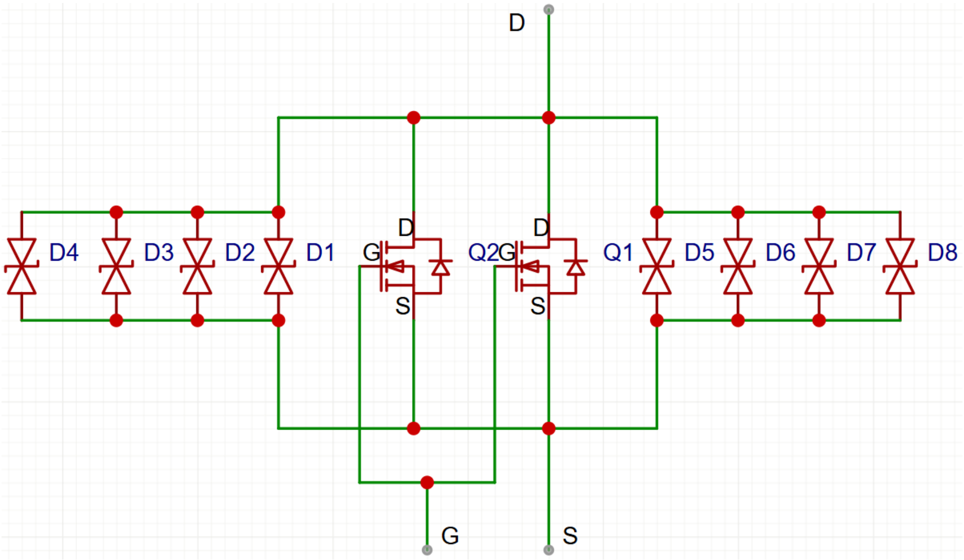
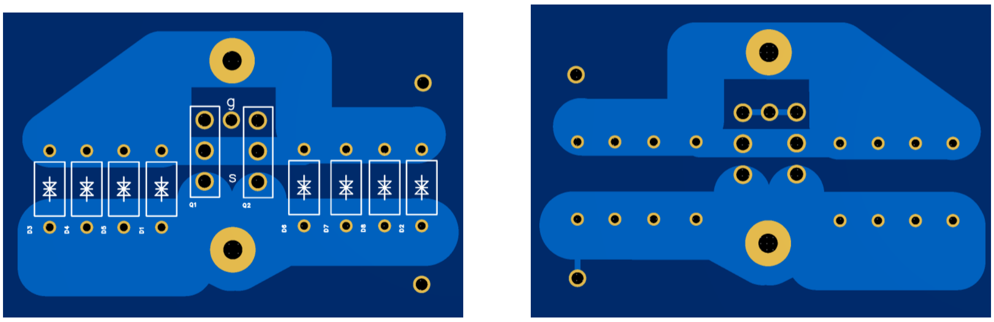


Figure B.1: The schematic diagram of the power circuit PCB for the high-current SC loop

B.2 PCB

The printed circuit board for the SCA^{2}M prototype design.



(a) (b)

Figure B.2: PCB layout: (a) power board top layer, and (b) bottom layer

B.3 MOSFET Datasheet

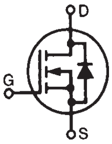
IXYS

TrenchT2™
GigaMOS™ HiperFET™
Power MOSFET

IXFK520N075T2
IXFX520N075T2

V_{DSS} = 75V
I_{D25} = 520A
$R_{DS(on)}$ ≤ 2.2mΩ

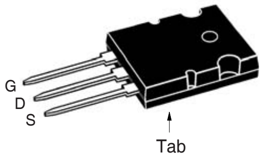
N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode



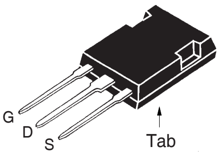
Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 175°C	75	V
V_{DGR}	T_J = 25°C to 175°C, R_{GS} = 1MΩ	75	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	T_C = 25°C (Chip Capability)	520	A
$I_{L(RMS)}$	External Lead Current Limit	160	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	1350	A
I_A	T_C = 25°C	200	A
E_{AS}	T_C = 25°C	3	J
P_D	T_C = 25°C	1250	W
T_J		-55 ... +175	°C
T_{JM}		175	°C
T_{stg}		-55 ... +175	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	°C
M_d	Mounting Torque (TO-264)	1.13/10	Nm/lb.in
F_C	Mounting Force (PLUS247)	20..120 /4.5..27	N/lb
Weight	TO-264	10	g
	PLUS247	6	g

Symbol	Test Conditions	Characteristic Values			
(T_J = 25°C Unless Otherwise Specified)		Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 3mA	75			V
$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 8mA	2.5		5.0	V
I_{GSS}	V_{GS} = ± 20V, V_{DS} = 0V			± 200	nA
I_{DSS}	V_{DS} = V_{DSS}, V_{GS} = 0V			25	µA
	T_J = 150°C			2	mA
$R_{DS(on)}$	V_{GS} = 10V, I_D = 100A, Notes 1 & 2			2.2	mΩ

TO-264 (IXFK)



PLUS247 (IXFX)



G = Gate
D = Drain
S = Source
Tab = Drain

Features

- International Standard Packages
- High Current Handling Capability
- Fast Intrinsic Diode
- Avalanche Rated
- Low $R_{DS(on)}$

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- DC-DC Converters and Off-Line UPS
- Primary-Side Switch
- High Speed Power Switching Applications

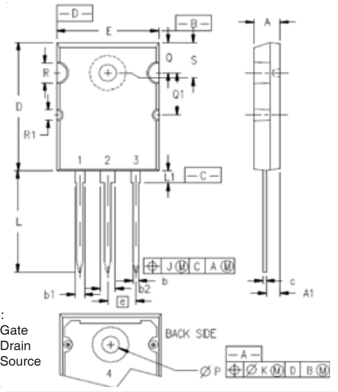
Symbol	Test Conditions	Characteristic Values			
	(T_J = 25°C, Unless Otherwise Specified)	Min.	Typ.	Max.	
g_{fs}	$V_{DS} = 10V$, $I_D = 60A$, Note 1	65	105		S
C_{iss}	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1MHz		41		nF
C_{oss}			4150		pF
C_{rss}			530		pF
R_{GI}	Gate Input Resistance		1.36		Ω
$t_{d(on)}$	**Resistive Switching Times** $V_{GS} = 10V$, $V_{DS} = 0.5 \bullet V_{DSS}$, $I_D = 200A$ $R_G = 1\Omega$ (External)		48		ns
t_r			36		ns
$t_{d(off)}$			80		ns
t_f			35		ns
$Q_{g(on)}$	$V_{GS} = 10V$, $V_{DS} = 0.5 \bullet V_{DSS}$, $I_D = 0.5 \bullet I_{DSS}$		545		nC
Q_{gs}			177		nC
Q_{gd}			135		nC
R_{thJC}				0.12	°C/W
R_{thCS}			0.15		°C/W

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values			
	(T_J = 25°C, Unless Otherwise Specified)	Min.	Typ.	Max.	
I_S	$V_{GS} = 0V$			520	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			1600	A
V_{SD}	$I_F = 100A$, $V_{GS} = 0V$, Note 1			1.25	V
t_{rr}	$I_F = 150A$, $V_{GS} = 0V$ $-di/dt = 100A/\mu s$ $V_R = 37.5V$			150	ns
I_{RM}			7		A
Q_{RM}			357		nC

Notes 1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.
2. Includes lead resistance.

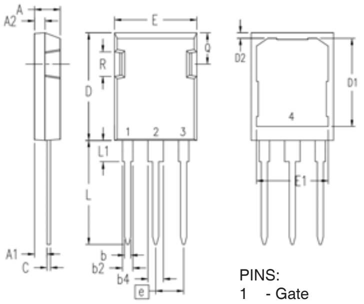
TO-264 Outline



PINS:
1 - Gate
2,4 - Drain
3 - Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.209	4.70	5.31
A1	.102	.118	2.59	3.00
b	.037	.055	0.94	1.40
b1	.087	.102	2.21	2.59
b2	.110	.126	2.79	3.20
c	.017	.029	0.43	0.74
D	1.007	1.047	25.58	26.59
E	.760	.799	19.30	20.29
e	.215BSC		5.46 BSC	
J	.000	.010	0.00	0.25
K	.000	.010	0.00	0.25
L	.779	.842	19.79	21.39
L1	.087	.102	2.21	2.59
ØP	.122	.138	3.10	3.51
Q	.240	.256	6.10	6.50
Q1	.330	.346	8.38	8.79
ØR	.155	.187	3.94	4.75
ØR1	.085	.093	2.16	2.36
S	.243	.253	6.17	6.43

PLUS247™ Outline



PINS:
1 - Gate
2,4 - Drain
3 - Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b2	.075	.087	1.91	2.20
b4	.115	.126	2.92	3.20
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
D1	.650	.690	16.51	17.53
D2	.035	.050	0.89	1.27
E	.620	.635	15.75	16.13
E1	.545	.565	13.84	14.35
e	.215 BSC		5.45 BSC	
L	.780	.810	19.81	20.57
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83

Fig. 1. Output Characteristics @ $T_J = 25^oC$

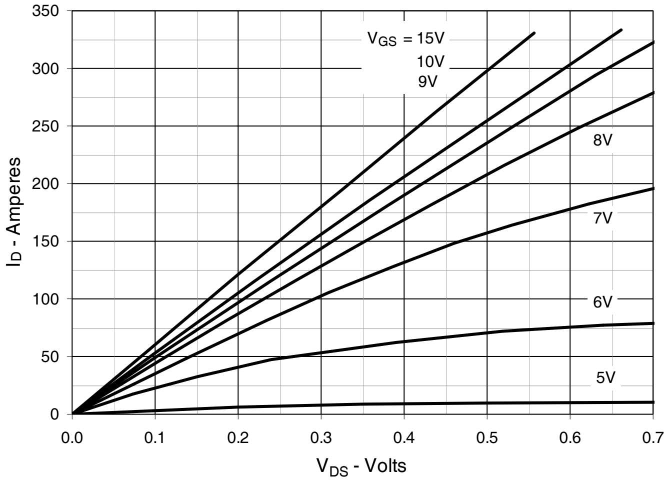


Fig. 2. Extended Output Characteristics @ $T_J = 25^oC$

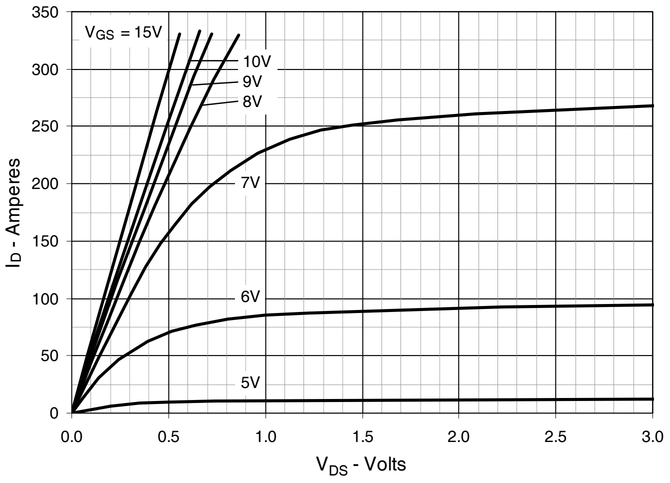


Fig. 3. Output Characteristics @ $T_J = 150^oC$

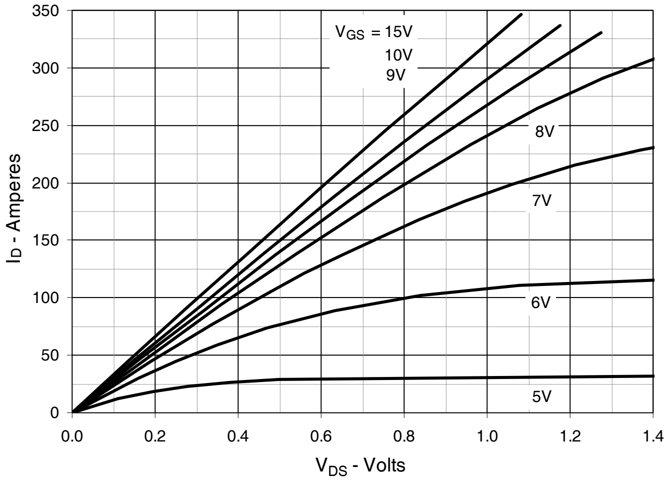


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 150A Value vs. Junction Temperature

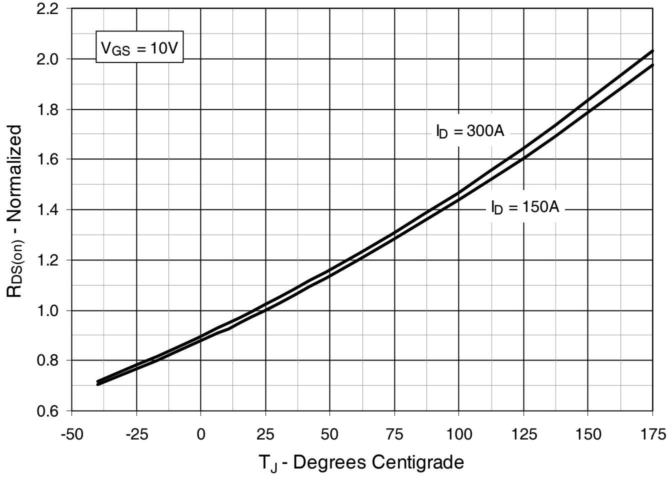


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 150A Value vs. Drain Current

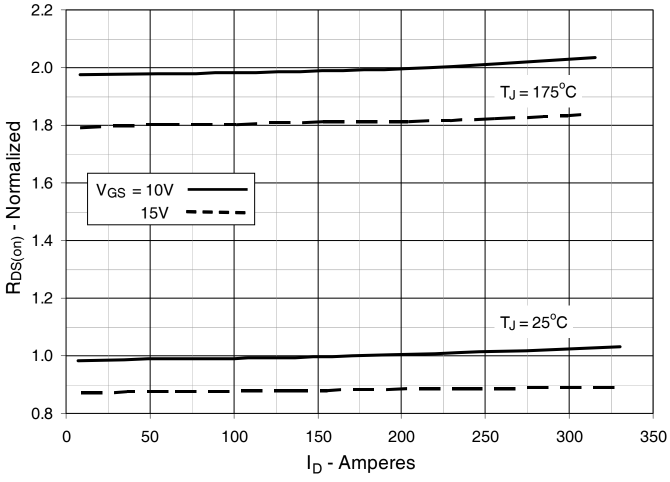


Fig. 6. Drain Current vs. Case Temperature

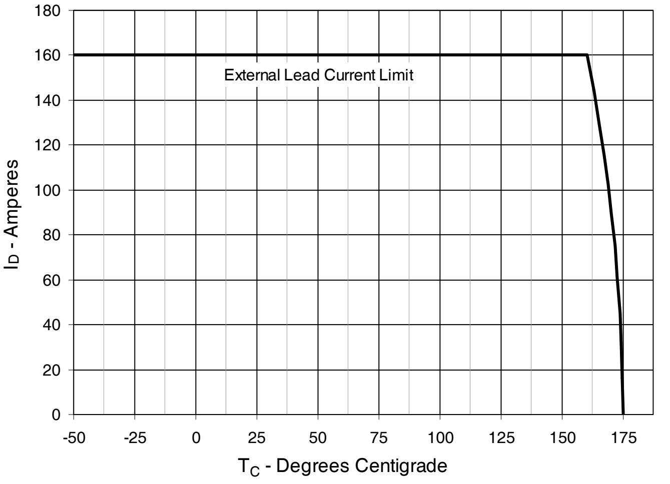


Fig. 7. Input Admittance

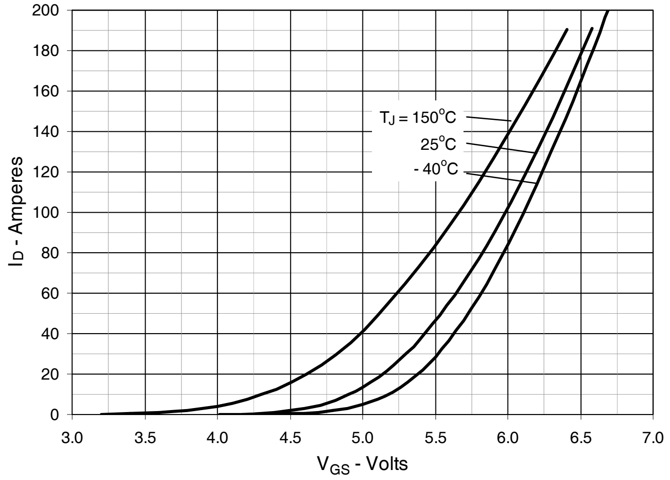


Fig. 8. Transconductance

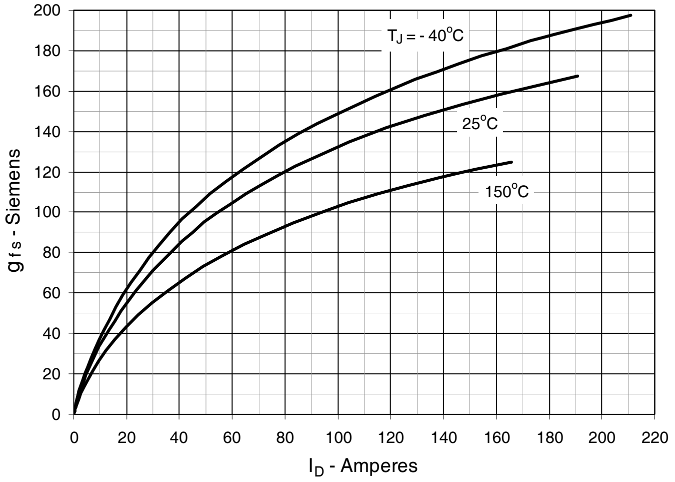


Fig. 9. Forward Voltage Drop of Intrinsic Diode

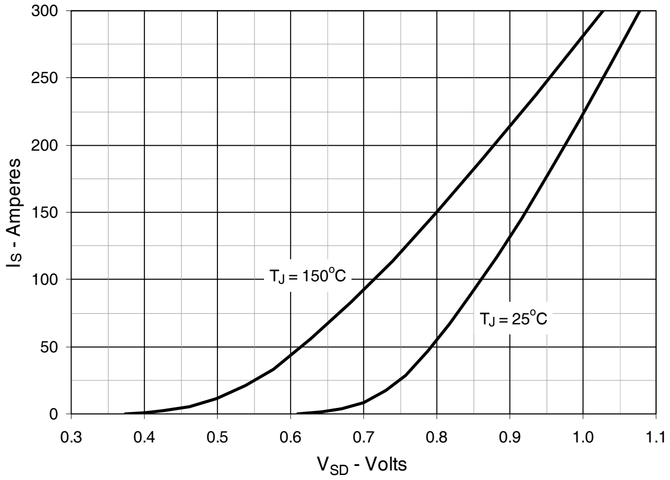


Fig. 10. Gate Charge

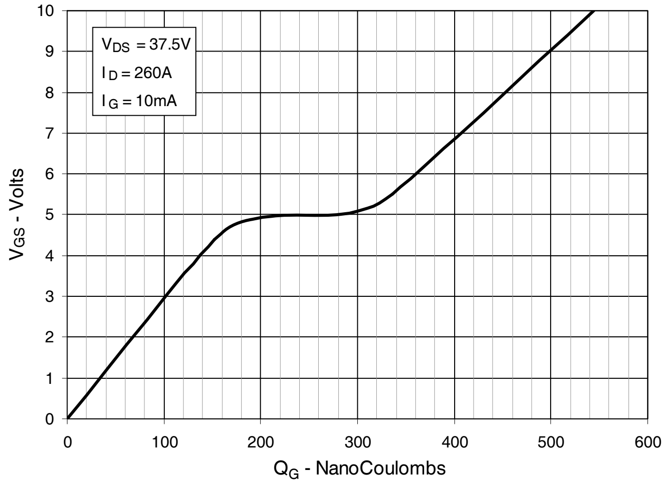


Fig. 11. Capacitance

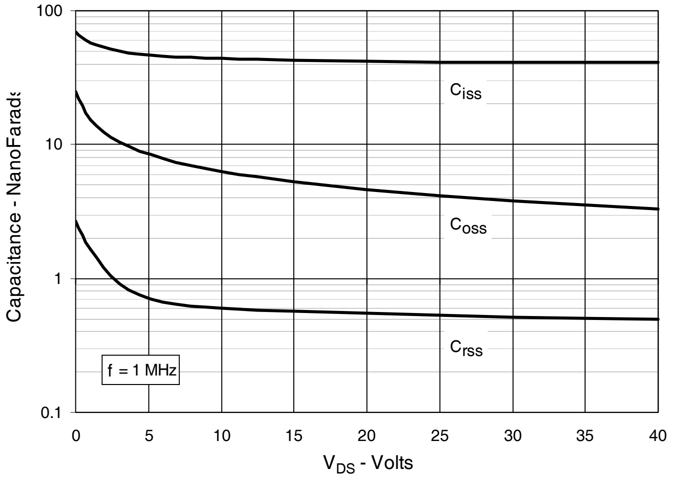


Fig. 12. Forward-Bias Safe Operating Area

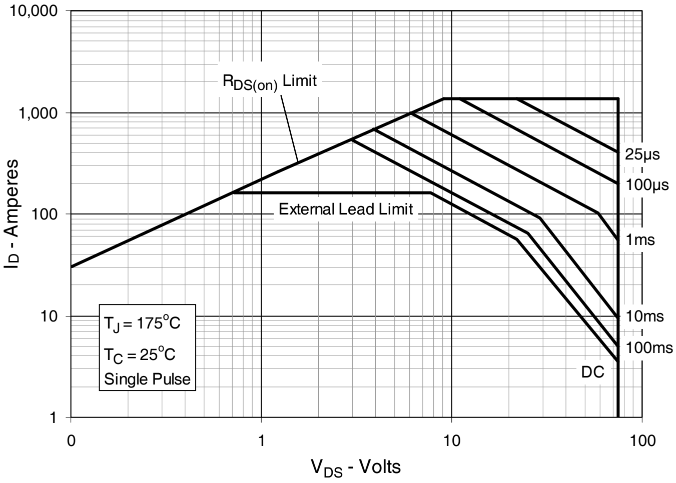


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

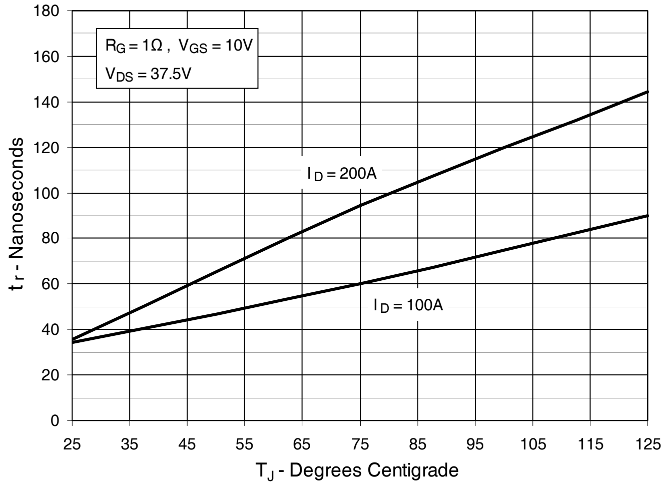


Fig. 14. Resistive Turn-on Rise Time vs. Drain Current

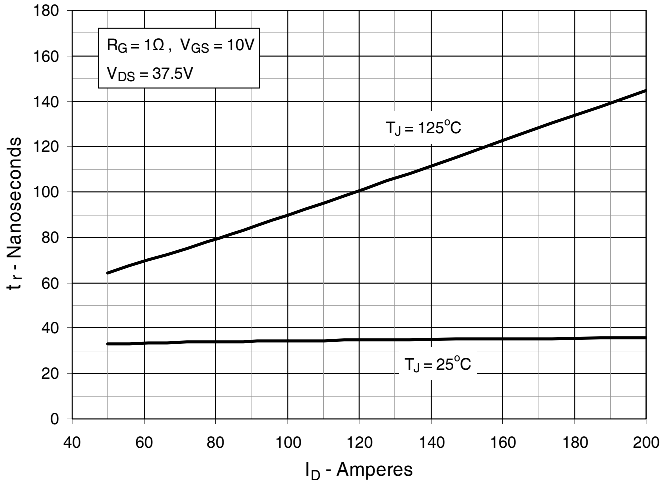


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

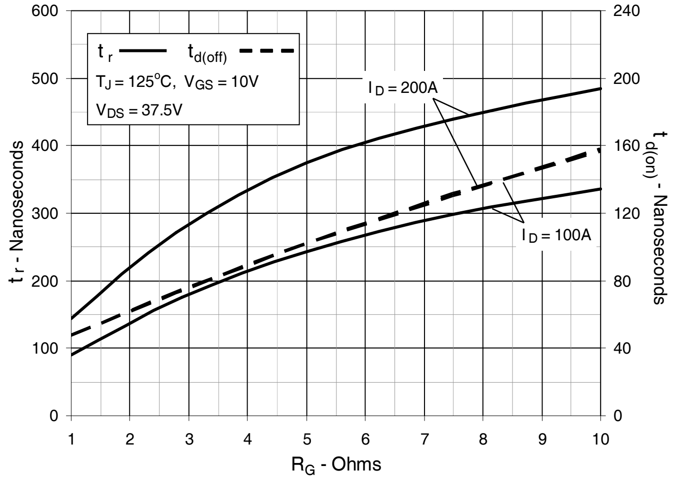


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

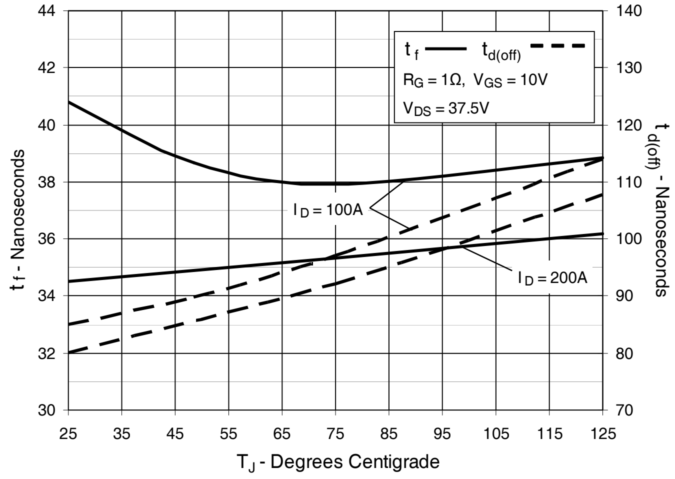


Fig. 17. Resistive Turn-off Switching Times vs. Drain Current

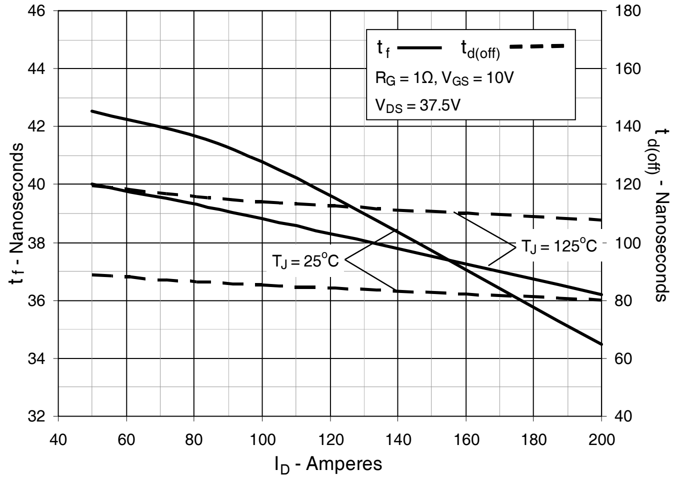
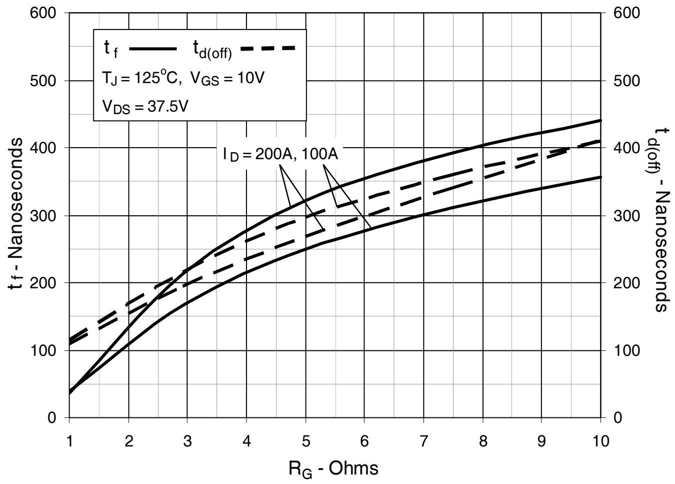
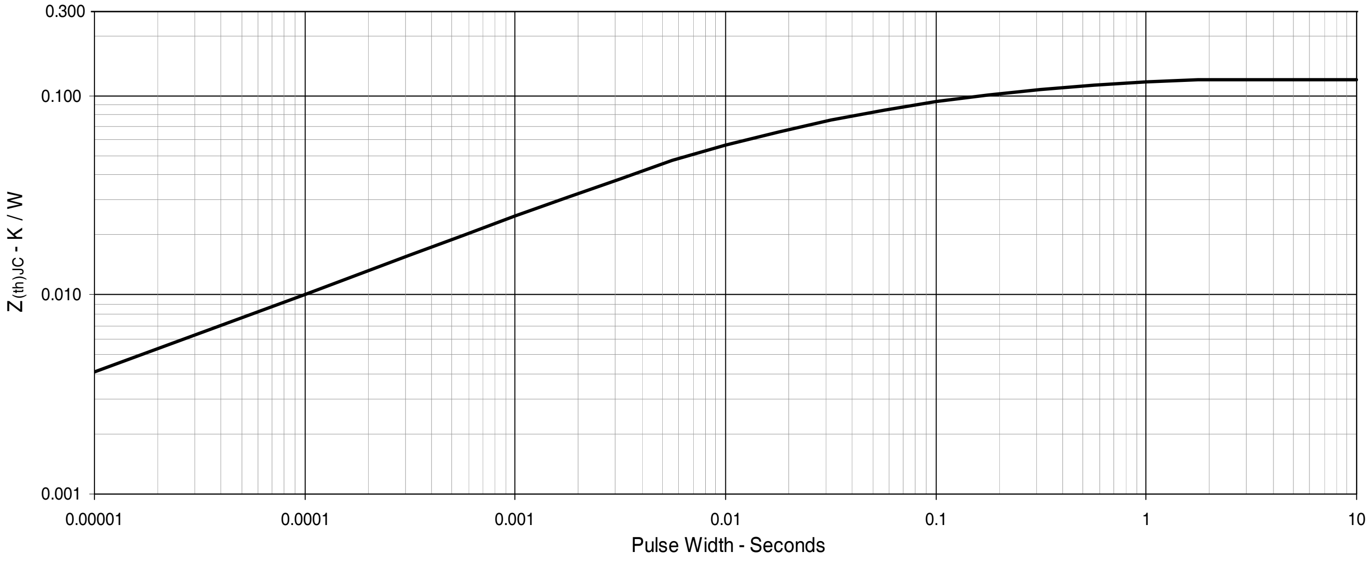


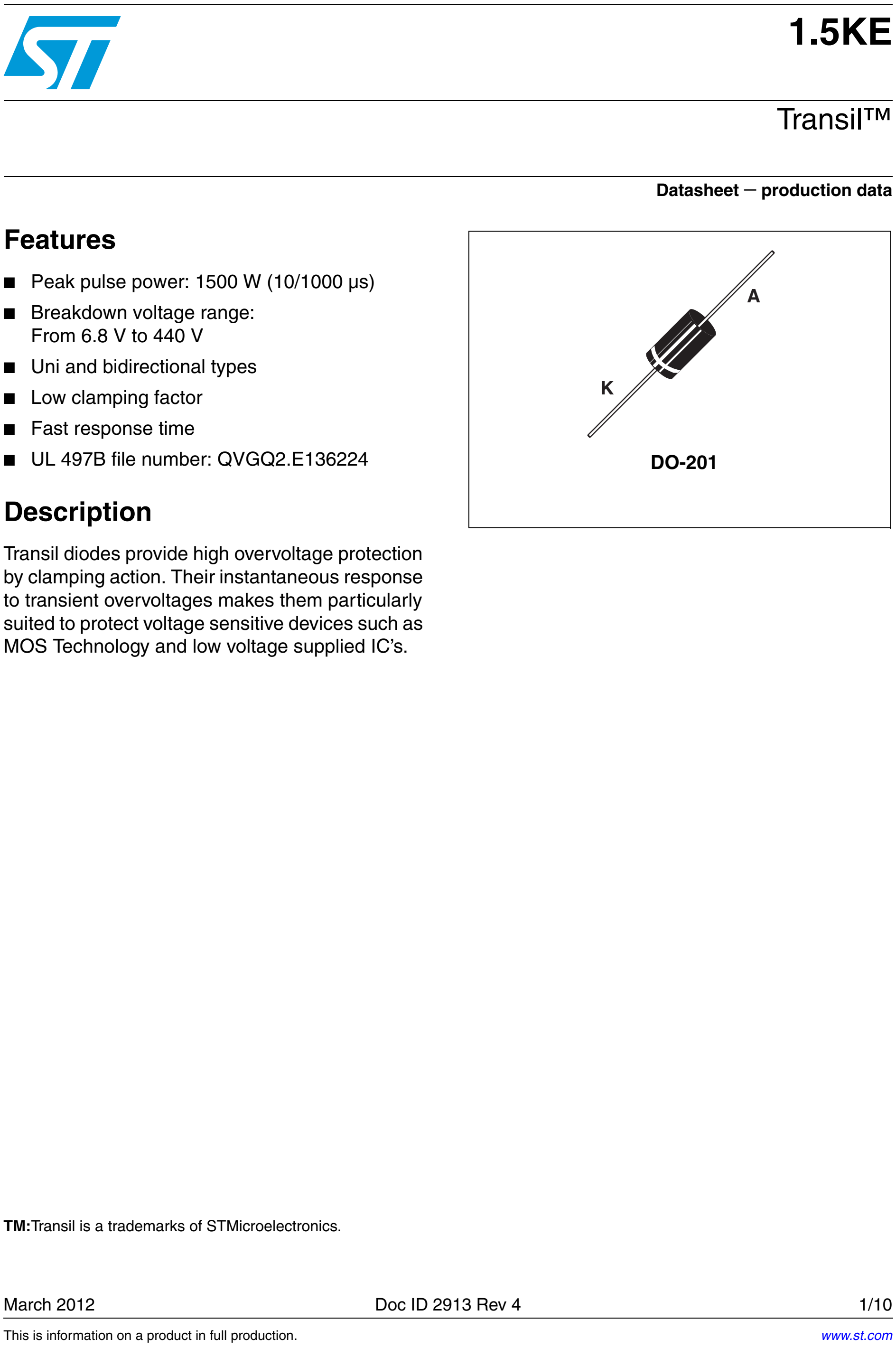
Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance





IXYS REF:F_520N075T2(V9)11-09-09

B.4 TVS Diode Datasheet



1.5KE

Transil™

Datasheet — production data

Features

- Peak pulse power: 1500 W (10/1000 µs)
- Breakdown voltage range:
  From 6.8 V to 440 V
- Uni and bidirectional types
- Low clamping factor
- Fast response time
- UL 497B file number: QVGQ2.E136224

DO-201

Description

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous response to transient overvoltages makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

TM: Transil is a trademarks of STMicroelectronics.

This is information on a product in full production. www.st.com

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
P_{PP}	Peak pulse power dissipation [1]	$T_{j\ initial} = T_{amb}$	1500	W
P	Power dissipation on infinite heatsink	T_{amb} = 75 °C	5	W
I_{FSM}	Non repetitive surge peak forward current for unidirectional types	t_p = 10 ms $T_{j\ initial} = T_{amb}$	200	A
T_{stg}	Storage temperature range		-65 to + 175	°C
T_j	Maximum operating junction temperature		175	°C
T_L	Maximum lead temperature for soldering during 10s at 5mm from case.		230	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Table 2. Thermal parameter

Symbol	Parameter	Value	Unit
$R_{th(j-l)}$	Junction to leads	20	°C/W
$R_{th(j-a)}$	Junction to ambient on printed circuit. L_{lead} = 10 mm	75	

Figure 1. Electrical characteristics - definitions

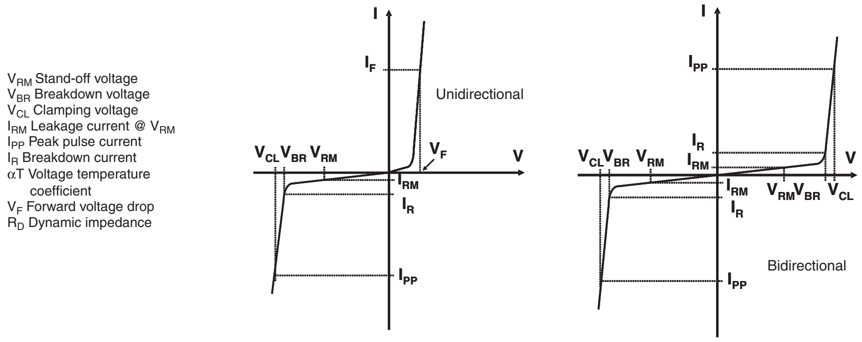


Table 3. Electrical characteristics - parameter values (T_{amb} = 25 °C)

Order code	I_{RM} @ V_{RM}		V_{BR}	@	I_R[1]		V_{CL} @ I_{PP} 10/1000 µs		V_{CL} @ I_{PP} 8/20 µs		αT[2]	C[3]
	max.		max.	nom.	min.		max.		max.		max.	typ.
	µA	V	V	V	V	mA	V	A	V	A	10-4/ °C	pF
1.5KE6V8A/CA	1000	5.8	6.45	6.8	7.14	10	10.5	143	13.4	746	5.7	9500
1.5KE7V5A/CA	500	6.4	7.13	7.5	7.88	10	11.3	132	14.5	690	6.1	8500
1.5KE10A/CA	10	8.55	9.5	10	10.5	1	14.5	100	18.6	538	7.3	7000
1.5KE12A/CA	5	10.2	11.4	12	12.6	1	16.7	90	21.7	461	7.8	6000
1.5KE15A/CA	1	12.8	14.3	15	15.8	1	21.2	71	27.2	368	8.4	5000
1.5KE18A/CA	1	15.3	17.1	18	18.9	1	25.2	59.5	32.5	308	8.8	4300
1.5KE22A/CA	1	18.8	20.9	22	23.1	1	30.6	49	39.3	254	9.2	3700
1.5KE24A/CA	1	20.5	22.8	24	25.2	1	33.2	45	42.8	234	9.4	3500
1.5KE27A/CA	1	23.1	25.7	27	28.4	1	37.5	40	48.3	207	9.6	3200
1.5KE30A/CA	1	25.6	28.5	30	31.5	1	41.5	36	53.5	187	9.7	2900
1.5KE33A/CA	1	28.2	31.4	33	34.7	1	45.7	33	59.0	169	9.8	2700
1.5KE36A/CA	1	30.8	34.2	36	37.8	1	49.9	30	64.3	156	9.9	2500
1.5KE39A/CA	1	33.3	37.1	39	41.0	1	53.9	28	69.7	143	10.0	2400
1.5KE47A/CA	1	40.2	44.7	47	49.4	1	64.8	23.2	84	119	10.1	2050
1.5KE56A/CA	1	47.8	53.2	56	58.8	1	77	19.5	100	100	10.3	1800
1.5KE62A/CA	1	53.0	58.9	62	65.1	1	85	17.7	111	90	10.4	1700
1.5KE68A/CA	1	58.1	64.6	68	71.4	1	92	16.3	121	83	10.4	1550
1.5KE82A/CA	1	70.1	77.9	82	86.1	1	113	13.3	146	69	10.5	1350
1.5KE100A/CA	1	85.5	95.0	100	105	1	137	11	178	56	10.6	1150
1.5KE120A/CA	1	102	114	120	126	1	165	9.1	212	47	10.7	1000
1.5KE150A/CA	1	128	143	150	158	1	207	7.2	265	38	10.8	850
1.5KE180A/CA	1	154	171	180	189	1	246	6.1	317	31.5	10.8	725
1.5KE200A/CA	1	171	190	200	210	1	274	5.5	353	28	10.8	675
1.5KE220A/CA	1	188	209	220	231	1	328	4.6	388	26	10.8	625
1.5KE250A/CA	1	213	237	250	263	1	344	5.0	442	23	11	560
1.5KE300A/CA	1	256	285	300	315	1	414	5.0	529	19	11	500
1.5KE350A/CA	1	299	332	350	368	1	482	4.0	618	16	11	430
1.5KE400A/CA	1	342	380	400	420	1	548	4.0	706	14	11	390
1.5KE440A/CA	1	376	418	440	462	1	603	3.5	776	13	11	360

1. Pulse test: t_p < 50 ms (see *Figure 2*)
2. $\Delta V_{BR} = \alpha T \times (T_{amb} - 25) \times V_{BR}(25\ °C)$
3. V_R = 0 V, F = 1 MHz. For bidirectional types, capacitance value is divided by 2.

Figure 2. Pulse definition for electrical characteristics

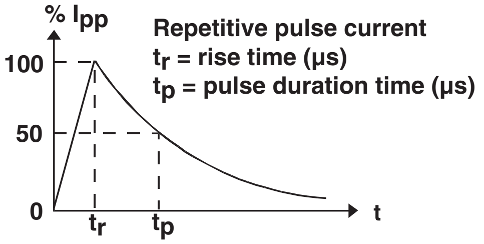


Figure 3. Peak pulse power dissipation versus initial junction temperature (printed circuit board)

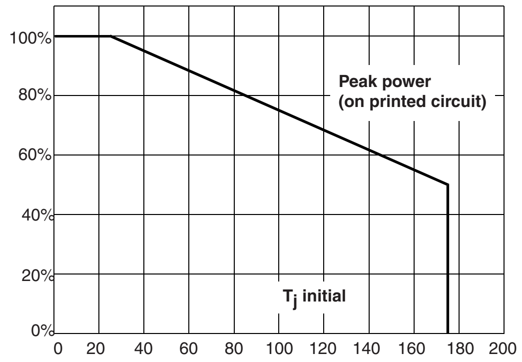


Figure 4. Peak pulse power versus exponential pulse duration

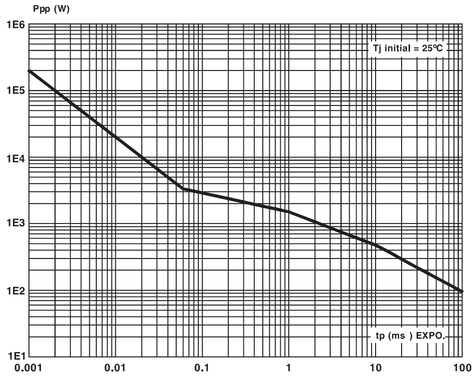


Figure 5. Clamping voltage versus peak pulse current

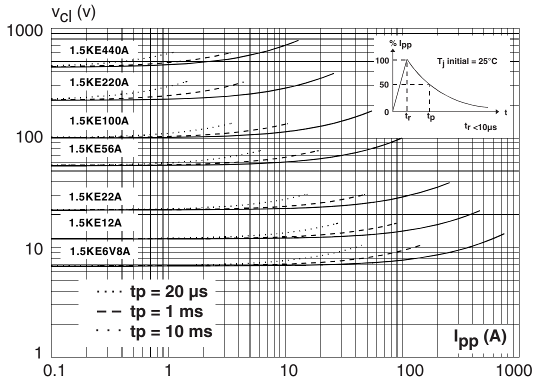
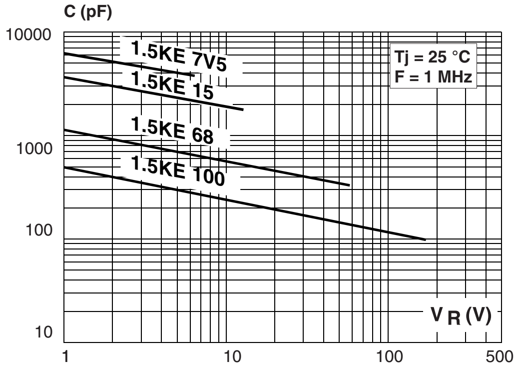


Figure 6. Capacitance versus reverse applied voltage for unidirectional types (typical values)



The curves of *Figure 5* are specified for a junction temperature of 25 °C before surge. The given results may be extrapolated for other junction temperatures by using the following formula:

$\Delta V_{BR} = \alpha T \times (Tamb - 25) \times V_{BR}$ (25 °C).

For intermediate voltages, extrapolate the given results.

Figure 7. Capacitance versus reverse applied voltage for bidirectional types (typical values)

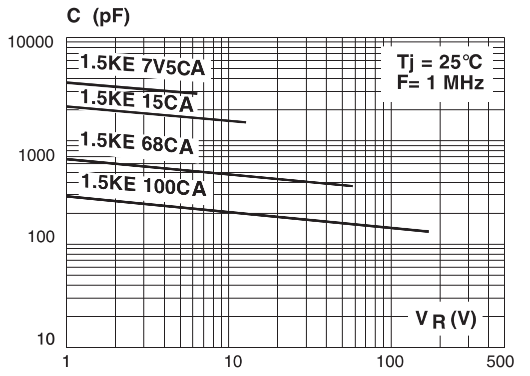


Figure 8. Peak forward voltage drop versus peak forward current (typical values for unidirectional types)

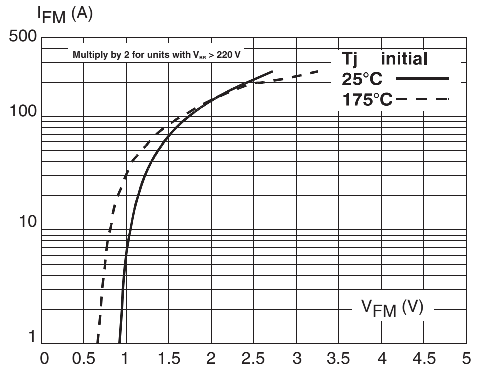


Figure 9. Transient thermal impedance junction-ambient versus pulse duration

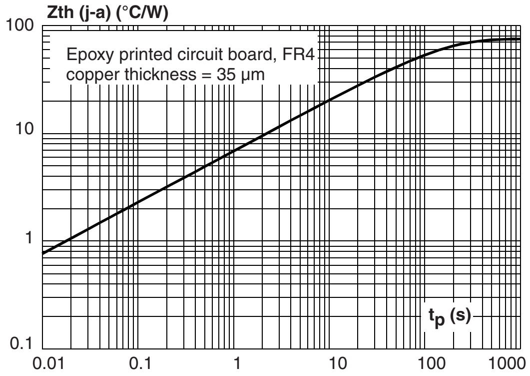
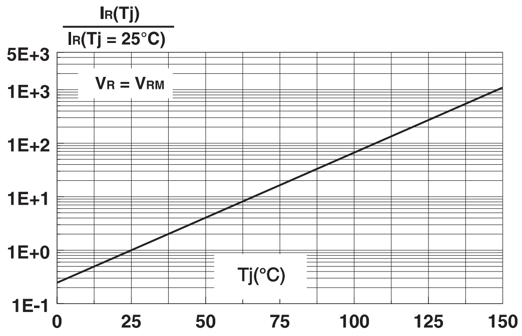


Figure 10. Relative variation of leakage current versus junction temperature



Appendix C

MOSFET Driver Circuit

C.1 PCB Schematic Layout

Schematic diagram of the MOSFET driver circuit PCB for the SCA^{2}M prototype design.

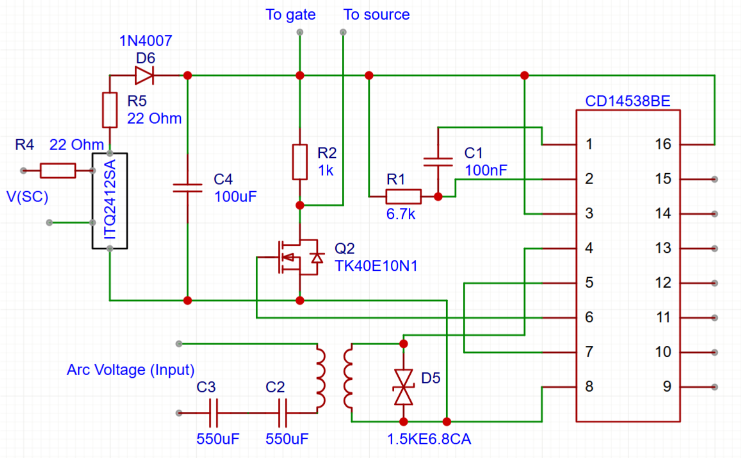
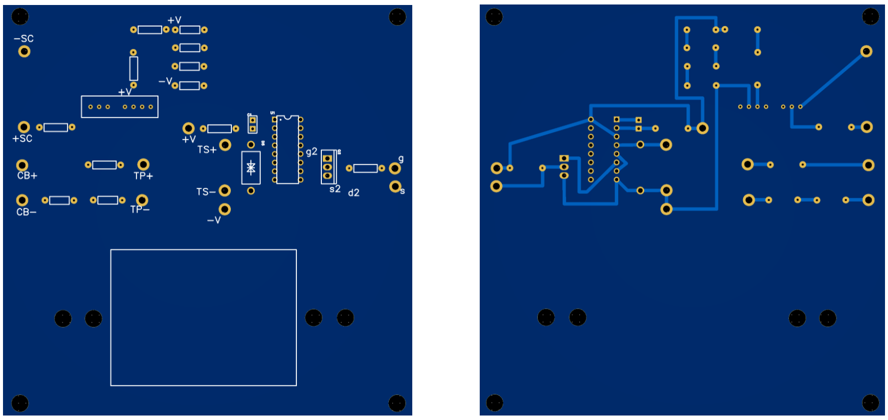


Figure C.1: Schematic diagram of the MOSFET driver circuit PCB. The datasheet for the CD14538BE IC is available at : https://tinyurl.com/ynuktkf4

C.2 PCB

The printed circuit board for the SCA^{2}M prototype design.



(a) (b)

Figure C.2: PCB layout: (a) MOSFET driver board top layer, and (b) bottom layer

C.3 DC-DC Converter Datasheet

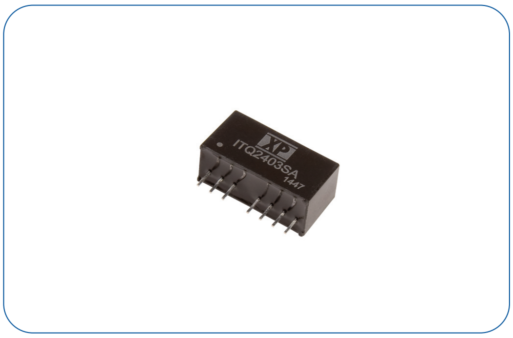
ITQ Series

DC-DC Converter

XP Power

6 Watts

- Regulated Single & Dual Outputs
- Wide 4:1 Input Range
- SIP 8 Package
- Operating Temperature -40 °C to +100 °C
- 1.5 kVDC Isolation
- Optional 3.0 kVDC Version
- UL62368-1 Safety Approved
- No Minimum Load Required
- Remote On/Off
- 3 Year Warranty



Dimensions:

ITQ:
0.86 x 0.36 x 0.44" (21.9 x 9.2 x 11.1 mm)

The ITQ Series offers a compact 6W, cost effective DC-DC module with wide 4:1 input ranges. Outputs are regulated single or dual options. Features include short circuit protection, no minimum load, high efficiency, remote on/off control.

Models & Ratings

Input Voltage	Output Voltage	Output Current	Input Current[1]		Maximum Capacitive Load[2]	Efficiency	Model Number[3]
			No Load	Full Load			
24V (9-36 V)	3.3 V	1500 mA	6 mA	261 mA	4700 µF	79%	ITQ2403SA
	5 V	1200 mA	6 mA	298 mA	2200 µF	84%	ITQ2405SA
	9 V	666 mA	6 mA	290 mA	1000 µF	86%	ITQ2409SA
	12 V	500 mA	6 mA	287 mA	470 µF	87%	ITQ2412SA
	15 V	400 mA	6 mA	287 mA	220 µF	87%	ITQ2415SA
	24 V	250 mA	6 mA	287 mA	100 µF	87%	ITQ2424SA
	±5 V	±600 mA	6 mA	298 mA	±330 µF	84%	ITQ2405S
	±12 V	±250 mA	6 mA	291 mA	±220 µF	86%	ITQ2412S
	±15 V	±200 mA	6 mA	287 mA	±100 µF	87%	ITQ2415S
48V (18-75 V)	3.3 V	1500 mA	6 mA	131 mA	4700 µF	79%	ITQ4803SA
	5 V	1200 mA	6 mA	151 mA	2200 µF	83%	ITQ4805SA
	9 V	666 mA	6 mA	147 mA	1000 µF	85%	ITQ4809SA
	12 V	500 mA	6 mA	144 mA	470 µF	87%	ITQ4812SA
	15 V	400 mA	6 mA	144 mA	220 µF	87%	ITQ4815SA
	24 V	250 mA	6 mA	144 mA	100 µF	87%	ITQ4824SA
	±5 V	±600 mA	6 mA	152 mA	±330 µF	82%	ITQ4805S
	±12 V	±250 mA	6 mA	147 mA	±220 µF	85%	ITQ4812S
	±15 V	±200 mA	6 mA	145 mA	±100 µF	86%	ITQ4815S

Notes

1. *Input currents measured at nominal input voltage.*
2. *Maximum capacitive load is per output.*
3. *For optional 3000VDC isolation add suffix '-H' to model number.*

Input

Characteristic	Minimum	Typical	Maximum	Units	Notes & Conditions
Input Voltage Range	9		36	VDC	24 V nominal
	18		75	VDC	48 V nominal
Input Filter	Capacitor				
Input Reflected Ripple			20/40	mA pk-pk	24/48 V input. Through 12 µH inductor and 47 µF capacitor
Input Surge			50	VDC for 100 ms	24 V models
			100	VDC for 100 ms	48 V models

Output

Characteristic	Minimum	Typical	Maximum	Units	Notes & Conditions
Output Voltage	3.3		24	VDC	See Models and Ratings table
Initial Set Accuracy			±1	%	
Minimum Load	0			A	No minimum load required
Line Regulation			±0.2	%	
Load Regulation			±0.5	%	Single output
			±1	%	Dual output
Cross Regulation			±5	%	On dual output models when one load is varied between 25% and 100% and other is fixed at 100%
Transient Response			±5/±3	% deviation	For 3V3 & 5V output models / all other models. Recovery within 2% in less than 2ms for a 25% load change
Ripple & Noise			125	mV pk-pk	20 MHz bandwidth. Measured using 0.1 µF ceramic capacitor
Short Circuit Protection					Continuous, with auto recovery
Maximum Capacitive Load					See Models and Ratings table
Temperature Coefficient			0.02	%/°C	
Remote On/Off	Output is on if Remote On/Off (pin 3) is open Output turns off if 2-4 mA is applied to Remote On/Off (pin 3). Referenced to -Vin. Maximum voltage 15VDC.				

General

Characteristic	Minimum	Typical	Maximum	Units	Notes & Conditions
Efficiency		87		%	See Models and Ratings table
Isolation: Input to Output	1500			VDC	3000 VDC option. Add '-H' to model number
Switching Frequency		580		kHz	
Isolation Resistance	10^9			Ω	
Isolation Capacitance		50		pF	
Power Density			44	Win^3	
Mean Time Between Failure	0.8			MHrs	MIL-HDBK-217F, +25 °C GB
Weight		0.01 (4.8)		lb (g)	

Environmental

Characteristic	Minimum	Typical	Maximum	Units	Notes & Conditions
Operating Temperature	-40		+100	°C	Derate from 100% load at +70 °C to no load at +100 °C
Storage Temperature	-55		+125	°C	
Case Temperature			+100	°C	
Humidity			95	%RH	Non-condensing
Cooling					Natural convection

EMC: Emissions

Phenomenon	Standard	Test Level	Notes & Conditions
Conducted	EN55032	Class A	External components required. See suggested filter below.
Radiated	EN55032	Class A	

EMC: Immunity

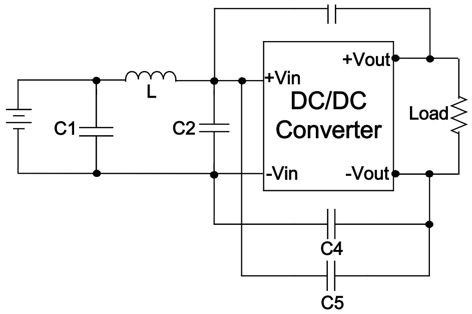
Phenomenon	Standard	Test Level	Criteria	Notes & Conditions
ESD Immunity	EN61000-4-2	3	A	
Radiated Immunity	EN61000-4-3	20 Vrms	A	
EFT/Burst	EN61000-4-4	3	A	External input capacitor required 330 µF/100 V
Surges	EN61000-4-5	Installation class 2	A	External input capacitor required 330 µF/100 V
Conducted Immunity	EN61000-4-6	3 V rms	A	
Magnetic Fields	EN61000-4-8	1 A/m	A	

Safety Approvals

Safety Agency	Safety Standard	Notes & Conditions
UL	UL60950-1, UL62368-1	
CSA	CAN/CSA C22.2 No. 60950-1 and CSA-C22.2 No. 62368-1	

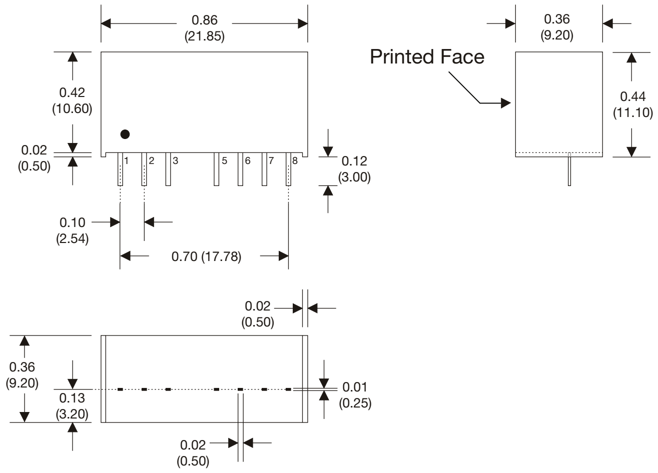
Application Notes

EMI Filter



	C1 & C2	L	C3 & C4	C5
ITQ24	10 µF (35 V)	12 µH	470 pF (3 kV)	n/a
ITQ48	2.2 µF (100 V)	12 µH	1000 pF (3 kV)	1000 pF (3 kV)

Mechanical Details



Pin Connections

Pin	Single	Dual
1	-Vin	-Vin
2	+Vin	+Vin
3	Remote On/Off	Remote On/Off
5	N/C	N/C
6	+Vout	+Vout
7	-Vout	Common
8	N/C	-Vout

Pin Connections

Pin	Single -H	Dual -H
1	-Vin	-Vin
2	+Vin	+Vin
3	Remote On/Off	Remote On/Off
5	No Pin	No Pin
6	+Vout	+Vout
7	-Vout	Common
8	N/C	-Vout

Notes

1. All dimensions are in inches (mm)
2. Weight: 0.01lbs (4.8 g) approx.
3. Pin diameter: 0.02±0.002 (0.5±0.05)
4. Pin pitch tolerance: ±0.014 (±0.35)
5. Case tolerance: ±0.02 (±0.5)

Appendix D

Magnetics Design Guides

D.1 Ferrite Magnetic Core

This appendix contains the industry datasheet of the ferrite core discussed in the thesis.

The following web link provides access to the data from the Fair–Rite website.

https://fair-rite.com/product/toroids-5975011121/

Fair-Rite Products Corp.
Your Signal Solution®

Toroids (5975011121)

Part Number: 5975011121

75 TOROID

Explanation of Part Numbers:
– Digits 1 & 2 = Product Class
– Digits 3 & 4 = Material Grade
– 9th digit 1 = Parylene Coating, 2 = Thermo-Set Plastic Coating

A ring configuration provides the ultimate utilization of the intrinsic ferrite material properties. Toroidal cores are used in a wide variety of applications such as power input filters, ground-fault interrupters, common-mode filters and in pulse and broadband transformers.

All toroidal cores are supplied burnished to break sharp edges.

Coating Options:
– Toroids with an outside diameter of 9.5 mm (0.375″) or smaller can be supplied Parylene C coate
The Parylene coating will increase the "A" and "C" dimensions and decrease the "B" dimension a maximum of 0.038 mm (0.0015″). The ninth digit of a Parylene coated toroid part number is a "1". See reference tables for the material characteristics of Parylene C. Parylene C coating is RoHS compliant.
– Toroids with an outside diameter of 9.5 mm (0.375″) or larger can be supplied with a uniform coating of thermo-set plastic coating. This coating will increase the "A" and "C" dimensions and decrease the "B" dimension a maximum of 0.5 mm (0.020″). The 9th digit of the thermo-set plastic coated toroid part number is a "2". Thermo-set plastic coating is RoHS compliant.
– Thermo-set plastic coated parts can withstand a minimum breakdown voltage of 1000 Vrms, uniformly applied across the "C" dimension of the toroid.

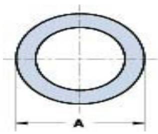
For any toroidal core requirement not listed in the catalog, please contact our customer service department for availability and pricing.

Catalog Drawing
3D Model

The C dimension may be modified to suit specific applications.

Weight: 188 (g)

Dim	mm	mm tol	nominal inch	inch misc.
A	75.65	Max	2.978	Max
B	37.6	Min	1.481	Min
C	13.6	Max	0.535	Max



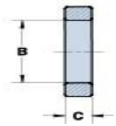


Chart Legend
$\Sigma l/A$: Core Constant, l_e : Effective Path Length, A_e : Effective Cross-Sectional Area, V_e : Effective Core Volume
A_L : Inductance Factor

Electrical Properties	
A_L(nH)	8100+25%, -30%
Ae(cm^2)	2.14
$\Sigma l/A$(cm^{-1})	7.7
l_e(cm)	16.5
V_e(cm^3)	35.3

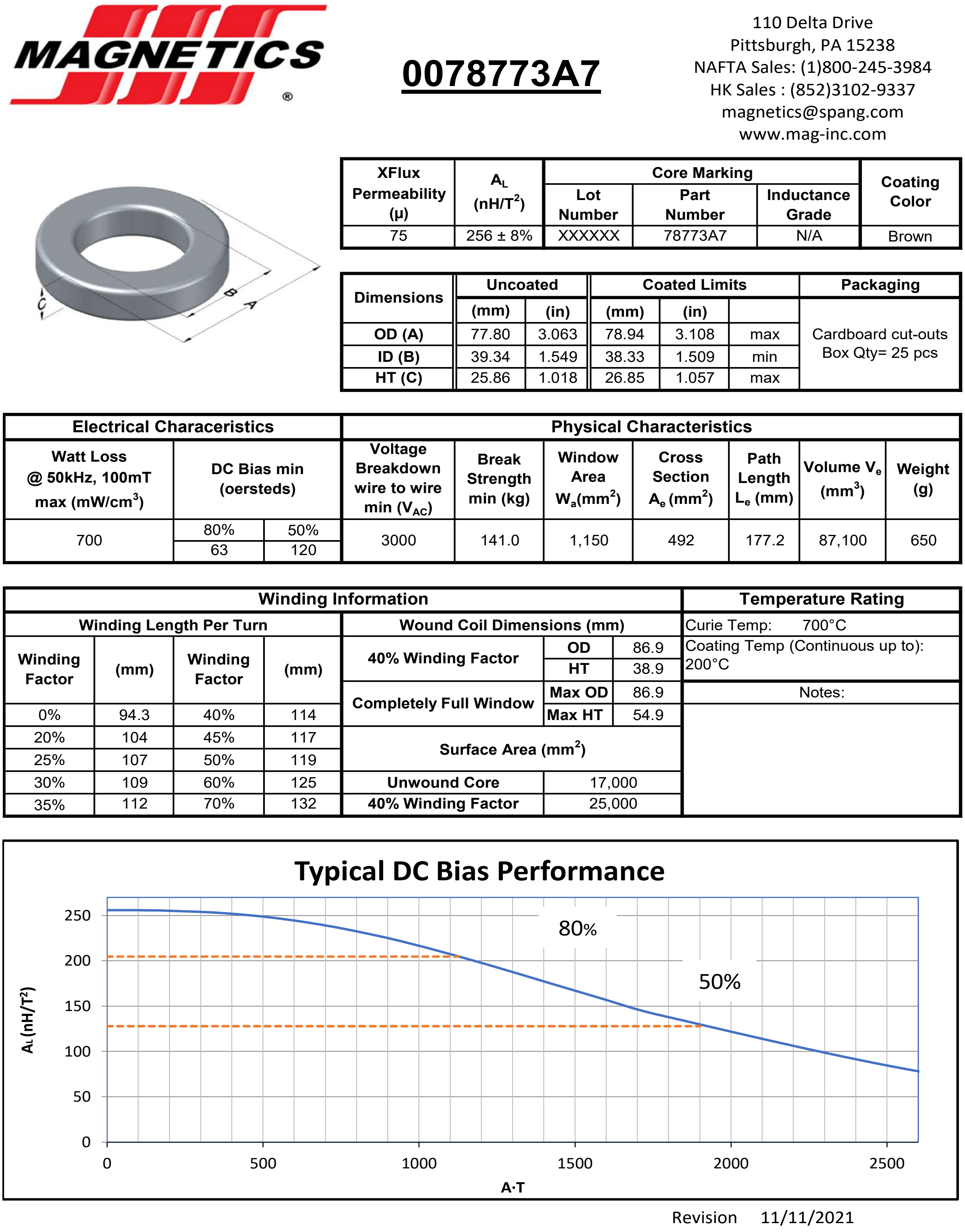
Toroids are tested for A_L values at 10 kHz.

Fair-Rite Products Corp. • One Commercial Row, Wallkill, New York 12589-0288
888-324-7748 • 845-895-2055 • Fax: 845-895-2629 • ferrites@fair-rite.com • www.fair-rite.com

D.2 Powdered Iron Magnetic Core

This appendix contains the industry datasheet of the powdered-iron core used in the (SCA^{2}M) prototype design.

The following web link provides access to the datasheet from the Magnetics website. https://www.mag-inc.com/Media/Magnetics/Datasheets/0078773A7.pdf



MAGNETICS®

0078773A7

110 Delta Drive
Pittsburgh, PA 15238
NAFTA Sales: (1)800-245-3984
HK Sales : (852)3102-9337
magnetics@spang.com
www.mag-inc.com

XFlux Permeability (µ)	A_L (nH/T^2)	Core Marking			Coating Color
		Lot Number	Part Number	Inductance Grade	
75	256 ± 8%	XXXXXX	78773A7	N/A	Brown

Dimensions	Uncoated		Coated Limits			Packaging
	(mm)	(in)	(mm)	(in)		
OD (A)	77.80	3.063	78.94	3.108	max	Cardboard cut-outs Box Qty= 25 pcs
ID (B)	39.34	1.549	38.33	1.509	min	
HT (C)	25.86	1.018	26.85	1.057	max	

Electrical Characteristics			Physical Characteristics						
Watt Loss @ 50kHz, 100mT max (mW/cm^3)	DC Bias min (oersteds)		Voltage Breakdown wire to wire min (V_{AC})	Break Strength min (kg)	Window Area W_a(mm^2)	Cross Section A_e (mm^2)	Path Length L_e (mm)	Volume V_e (mm^3)	Weight (g)
	80%	50%							
700	63	120	3000	141.0	1,150	492	177.2	87,100	650

Winding Information

Winding Length Per Turn			
Winding Factor	(mm)	Winding Factor	(mm)
0%	94.3	40%	114
20%	104	45%	117
25%	107	50%	119
30%	109	60%	125
35%	112	70%	132

Wound Coil Dimensions (mm)		
40% Winding Factor	OD	86.9
	HT	38.9
Completely Full Window	Max OD	86.9
	Max HT	54.9

Surface Area (mm^2)	
Unwound Core	17,000
40% Winding Factor	25,000

Temperature Rating

Curie Temp: 700°C
Coating Temp (Continuous up to): 200°C
Notes:

Revision 11/11/2021

Appendix E

Datasheet of the Lightning Surge Simulator

This appendix accommodates a selected page of user manuals of Noiseken lightning surge simulator model, LSS–6230 developed by Noiseken Laboratories, Japan.

Lightning Surge Simulator

LSS-6230

- Lightning Surge Simulator
- Conforming to IEC61000-4-5 ed2 Standard
- Ring wave conforming to ANSI/IEEE C62.45 available
- Max. voltage 6.6kV output focusing on the practical use
- Monitor terminal standard equipped so as for easy waveform pre-checking
- Interlock built-in as the emergency stop function for safety
- Remote control software from PC ready as the option besides the stand-alone operation
- AC/DC CDN standard equipped. Available up to 3-phase AC500V 50A as the option
- CDN for Telecom lines, CDN for interconnection lines, isolation transformer, etc. ready as the option

Specification

Parameter	Specification		
■ Common			
Polarity	Positive / Negative		
Interval	(Minimum charging time) ∼999 sec. 1 sec. step		
No. of output setting	1∼999 times 1 time step		
■ Surge generating unit			
1.2/50μs-8/20μs Combination waveforms	Voltage surge	Output voltage	0.5∼6.0kV ±10%
		Front time	1.2μs±30%
		Duration	50μs±20%
	Current surge	Output current	250∼3000A ±10%
		Front time	8μs±20%
		Duration	20μs±20%
	Minimum charge time		10 Sec.
	Output impedance		2Ω±10%
0.5μs-100kHz Ring wave	Voltage surge	Output voltage	0.5∼6.0kV ±10%
		Rise time	0.5μs±0.15μs
		Frequency	100kHz±20kHz
	Current surge	2nd peak voltage	40-110% of 1st peak voltage
		3rd peak voltage	40-80% of 2nd peak voltage
		4th peak voltage	40-80% of 3rd peak voltage
	Minimum charge time		5 Sec.
	Output impedance		12 Ω±3 6 Ω at 12 Ω selection in interruptive resistance 30 Ω±8 Ω at 30 Ω selection in interruptive resistance
Coupling network	Line - Line : 18μF, Line - PE : 10Ω+9μF, Line - PE simultaneous coupling (L+N-PE) : 9μF/9μF		
Decoupling coil	1.5mH		
AC EUT power capacity	Single phase AC 240V 16A MAX (50/60Hz)		
DC Eat power capacity	DC125V/16A MAX		
Phase angle control	0∼360°±10°, Based on set injection / return angle		
■ Surge generating unit for external CDN			
10/700μs-5/320μs Combination waveforms	Voltage surge	Output voltage	0.5∼6.0kV ±10%
		Front time	10μs±30%
		Duration	700μs±20%
	Current surge	Output current	12.5∼150A ±10%
		Front time	5μs±20%
		Duration	320μs±20%
	Minimum charge time		15 Sec.
	Output impedance		40Ω±10%
■ Other			
Voltage monitor	BNC output, 1/1000±10%		
Current monitor	BNC output, 1mV/A±10%		
External communication	RS-232C optical communication		
Power supply	AC100V ∼120V±10%, AC200V ∼240V±10%,50/60Hz Power consumption : Less than 300VA		
Dimension	W430×H515×D500 mm(Projection excluded)		
Mass	Approx. 65kg		

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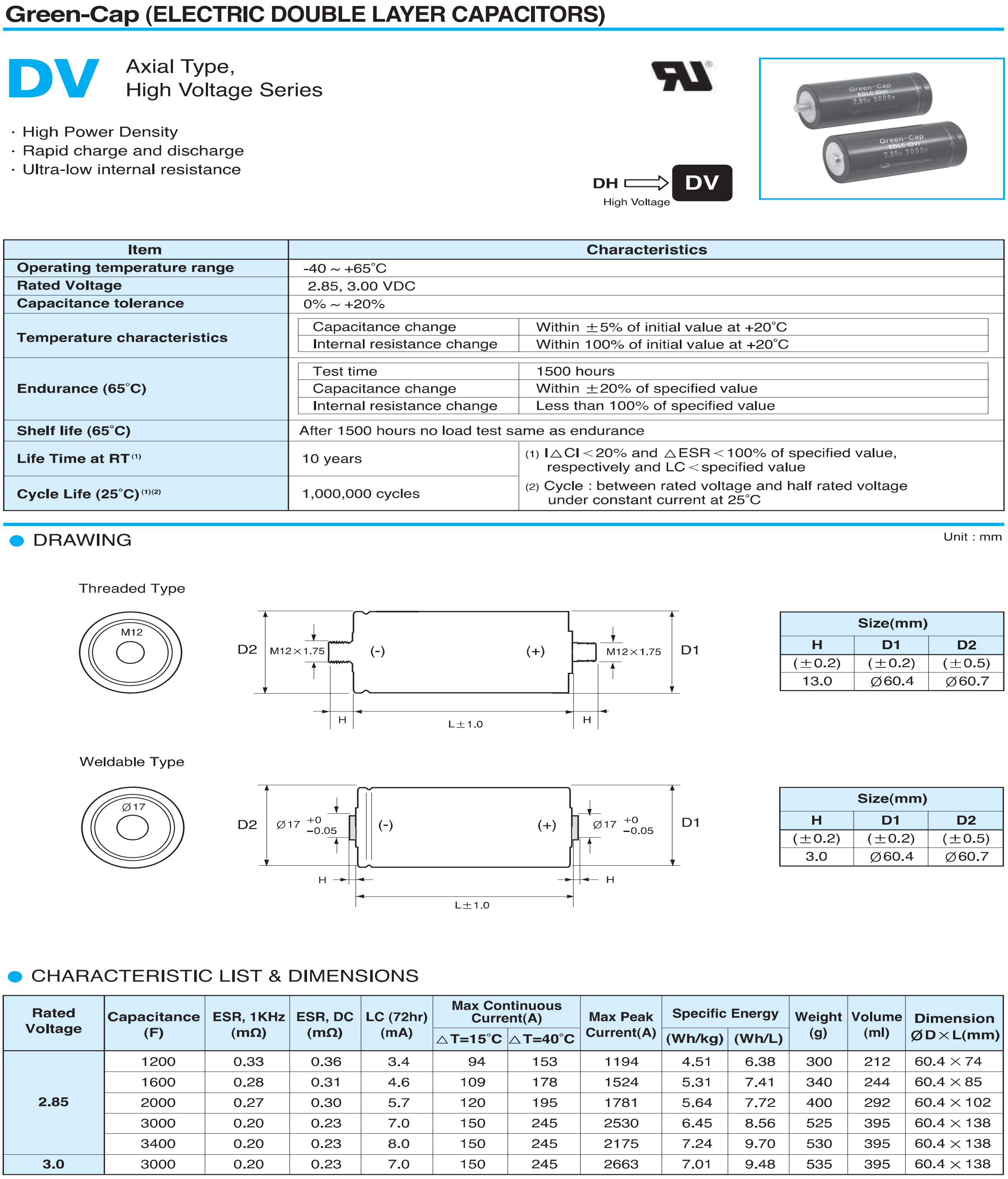
Appendix F

Supercapacitor Datasheet

This appendix presents the corresponding page from Samwha Capacitors Catalogue.



Green-Cap (ELECTRIC DOUBLE LAYER CAPACITORS)

DV Axial Type,
High Voltage Series

- High Power Density
- Rapid charge and discharge
- Ultra-low internal resistance

Item	Characteristics	
Operating temperature range	-40 ~ +65°C	
Rated Voltage	2.85, 3.00 VDC	
Capacitance tolerance	0% ~ +20%	
Temperature characteristics	Capacitance change Internal resistance change	Within ±5% of initial value at +20°C Within 100% of initial value at +20°C
Endurance (65°C)	Test time Capacitance change Internal resistance change	1500 hours Within ±20% of specified value Less than 100% of specified value
Shelf life (65°C)	After 1500 hours no load test same as endurance	
Life Time at RT (1)	10 years	(1) I△CI < 20% and △ESR < 100% of specified value, respectively and LC < specified value
Cycle Life (25°C) (1)(2)	1,000,000 cycles	(2) Cycle : between rated voltage and half rated voltage under constant current at 25°C

DRAWING

Unit : mm

Threaded Type

Size(mm)		
H	**D1**	**D2**
(±0.2)	(±0.2)	(±0.5)
13.0	Ø60.4	Ø60.7

Weldable Type

Size(mm)		
H	**D1**	**D2**
(±0.2)	(±0.2)	(±0.5)
3.0	Ø60.4	Ø60.7

CHARACTERISTIC LIST & DIMENSIONS

Rated Voltage	Capacitance (F)	ESR, 1KHz (mΩ)	ESR, DC (mΩ)	LC (72hr) (mA)	Max Continuous Current(A)		Max Peak Current(A)	Specific Energy		Weight (g)	Volume (ml)	Dimension ØD×L(mm)
					△T=15°C	△T=40°C		(Wh/kg)	(Wh/L)			
2.85	1200	0.33	0.36	3.4	94	153	1194	4.51	6.38	300	212	60.4 × 74
	1600	0.28	0.31	4.6	109	178	1524	5.31	7.41	340	244	60.4 × 85
	2000	0.27	0.30	5.7	120	195	1781	5.64	7.72	400	292	60.4 × 102
	3000	0.20	0.23	7.0	150	245	2530	6.45	8.56	525	395	60.4 × 138
	3400	0.20	0.23	8.0	150	245	2175	7.24	9.70	530	395	60.4 × 138
3.0	3000	0.20	0.23	7.0	150	245	2663	7.01	9.48	535	395	60.4 × 138

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