Design and Implementation of an AC Voltage Regulator based on Series Power Semiconductor Array

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Abstract

This thesis describes the use of an array of power semiconductors (series transistor array) and a buck-boost transformer in the design and implementation of a single phase AC voltage regulator. The power semiconductor array was used to act as variable impedance across the bridge points of a rectifier. The input point of the bridge rectifier was also connected directly to the primary winding of the buck-boost transformer. A closed loop circuit was designed using an RMS/DC converter chip, with complete electrical isolation between the low voltage control circuits and the power circuits. The major advantages of this technique are: fast response to RMS voltage fluctuation; waveform fidelity; light weight; and reduced size compared to that of a servo-driven AC voltage regulator such as the PS10 Smart Power Station, which was used in this project as a benchmark for the AC voltage regulator using the power semiconductor array. The device used for testing the performances of both AC voltage regulators was the NoiseKen VDS-2002 Voltage Dip and Swell Simulator. This simulator was used to perform voltage dip, swell, interruption, and variation tests in a manner fully compliant with IEC 61000 – 4 – 11.

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Chapter 1

1.1 Introduction

AC voltage regulators including ferroresonant, thyristor control, and servo-driven types have been designed and implemented by AC voltage regulator manufacturers for the past seven decades. Careful analysis of the fundamental techniques used in these designs indicates that each of them has advantages and disadvantages.

The ferroresonant version has the advantage that it is easy to design but it also has very high no-load power consumption and is very sensitive to frequency change, which is a serious disadvantage. The servo-driven auto transformer version is very bulky and hence slow, though the waveform defects are quite minimal. The thyristor types suffer radio frequency and electromagnetic interferences (RFI and EMI) and therefore require specially designed filters for optimal operation. Though bipolar junction and field effect transistors (BJTs and FETs), along with other power semiconductors, are also used in power conditioning equipment, their use in the design of AC voltage regulators is a fairly new technique [1]. However, switch mode AC voltage regulators have used BJTs/FETs.

1.2 Objectives

In this project, a low-cost, fast-response AC voltage regulator was designed and implemented using power semiconductors (bipolar power transistors). The design approach was quite similar to that of a linear DC regulator, but required the use of an RMS/DC converter and an opto-isolation component in order to achieve a reliable, compact and light-weight unit compared to a ferroresonant type, and a faster response compared to a servo-driven AC voltage regulator. This technique used a buck/boost transformer where the primary winding was connected in series

with a bridge rectifier and a series connected bipolar transistor array was used to simulate the variable impedance across the bridge points. The main function of the bridge rectifier was to avoid voltage reversal across the power transistor array, which consisted of multiple Darlington pairs of transistors connected in series.

An electrically isolated low voltage control circuit was used to complete the system. The overall objectives of the design were as follows:

- Develop a technique to speed up the operation of a servo driven unit, which is commercially available
- Provide electrical isolation for the control loop to ensure safety and reliability of the regulator
- Provide fast response decisions with a soft start
- Investigate possibilities for reducing losses and improving the efficiency of the system.

1.3 Outline

This work is divided into six chapters:

Chapter 1 gives a summary of the entire content of the thesis, including the reason for implementing this project and a brief description of each of the following chapters.

Chapter 2 is a general overview of power quality and power conditioning equipment. This chapter aims to give a general understanding of the causes of power line disturbances (voltage sags, surges, transients, electrical noise, harmonics and power outages) and the use of various types of AC voltage regulators to solve the problem of power line disturbances. The chapter also compares these types of AC voltage regulators in terms of the techniques used and

their advantages and disadvantages. Finally, there is an overview of the various types of uninterruptible power supplies (offline, hybrid, and online UPSs).

Chapter 3 deals with the field measurement of AC voltage regulation and the laboratory test equipment used for voltage regulation measurement. The field measurements were done in the Western Area of Freetown, the capital city of Sierra Leone (located on the west coast of Africa). The laboratory measurements were carried out on a PS10 Smart Power Station (AC voltage regulator) designed by Thor Technologies (Perth, Australia). The equipment used during the laboratory tests was the VDS-2002 Voltage Dip and Swell Simulator (NoiseKen Laboratory Co., Ltd, Sagamihara, Japan)

The main aim of this chapter is to measure the performance of the PS10 AC voltage regulator, which is mechanically driven, so that at a later stage, its performance can be compared with that of an AC voltage regulator with power semiconductors (AC voltage regulator based on a series transistor array).

Chapter 4 deals with the design of the AC voltage regulator based on a series transistor array. This chapter is broadly divided into two sections: the first section is the power stage design which comprises the bridge rectifier, buck/boost transformer, heat sinks and power semiconductors (series transistor array). The second section is the control circuit design which is divided into the following areas: sampling circuit with isolation; RMS-DC converter stage; and finally the transient drive stage. The power and control circuits are coupled together to form the AC voltage regulator.

Chapter 5 is concerned with the practical implementation of both the power and control circuits. Based on the design requirements, the components required were selected and in cases where such components were no longer being manufactured, functional compatible counterparts were used. Both the power and control circuits were built and tested. The transistor array was tested at both 160V and 260V by varying the control current through the quad-opto-isolator and the changes in the array resistance were measured and recorded. Graphs of array resistance versus control current were also plotted for different values of base resistance.

Chapter 6 focuses on the research results, main findings and discussion, including the reasons for various design decisions taken during the implementation stage. It also compares the results for the series transistor array AC voltage regulator with those of the PS10 Smart Power Station in terms of their responses to RMS voltage fluctuation. There is also a discussion on the possible development of this type of AC voltage regulation in order to improve the harmonics content and high power capability. There are some recommendations for improving the performance of the system and a conclusion about the present system.

Chapter 2

2.1 Power Quality and Power Conditioning Systems

Modern electronic systems are exceptionally susceptible to power line disturbances, mainly due to the fact that they are comprised of both high energy power lines and low-power integrated circuits. Power quality describes the quality of voltage and current a facility has, and is one of the most important considerations in modern industrial and commercial applications. It is essential that processes, especially in industrial plants, operate uninterrupted where high productivity levels are an important factor. Power quality problems commonly faced by industrial operations include transients, sags, swells, surges, outages, harmonics, and impulses that vary in duration or magnitude of the voltage [2].

Usually, the energy provided by an electrical utility company is safe and reliable. However, irregularities do occur due to severe storms, equipment failures, and high winds. Lightning striking the utility transmission and distribution system can also cause power line disturbances. In general, most pieces of conventional electrical equipment can tolerate short-term power quality issues without any noticeable effects, but others, including solid-state or electrical equipment like computers and industrial process controls, are more sensitive to changes in power.

Power disturbances can cause data or memory losses, altered data and other functional errors, as well as equipment damage. These, in turn may cause scheduling problems, downtime and expensive troubleshooting.

2.1.1 Electrical Power Transmission and Distribution Systems

The transmission of electrical power refers to the bulk transfer of energy from the plant that generates the power to the required electrical substations which are usually located near demand centres. On the other hand, the distribution of electrical power is the last stage in the supply of electricity to the consumers. That is, the main purpose of a distribution network is to carry electricity from the transmission system to the consumers.

Figure 2.1 shows a typical electrical generation, transmission and distribution system.

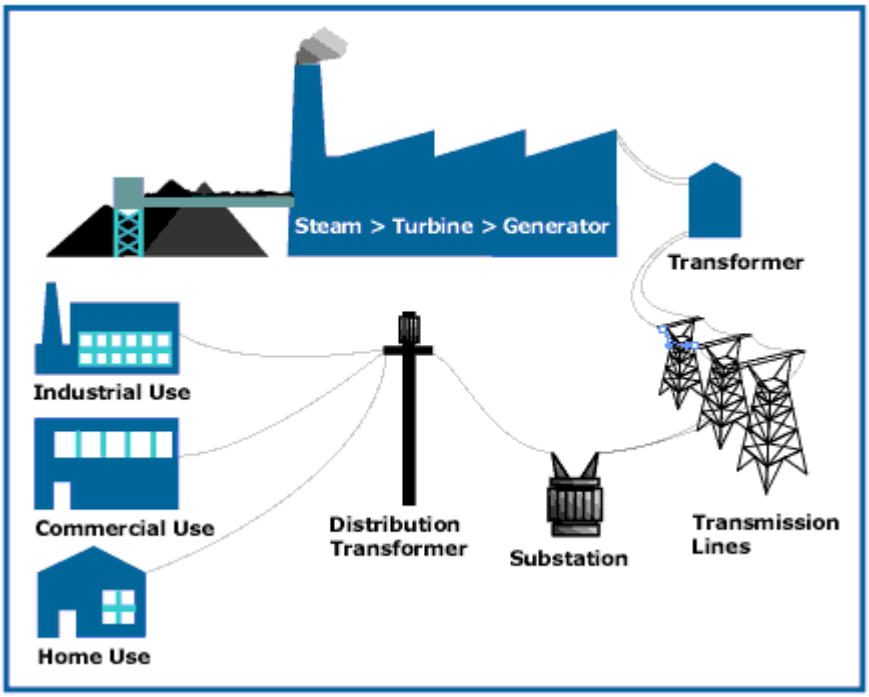


Figure 2.1: Electricity generation, transmission and distribution systems

Normally, the intended voltage supply to consumers is either 110V or 230V ± 6% for an operating frequency of either 60Hz or 50Hz, depending on the country of operation. However, for various reasons, the voltage at the consumer end can either be above or below the intended voltage.

2.1.2 Causes of power line disturbances

Electrical power can be affected by several types of irregularities, including;

- Voltage sags
- Voltage surges
- Voltage transients
- Electrical noise
- Harmonics
- Power outage

2.1.2.1 Voltage Sags

Voltage sags can be described as short-term RMS voltage fluctuations below the normal voltage levels. Sags often fall to twenty percent (20%) below the nominal voltage and are caused when large loads are connected to a power line [3]. They are the most common form of electrical power disturbance. A sag that lasts for more than two seconds is typically referred to as an under voltage [3].

2.1.2.2 Voltage Surges

Voltage surges are short-term RMS voltage fluctuations above the normal voltage levels. Surges are less common than sags, but often more damaging to electronic equipment. They are seen more frequently in facilities with rapidly varying electrical loads, often caused by the switching on or off of electric motors (inductive load switching). A surge that lasts for more than two seconds is referred to as an over voltage [3]. Figure 2.2 is an illustration of voltage sag, surge, overvoltage and under voltage on an AC power supply.

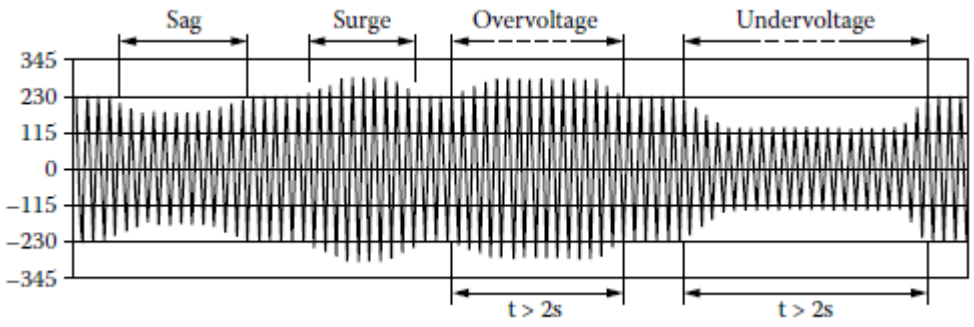


Figure 2.2: Disturbances on a 230 V RMS, 50 Hz utility AC power supply: RMS voltage fluctuation

2.1.2.3 Voltage Transients

Voltage transients are sharp, very brief increases in electrical energy. Such spikes are commonly caused by the ON and OFF switching of heavy loads such as air conditioners, electric power tools, business machines, and elevators [3]. In computers, transient voltages can alter or erase data stored in memories, creating output errors and/or equipment damage which will reduce equipment service life. Normally, the presence of transient voltages can only be detected with special monitoring equipment.

As shown in Figure 2.3, voltage transients are high-pitched, very momentary increases in the supply waveform. Figure 2.4 shows an ideal waveform where all the currents and voltages have a single frequency.

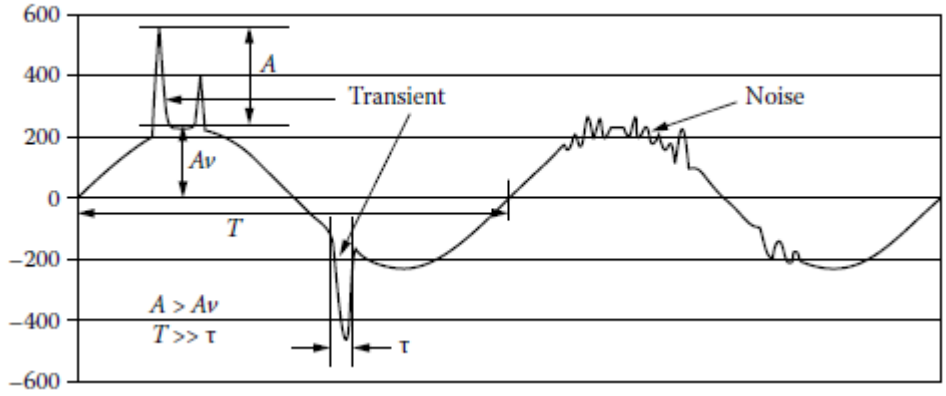


Figure 2.3: Transients and noise superimposed on the waveform

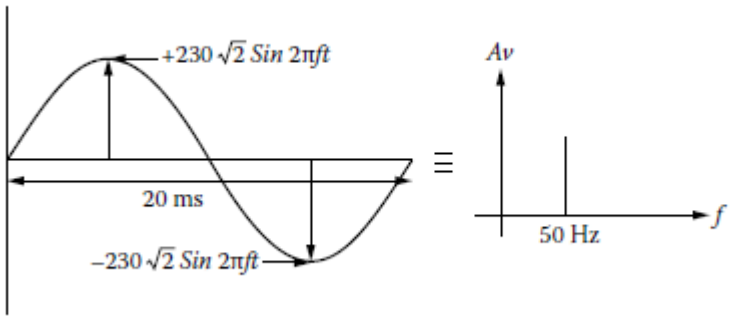


Figure 2.4: An ideal waveform and its frequency spectrum

2.1.2.4 Electrical Noise

Electrical noise is high-frequency interference in the frequency spectrum of 7 KHz to 50MHz [3]. Defective or improperly installed electrical equipment is usually the main source of noise. This equipment can include radio transmitters, microwave transmission and radar, among others.

2.1.2.5 Harmonics

The waveforms of all the voltages and currents in an ideal power system would have the same frequency sine waves. However, the actual voltages and currents of a power system are not pure sinusoidal, although their frequencies are alike when considering the steady state. Such a repeating function, which is actually a series of components, is called harmonics [4]. Figure 2.5 shows a sine wave as the summation of the first and fifth harmonics.

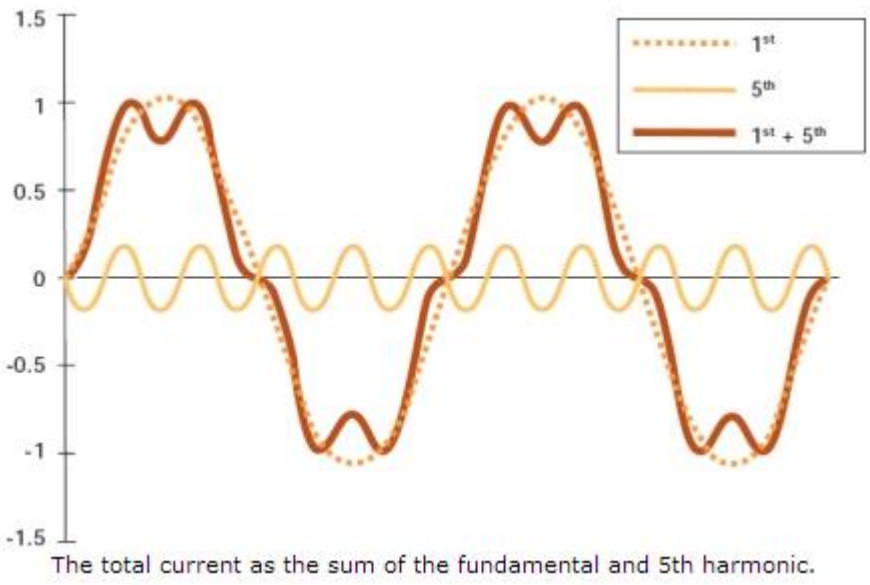


Figure 2.5: A Sine wave as the sum of various harmonics

2.1.2.5.1 Effects of Harmonics on the System Voltage

Harmonic currents drawn from the power system by nonlinear loads create harmonic voltages ($RI + j\omega_n LI$) across the system impedance, and their effect can be significant for higher-order harmonics because inductive reactance increases with frequency. The load voltage is the difference between the source voltage and the voltage drop across the system impedance. Since the voltage drop across the system impedance contains harmonic components, the load voltage may become distorted if the nonlinear loads are a large fraction of the system capacity [3].

2.1.2.6 Power outage/Blackouts

Blackouts are total losses of power and can be momentary or last for extended periods of time. Outages are often caused by electrical load switching in utility power stations. Electrical equipment malfunctions or faults in a facility's power station can also cause power outage.

There are several conditioning solutions for voltage regulation currently available in the marketplace. Among the most common are tap-changing transformers, which are the types of voltage regulators used in today's power distribution systems. However, these methods have significant shortcomings. For instance, a tap-changing transformer requires a large number of thyristors, which results in highly complex operation for fast responses [5].

2.2 Power Protection Equipment

Power line disturbances are the main concern of most industries today. There are tendencies for these voltages to cause high negative impacts on productivity, which is certainly an undesirable aspect in industrial and commercial applications. A solution to these problems is to install a power enhancement system along with a power synthesis system between the utilities and the load to be supplied.

2.2.1 Power Enhancement Systems

These are systems that help to improve the power being supplied by a utility so as to reduce the vulnerability of the load. Among the available power enhancement systems are the following.

- AC Voltage Regulators (ACVR)
- Transient Voltage Surge Suppressors (TVSS)
- Harmonic Eliminators

2.2.1.1 Automatic AC voltage Regulators

As the name implies, an automatic voltage regulator or AVR is basically a device that is intended to regulate AC line voltage automatically: it takes a varying voltage level and regulates it into a relatively constant voltage level.

In AC voltage regulators, the limited range of regulation can be anything from less than one percent change, over a given line and load variation range, to about ten percent or greater, depending on the need and the level of technology implemented [3].

There are various types of AVR, including the following:

- Electronic tap changers
- Motor driven variacs (As in the PS10 Smart Power Station used in this project)
- Ferroresonant regulators
- Thyristor-driven regulators
- Solid state regulators
    - Switch mode regulators
    - Linear regulators

2.2.1.1.1 Electronic tap changer regulators

The electronic voltage regulator is a more practical type with the advantages of power semiconductors, light weight and low cost. Electronic tap changers are electronically controlled devices designed to compensate for line voltage fluctuations by sensing and switching buck or boost taps to vary the primary to secondary turns' ratio in the power transformer [3].

However, in contrast with motor-driven variac regulators, electronic voltage regulators are only used in power quality applications, due to the fact that they are designed for low voltage (<600V) and their higher performance is not necessarily an advantage in line drop compensation applications [6].

As electronics become more prevalent in industrial and commercial applications, the speed and performance advantages of the electronic voltage regulator make it a better fit than the mechanical voltage regulator [6].

Since the design consists of a transformer with multiple taps and a feedback loop to automatically change the taps, it has high efficiency and simple construction. However, with a frequently fluctuating input voltage, there is a possibility of the occurrence of "tap dancing" which creates arcing that is harmful to inductive loads.

A typical example of this type of regulator is the PS10 Smart Power Station designed by Thor Technologies, which is a system that regulates by means of turns ratio variation as detailed in Chapter Three.

2.2.1.1.2 Motor driven variac regulators

The oldest and simplest types of automatic voltage regulators are the motor-driven variacs, where the tap setting of a transformer is changed with the feedback signal from an output monitoring circuit [3]. As more electronics are deployed in industrial settings worldwide, the mechanical voltage regulator is being displaced by the electronic voltage regulator.

The common characteristic of electromechanical voltage regulators is that they all have one or more servomotors to physically move some components within the unit. The purpose of this movement is to affect voltage regulation by changing the turns ratio or magnetic coupling of a transformer. However, there are other devices in these voltage regulators that are used for power quality control.

There are basically two primary methods of operation used by motor-driven variac regulators, which are:

- By simply changing the turns ratio or
- By altering the magnetic induction between the primary and secondary coils of a transformer by physically changing their orientation.

2.2.1.1.3 Ferroresonant regulators

The ferroresonant regulator, also known as a constant voltage transformer, uses the principle of ferroresonance operation of a transformer in the magnetic saturation region. When the iron core of a transformer is in saturation, a relatively large change in winding current will create a very small change in the magnetic flux, since the winding current and magnetic flux are proportional to the input and output voltages, respectively. This means that relatively large changes in input voltage result in small changes in output voltage: this is the fundamental purpose of an automatic voltage regulator.

In Figure 2.6, a simplified version of a magnetization (B/H) curve is used to demonstrate the concept of ferroresonance. The region of saturation is shown in red, where it can be seen that a large change in input voltage results in a small change in the output voltage. Operation in the saturation region has the disadvantage of very poor electrical efficiency. Standard power transformers are designed to operate in the normal range (blue) where electrical efficiency is higher.

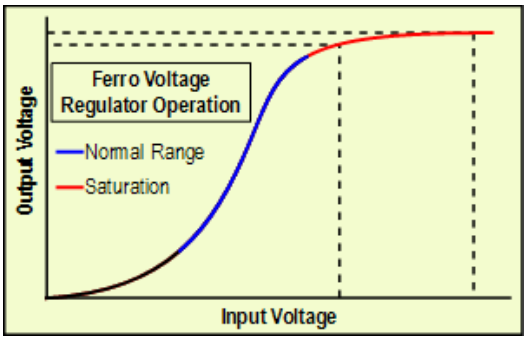


Figure 2.6: Magnetization curve of a Ferroresonance voltage regulator [6]

The major advantage of the constant voltage transformer is that this type of regulator can have electrical efficiency of up to 92 percent at full load and ideal conditions, but the efficiency drops substantially at low loads. Figure 2.7 shows the typical range of ferroresonant regulator efficiency versus percentage load. It can be seen that at 50% load, the voltage regulator efficiency ranges from 75 to 85%. By comparison, a typical power transformer would have an efficiency of 90% or more at 50% load [3].

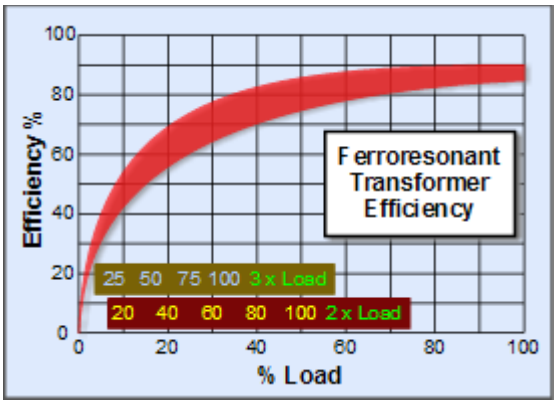


Figure 2.7: AC voltage Regulator efficiency vs load [6]

Resonance

The inductive and capacitive reactances of a resonance circuit are equal to each other [7]. The resistance of the circuit is the only opposition to the flow of current in the resonant circuit, resulting in undesired under voltages and over voltages at the resonance frequency [8]. This resonance effect presents a stable operation state, and its effects are mitigated by the system frequency control or by the introduction of pure resistances.

As stated, since the inductive and capacitive reactances are considered to be equal, then

$$\omega L = \frac{1}{\omega C} \dots\dots\dots\dots\dots\dots\dots (2.1)$$

From which $$f = \frac{1}{2\pi\sqrt{(LC)}} \dots\dots\dots\dots\dots\dots\dots (2.2)$$

where f is the resonant frequency, and L and C represent the inductance and capacitance of the circuit respectively.

Ferroresonance is a special type of resonance situation with nonlinear inductance; hence, the inductance does not only depend on frequency, but also on the magnetic flux density of an iron core coil. Since the inductive reactance is represented by the saturation curve of the magnetic iron core, this nonlinear inductance can be represented by two inductive reactances, according to the location on the saturation curve [9].

For the linear zone,

$$X_{L,linear} = \omega L_{linear} \ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.3)$$

For the saturation zone,

$$X_{L,sat} = \omega L_{sat} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.4)$$

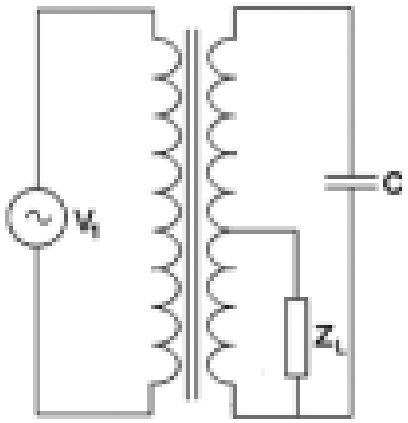


Figure 2.8: Electric circuit of a ferroresonant transformer [10]

The output waveform of a fundamental ferroresonant transformer as shown in Figure 2.8 will take the form of a square wave (as a result of the flattened top) which results in its suitability for many types of loads. However, it is not a very good power supply for some electronic loads without the addition of a harmonic filter choke. With such a filter, a large part of the output harmonic content is cancelled, producing sine waves with relatively low total harmonic content [3].

2.2.1.1.4 Thyristor Driven voltage regulator

Another efficient and very simple type of AC voltage regulator is the thyristor or Silicon Controlled Rectifier (SCR) AC voltage regulator. In this design, whenever the output voltage is below the desired value, the SCR is triggered, allowing electricity to flow into the load until the AC mains voltage passes through zero, which is usually the end of the half cycle. However, SCR-controlled voltage regulators are not capable of very accurate voltage regulation in response to rapidly changing load. Figure 2.9 shows a thyristor-controlled AC voltage regulator.

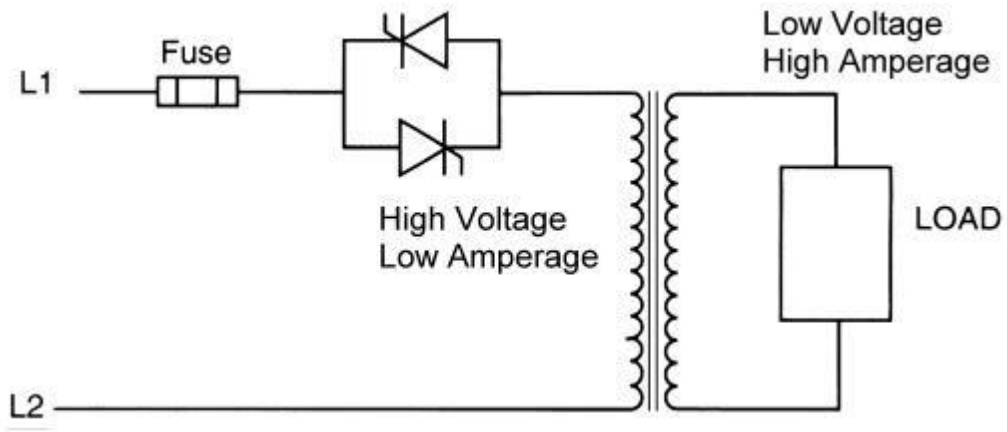


Figure 2.9: Thyristor controlled AC voltage regulator [11]

2.2.1.1.5 Solid State Voltage Regulator

The solid state voltage regulators that will be discussed in this section are

- Switched-mode AC voltage regulators and
- Linear AC voltage regulators

Switch-mode AC voltage regulator

Numerous AC voltage regulators have been considered as a solution to RMS voltage fluctuation. But in every case, it has been observed that the power factor

at the input is extremely low and the efficiency is also very poor [12]. The power factor and the efficiency can be enhanced by applying a switch-mode technique.

AC Switch Mode Power Supplies (SMPS) use power-handling electronic components which are continuously switching on and off at a very high frequency in order to achieve transfer of electrical energy. In this case, the output voltage is controlled by varying the duty cycle. The typical frequency range of SMPS is from several KHz up to several MHz. The smaller size of SMPS is due to the high operating frequency since the sizes of power transformers, inductors, and filter capacitors are inversely proportional to the frequency.

Figure 2.10 shows the power circuit of a switch mode AC voltage regulator.

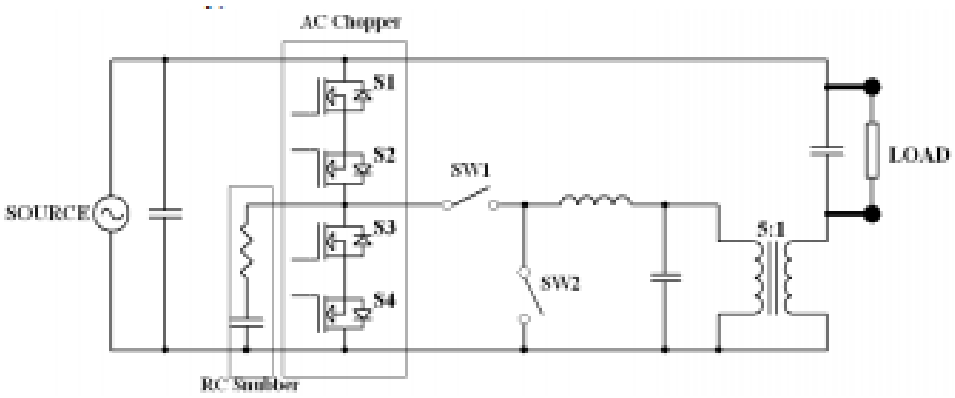


Figure 2.10: Power Circuit of the switch mode AC voltage regulator [13]

The main features of this type of regulator can be summarized as:

- Rapid dynamic response
- Capability of removing voltage harmonics
- Improvement of input power factor
- Paralleling individual modules to achieve higher power ratings

- Low number of active power switches, hence low losses, higher efficiency and better economy

The major limitation in using high frequency AC-AC voltage converters is the commutation problem. This problem causes voltage spikes, especially when the load is inductive [14].

A suitable way to protect the switches of a switch mode AC regulator against voltage spikes is shown in Figure 2.10 using RC snubbers. The switching pattern is based on the voltage sign and during the dead time when all switches are off, the current passes through the snubber. Using RC snubbers leads to higher losses and lower efficiency. This method is not efficient in high inductive loads [14].

Linear AC voltage regulators

Linear regulators are mostly centred on devices that usually operate in the linear region, as opposed to the switch mode counterpart which is based on a device forced to act as an on/off switch. Formerly, different components were used as the variable impedance. However, contemporary designs use one or more transistors instead, as in the case of the voltage regulator in this project (voltage regulator based on a series transistor array).

- **AC voltage regulator based on a series transistor array**

  The technique used in the design of a series transistor array voltage regulator uses a power semiconductor array associated with a non-resonant transformer for AC line voltage regulation, using a closed loop circuit designed around a

commercial RMS/DC converter chip. The technique can achieve an overall weight and size reduction, fast response and waveform fidelity [15].

The techniques used in the design of a series transistor array voltage regulator are summarised in Figure 2.11. The implementation uses a buck/boost transformer where the primary is connected in series with a bridge rectifier and a bipolar power transistor array is used as variable impedance across the bridge points.

The bridge rectifier prevents the reversal of voltage across the array of power transistors, which consists of multiple Darlington pairs of bipolar junction transistors.

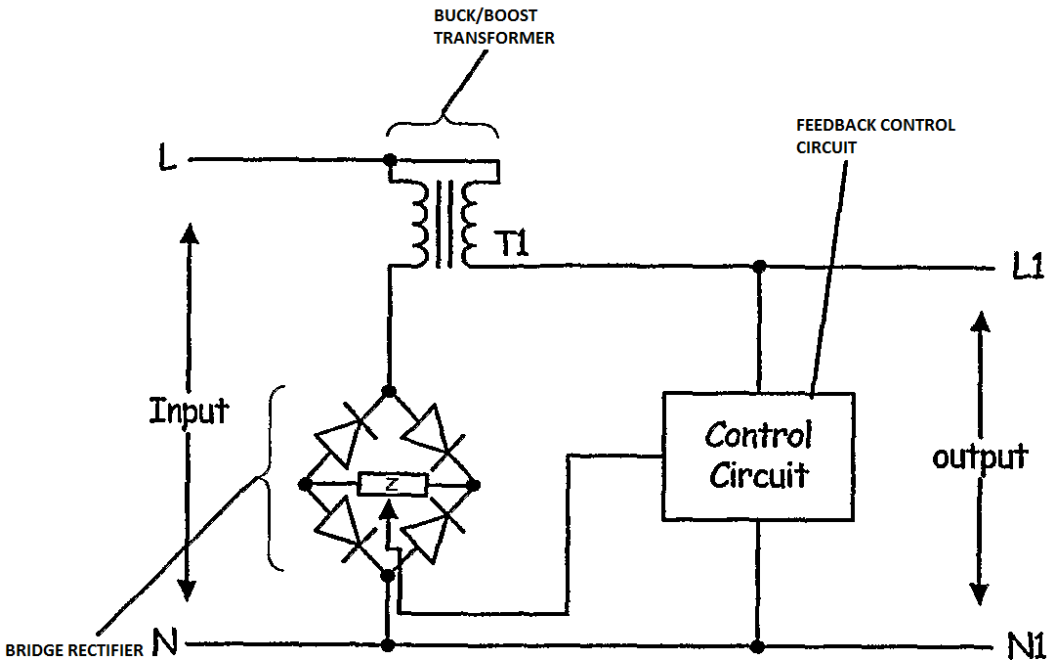


Figure 2.11: Complete block diagram of the voltage regulator based on series transistor array

- **Basic concept of a Series Power Semiconductor Array**

If we consider the turns ratio of the transformer used in the design to be n, with a nominal output voltage V_O and maximum RMS load current I_L, then the regulator can regulate the input voltage V_{IN} varying between,

$$\left\langle Vo(1-\frac{1}{1+n}) < \left|Vo\right| < Vo(1+\frac{1}{1+n}) \right\rangle \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.5)$$

If the bipolar power transistor array consists of m elements, the voltage across the array will be given by

$$V_{Array} = \left((mR_B/h_{FE}) * I_C(1+\left(\frac{h_{ie}}{R_e}\right)) + (mR_B/R_e) * V_{be} \right) \ldots\ldots\ldots\ldots (2.6)$$

For the same m-elements BJT array, it can be shown that the approximate effective instantaneous resistance R_{Array} at the AC input of the circuit is given by,

$$R_{Array} \approx \left(\left(\frac{mR_B}{\beta}\right) * \left[1+\left(\frac{I_x}{I_b}\right)\right] \right) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.7)$$

Where I_x is the amount of base current diverted by the opto isolator, I_b is the instantaneous base current and R_b is the resistance between collector and base of the m^{th} transistor [16].

For a 4-element array, where m = 4, the effective instantaneous resistance becomes

$$R_{Array} \approx \left(\left(\frac{4R_B}{\beta}\right) * \left[1 + \left(\frac{I_x}{I_b}\right)\right]\right) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.8)$$

and

$$\left(R_1 = \left(\frac{R_B}{4}\right); R_2 = \left(\frac{R_B}{3}\right); R_3 = \left(\frac{R_B}{2}\right); R_4 = R_B\right) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2.9)$$

This in effect indicates that the ratio $(Ix|Ib)$, which is defined as the base current diversion ratio (BCDR) needs to be controlled. This technique also provides the necessary electrical isolation between the low voltage control circuits and the power stage.

2.2.1.1.6 Reasons for Implementing the Series Transistor Array voltage regulator

Among all the AC voltage regulator techniques outlined above, the series transistor array technique is light-weight, cost effective and quite easy to assemble compared to its counterparts. Also, since servo-driven auto transformer voltage regulators are bulky and slow in response to voltage fluctuation, the transistor array technique can safely supplant the servo-driven type due to its fast response. Hence, this project outlines the detailed design and implementation of a series transistor array AC voltage regulator.

2.2.1.2 Transient Voltage Surge Suppressor (TVSS)

Surge suppression is crucial to any power quality and power protection system, including lightning protection and three phase power systems. TVSSs guard against transient overvoltage, sometimes called transients, spikes or surges, hence the name Transient Voltage Surge Suppressor or TVSS. Transients are known to damage sensitive electronic equipment in homes, schools, commercial, industrial, and medical facilities, wastewater treatment plants, and factories.

The downtime, damage, and destruction caused to critical or electronic loads costs billions of dollars a year. TVSS is now the standard technology for increasing the reliability and uptime of microprocessors [17].

Table 2.1 briefly compares the various available TVSS devices.

Table 2.1: Comparison of TVSS devices

Suppression element	Advantages	Disadvantages	Expected life
Gas tube	·Very high current handling capability ·Low capacitance ·High insulation resistance	▪Very high firing voltage ▪Finite life cycle ▪Slow response times ▪Non restoring under DC	·limited
MOV	·High current handling capability ·Broad current spectrum ·Broad voltage spectrum	·Gradually degradation ·High clamping voltage ·High capacitance	·Degrades
TVS diodes	·Low clamping voltage ·Does not degrade ·Broad voltage spectrum ·Extremely fast response time	·Limited surge current rating ·High capacitance for low voltage types	·Long limited
TVS thyristors	·Does not degrade ·Fast response time ·High current handling capability	·Non restoring under DC ·Narrow voltage range ·Turn-off delay time	·long

2.3 Comparing Different types of Voltage Regulators

The performance of different commercial families of AC Voltage Regulators is compared in Table 2.2. However, the information is particularly applicable to the single phase systems used by end users with output ratings ranging from a few hundred Watts to a few kiloWatts [22].

Table 2.2: Comparison of AC voltage regulators [22].

Family	Basic Technique used	Advantages	Disadvantages
Motor driven variacs	A servo motor-based auto transformer with a voltage feedback loop	Simple construction High capacity Simple electronics High efficiency	Bulky Slow response Can get stuck at the lowest input voltage and create an over-voltage when the line voltage returns to normal
Transformer tap changers	A transformer with multiple taps and a feedback loop to automatically change the taps	High efficiency Easy to design Simple construction Low cost	If input voltage fluctuates frequently "tap dancing" can occur Arcing in taps can create problems with inductive loads Voltage transients may appear at the output during tap changes
Thyristor-based designs	A series secondary winding or an auto transformer is used with a thyristor phase controlled technique to maintain the RMS voltage constant	Compact Low cost Efficient Fast response	High harmonic content at the output Could cause problems with inductive loads Filtering at output may be necessary for reducing RFI/EMI issues

Family	Basic Technique used	Advantages	Disadvantages
Ferro-resonant regulators	A precisely gapped transformer is used in resonance with a capacitor to create a resonant circuit, while core saturation is used for regulating the output voltage.	Very reliable Simple design Can withstand a fractional or few cycle outage at the input side Differential mode transients can be tolerated	Non-sinusoidal output with flattened top Power factor dependant load regulation Extremely sensitive to frequency fluctuations on the input side (*i.e.*: when a small standby generator is used as the AC input) Low efficiency and no load power consumption of 20% - 30% of the VA rating
Solid state types	Either linear amplifier based technique or switching technique based compensation is used	Wide input range is possible Compact design may be possible (with a switching technique for voltage buck or boost)	Complex circuitry RFI/EMI problems (in switching technique based ones) Reliability issues in environments with high common mode transient surges

2.4 Uninterruptible Power Supplies

Concerns over process disruptions, which involve critical and sensitive loads, have prompted researchers to find ways to enhance power quality, such as developing voltage sag and surge mitigation techniques. Effectively, these mitigation devices can be grouped into two classes: custom power devices and power line conditioners [19]. However, more emphasis is focused on one type of power line conditioner, which is the uninterruptible power supply (UPS).

UPSs may be classified as emergency power sources which have various applications in critical equipment, such as computers, automated process controllers and hospital instruments. With rapid growth in the use of high efficiency power converters, more and more electrical loads are nonlinear and generate harmonics. It is a big challenge for a UPS to maintain a high-quality sinusoidal output voltage under nonlinear loading conditions [20].

Modern UPSs can be categorised into three basic types, namely:

- Offline UPS
- Hybrid UPS
- Online UPS

2.4.1 Off-Line UPS

The simplest form of backup power systems are offline UPSs. This type of UPS system normally operates in the offline mode, that is, the load is generally powered by the utility line. When the utility power supply goes beyond the acceptable limits of the system, or there is an outage, the load is automatically transferred from the utility line to the UPS.

An offline UPS has the advantages of lower cost, smaller size and higher efficiency due to the fact that the system is offline and the load is directly powered by the utility supply. However, switching to the inverter is only required when the load is vulnerable and hence this approach is not suitable for situations with frequent power failures.

The time taken by the system to change from the utility supply to the UPS is called the *transfer time* of the system. Figures 2.12 and 2.13 are, respectively, the block diagram of an offline UPS and a display of an oscilloscope graph of AC output during the transfer process of a typical offline UPS.

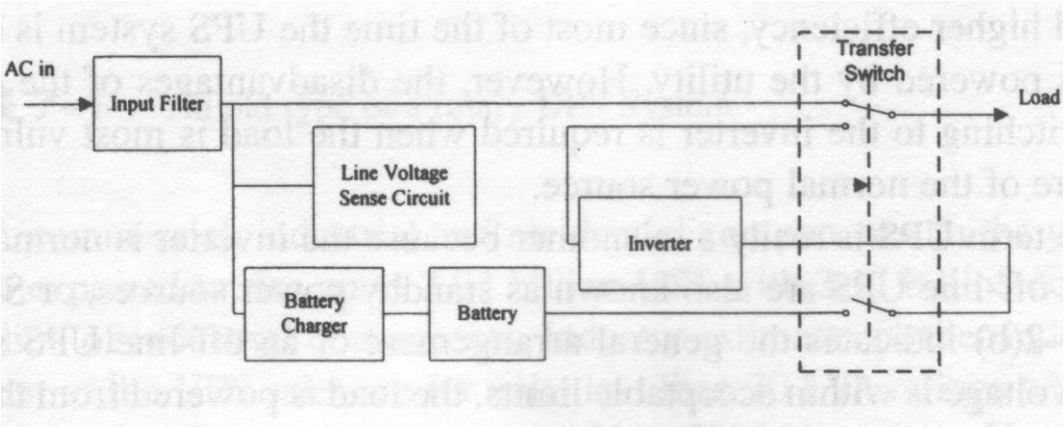


Figure 2.12: Block diagram of an offline UPS with transfer process [3]

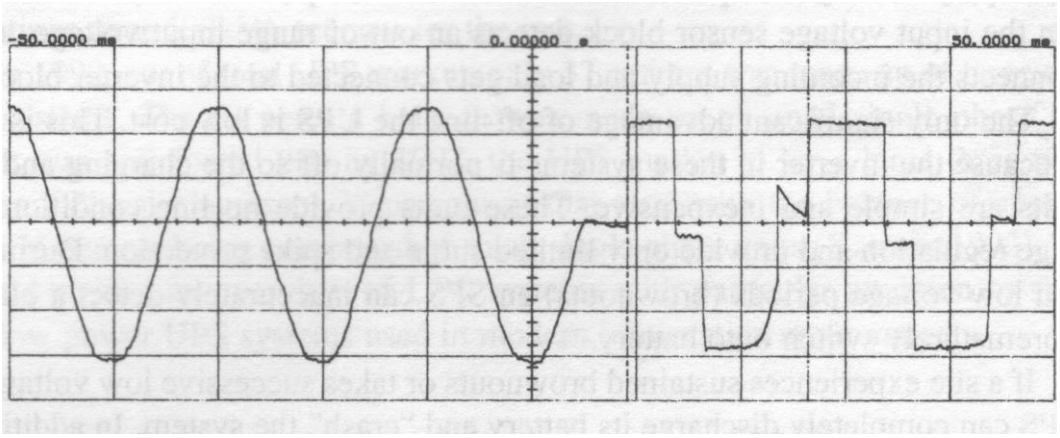


Figure 2.13: An oscillograph of AC output during transfer process [3]

2.4.2 Line Interactive UPS Systems

In the design of this type of UPS, the battery and the AC power inverter are perpetually connected to the UPS output. In the event of power failure, the transfer switch can shift electrical flow from the battery to the system output. Because the inverter is continuously connected to the output, the UPS provides additional filtering and lowers the risk of switching transients. This design (Figure 2.14) has a high level of efficiency and reliability in addition to its small size and low cost, making it suitable for a range of uninterruptible power applications [21].

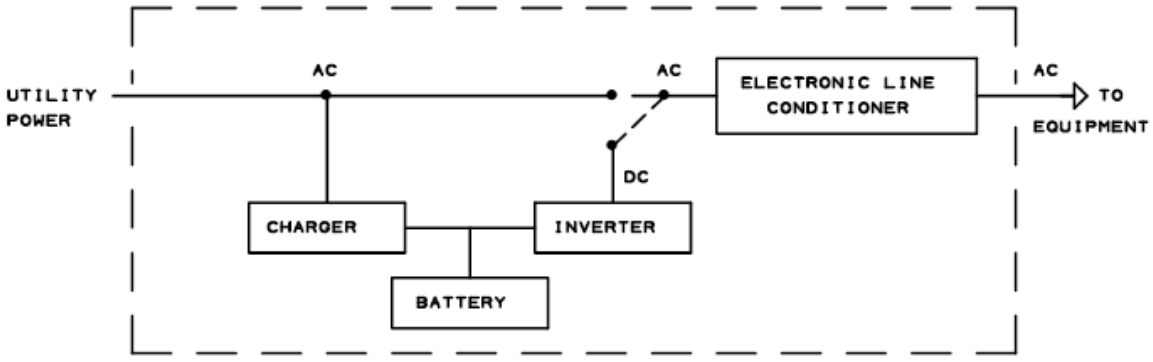


Figure 2.14: Block diagram of a Line Interactive UPS with an electronic line conditioner [3]

A line interactive UPS will provide all the features of an offline model, with the additional features of Boost and Buck which allow the load to be supplied from the mains by providing a low and high voltage operation mode [3].

2.4.3 On-Line UPS Systems

This type of UPS is the ideal type with maximum performance. The charger and inverter operate all the time. Since they continuously regenerate clean AC power, they provide the highest level of protection available, regardless of the utility line condition. However, these units have much more complex designs than the other two systems previously discussed, while the price, weight and size are also higher.

Figure 2.15 shows a block diagram of a typical Online UPS;

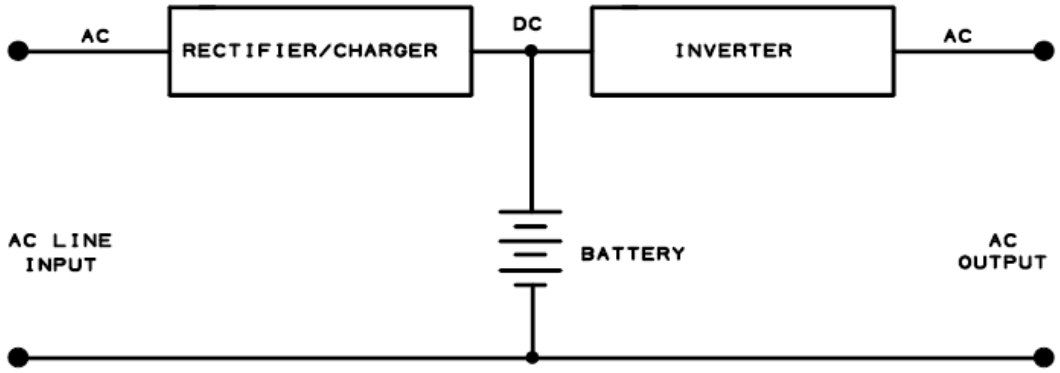


Figure 2.15: Block diagram of an Online UPS [3].

Chapter 3

3.1 Field measurements of AC voltage regulation

The ability of an electrical system to maintain a near-constant voltage over a wide range of load conditions is referred to as the voltage regulation of the system. In this project, a load regulation survey was carried out in Sierra Leone, West Africa, to monitor the variation in the power supplied by the National Power Authority (NPA) as the load conditions changed.

3.2 Voltage fluctuations in the Western Area of Sierra Leone

Sierra Leone is a country which is located on the west coast of Africa. Due to very wide fluctuations and poor conditioning of the power supplied by its National Power Authority, the use of a fast-response AC voltage regulator is very necessary for both domestic and commercial use of the supplied power. During this research, the pattern of AC voltage distribution in Sierra Leone was monitored and recorded at three locations in the western area: Lumley, Kissy and Crab Town, all located in the capital city, Freetown.

Figures 3.1 to 3.3 show the voltage distribution in these areas for 24 hours' complete monitoring.

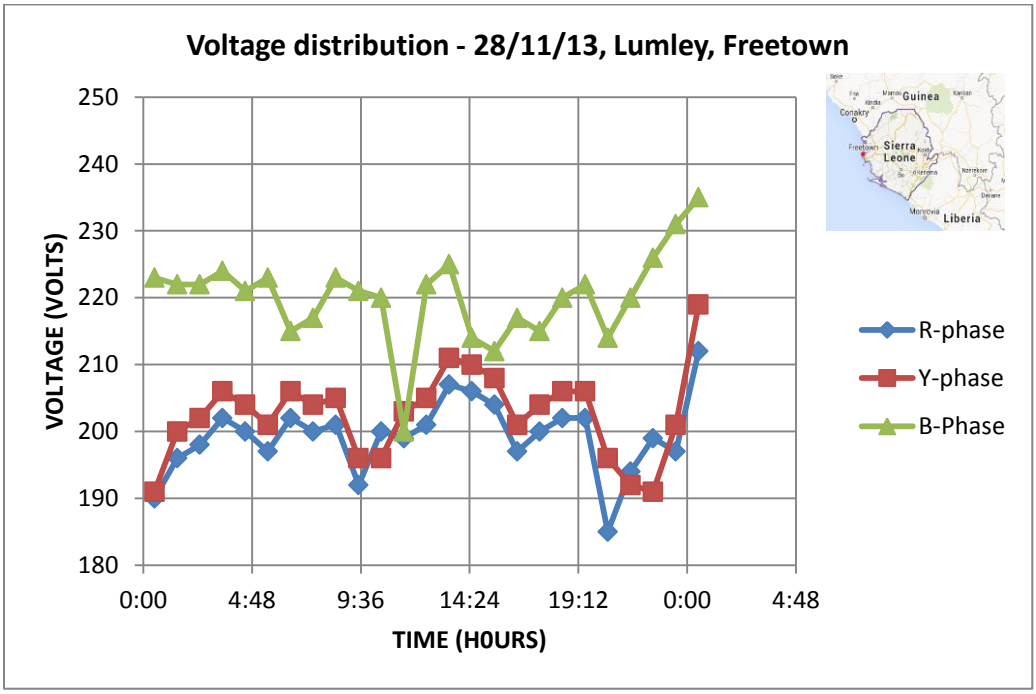


Figure 3.1: Voltage variations in an over-loaded distribution line in Lumley-Sierra Leone

(Source: National Power Authority, Sierra Leone)

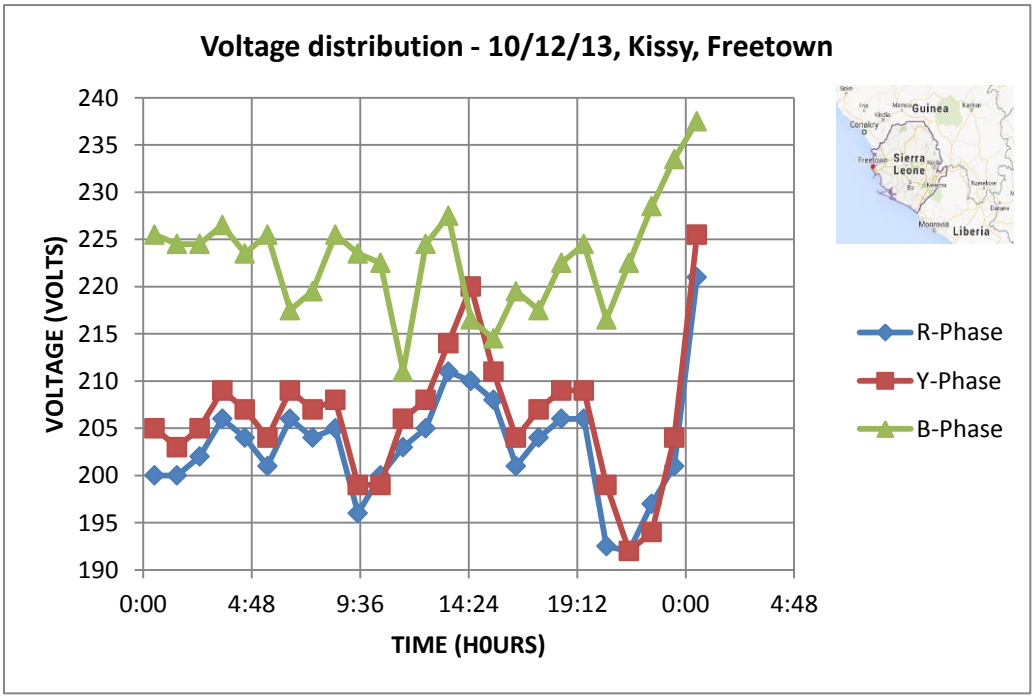


Figure 3.2: Voltage variations in an over-loaded distribution line in Kissy-Sierra Leone

(Source: National Power Authority, Sierra Leone)

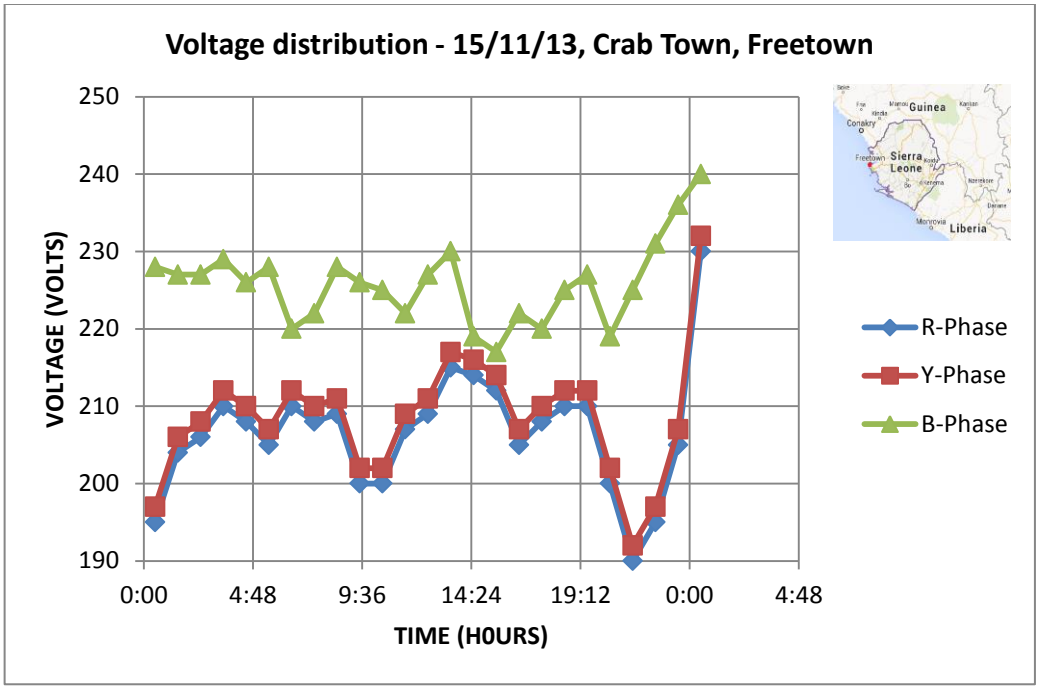


Figure 3.3: Voltage variations in an over-loaded distribution line in Crab Town-Sierra Leone

(Source: National Power Authority, Sierra Leone)

The results indicate that there is a wide range of RMS voltage fluctuation over a period of time. The minimum voltage at peak load was found to be 190VAC which does not comply with the desired voltage of 230VAC ± 6% as per British regulation standard (BS 7671). The B-phase was always at a higher voltage than the others which indicates load misbalancing. As a result of this wide range of RMS voltage fluctuation, there is a need for the use of fast-response AC voltage regulators between the utility and the loads to be supplied. In that regard, this project will be examining the possibility of replacing the servo motor of an existing AC voltage regulator designed by Thor Technologies (PS 10 Smart Power Station) with semiconductor electronic components (series transistor array) in order to improve the response time to fit a widely fluctuating utility.

3.3 Laboratory Simulation of Field Conditions

The conditions from the field survey of AC voltage regulation discussed in the previous section were simulated in the laboratory using a Voltage Dip and Swell Simulator to examine the performance and responsiveness of the PS10 Smart power station designed by Thor Technologies.

3.3.1 The Voltage Dip and Swell Simulator

The Voltage Dip and Swell Simulator used in this project was the VDS-2002 (NoiseKen Laboratory Co., Ltd, Sagamihara, Japan) which can be used to perform voltage dip, swell interruptions, and variation tests in a manner which is fully compliant with the International Electrotechnical Commission (IEC) IEC 61000 – 4 – 11 (1994) standard and its second edition (2004). The optional remote control software can expand the variation of the tests for AC as well as DC voltage interruption in a more convenient and extensive manner.

Figure 3.4: VDS 2002 dip and swell voltage simulator

3.3.2 Basic features of the Voltage Dip and Swell Simulator

The most prominent feature of this device is that in addition to manual control, it can be controlled by a PC via an optical interface which enables the device to be controlled remotely. Various tests can be run remotely using the PC, which has the advantage of giving an increase in the range of parameters.

In addition, the simulator also has High Inrush current capability and floated Trig OUT output so that relevant waveforms can be easily captured. The Trig OUT always outputs a Transistor -Transistor Logic (TTL) signal that is synchronized with switching between the base level and the test level. The output of the TTL signal is HIGH when the equipment under test output is at test level; otherwise it is low.

The equipment under test output has a block terminal and plug-in terminals both in parallel that can be connected to the block terminal with a probe in order to view the voltage level on an oscilloscope. Figure 3.5 shows the electrical schematic of the VDS-2002 simulator.

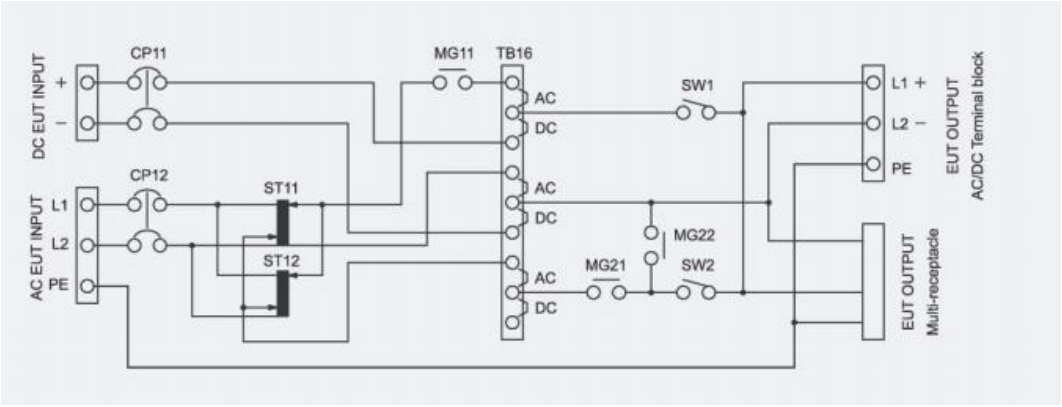


Figure 3.5: Electrical schematic of the VDS-2002 simulator

3.3.2.1 Manual tests performed on the Voltage Dip and Swell Simulator

The following tests were performed manually using the voltage dip/swell simulator:

- Voltage dip/short interruption and swell tests
- Voltage variation tests

The Voltage Dip/Swell test was done by setting the following parameters on the voltage simulator to levels as follows:

Test Level: 0%, 40%, 70%, 80%, and 120%.

Dip Cycles: 0.5, 1, 5, 10, 12, 25, 30, 50, 250, 300

Dip Phase: 0, 45, 90, 180, 225, 270, 315, and 360 degrees.

Interval cycles: this is usually done by setting the IEC to 10s and can be changed from one interval to another from 1, 3, 5, 10, 30, 50, 100, 300, and 500.

Interruption Test: this is achieved by setting the Test Level to 0%

The voltage variation test was achieved with the following settings:

Dip Cycles: it should be slightly changed until it indicates “vary” which means that the voltage variation test mode is set.

Dip Phase: Not needed.

3.3.2.2 PC Remote Interface

The dip/swell voltage simulator can be connected to a PC using an optical cable so that tests can be performed through the PC using the VDS-2002 interface. The main advantage of this mode is that parameters can be changed to a larger extent.

The following are the tests that can be performed:

- IEC Test
- AC variation Test
- AC Dip Test
- DC interruption test.

In IEC tests, the test level was set at 0, 40, 70 and 120% of base voltage.

3.3.2.3 Safe Operating Procedures of the Voltage Dip and Swell Simulator

The Voltage Dip and Swell Simulator is a testing instrument which receives AC mains and modifies its RMS value, waveform to feed the device under test. It works as an AC power source derived from an AC mains and it can be dangerous if not used correctly. The following are the most important safety precautions to be followed when using the equipment.

- The instrument has a 3-pole AC inlet. Be sure to connect it to an appropriate grounded AC outlet to avoid shock hazard
- Use proper AC cord according to the local AC supply voltage
- When replacing fuses, use ones with the same blow characteristics and rating. Before replacement, be sure to disconnect the instrument from AC supplies
- The Protective Earth (PE) terminal of the Equipment Under Test (EUT) input is independent from the ground conductor of the 3-pole AC inlet of the instrument supply. When testing for EUT with PE, be sure to connect the PE terminal of the EUT INPUT to an appropriately grounded AC supply.

- The EUT and relevant AC supply shall not exceed AC 240V 16A. In-rush current shall be suppressed to <500A (10ms). In the event of a higher value, the instrument may be damaged.

3.4 The PS10 Smart Power Station AC voltage regulator

The PS10 Smart Power Station is a servo-driven AC voltage regulator with a default output voltage setting of 240V. However, the select switch at the rear position can be changed to 220V. The PS10 Smart Power Station does not regenerate the sine wave. This means the total harmonic distortion (THD) that the power station delivers is exactly what the power utility supplies. This ensures that the output isn't compromised. Figure 3.6 shows a summarised block diagram of a servo-driven AC voltage regulator.

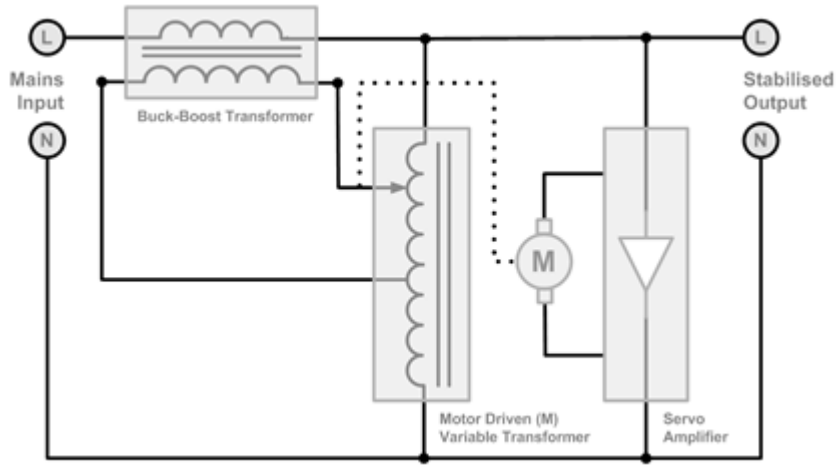


Figure 3.6: Block diagram of a servo-driven AC voltage regulator

3.5 PS10 Performance test using the Voltage Dip and Swell Simulator (VDS 2002)

There are various tests that can be performed on the PS10 AC voltage regulator to measure its performance. The following tests were carried out:

- Delays seen during voltage dip and voltage swell
- Load regulation test
- Line regulation test

During these tests, the test equipment was connected as shown in Figure 3.7. The PS10 Smart Power was powered from the equipment under test (EUT) output of the dip and swell simulator and the lamp load was supplied by the output of the PS10. With this configuration, both the input and output waveforms were captured for analysis.

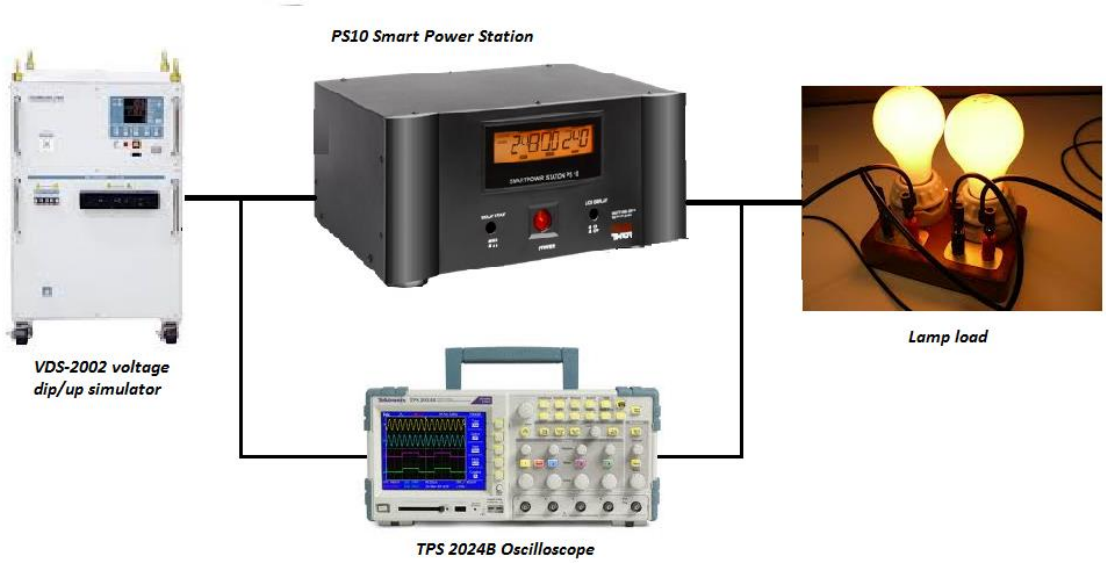


Figure 3.7: Laboratory setup for measuring the performance of the PS10 AVR

3.5.1 Using the VDS-2002 Voltage Dip and Swell Simulator to measure the performance of the PS10 AC voltage regulator

The VDS-2002 has the ability to output the exact waveform that is supplied by the AC mains. However, by setting appropriate parameters, voltage dip or swell can be created. In these tests, both voltage dip and swell were created and then inputted to the PS10 and the delays in response were measured for both cases. The parameters of the VDS-2002 Dip/swell simulator were set to the values shown below so that the performance of the PS10 Automatic Voltage Regulator could be monitored.

3.5.1.1 Voltage dip test

The voltage dip test was done by setting the simulator test level to 40 percent of the base voltage and the other parameters were set as follows:

Test Level: 40%, Dip Cycles: 5, Dip Phase: 45 degrees, Interval: (10s), Repeat count: 1, Figure 3.8 shows the output waveform of the simulator during the voltage dip test. This was fed to the PS10 input and the output delay was observed.

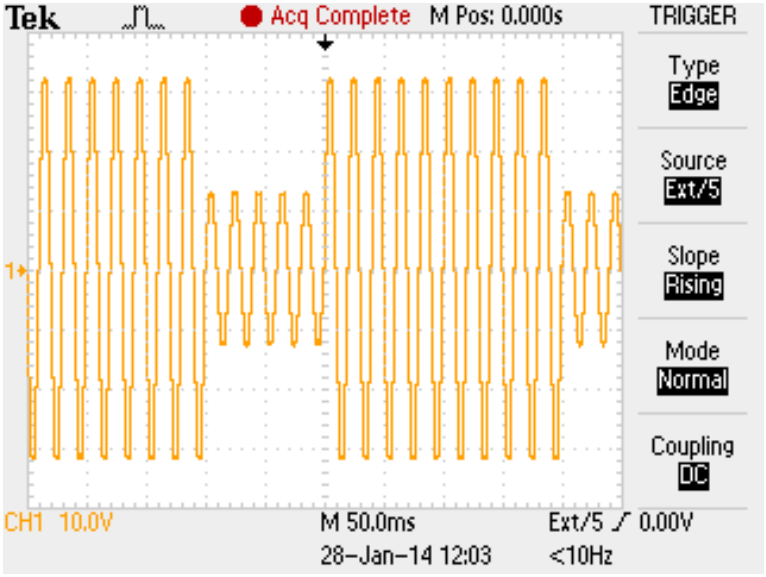


Figure 3.8: Input waveform (output of simulator) to the PS10 AVR with 40% base voltage

Figure 3.8 is a snapshot of the output voltage from the Voltage Dip and Swell Simulator with a Dip cycle of 5. The output is a top-flattened sine wave at an output voltage of 240 Volts.

Figure 3.9 shows the output waveform of the Dip and Swell Simulator at a dip phase of 45 degrees and the delay seen from low to high at this trigger point. The delay at the simulator output (PS10 input) was approximately 3.5µs at a dip phase of 45°.

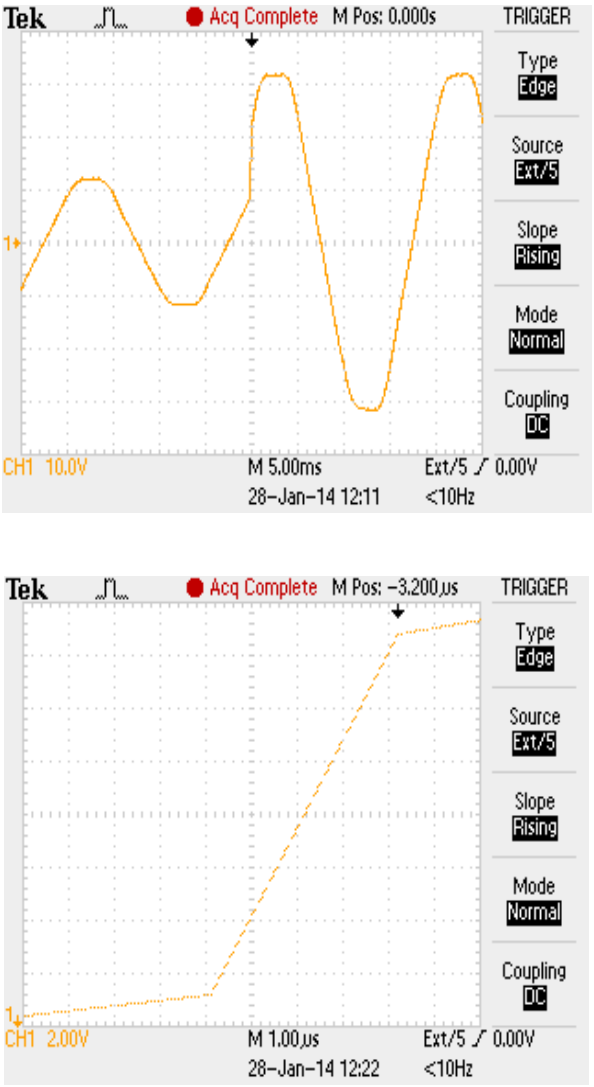


Figure 3.9; PS10 Input waveform (output of simulator) and delay seen at trigger point with a Dip phase of 45 degrees and 40% base voltage

The Dip phase was then set to 90 degrees and all the other parameters of the Dip/swell simulator remained the same. Figure 3.10 shows the output waveform of the simulator and the delay seen at this trigger point. At a dip phase of 90̊, the delay seen at the output of the simulator (input to PS10) was approximately 2µs.

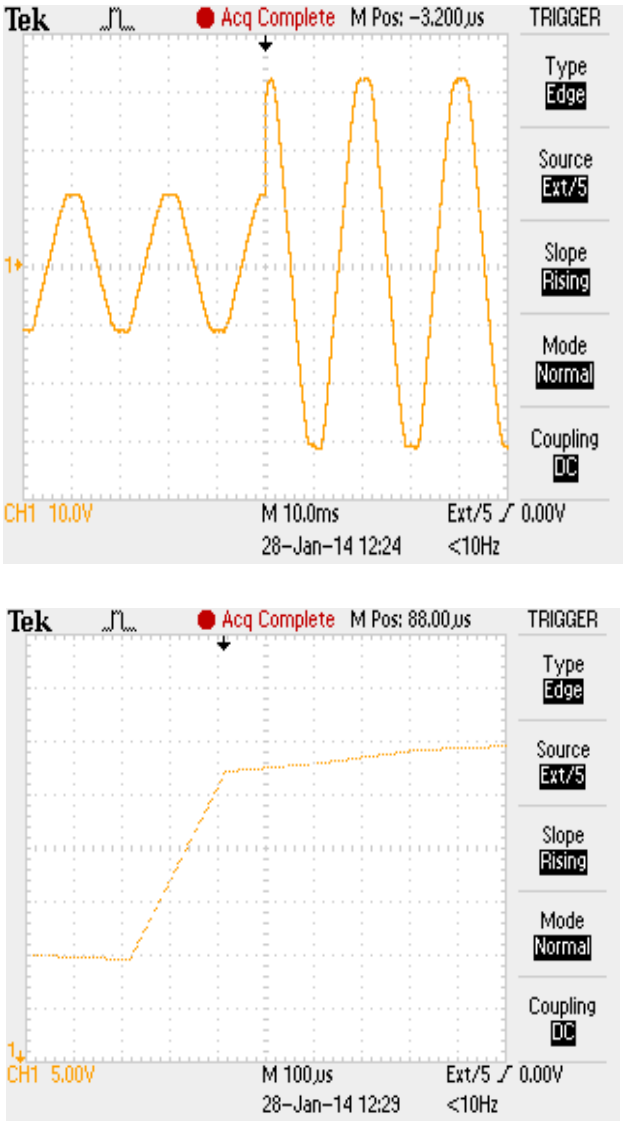


Figure 3.10: PS10 Input waveform (output of simulator) and delay seen at trigger point with a Dip phase of 90 degrees and 40% base voltage

3.5.1.2 Voltage swell test

The voltage dip/swell simulator was then set to 120 percent of base voltage and the other parameters were set as outlined below.

Test Level: 120%, Dip Cycles: 5, Dip Phase: 45 degrees, Interval: (10s), Repeat count: 1, Lamp loads. The input waveform to the PS10 automatic voltage regulator is shown in Figure 3.11.

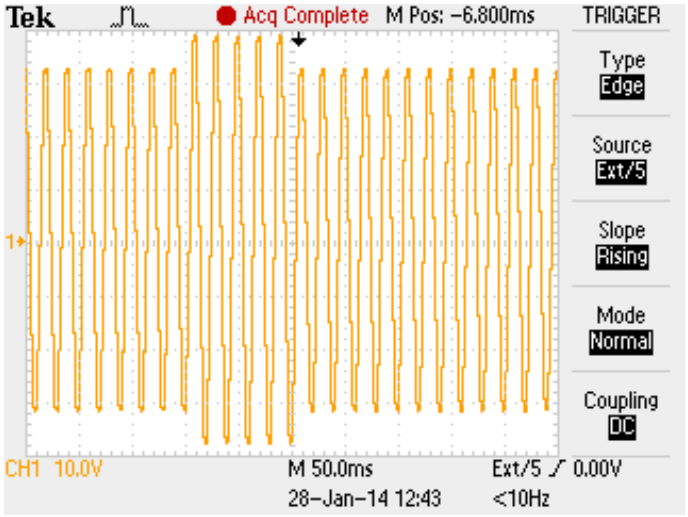
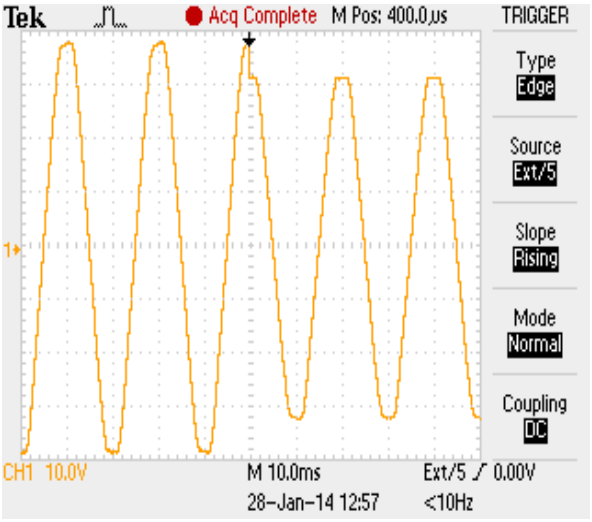


Figure 3.11: Input waveform (output of simulator) to the PS10 AVR with 120% base voltage

The waveform and the delay seen at this point of trigger from high to low are shown in Figure 3.12 at a dip phase of 45°.



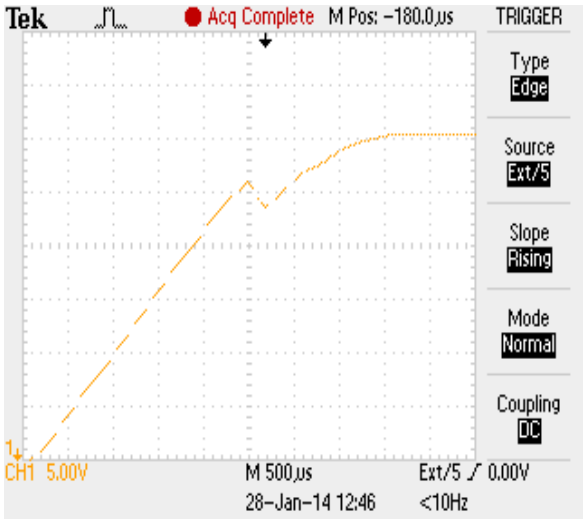


Figure 3.12: PS10 Input waveform and delay seen at trigger point with a Dip phase of 45 degrees and 120% base voltage

3.5.1.3 Delays seen at the output of PS10 voltage regulator for voltage dip test

The delay seen at the output of the PS10 Smart Power Station during the voltage dip test is shown in Figure 3.13. The delay was approximately 1.5s as seen from the waveform.

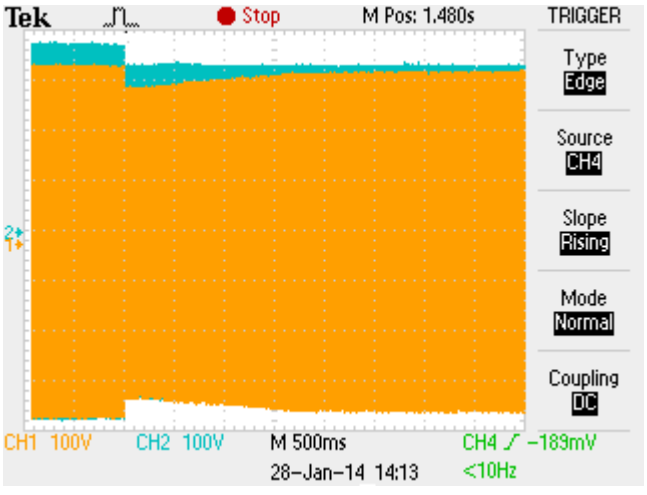


Figure 3.13: Delay observed at the output of the PS10 during the voltage dip test (blue and yellow colours indicate input and output waveforms respectively)

3.5.1.4 Delays seen at the output of PS10 voltage regulator for voltage swell test

The delay seen at the output of the PS10 Smart Power Station during the voltage dip test is shown in Figure 3.14. The delay was approximately 1.3s as seen from the waveform.

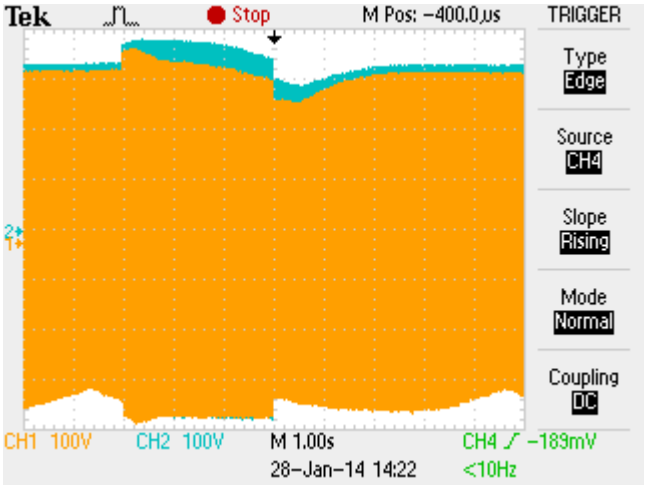


Figure 3.14: Delay observed at the output of PS10 during the voltage swell test (blue and yellow colours indicate input and output waveforms respectively)

3.6 Testing the regulation (load and line regulations) performance of PS10 smart power station

The output of the voltage regulator is a top-flattened sine wave at 240V. It has a digital display panel which indicates the input voltage to the PS10 and the output voltage from the PS10 (AVR). In addition to this display, it also contains a delay start button which can be set to either 180s or 6s delay. This is a very useful feature that helps prevent a sudden spike in current due to abrupt outage or over load.

The output voltage of the AVR can be set to either 220V or 240V via a button at the rear end of the regulator. However, for this test, the output voltage was set at 240V.

3.6.1 Load Regulation of PS10 Smart Power Station

The capability of an automatic voltage regulator to maintain a constant output voltage level as the load changes is determined by its load regulation. In this test, the input voltage was set at 245V and the load current was varied by increasing the load. The output voltage and load current were measured and recorded.

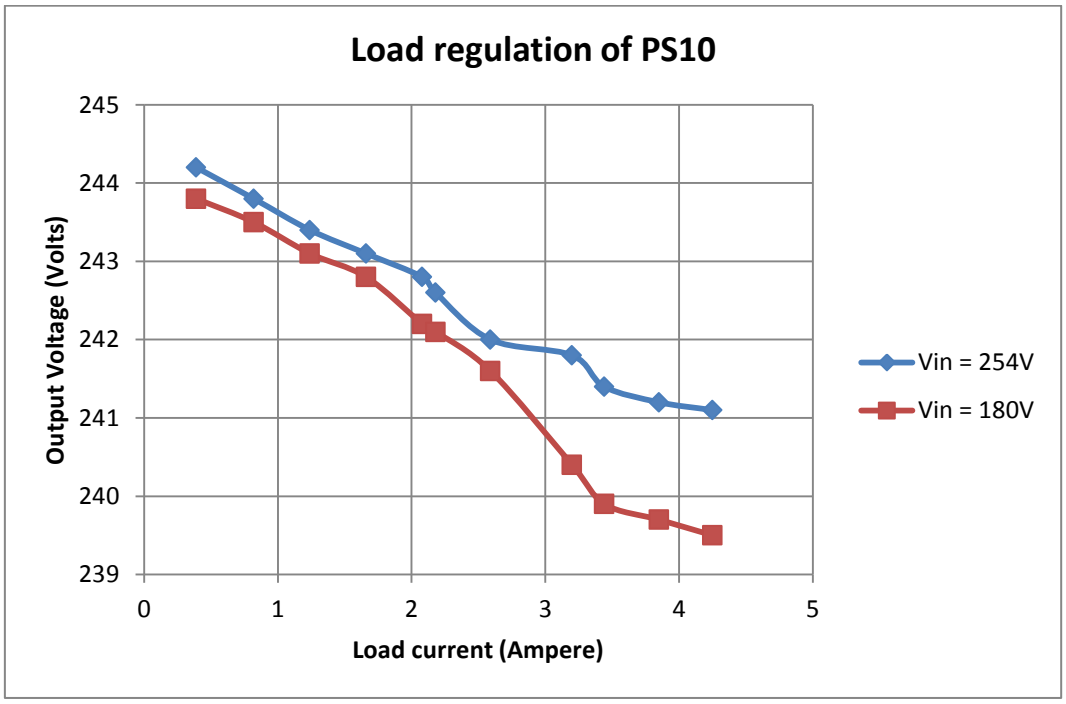


Figure 3.15: Load Regulation of the PS10 Smart Power Station

The same procedure was repeated for an input voltage of 180V. Figure 3.15 shows the load regulation at the two different voltages. The line regulation at input voltages of 180V and 254V was also measured and recorded.

3.6.2 Line Regulation of PS10 Smart Power Station

Line regulation can be explained as the capability of an automatic voltage regulator to maintain a constant output voltage irrespective of changes to the input voltage level. It is normally expressed as percentage change in output voltage with respect to the change in the input line voltage.

The line regulation of the AVR was achieved by setting the load current to 4.25A, the input voltage was varied and the output voltage was measured and recorded. The same procedure was repeated for a load current of 2.53A.

Figure 3.16 shows the graphs of line regulations at different load currents.

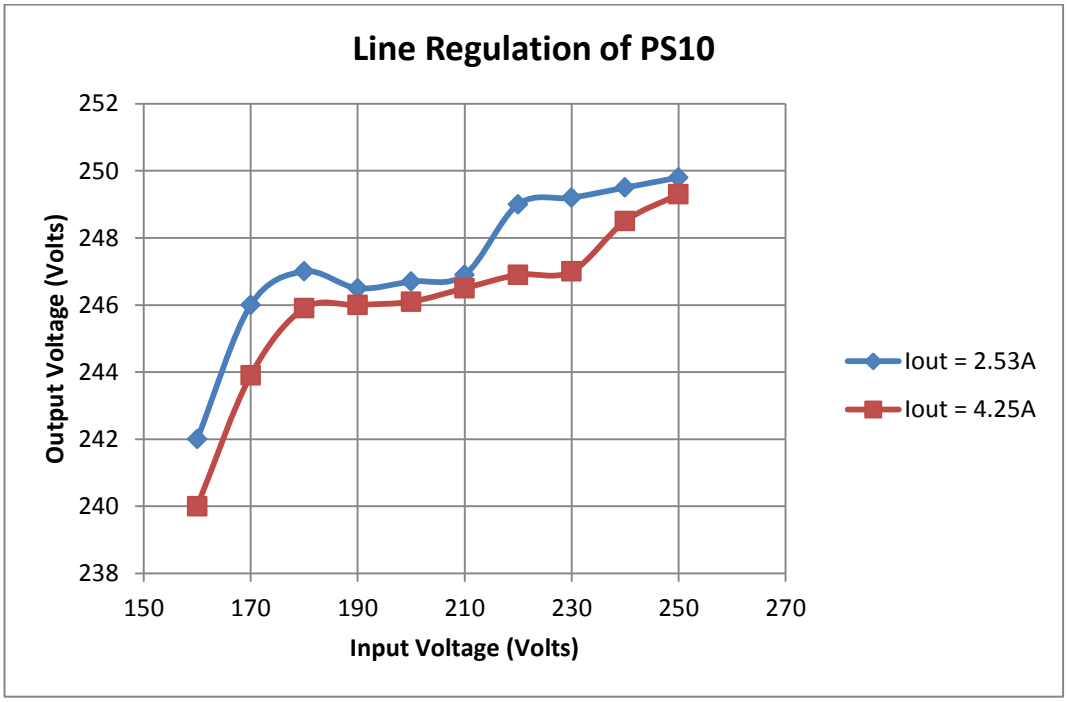


Figure 3.16: Line Regulation of the PS10 Smart Power Station

3.7 Input and output waveforms of PS10 Smart Power Station

The input voltage to the PS10 AC voltage regulator was varied from 160V to 260V. In this case, both the input and output waveforms of the regulator were captured on the oscilloscope. Figures 3.17 to 3.19 show the waveforms at various input voltages (160Vac to 260Vac).

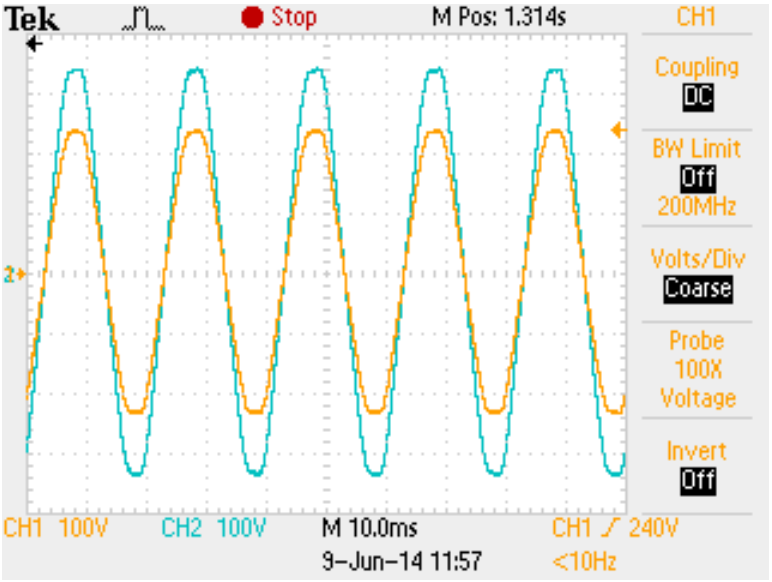


Figure 3.17: Waveforms of input and output at Vin = 160V and IL = 3.5A (CH1 indicates the input and CH2 indicates the output)

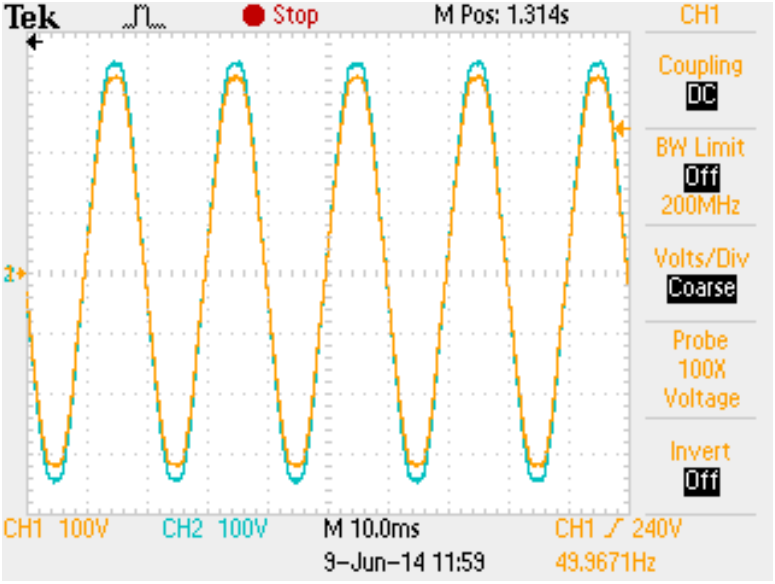


Figure 3.18: Waveforms of input and output at Vin = 230V and IL = 3.5A (CH1 indicates the input and CH2 indicates the output)

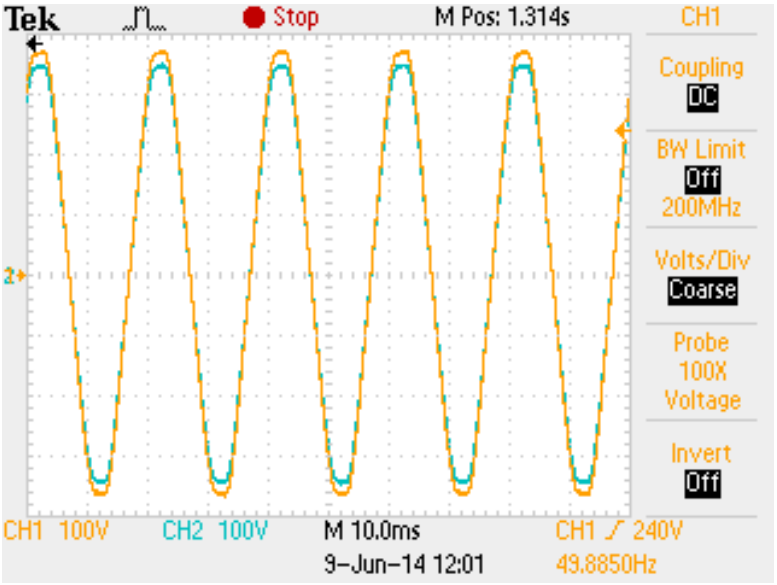


Figure 3.19: Waveforms of input and output at Vin = 260V and IL = 3.5A (CH1 indicates the input and CH2 indicates the output)

3.7.1 Interpretation of Performance Test Results

- When the Test level was set to 90% of the base voltage (212V), there was a delay of approximately 1.3s at the output of the AVR. The lamp load dropped to 212V and then stabilised again at 240V.
- The delay was slightly less at a test level of 80% and was recorded at approximately 1second.
- The delay did not seem to increase with the lamp load as this was tested when the load was increased from 100W to 1.5KW due to the available load.
- When the voltage was above 260V, the AVR automatically restarted itself.
- The average delay was about 1-2 seconds.

3.7.2 Conclusion on the PS10 Smart Power Station Test Results

Due to the delay in response to voltage fluctuation (change in supply voltage) by the PS10 Smart Power Station as shown by the test results above, it is necessary to replace the slow-response mechanical servomotor with semiconductor electronics (transistor array) which have the features of fast response, light weight and low cost, and which produce an AC voltage output that is not sensitive to frequency changes.

Chapter 4

4.1 Transistor array based AC Voltage Regulator Design

The power stage of the AC voltage regulator designed in this project consists of a full bridge rectifier, a buck/boost transformer and four sets of Darlington pair transistors connected in series to form the series transistor array. The transistor array was designed in such a way that it achieved a uniform power and voltage distribution across each transistor pair.

The main aim of the power stage is to achieve variable AC impedance which has a fast transient response by simply using bipolar junction transistors (BJTs) and to convert the sinusoidal line voltage at the input to a fully rectified output.

4.1.1 Line Voltage Rectification

Because of the manufacturers' design of bipolar junction transistors (BJTs), it is impossible for the transistors to handle negative voltage; hence, there was a need for rectification at the input stage. This was done by using a full bridge rectifier consisting of four rectifier diodes. The series transistor array was used as variable AC impedance across the bridge points of the rectifier while the other two points were directly connected to the input supply via a buck/boost transformer. Figure 4.1 below shows the full bridge rectifier with the series transistor array indicated as a variable resistor.

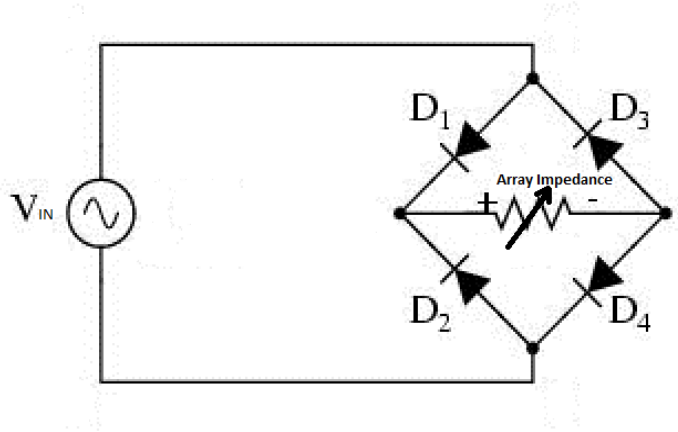


Figure 4.1: Full bridge rectifier with transistor array impedance at the bridge points

4.1.2 The Buck/Boost Transformer

This transformer allows step-up or step-down (boost or buck) operation. A primary winding with N turns is connected in series with the power semiconductor array which is placed across the bridge point of the full bridge rectifier. With such an arrangement of the transformer, for any load connected at the output terminals, the regulated output voltage can be derived as follows:

The voltage across the primary winding of the transformer is given by

$$V_p = V_{In} - I_p * R_{Array} \dots\dots\dots\dots\dots\dots\dots\dots (4.1)$$

where V_{in} and V_p are the input voltage and transformer primary voltage respectively. I_p and R_{Array} are the primary current and the array resistance respectively. Since the load current (I_L) is the same as the secondary current, then $I_p = NI_L$ where N is the transformer turns ratio. Equation 4.1 becomes;

$$V_p = V_{In} - NI_L * R_{Array} \dots\dots\dots\dots\dots\dots\dots\dots (4.2)$$

And $$NV_p = NV_{In} - N^2 I_L * R_{Array} \dots\dots\dots\dots\dots\dots (4.3)$$

The regulated output voltage in terms of the secondary voltage (V_s) is given by

$$V_{out} = V_{In} + V_s \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.4)$$

But $V_s = NV_p$ so equation 4.4 becomes

$$V_{out} = V_{In} + NV_p \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.5)$$

Substituting equation 4.3 into 4.5 yields

$$V_{Out} = V_{In}\,(1 + N) - R_{Array}N^2 I_L \ldots\ldots\ldots\ldots (4.6)$$

Where V_{Out} and V_{In} are the output and input voltages and I_L is the load current in their respective vector quantities.

4.1.2.1 Cases under consideration

The buck or boost operation of the transformer comes into play when the input voltage is above or below the regulated output voltage. In this section, both cases are considered and the limits of regulation are determined.

4.1.2.1.1 Input voltage less than the regulated output voltage ($V_{in} < V_{out}$) or boost mode

When the regulated output voltage is higher than the input voltage, with the load current lagging the supply voltage by an angle Φ, from the relationship in equation 4.6 with pure resistive impedance of the transistor array, the control circuits could regulate the output voltage by maintaining the regulated output voltage within the arc of the circle with a radius of V_{out} in the region where the tangential points of the worst case phase angle of the load falls within $\pm\Phi_{max}$.

Over these limits of the tangential points T and T' of the power diagram (Figure 4.2), regulation is not possible for a given transformer turns ratio N.

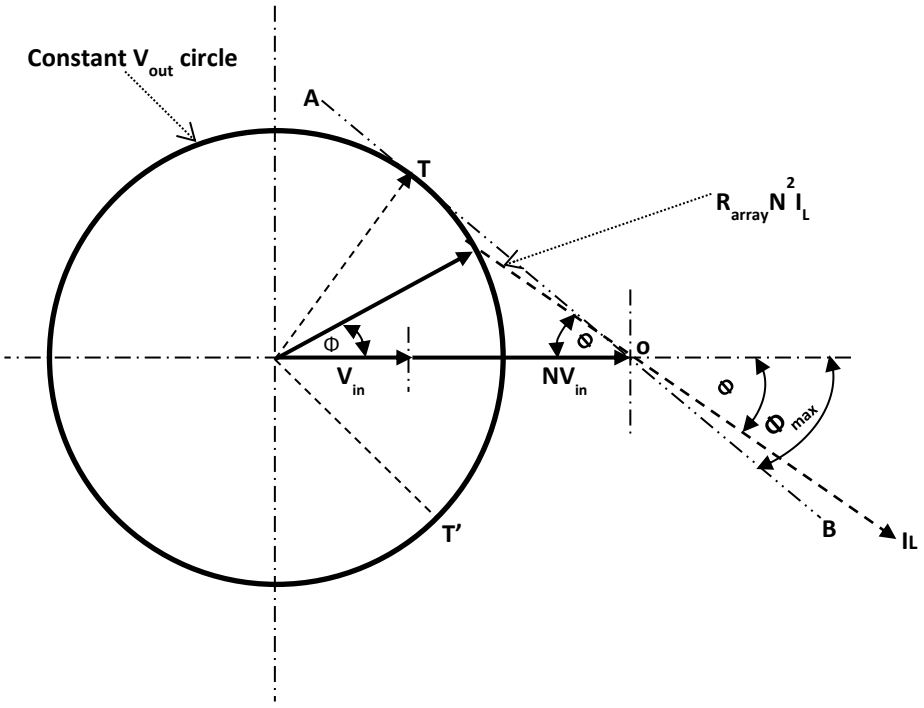


Figure 4.2: Phasor diagram with input less than regulated output (boost mode) [22]

Hence, when the input voltage is less than the regulated output voltage, the transformer operates in the step-up or boost mode.

4.1.2.1.2 Input voltage greater than regulated output voltage ($V_{in} > V_{out}$) or buck mode

In this case, the transformer operates in the buck mode since the input voltage is higher than the regulated output voltage. Here, a very high voltage is created across the transistor array and practically reversing the voltage across the primary winding of the transformer and voltage regulation is then achieved. In the case of pure resistive load, the regulated output voltage will be in phase with the input voltage.

In this situation,

$$V_{out} = V_{in} - V_s \ldots\ldots\ldots\ldots\ldots\ldots (4.7)$$

where V_{out}, V_{in} and V_s all have their usual meanings and

$$V_{Array} = V_{in} + NV_s \ldots\ldots\ldots\ldots\ldots\ldots (4.8)$$

Hence, the transformer operates in the buck mode.

The load power is given by

$$P_{load} = V_{out} * I_L \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.9)$$

The power across the transistor array is also given by

$$P_{Array} = V_{Array} * I_p \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.10)$$

Substituting equation 4.8 into 4.10 gives

$$P_{Array} = (V_{in} + NV_s) * I_p \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.11)$$

Since $I_p = NI_L$, and from equation 4.9 $I_L = P_{load}/V_{out}$, then equation 4.11 becomes

$$\frac{P_{Array}}{P_{load}} = \frac{V_{in} + NV_s}{V_{out}} * N \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.12)$$

Also, making V_s the subject of equation 4.7 and substituting in equation 4.12 yields

$$\frac{P_{Array}}{P_{load}} = \frac{V_{in}(1+N) - NV_{out}}{V_{out}} * N \ldots\ldots\ldots\ldots\ldots (4.13)$$

P_{Array} is maximum when V_{in} is maximum since V_{out} and N are constants. This implies that the system is in the buck mode.

For maximum power dissipation in the transistor array, the input voltage should be at maximum level. From equation 2.5, the maximum input voltage of the system is given by

$$V_{in} = V_{out}(1 + \frac{1}{1+N})$$

Therefore, $$\frac{V_{in}}{V_{out}} = \left(1 + \frac{1}{1+N}\right) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.14)$$

Substituting equation 4.14 into 4.13 gives

$$\frac{P_{Array}}{P_{Load}} = \left[\left(1 + \frac{1}{1+N}\right)(1+N) - N\right] * N \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.15)$$

From which,

$$P_{Array} \approx 2N * P_{Load} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.16)$$

Figure 4.3 shows the phasor diagram in the case where the transformer is operating in buck mode, that is, when the input voltage is higher than the regulated output voltage. The arc included within T and T' indicates the limits of the reactive components of the load to maintain the regulation.

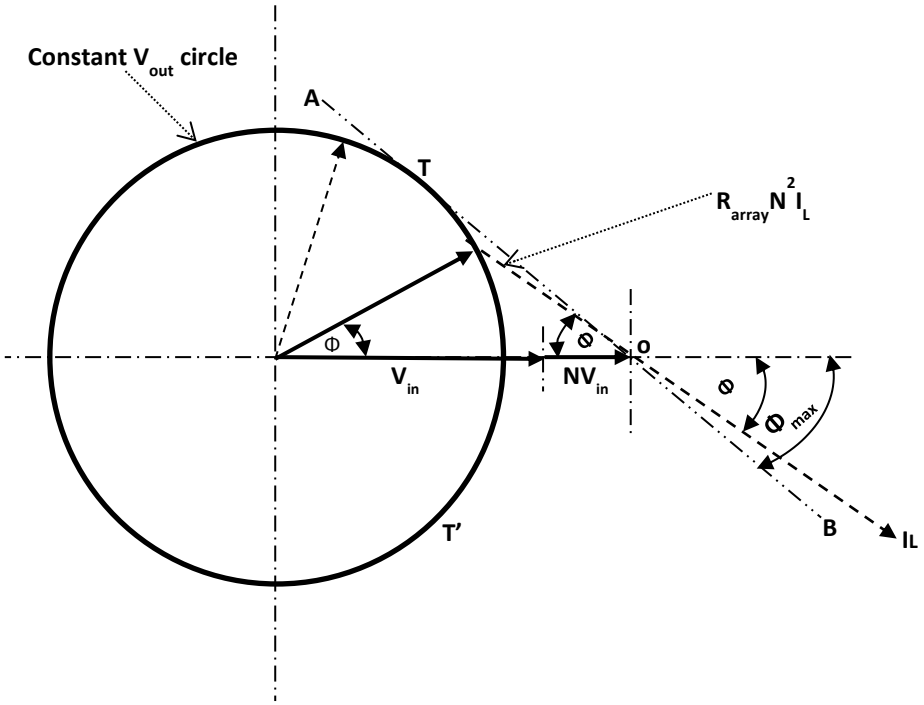


Figure 4.3: Phasor diagram with input greater than regulated output (buck mode) [22]

4.1.3 Series Transistor Array

The objective of this array is to act as variable impedance which can be varied across the bridge points of the full bridge rectifier. This can be achieved by changing the resistance across the collector-emitter junction of the bipolar junction transistors (BJTs). Figure 4.4 shows the transistor array as a single transistor across the bridge points of the rectifier.

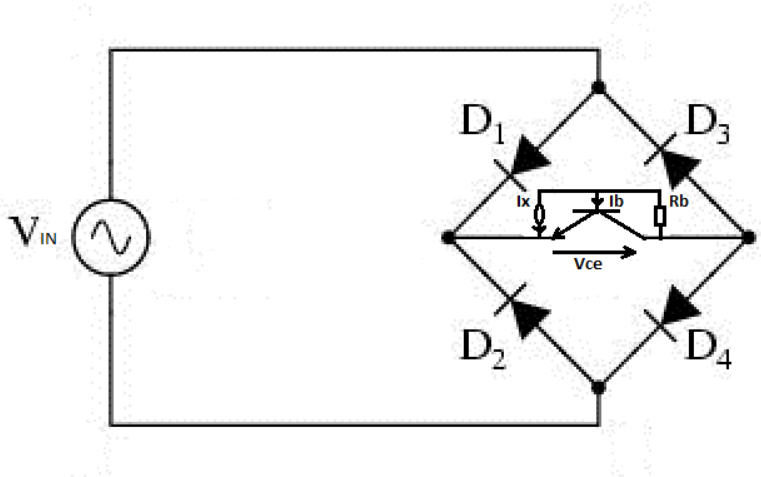


Figure 4.4: Full bridge rectifier with transistor array shown as single transistor

To control the impedance of the collector base junction, it is necessary to divert some of the base current using a constant current sink as shown in Figure 4.4. When the transistor is in the active mode, the instantaneous collector-emitter voltage is given by

$$V_{CE}(t) = V_{be} + R_B * I_b + R_B * I_x$$

$$V_{CE}(t) = V_{be} + R_B(I_b + I_x) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (4.17)$$

where:

$V(t)_{CE}$ = instantaneous collector-emitter voltage

I_b = instantaneous base current

V_{BE} = base-emitter voltage

I_X = amount of current sink

R_B = resistance between the collector and base

Also,

$$V_{CE}(t) = I_C * R_C \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.18)$$

and

$$I_C = \beta I_B \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.19)$$

Equating equations (4.17) to (4.18) and substituting equation (4.19) for I_c yields

$$R_{CE} = \left(\left(\frac{V_{BE}}{\beta I_b} \right) + \frac{R_B}{\beta} (1 + \frac{I_x}{I_b}) \right) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.20)$$

Equation 4.20 was manipulated to achieve the ratio $\frac{Ix}{Ib}$ which is called the base current diversion ratio (BCDR). It is clear from the equation that the collector-emitter resistance can be controlled by adjusting the BCDR ($\frac{Ix}{Ib}$) or the resistance between the collector and base, R_B. Also, from equation 4.20, if R_B is far greater than the base-collector resistance $\frac{Vbe}{\beta Ib}$, then one can ignore $\frac{Vbe}{\beta Ib}$ as its effect is not significant.

4.1.4 Basic Concepts Applied to Multiple Transistors (Series Array)

The concept detailed in section 4.1.3 can be applied to multiple transistors connected in series, known as the series transistor array. One of the most important considerations in the design of this array is the power and voltage sharing across the elements present in the array.

The configuration of an array containing m elements is shown in Figure 4.5 so as to achieve some significant wattage without compromising the equal voltage distribution and power dissipation among all the elements present in the array.

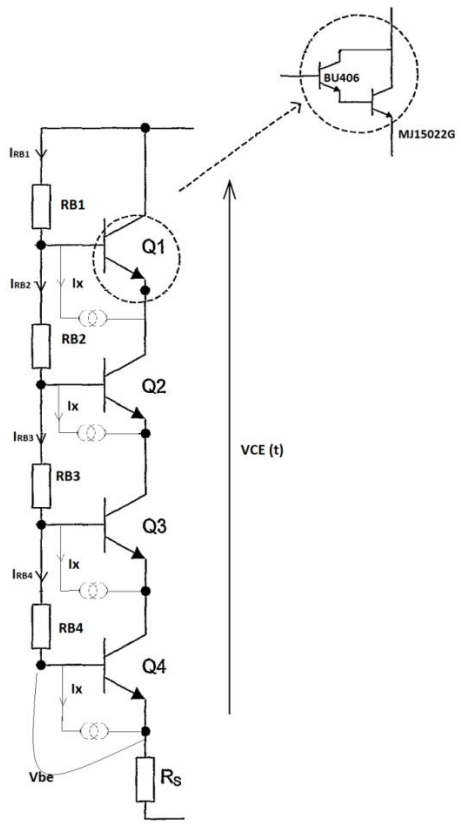


Figure 4.5: Series transistor array with four elements

Since all the transistors in the series array have approximately the same voltage, then the voltage across the nth transistor V_{CEn} is given by$\frac{Vce(t)}{n}$, where V_{CE} (t) is the instantaneous voltage across the array and n is the number of transistors present in the array.

For the power dissipation across the transistor array to be the same, the base currents of all the transistors must be approximately the same. Similarly, the collector currents of all the transistors must also be the same.

Therefore,

$$i_{b1} = i_{b2} = i_{b3} = \cdots = i_{bn} = i_b \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.21)$$

And $i_{c1} = i_{c2} = i_{c3} = \cdots = i_{cn} = i_c \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.22)$

For large and almost identical transistor gain, β for all the transistors, where each transistor carries approximately the same collector current I_C, then using the relationship between collector current I_C and base current I_B, $ic = \beta ib$, from equation (4.22), this implies;

$$i_{c1} = \beta i_{b1}, \quad i_{c2} = \beta i_{b2}, \quad i_{c3} = \beta i_{b3} \quad , \ldots , \quad i_{cn} = \beta i_{bn}$$

And

$$iRbn = i_b + i_x$$

$$iR_{B(n-1)} = 2(i_b + i_x)$$

$$iR_{B(n-2)} = 3(i_b + i_x)$$

$$\ldots\ldots$$

$$iR_{B3} = (n-2)(i_b + i_x)$$

$$iR_{B2} = (n-1)(i_b + i_x)$$

$$iR_{B1} = n(i_b + i_x) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.23)$$

Hence, the instantaneous voltage across the array V_{CE} (t) is given by

$$V_{CE}(t) = i_{RB1}R_{B1} + i_{RB2}R_{B2} + i_{RB3}R_{B3} + \cdots + i_{RBn}R_{Bn} + V_{BE} \ldots\ldots\ldots\ldots (4.24)$$

where R_{B1} to R_{BN} represent the resistors connected between the collector and base of each pair of transistors.

Substituting for i_{RB1} up to i_{RBn} from (4.23) into (4.24) yields

$$V_{ce}(t) - V_{BE} = R_{B1}(i_b + i_x)n + R_{B2}(i_b + i_x)(n-1) + R_{B3}(i_b + i_x)(n-2) + \cdots + R_{Bn}(i_b + i_x) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.25)$$

If $R_{B1} = \frac{R_B}{n}, R_{B2} = \frac{R_B}{n-1}, R_{B3} = \frac{R_B}{n-2}, \ldots R_{Bn} = R_B$

Equation (4.25) becomes

$$V_{ce}(t) - V_{BE} = nR_B(i_b + i_x)$$

$$V_{ce}(t) - V_{BE} = ni_bR_B\left(1 + \frac{i_x}{i_b}\right) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.26)$$

This implies that

$$\left(\frac{Vce(t)}{i_c}\right) = \frac{ni_bR_B}{i_c}\left(1 + \frac{i_x}{i_b}\right) + \frac{V_{be}}{i_c} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.27)$$

Since $i_c = \beta i_b$, and $Vce(t) = R_{ce} * i_c$, then equation (4.27) becomes

$$R_{ce} = \frac{nR_b}{\beta}\left(1 + \frac{i_x}{i_b}\right) + \frac{V_{be}}{\beta i_b} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.28)$$

If the base-emitter voltage, $V_{BE,}$ is small compared to the instantaneous voltage across the transistor array, then equation 4.28 becomes

$$R_{ce} \approx \frac{nR_b}{\beta}\left(1 + \frac{i_x}{i_b}\right) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.29)$$

In this case, when the base current diversion ratio (BCDR) is high, the transistor array reaches its maximum effective resistance, R_{CEmax}, which is given by the expanded series in equation 4.30.

$$R_{cemax} = R_B + \frac{R_B}{2} + \frac{R_B}{3} + \frac{R_B}{4} + \cdots + \frac{R_B}{n} \ldots\ldots\ldots (4.30)$$

However, in the case of low or minimum BCDR, the effective resistance of the transistor array is minimum, R_{CEmin}, and can be reduced to equation 4.31 by letting $(Ix = 0)$ in equation 4.29.

$$R_{ce,min} = \frac{nR_B}{\beta} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.31)$$

Hence, the limit of the effective resistance of the series transistor array can range from R_{CEmin} up to R_{ECmax} and can be controlled by varying the current through the diode of the opto-isolator.

Since the series transistor array used in this project was a four-element transistor array, that is n = 4, then the effective resistance of the array can range from

$$R_{ce,min} = \frac{4R_B}{\beta} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.32)$$

To

$$R_{ce,max} = 2.1R_B \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.33)$$

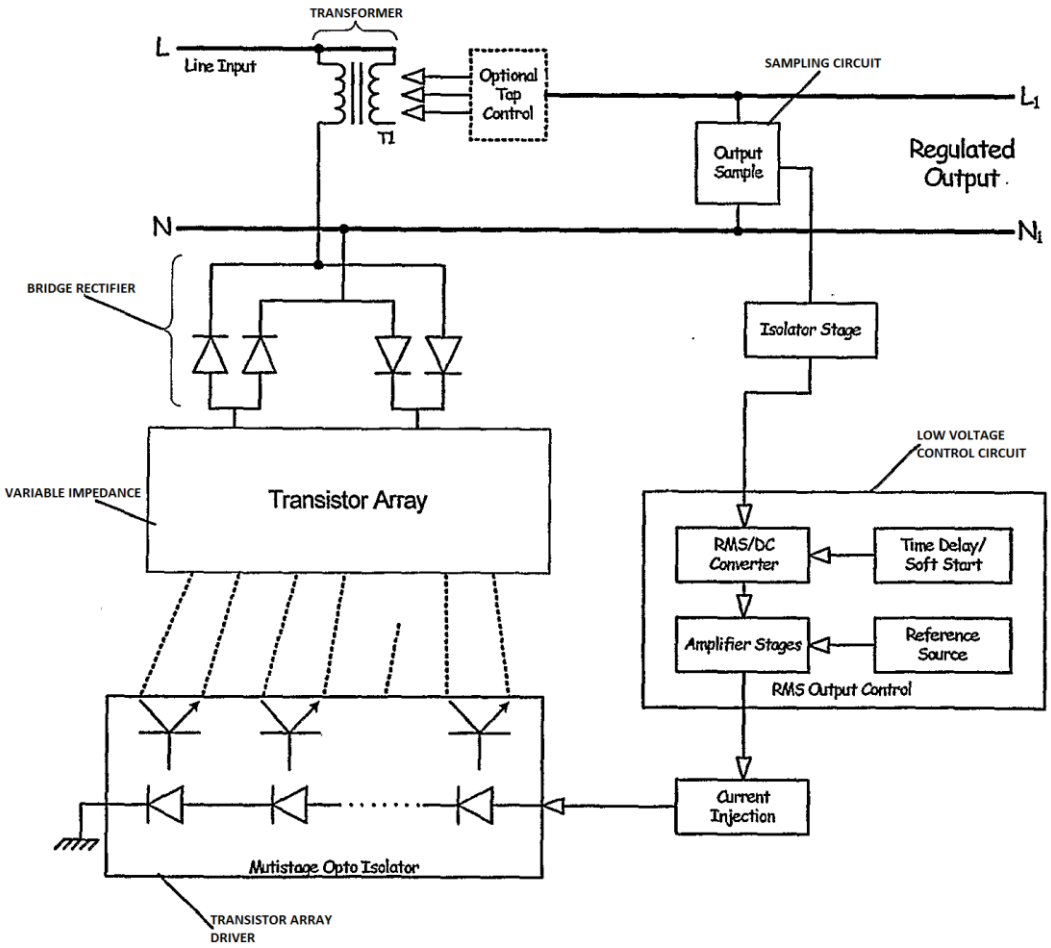


Figure 4.6: Detailed block diagram of the voltage regulator based on series transistor array

Figure 4.6 indicates the block diagram implementation of the AC voltage regulator based on a series transistor array which was developed to address the various problems associated with ferroresonant regulators and motor-driven variacs such as slow response to RMS voltage fluctuation, waveform distortion etc. [3].

For RMS output voltage control, the effective resistance of the array varies depending on the load and the input voltage. An RMS control circuit compares the actual AC output sample, converted to a DC value using an RMS-DC converter IC, with a reference DC voltage. A current injection circuit adjusts the current

injected into the series connected input diodes of the opto isolator, based on the output of the RMS control circuits. This effectively controls the value of R_{array} in such a way that the loop keeps the output RMS value regulated at a pre-set value such as 230 V, for a wide range of input voltages [22].

4.1.5 The heat sink capacity calculation

The main function of the heat sink is to transfer heat from the transistor as a means of keeping the junction temperature of the main power transistor within the specified limits. The specified heat sink for a given power transistor can be chosen based on the junction temperature specified in the manufacturer's data sheet. One of the most important parameters that determines the type of heat sink for a given power transistor is the thermal resistance between the heat sink and the ambient, $R_{\theta SA}$.

Other worst case design parameters that can be found in the manufacturer's data sheet are:

- Maximum junction temperature $T_{j,max}$
- Maximum ambient temperature $T_{a,max}$
- Maximum operating voltage $V_{CE,peak}$
- Maximum on state current $I_{C,peak}$

From the above parameters, if the base-emitter heat generation of the transistor is neglected, then the maximum power loss can be calculated from the following equation

$$Maximum\ power\ loss = V_{ce,peak} * \frac{I_{ce,peak}}{2} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.34)$$

The junction to ambient resistance, $R_{\theta ja}$ can be obtained from

$$R_{\theta ja} = \frac{T_{j,max} - T_{a,max}}{P_{Loss}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.35)$$

The junction to case thermal resistance, $R_{\theta jc}$, can also be obtained from the manufacturer's data sheet.

Given all these parameters, the thermal resistance of the heat sink to ambient, $R_{\theta sa}$, can be determined as follows

$$R_{\theta ja} = R_{\theta jc} + R_{\theta cs} + R_{\theta sa}$$

From which

$$R_{\theta sa} = R_{\theta ja} - R_{\theta jc} - R_{\theta cs} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.36)$$

4.1.5.1 The MJ15022 Power Transistor

The transistors used in this project were MJ15022 power transistors and the following parameters can were extracted from the manufacturer's data sheet:

$R_{\theta jc}$ = 0.70℃/W

$T_{j,\,max}$ = 200℃

$T_{a,\,max}$ = 25℃

Maximum power dissipation P_D = 150W

Therefore, $R_{\theta ja} = \frac{200-25}{150} = 1.166\ °C/W$

$R_{\theta sa} = 1.166 - (0.70 + 0.40) = 0.066\ ℃/W$

With this thermal resistance, the heat sink that can contain all the four power transistors in the array must have $R_{\theta sa}$ = 0.267℃/W. Since this heat sink is fairly large and expensive, each transistor can be mounted on an individual heat sink.

Based on the specifications of the drive transistors (BU406), the amount of heat dissipated is small enough that they can be used without mounting them on a heat sink.

4.2 Complete Power Stage Design of the AC Voltage Regulator

Figure 4.7 shows the complete power stage of the AC Voltage Regulator with all components as described in the previous sections.

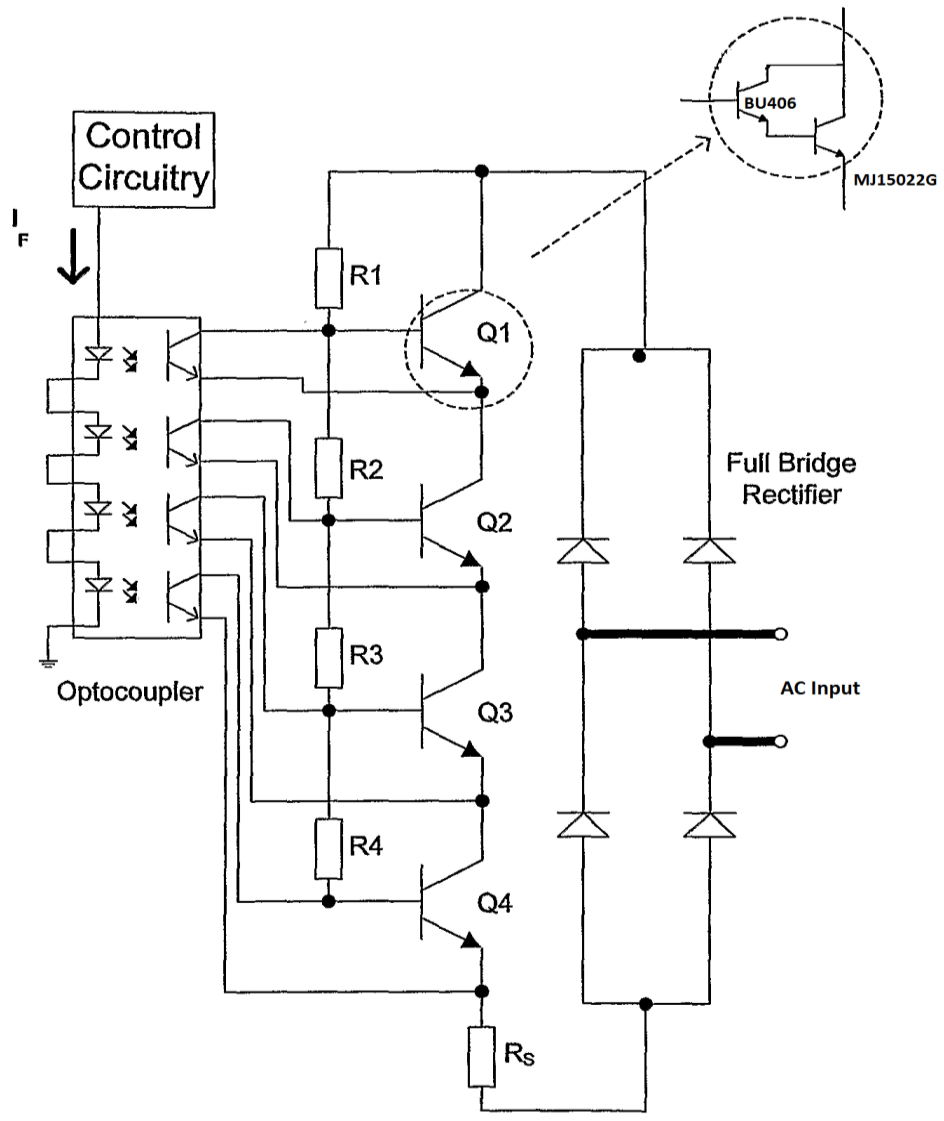


Figure 4.7: Complete power stage design of an AC voltage regulator based on transistor array

4.3 The Control Circuit

The low voltage control circuit samples the voltage across the output through an RMS/DC converter chip. This AC sample from the output is derived from the potential divider stage. The AC sample is then fed into the RMS/DC converter input. The resulting DC output from the RMS/DC converter is then applied to an Op Amp which compares the output sample with the DC voltage from the reference source. The final output of the Op Amp is used to drive the Quad opto-isolator stage, which in turn controls the base currents across the series transistor array.

4.3.1 Sampling circuit with isolation

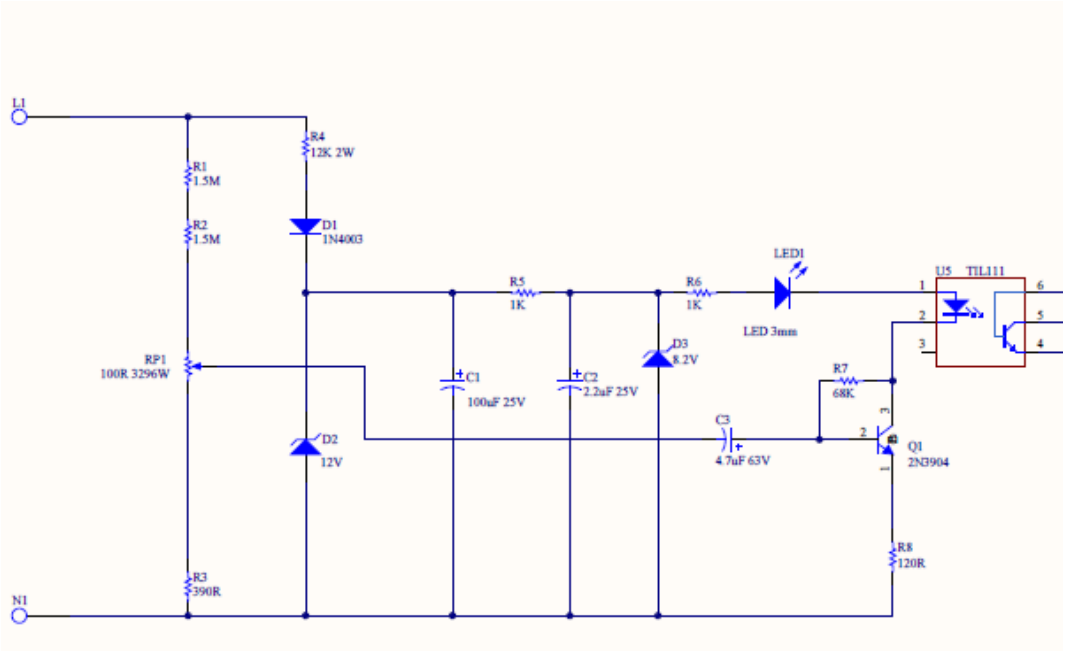


Figure 4.8: Sampling circuit with isolation

The AC sample from the output is derived from the potential divider stage and fed into the 2N3904 transistor (Q1 in Figure 4.8), where the collector is connected in series with the input of the opto-isolator, TIL 111 (U5, Figure 4.8). This configuration allows the isolation of the AC power block from the low voltage control circuits.

4.3.1.1 Isolation characteristics of the opto-isolator, TIL111

The TIL111 is a phototransistor-type optically coupled isolator. An infrared emitting diode is selectively coupled with an NPN silicon phototransistor. The minimum input to output isolation voltage of the TIL111 is $7500V_{AC\ (pk)}$. The isolation resistance is $10^{11}\Omega$ and the isolation capacitance is 0.2pF. All the above ratings are typical for a room temperature of 25℃.

4.3.2 RMS-DC converter

RMS or Root Mean Square is the fundamental measurement of the magnitude of an AC signal. Its definition can be both practical and mathematical. Defined practically, the RMS value assigned to an AC signal is the amount of DC required to produce an equivalent amount of heat at the same load. Mathematically, the RMS value of a voltage is defined as

$$E_{rms} = \sqrt{AVG.(V^2)} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.37)$$

The above formula is equivalent to the standard deviation of the zero average statistical signals. This involves squaring the signal, taking the average and obtaining the square root [27].

An ideal RMS-DC converter would provide a DC output voltage exactly equal to the RMS value of its input voltage, regardless of the amplitude, frequency, or wave shape of the input waveform.

The RMS-DC converter chip used in this project was the AD536AJ. The AD536AJ uses an implicit method of RMS computation employing an absolute value V/I converter, a square/divider, low pass filter, precision current mirror and an output buffer as shown in Figure 4.9 [27].

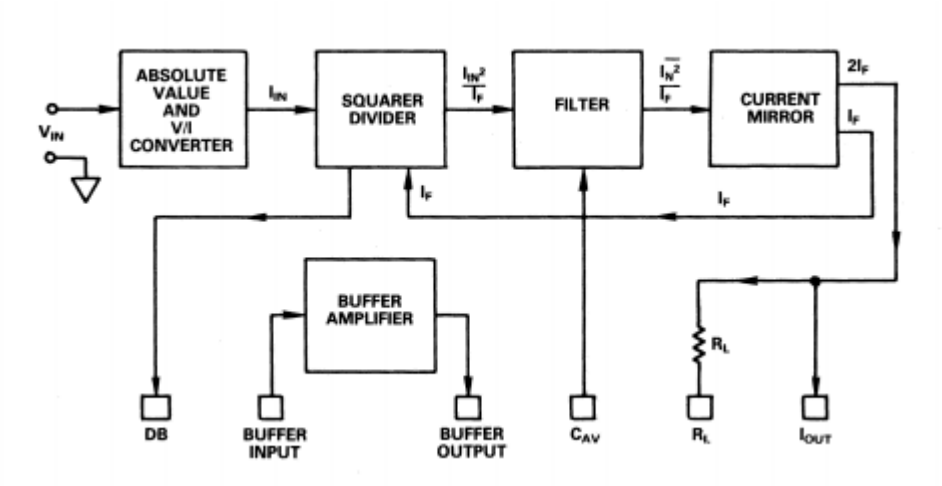


Figure 4.9: Block diagram of the AD536AJ RMS-DC converter [27]

The voltage input to the AD356AJ is first processed by an absolute value circuit (a precision rectifier) which has a single polarity output. This output drives the voltage to current converter (an operational amplifier) whose current output, I_N, is the rectified input signal [27].

The AD356AJ is configured to have an average timing of about 1.25 cycles (50Hz) by using an averaging capacitor of 1µF. Figure 4.10 shows the pin configuration of the AD536AJ RMS-DC converter chip.

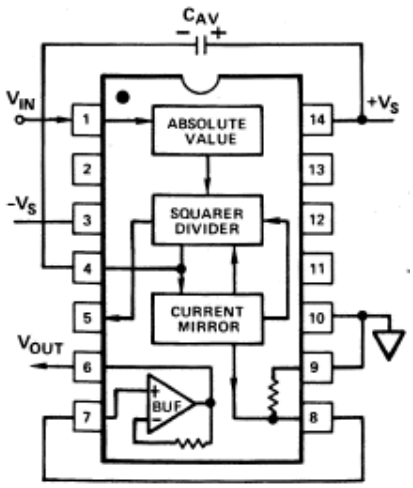


Figure 4.10: standard pin connections for the RMS-DC converter

4.3.3 The monostable stage

During start-up, the monostable stage, shown in Figure 4.11, an MC14538 chip (U3) is used to drive the transistor Q2 (2N3904) off for approximately two seconds until the transient stages have passed. As this transistor is connected in series with the internal chip resistor, this will effectively create a high DC voltage at the output of the RMS/DC Converter stage. This prevents overshooting the AC output voltage at start-up.

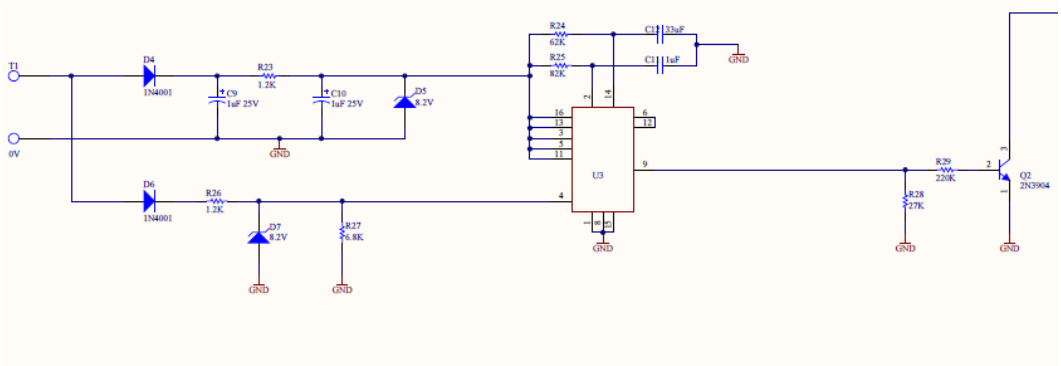


Figure 4.11: The monostable stage circuit

Figure 4.12 shows the behaviour of the opto-isolator (TLI111) and the RMS/DC converter (AD536AJ) as the output voltage changes due to change in the supply voltage. During the test, it was observed that there was a linear increase in the outputs of both the opto-isolator and the RMS/DC converter as the output voltage increased and this is shown in Figure 4.12.

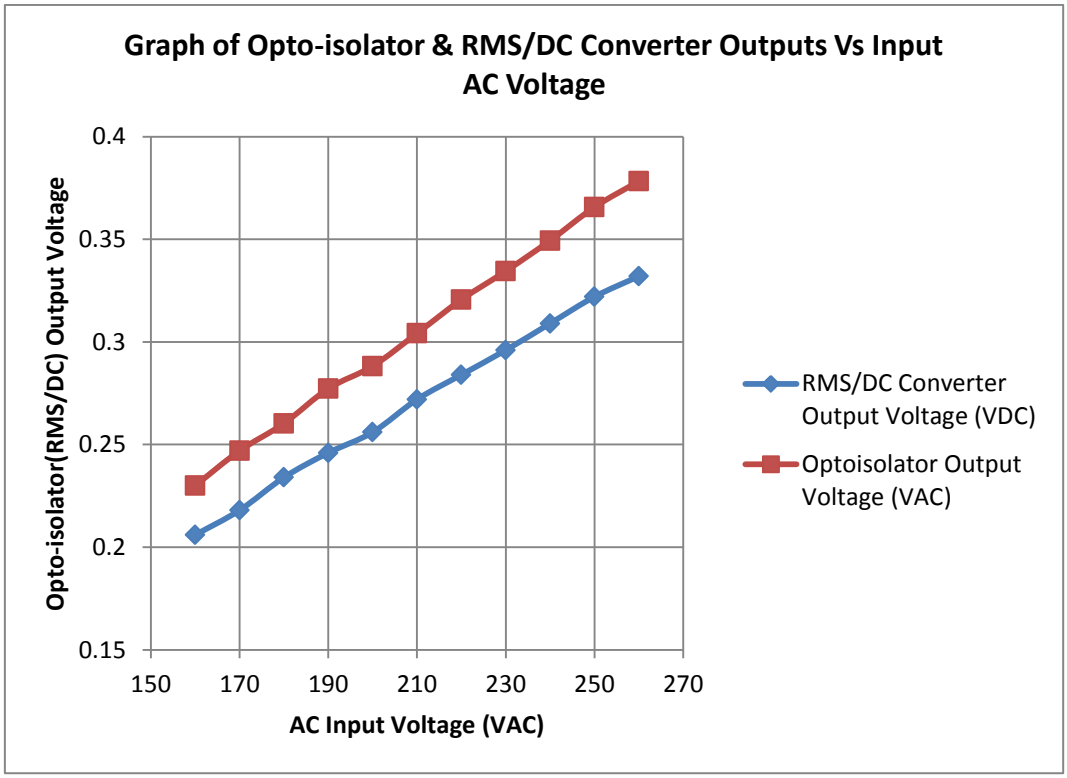


Figure 4.12: Graph of opto-isolator & RMS/DC converter outputs vs AC input voltage

The snapshots in Figures 4.13 to 4.15 show the input and output waveforms of the opto-isolator at various input voltages within the range of 160VAC to 260VAC. Note that the input and output waveforms of the opto-isolator are shown in blue and yellow respectively.

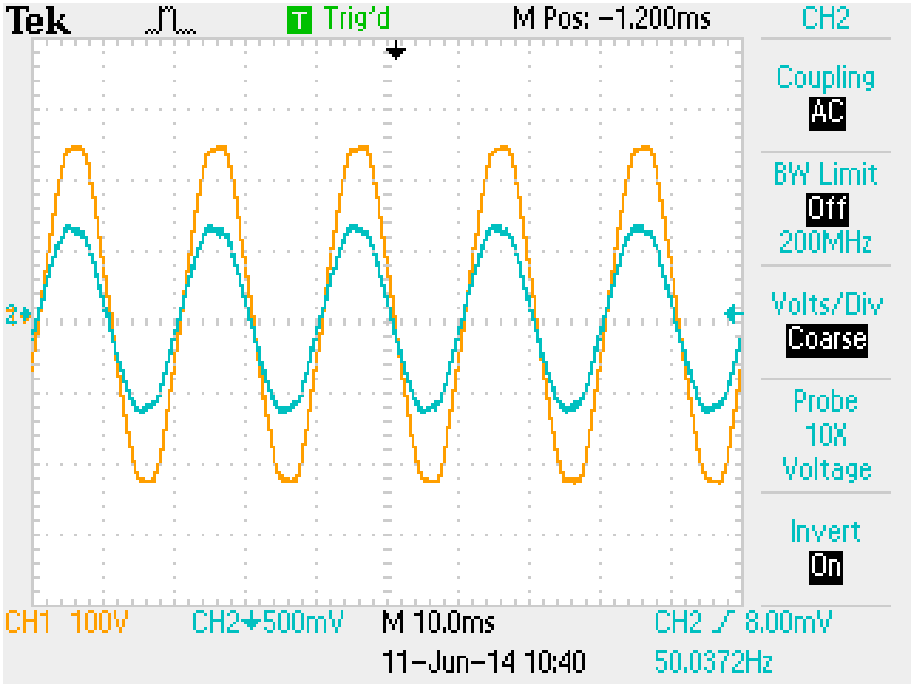


Figure 4.13: Opto-isolator Input and Output waveforms at an input voltage of 160VAC

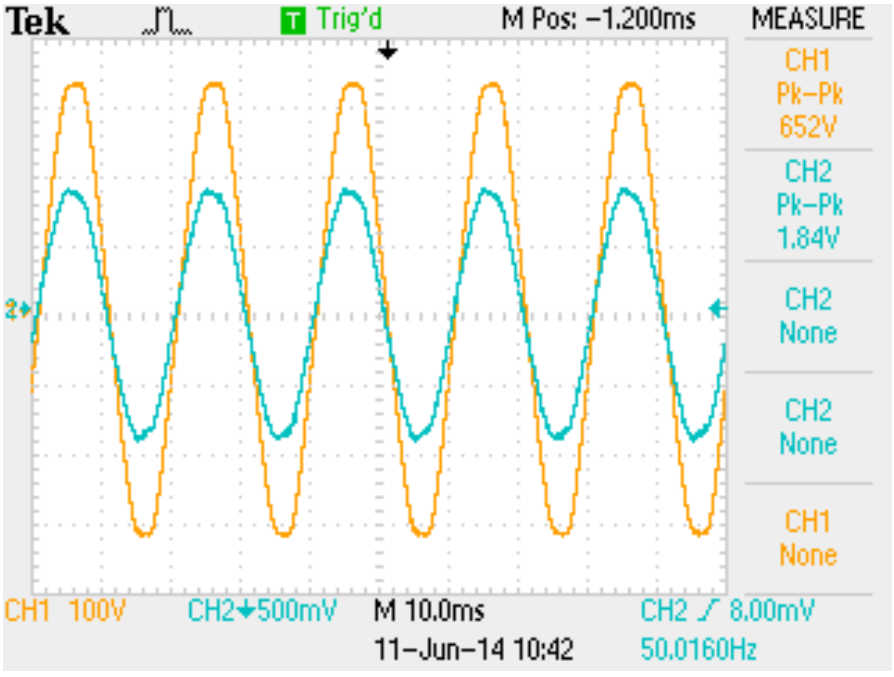


Figure 4.14: Opto-isolator Input and Output waveforms at an input voltage of 230VAC

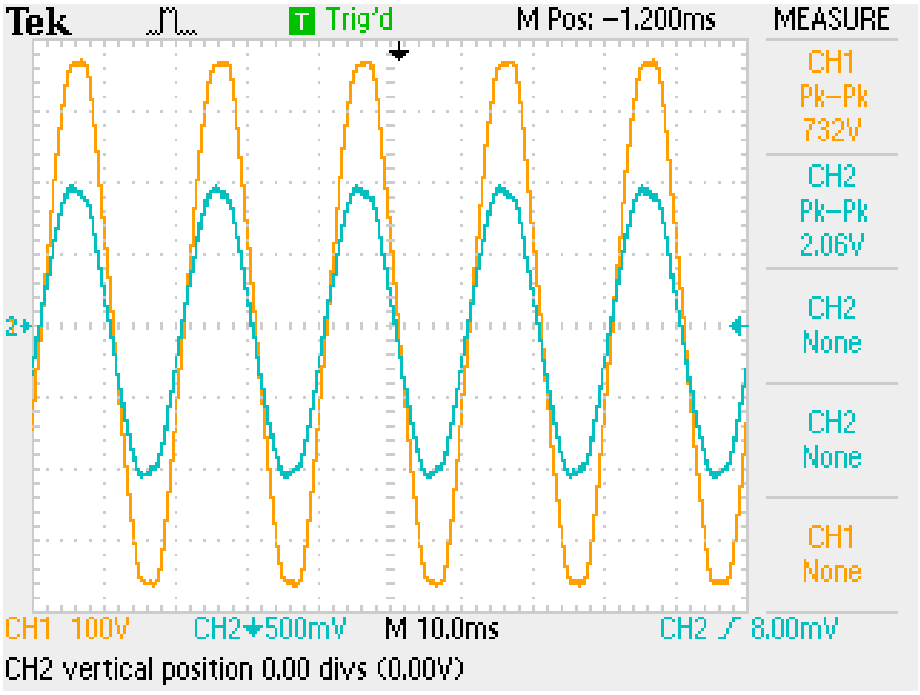


Figure 4.15: Opto-isolator Input and Output waveforms at an input voltage of 260VAC

The control circuit output voltage is applied across the quad-opto-isolator in which the four LEDs of this opto-isolator are connected in series with the aim of diverting equal amounts of current from the bases of the drive transistors in the Darlington pairs and hence keeping a fairly constant base current diversion ratio. It can be seen that as the sampling AC voltage at the input of the control circuit increases, there is a corresponding increase in the voltage supplied to the quad-opto-isolator over a closed range as shown in Figure 4.16.

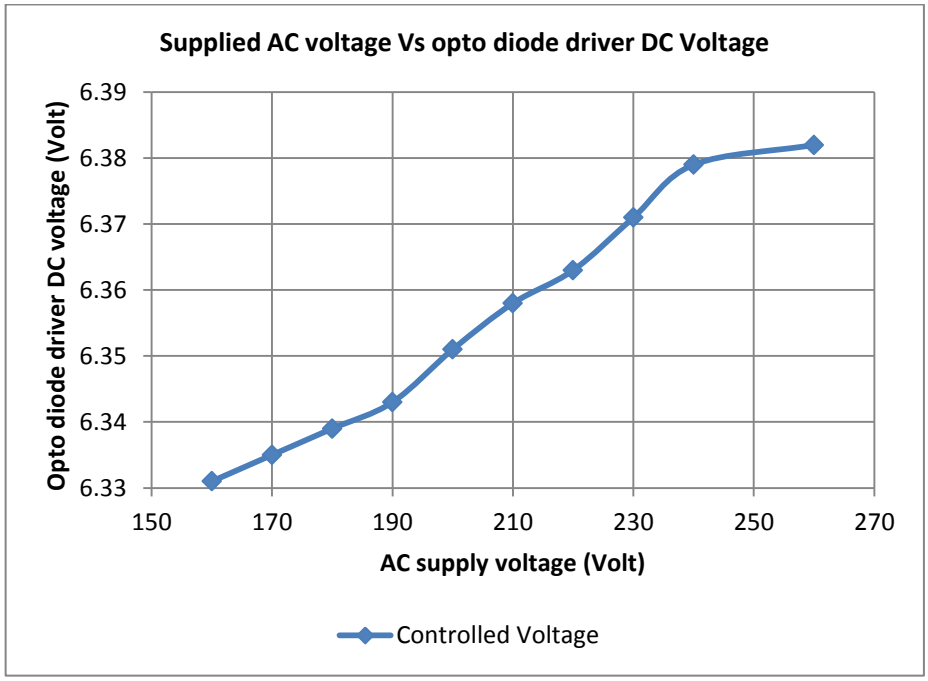


Figure 4.16: Variable Supplied Voltage plotted against the Opto diode driver DC voltage

Chapter 5

5.1 Implementation of the power stage circuit

The implementation of the power stage and the control circuit involved selecting the appropriate circuit components via theoretical calculations to meet the design specifications detailed in the previous chapter. The main components used during the power stage implementation are as follows:

- Bridge rectifier
- Power and base drive transistors
- Buck/Boost transformer
- Opto-isolator

5.2 Bridge Rectifier

The bridge rectifier used in this project was a GBPC2506 (Fairchild Semiconductor, San Jose, CA). This is a single phase bridge rectifier with a Peak Reverse Voltage of 600V and a Maximum RMS Reverse Voltage of 420V. The Forward Continuous Current rating is 25A and there is a 1.1V Forward Voltage Drop. Table 5.1 shows its absolute maximum ratings as extracted from the data sheet.

Table 5.1: Bridge Rectifier specifications sheet "Fairchild Semiconductor"

Absolute Maximum Ratings(1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter		Value							Units
			005	01	02	04	06	08	10	
V_{RRM}	Maximum Repetitive Reverse Voltage		50	100	200	400	600	800	1000	V
V_{RMS}	Maximum RMS Bridge Input Voltage		35	70	140	280	420	560	700	V
V_R	DC Reverse Voltage (Rated V_R)		50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current at T_C = 55°C	GBPC12	12							A
		GBPC15	15							
		GBPC25	25							
		GBPC35	35							
I_{FSM}	Non-Repetitive Peak Forward Surge Current	GBPC12, 15, 25	300							A
	8.3ms Single Half-Sine-Wave	GBPC35	400							A
T_{STG}	Storage Temperature Range		-55 to +150							°C
T_J	Operating Junction Temperature		-55 to +150							°C

Note:

1. These ratings are limiting values above which the serviceability of any semiconductor device may by impaired.

5.3 The Darlington pair

In order to achieve the high current specification of the AC voltage regulator, the transistors used in this project were connected in such a way to form a high current-capable Darlington pair. After taking into consideration the basic requirements of the transistors for choosing the correct Darlington pair, MJ15022 transistors were used as the power transistors whilst BU406 transistors were used as the base drive transistors.

5.3.1 High power MJ15022 transistor

MJ15022 power transistors are manufactured by ON Semiconductor (Phoenix, AZ). They are designed for high power and other linear applications. The basic features of the device are listed as follows:

• High Safe Operating Area

• High DC Current Gain

• These Devices are Pb−Free and are RoHS Compliant

Table 5.2 is an extract from the manufacturer's specification sheet for the MJ15022 power transistor with its maximum ratings.

Table 5.2: Specification sheet for the MJ15022 power transistor

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage MJ15022 MJ15024	V_{CEO}	 200 250	Vdc
Collector−Base Voltage MJ15022 MJ15024	V_{CBO}	 350 400	Vdc
Emitter−Base Voltage	V_{EBO}	5	Vdc
Collector−Emitter Voltage	V_{CEX}	400	Vdc
Collector Current – Continuous	I_C	16	Adc
Collector Current – Peak (Note 1)	I_{CM}	30	Adc
Base Current – Continuous	I_B	5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

Figure 5.1 is a graphical representation of how the DC current gain, h_{HF} of the MJ15022 transistor varies vary with respect to the collector current over a range of given voltages.

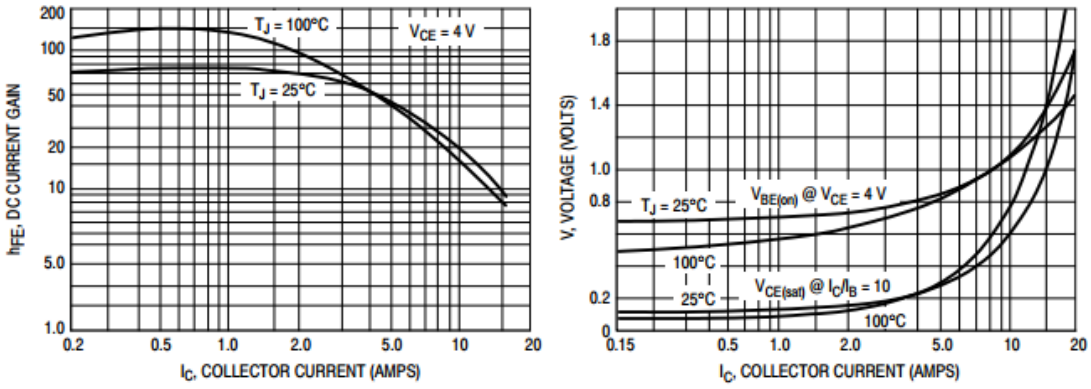


Figure 5.1: Variation of the transistor gain with respect to the collector voltage

5.3.2 Base drive BU406 transistor

BU406 transistors were used to drive the bases of the MJ15022 power transistors in the Darlington pairs. These transistors are also manufactured by ON Semiconductor and have high voltage and high speed in addition to fast switching speed and low saturation voltage. Manufacturer's specifications are provided in Table 5.3.

Table 5.3: Specifications of the base drive BU406 transistor

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector–Emitter Voltage	BU406 BU407	V_{CEO}	200 150	Vdc
Collector–Emitter Voltage	BU406 BU407	V_{CEV}	400 330	Vdc
Collector–Base Voltage	BU406 BU407	V_{CBO}	400 330	Vdc
Emitter–Base Voltage		V_{EBO}	6	Vdc
Collector Current – Continuous – Peak Repetitive		I_C	7 10	Adc
Collector Current – Peak (10 ms)		I_{CM}	15	Adc
Base Current		I_B	4	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	60 0.48	W W/°C
Operating and Storage Junction Temperature Storage		T_J, T_{stg}	–65 to 150	°C

5.4 Quad-Opto-isolator

The opto-isolator used in this project was the TLP504A-2 (Toshiba, Tokyo, Japan) which consists of a photo-transistor optically coupled to a gallium arsenide infrared emitting diode. The TLP504A-2 provides four isolated channels in a sixteen pin plastic DIP package. It has the following features:

• Collector−emitter voltage: 55 V (min.)

• Current transfer ratio: 50% (min.), Rank GB: 100% (min.)

• Isolation voltage: 2500 Vrms (min.).

The TOSHIBA TLP504A-2 opto-isolator was selected in order to get four channels in one package to divert some of the base current of the four BU406

transistors used. An extract from the manufacturer's data sheet at absolute maximum ratings is shown in table 5.4.

Table 5.4: Absolute maximum ratings of the TLP504A-2 opto-isolator

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating		Unit
			TLP504A	TLP504A–2	
LED	Forward current	I_F	60	50	mA
	Forward current derating	ΔI_F / °C	–0.7 (Ta ≥ 39°C)	–0.5 (Ta ≥ 25°C)	mA /°C
	Pulse forward current	I_{FP}	1 (100μs pulse, 100pps)		A
	Reverse voltage	V_R	5		V
	Junction temperature	T_j	125		°C
Detector	Collector–emitter voltage	V_{CEO}	55		V
	Emitter–collector voltage	V_{ECO}	7		V
	Collector current	I_C	50		mA
	Collector power dissipation (1 circuit)	P_C	150	100	mW
	Collector power dissipation derating (1 circuit Ta ≥ 25°C)	ΔP_C / °C	–1.5	–1.0	mW /°C
	Junction temperature	T_j	125		°C
Storage temperature range		T_{stg}	–55~150		°C
Operating temperature range		T_{opr}	–55~100		°C
Lead soldering temperature		T_{sol}	260 (10 s)		°C
Total package power dissipation		R_T	250	150	mW
Total package power dissipation derating (Ta ≥ 25°C)		ΔP_T / °C	–2.5	–1.5	mW / °C
Isolation voltage		BV_S	2500 (AC, 1min., R.H.≤ 60%) (Note 1)		Vrms

The isolation voltage of the TLP504A-2 is 2500Vrms with an isolation resistance of $10^{14}\Omega$. The input to output capacitance is 0.8pF, all measured at a standard room temperature of 25℃.

5.5 Testing the transistor array of the power stage

The power stage of the design, which consisted of the series transistor array, bridge rectifier, buck/boost transformer and the quad-opto-isolator was tested at various AC supply voltages of 180V, 230V and 260V. The behaviour of the transistor array was then observed with respect to change in the control current via the opto-isolator.

In this test, the opto-isolator was supplied with current from a regulated power supplied through a DC active load of maximum rating 50W, 30V. The control current through the opto-isolator was varied by changing the resistance of the active load. While the control current was varied, the voltage, V_{CE} across the array and the current I_C through the collector of the transistor array were measured and recorded, from which the resistance, R_{CE} of the transistor was determined.

The array resistance, R_{CE} was then plotted against the control current, I_F as shown in Figure 5.2.

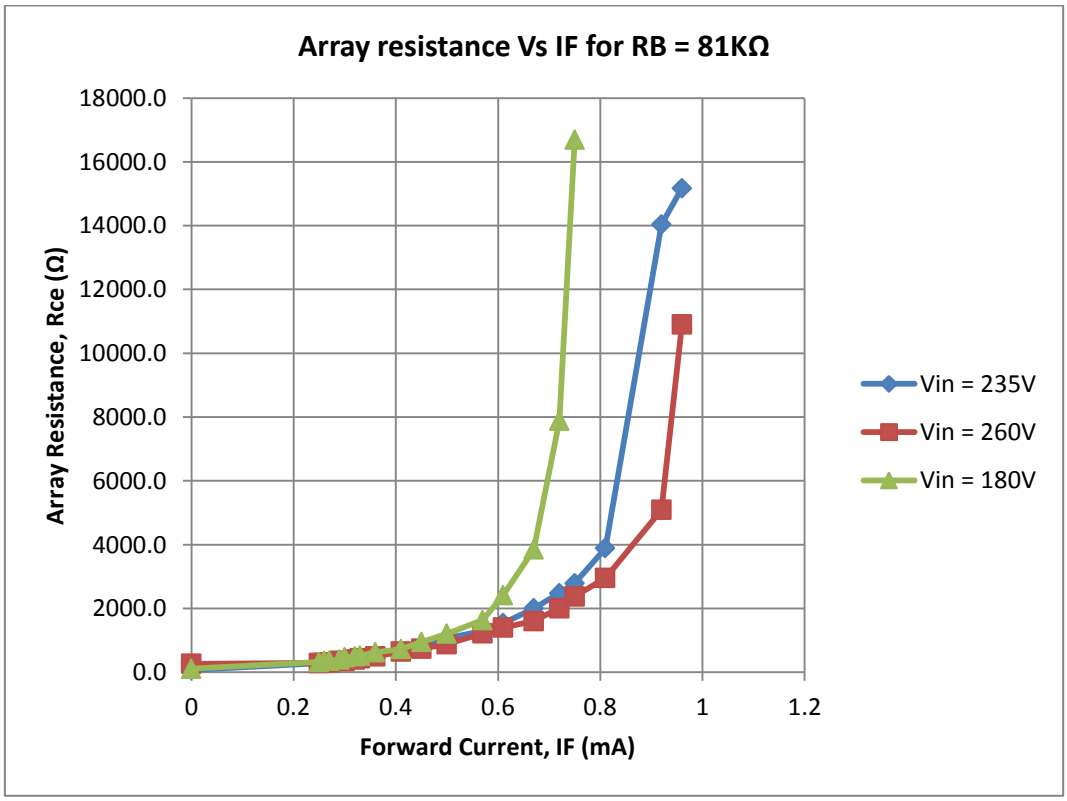


Figure 5.2: Array resistance Vs control current with RB = 81KΩ

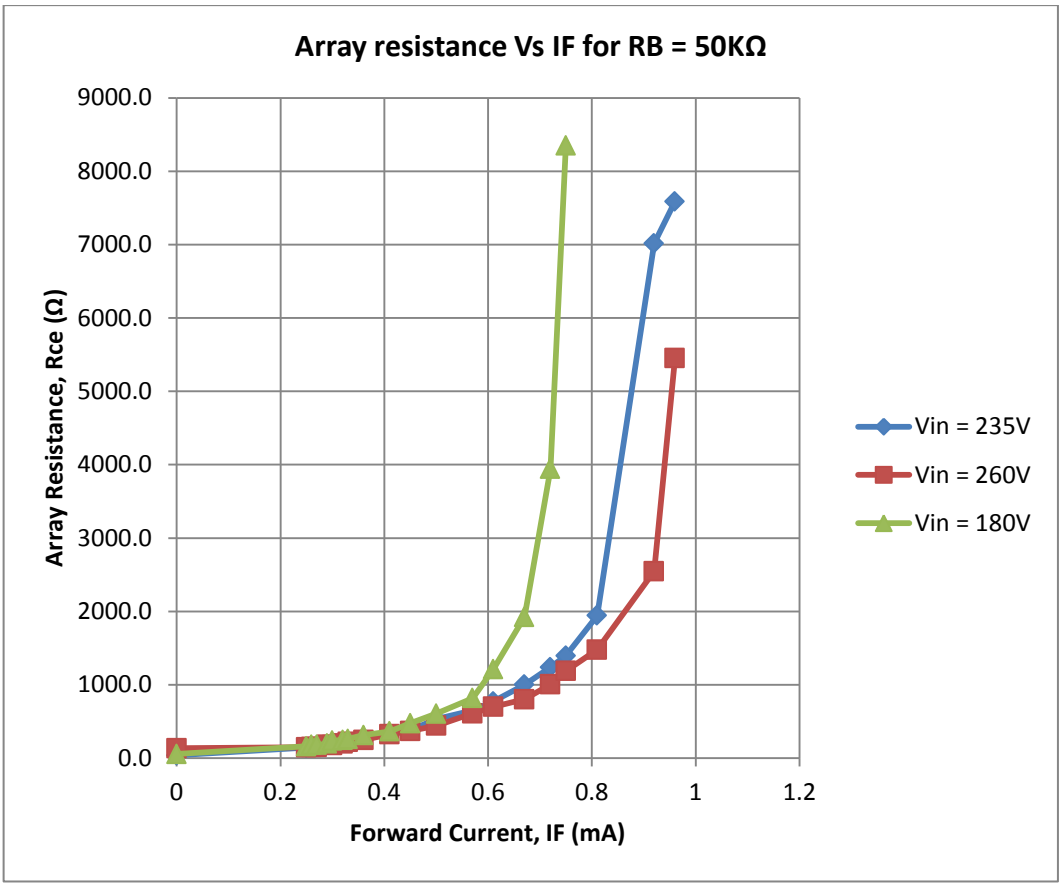


Figure 5.3: Array resistance Vs control current with RB = 50KΩ

Figures 5.2 and 5.3 indicate how the effective array resistance varied with the forward current of the opto-isolator for RB values of 81KΩ and 50KΩ. It is quite clear that the practical minimum value was approximately the same as the theoretical value expected from equation 4.31 ($R_{ce,min} = \frac{nR_B}{\beta}$). However, the practical maximum value was lower than the expected theoretical value as a result of some leakage current in the Darlington pairs of transistors. Finally, the graphs indicate that the effective resistance of the transistor array was also dependent on the AC line voltage.

Figure 5.4 shows the practical implementation of the transistor array with the power transistors mounted on the heat sink.

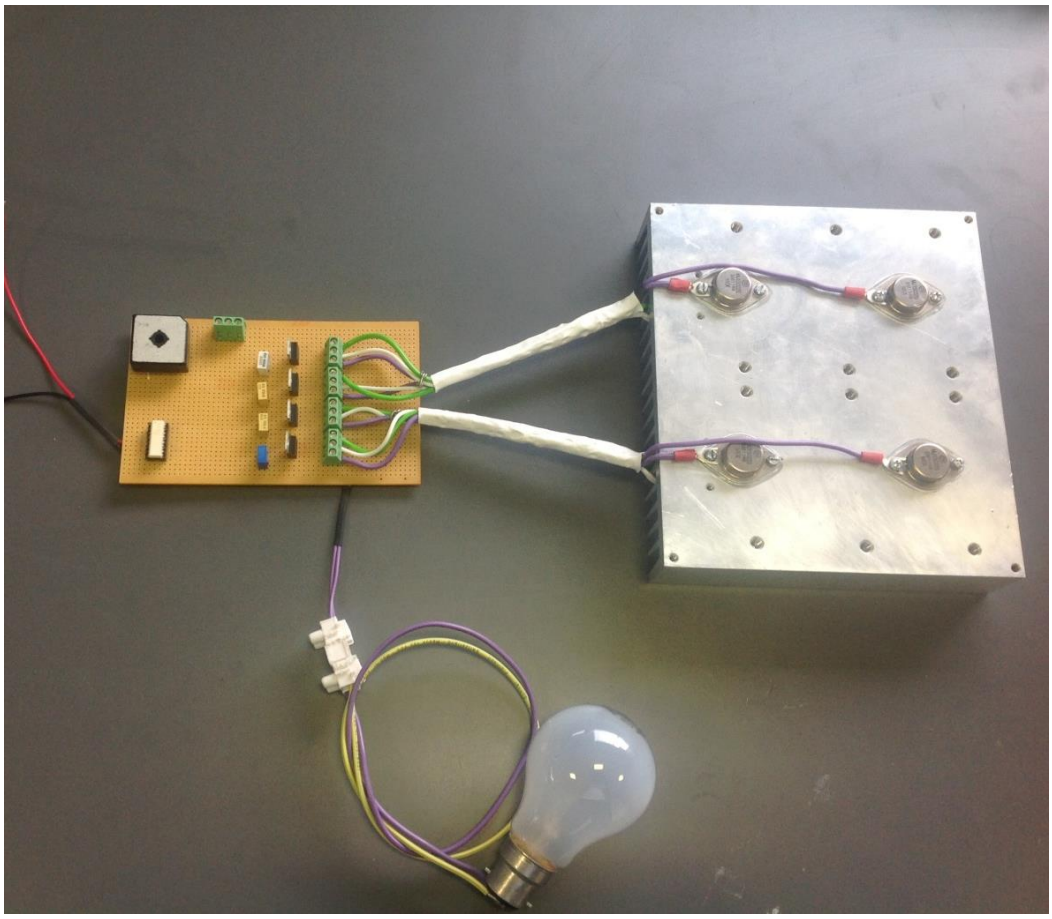


Figure 5.4: Power sharing transistor array of Darlington pair transistors

5.6 The Buck/Boost Transformer

The practical buck/boost transformer used in the implementation was the TELECO transformer, type AS-75 (Teleco, New Zealand). The maximum primary voltage rating is 260V, 50Hz and the secondary voltages are 16V each for both buck and boost with a current rating of 4Amps.

The transformer primary winding was connected in series with the bridge rectifier in such a way that at any instant, the supply voltage was shared between the primary winding and the transistor array. At the secondary winding, there are three wires as can be seen in Figure 5.5. The yellow wire is neutral and the other two wires are for the buck and boost configurations of the transformer.

The voltage on the secondary side between either buck or boost and neutral was 16V and that between buck and boost was 32V.

To improve efficiency, a multi-winding transformer and/or tap change configurations can be incorporated into the system with less side-effect compared to other configurations.

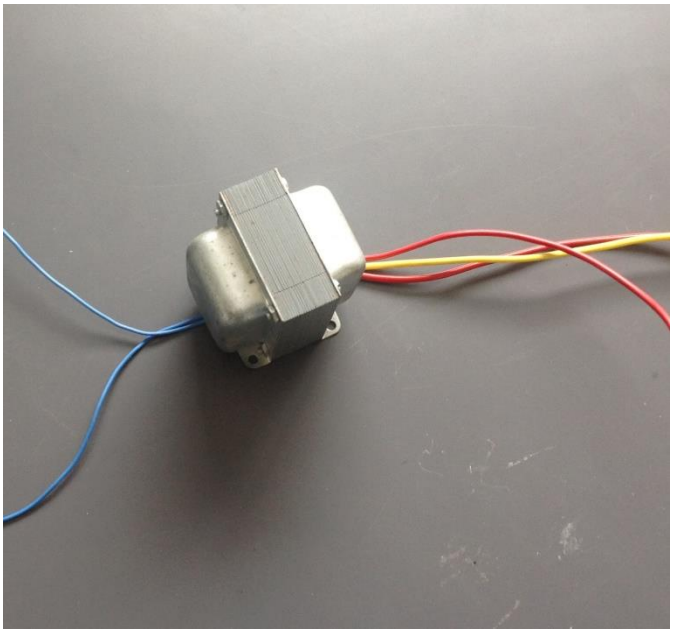


Figure 5.5: The Buck/Boost transformer

5.7 Control Circuit Implementation

The low voltage control circuit was powered from a single rail power supply of +15V. The circuit sampled the AC voltage from the output using a potential divider and then fed it to the input diode of the TIL111 (opto-isolator). The AC sample appearing at the opto-isolator output was then fed to the AD536AJQ (RMS/DC converter). The resulting DC output of the RMS/DC converter was finally amplified by the TIL084 (operational amplifier).

The MC14538 (monostable) stage was used for shorting driving of the 2N3904 transistor during the transient period. Figure 5.6 shows the assembled version of the low voltage control circuit.

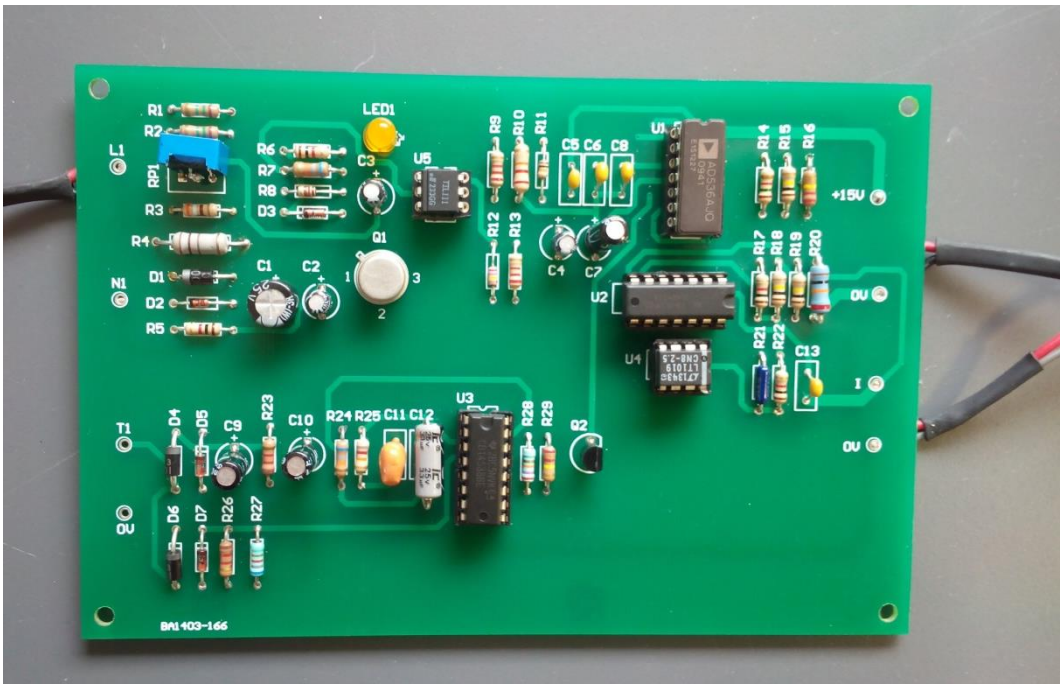


Figure 5.6: Assembled version of the low voltage control circuit

5.8 The Complete AC Voltage Regulator based on Series Transistor Array

The power and control circuits were assembled together to form the series transistor array AC voltage regulator. From this regulator, the load regulations, line regulations, and transient delays were measured and recorded to enable comparison with the PS10 Smart Power Station. Figure 5.7 shows the complete AC voltage regulator based on the series transistor array technique.

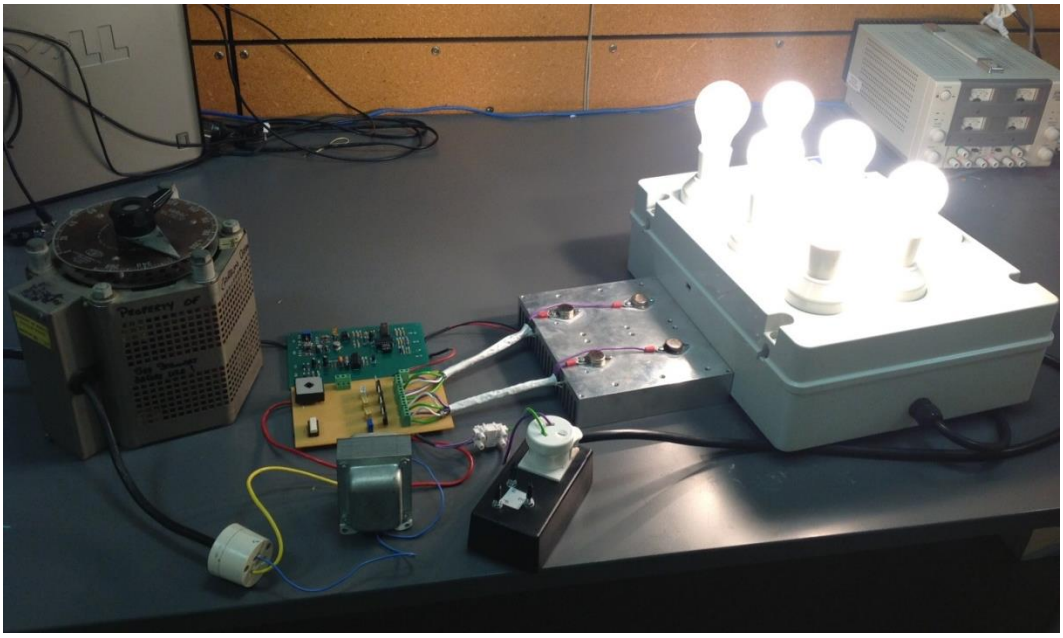


Figure 5.7: AC voltage regulator based on a series transistor array technique

Chapter 6

6.1 Results

The series transistor array AC voltage regulator was tested to determine the following behaviours:

- How the regulated output voltage changes in response to a change in the input voltage at different load conditions (line regulation)
- The change in the regulated output voltage with respect to a continuous change in the load current at different input voltages and efficiency (load regulation).
- The delay seen at the trigger point of the waveform during the transient stage from low to high voltage and from high to low voltage.

6.1.1 Line and load regulations of the transistor array AC voltage regulator

The line regulations of the series transistor array AC voltage regulator were measured and recorded at various loads to determine the variation of the regulated output voltage with respect to change in the supply voltage of the system. Figure 6.1 shows the line regulation curves of the regulator at three different loading conditions.

Similarly, the load regulation of the series transistor array AC voltage regulator was measured and recorded at various input voltages. Figure 6.2 shows how the regulated output voltage of the regulator varies with respect to change in the load current.

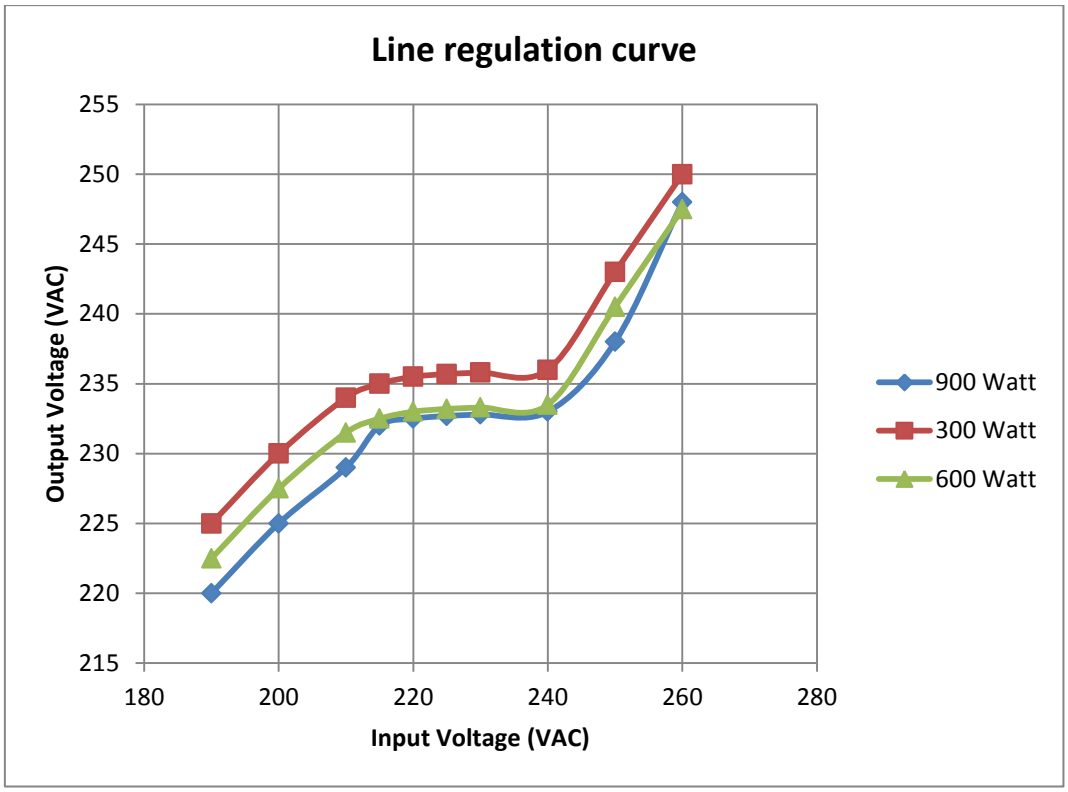


Figure 6.1: AC Voltage regulator line regulation curve

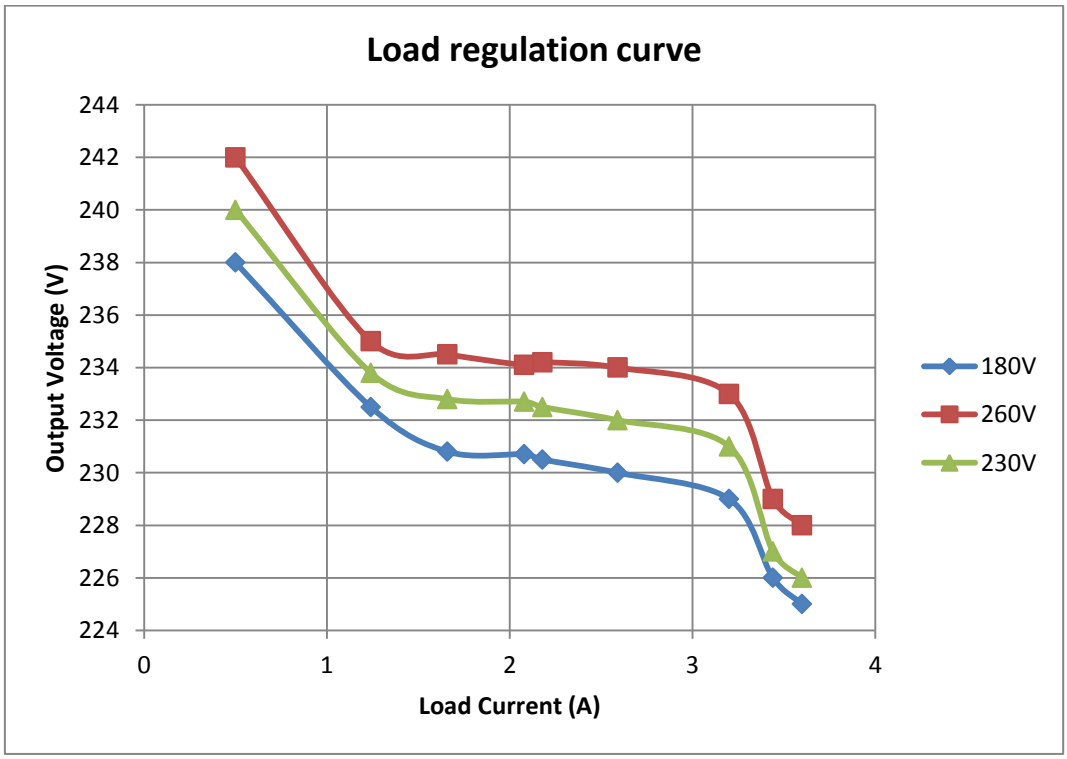


Figure 6.2: AC Voltage regulator line regulation curve

6.1.2 Efficiency of the transistor array AC voltage regulator

The input and output powers were also measured and recorded during the test of the AC voltage regulator from which the efficiency of the system can be calculated. Figure 6.3 shows how the efficiency of the system varied at various line voltages.

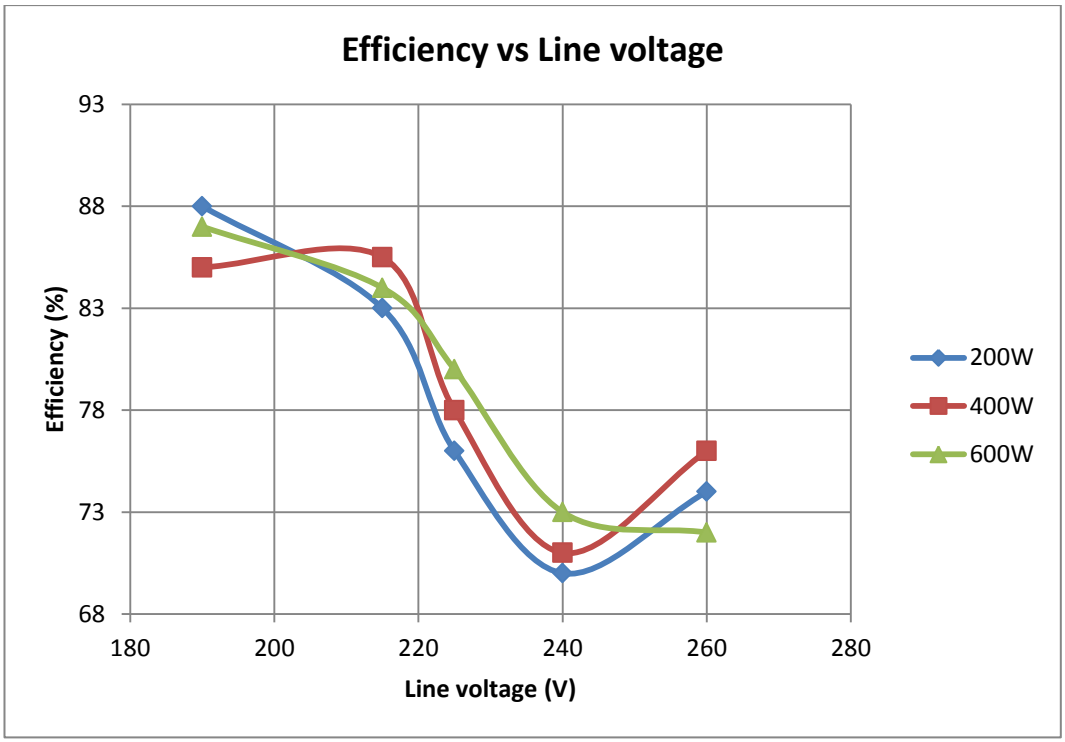


Figure 6.3: Efficiency vs line voltage at various loads

6.1.3 Input and output waveforms of the transistor array AC voltage regulator

At a load current of 1.5A, the input and out voltages of the regulator were observed at low and high input voltages. At low voltage (160V), the input and output waveforms were almost the same as shown in Figure 6.4. However, at high voltage (260V), there was a cross-over distortion in the output waveform as shown in Figure 6.5.

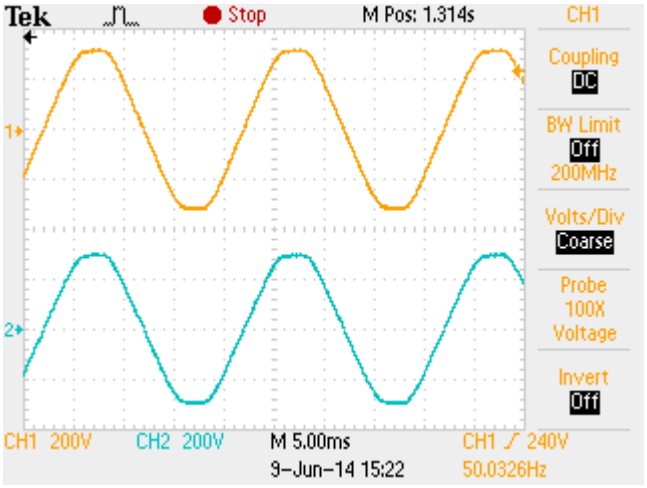


Figure 6.4: Input and output waveforms at an input voltage of 160V and a load current of 1.5A

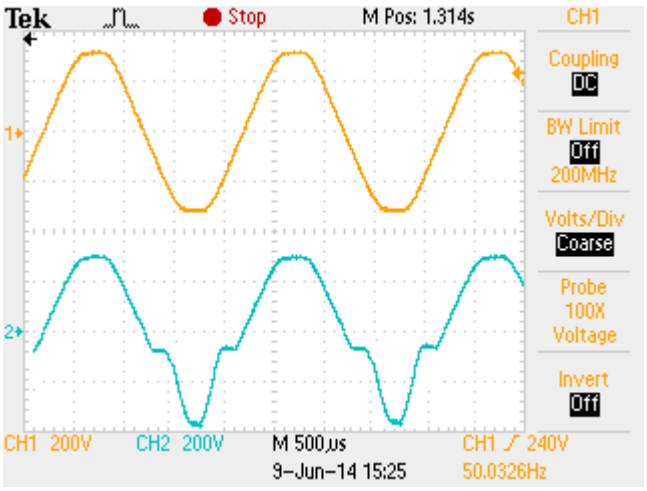


Figure 6.5: Input and output waveforms at an input voltage of 260V and a load current of 1.5A

6.1.4 Using the Voltage Dip and Swell Simulator to measure the response of the transistor array AC voltage regulator

Similar to the PS10 Smart Power Station, the performance of the series transistor array AC voltage regulator was measured using the VDS-2002 Voltage Dip and Swell Simulator. The tests performed were voltage dip and voltage swell tests to measure the response time of the regulator to change in RMS voltage.

Figure 6.6 shows the delay at the output of the transistor array AC voltage regulator at a base voltage of 40%, dip of 5s and interval of 10s. (voltage dip test)

From Figure 6.6, the delay seen at the output of the regulator during the voltage dip test is approximately 700ms.

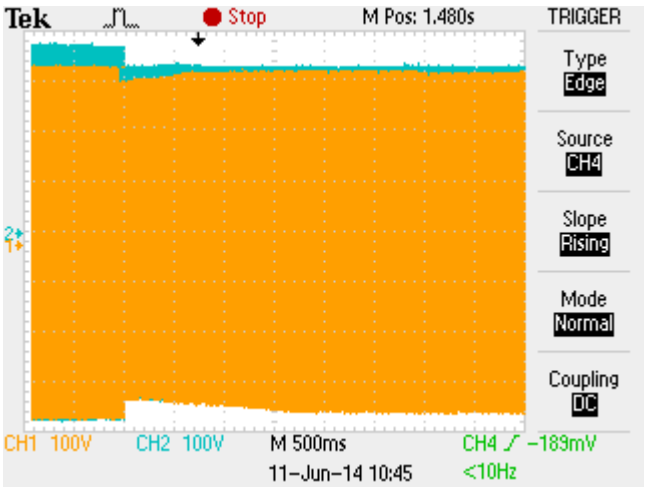


Figure 6.6: Delay seen at a base voltage of 40% (dip test)

The test voltage was then increased to 120% of the base voltage to perform the voltage swell test and the delay observed is shown in Figure 6.7. The delay seen at the output of the regulator during the voltage swell test is approximately 500ms.

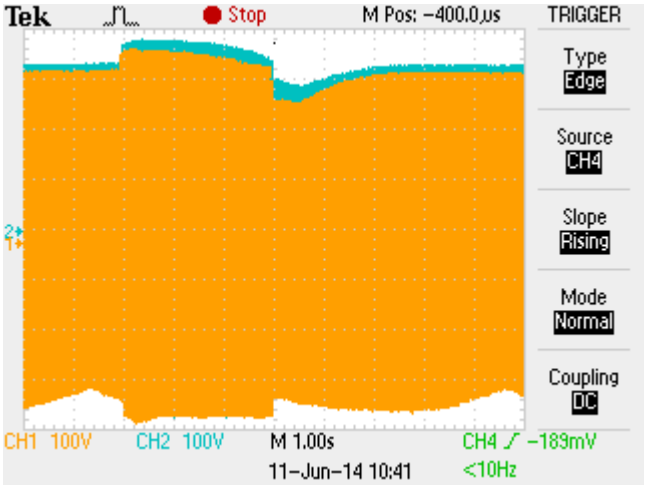


Figure 6.7: Delay seen at a base voltage of 120% (swell test)

6.2 Conclusion and future developments

This thesis provides details of the design techniques and advantages of using bipolar power transistors to construct a fast response, low-cost, light-weight AC voltage regulator. This concept of using a series power semiconductor array that incorporates an opto-isolator-based isolation is applicable to several AC power control applications suitable for low power and single phase requirements.

This work focuses primarily on the design and implementation details of a 2KVA capacity AC voltage regulator. However, this technique could also be extended into other higher power levels (up to 5KVA). One of the major advantages of this technique is that it has the ability to incorporate digital control algorithms to minimize harmonics due to the nonlinear nature of the power semiconductor array. Given these details, the technique could be used to develop AVRs with performance far superior to ferroresonant versions and other slow responding transformer tap changers [22].

Finally, the overall efficiency could be improved by using a combination with other common AC voltage regulator techniques such as transformer tap changers. There is also another possible application in electronic AC loads which includes harmonic control.

Comparing the response time to RMS voltage fluctuation, the AC voltage regulator using a series transistor array is quite fast compared to servo-driven AC voltage regulators, as seen in the results from the PS10 Smart Power Station voltage regulator and the series transistor array-based AC voltage regulator.

6.2.1 Future developments

Future research could aim to improve the structure of the output waveform of the AC voltage regulator at higher voltages in order to minimise unwanted output effects such as crossover distortion. The following sections present some important developments that could be incorporated into the system for better performance.

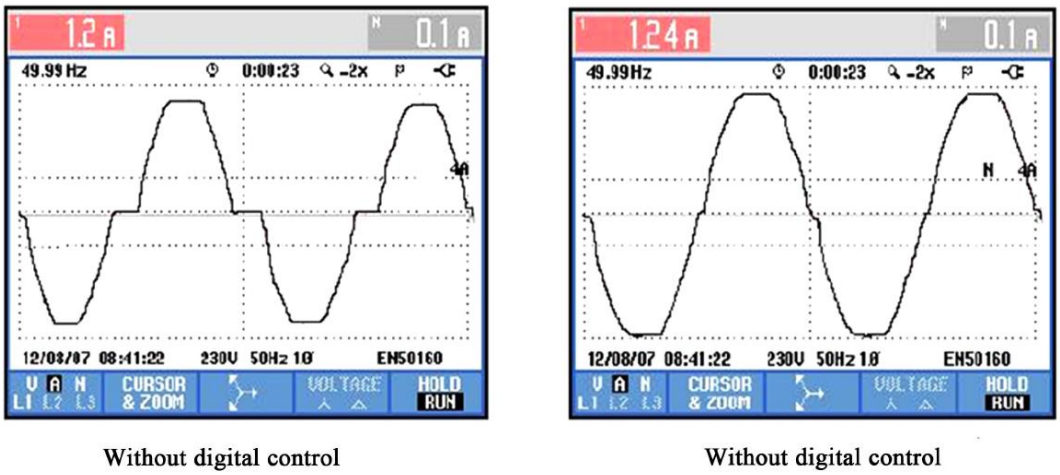
6.2.1.1 Microprocessor based approach for linearizing the array resistance

As a result of the nonlinear behaviour of the series transistor array, the instantaneous current in the array is also nonlinear under general conditions. However, it has a direct dependence on the instantaneous AC line voltage as well as the gain of the transistor on its collector current [23]. Using this approach, a digital control algorithm, injected opto diode current could be controlled so that the instantaneous current through the transistor array could also be controlled by taking relatively larger numbers of samples of the AC voltage waveform.

The overall effect of the microprocessor-based system is to control the opto diode current to achieve the expected impedance, based on the behaviour of the array

during each sampling period. With the sampling of the instantaneous AC line voltage, the microprocessor programme will calculate the required opto diode current (output from the DAC) over each sampling period within the 50 or 60 Hz AC cycle [24].

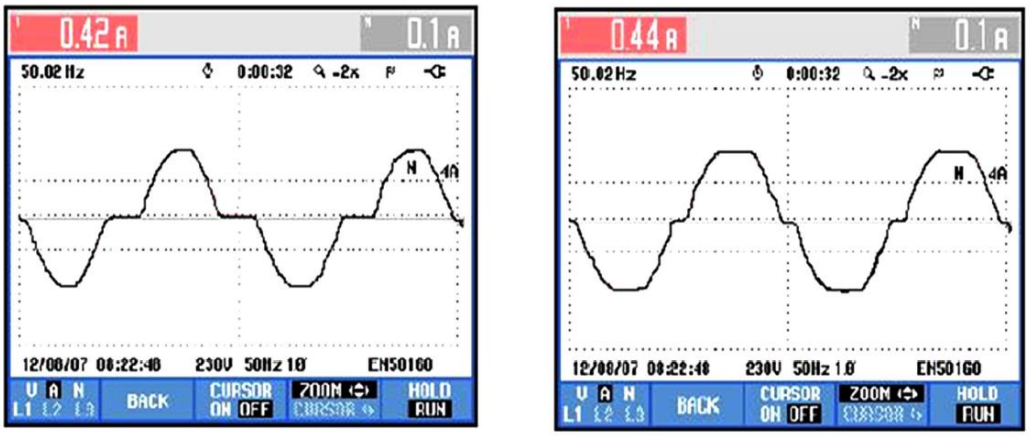
Figures 6.8 and 6.9 compare the array performance with and without digital control at different resistance settings. It is clear from these oscilloscope graphs that the digital control technique reduces the harmonics in the waveform [22].



Without digital control

Without digital control

Figure 6.8: Waveforms with and without digital control at an array resistance of 75Ω [22]



Without digital control

Without digital control

Figure 6.9: Waveforms with and without digital control at an array resistance of 200Ω [22]

Overall achievements in this approach are:

1) A versatile AC impedance control technique which can be used in applications such as AVRs and power conditioners;

2) A new digital control technique where additional digital waveform control can be added to the system to minimize harmonics in the current waveforms [22].

6.2.1.2 Improving the power rating

Metal Oxide Semiconductor Field Effects Transistors or Insulated Gate Bipolar Transistors (MOSFETs or IGBTs) can be used instead of the BJTs used in this project so that the regulator can handle higher power and voltage capability.

References

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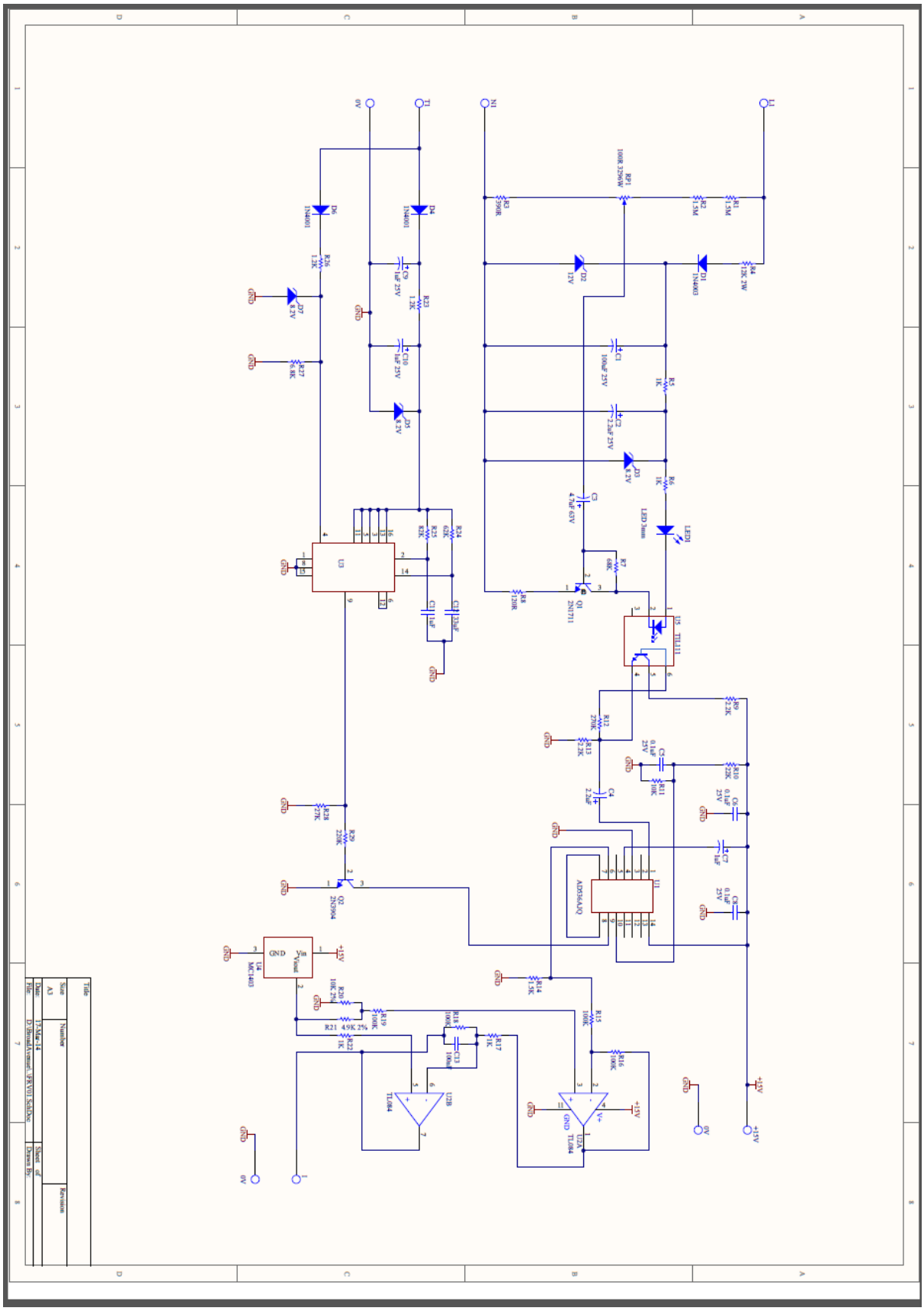
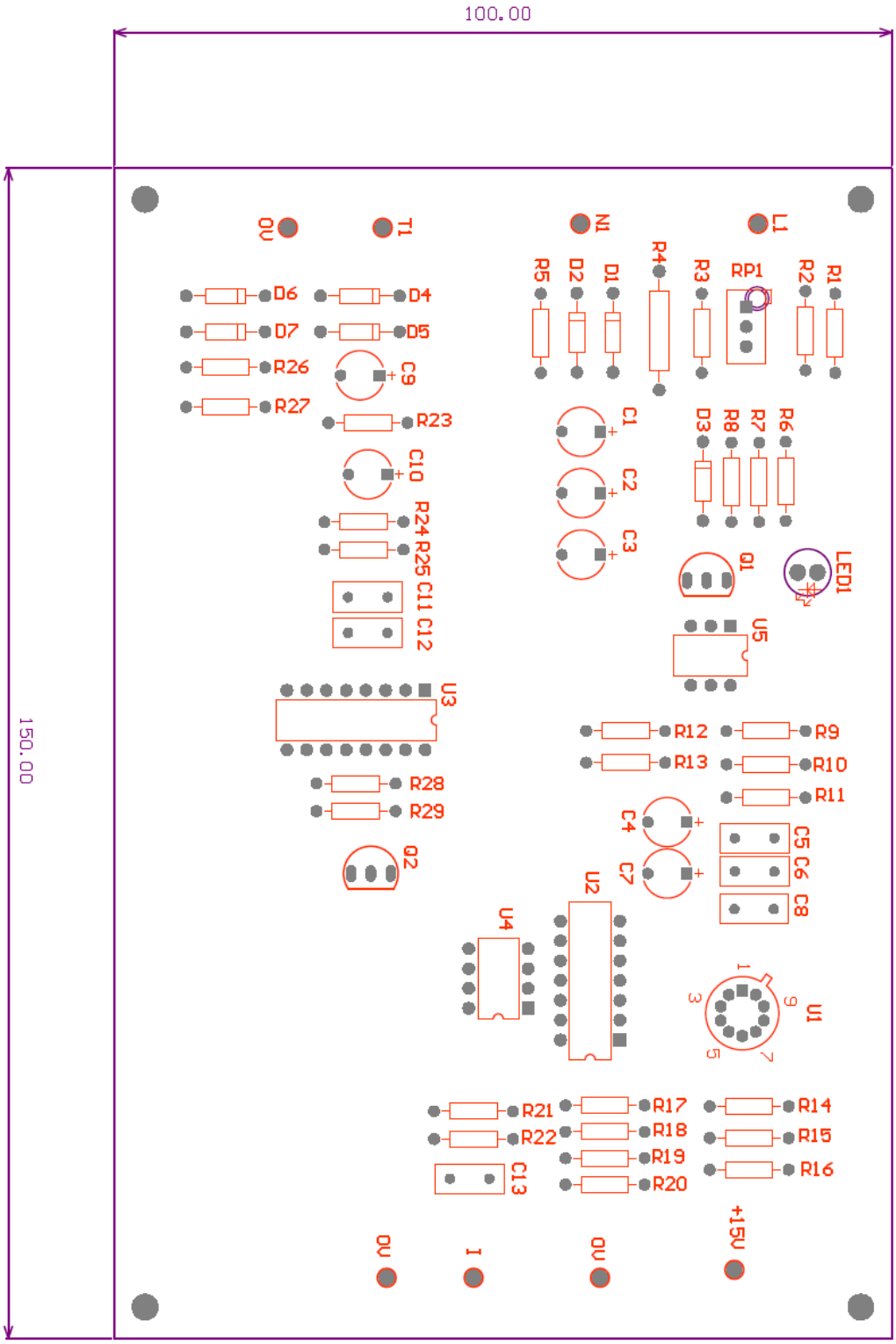
Appendix A.1



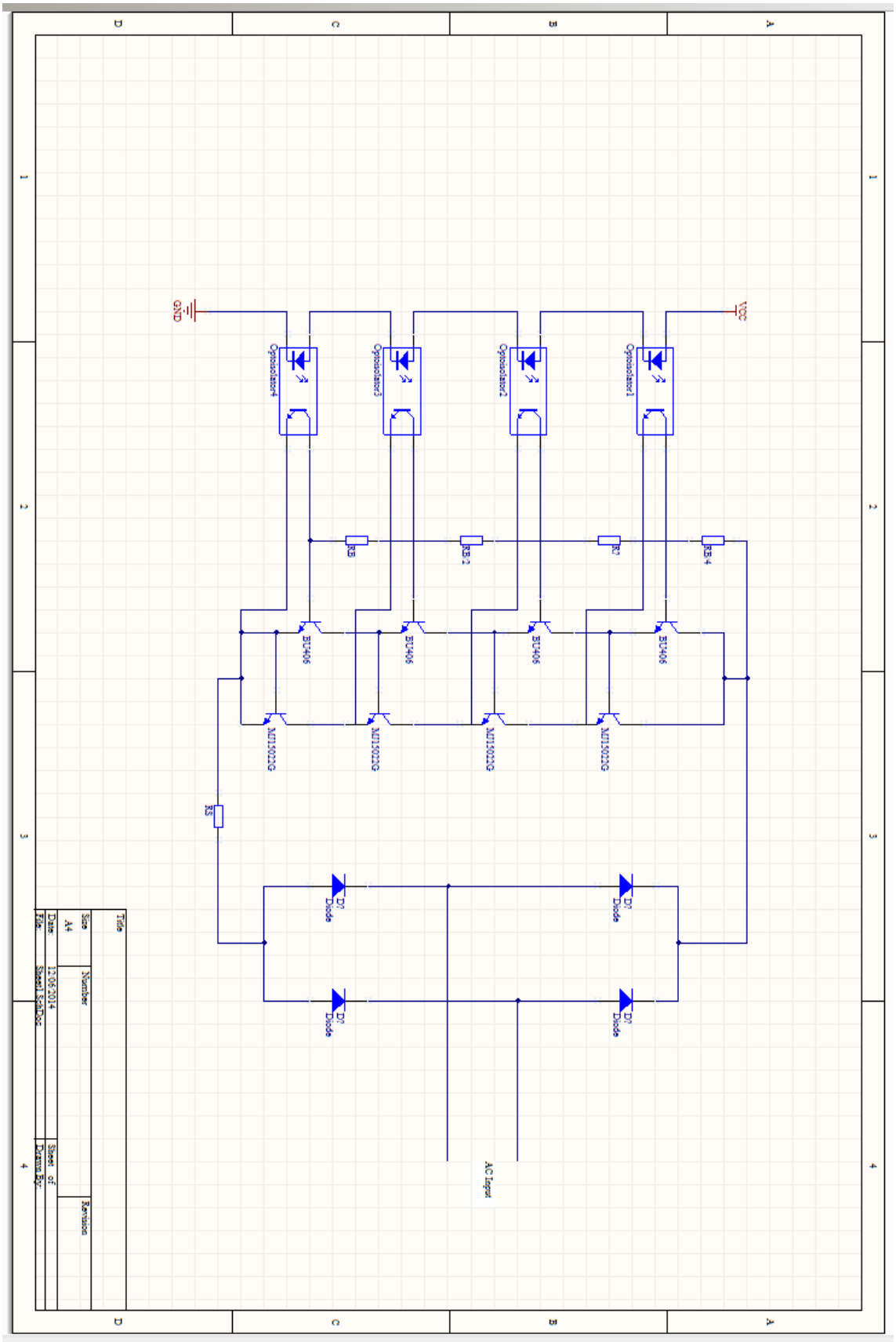
Low voltage control circuits schematics

Appendix A.2



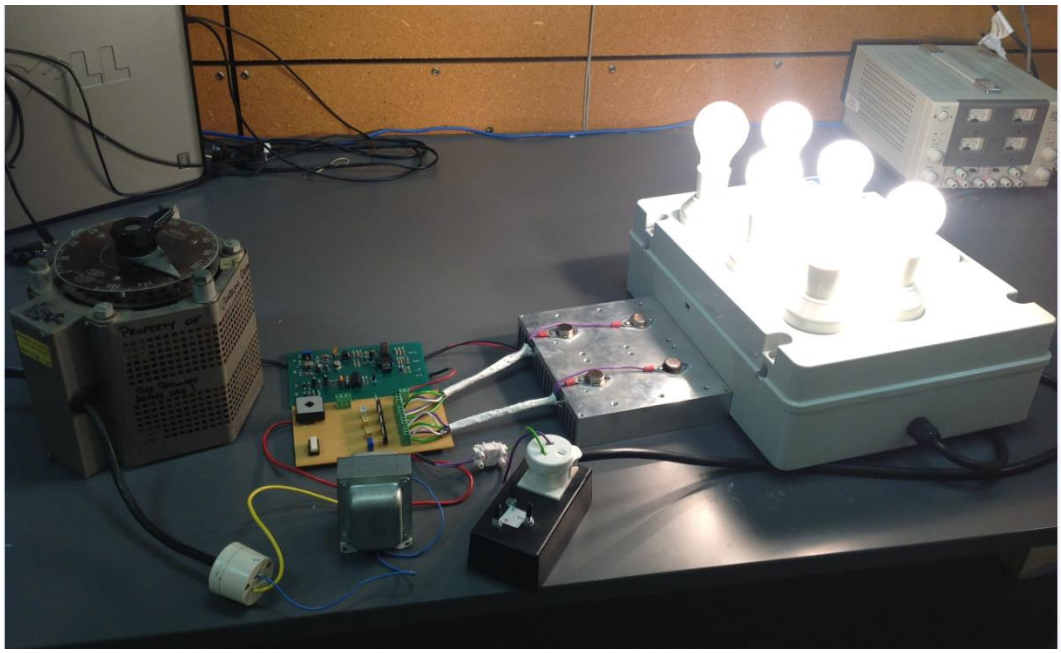
PCB layout of the low voltage control circuit

Appendix A.3



Series transistor array circuit schematics

Appendix A.4



AC voltage regulator using series transistor array

Appendix A.5

MJ15022 (NPN), MJ15024 (NPN)

Silicon Power Transistors

The MJ15022 and MJ15024 are power transistors designed for high power audio, disk head positioners and other linear applications.

Features

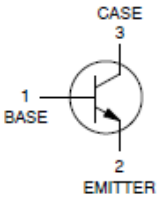
- High Safe Operating Area
- High DC Current Gain
- These Devices are Pb−Free and are RoHS Compliant*
- Complementary to MJ15023 (PNP), MJ15025 (PNP)

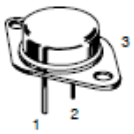
ON Semiconductor®

http://onsemi.com

16 AMPERES
SILICON POWER TRANSISTORS
200 – 250 VOLTS, 250 WATTS

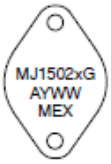
SCHEMATIC





TO−204AA (TO−3)
CASE 1−07
STYLE 1

MARKING DIAGRAM



MJ1502x = Device Code, x = 2 or 4
G = Pb−Free Package
A = Assembly Location
Y = Year
WW = Work Week
MEX = Country of Origin

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage MJ15022 MJ15024	V_{CEO}	200 250	Vdc
Collector−Base Voltage MJ15022 MJ15024	V_{CBO}	350 400	Vdc
Emitter−Base Voltage	V_{EBO}	5	Vdc
Collector−Emitter Voltage	V_{CEX}	400	Vdc
Collector Current – Continuous	I_C	16	Adc
Collector Current – Peak (Note 1)	I_{CM}	30	Adc
Base Current – Continuous	I_B	5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.70	°C/W

ORDERING INFORMATION

Device	Package	Shipping
MJ15022G	TO−204 (Pb−Free)	100 Units / Tray
MJ15024G	TO−204 (Pb−Free)	100 Units / Tray

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MJ15022 Transistor data sheet

MJ15022 (NPN), MJ15024 (NPN)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Note 2) (I_C = 100 mAdc, I_B = 0)	MJ15022 MJ15024	$V_{CEO(sus)}$	 200 250	 – –	–
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	 MJ15022 MJ15024	I_{CEX}	 – –	 250 250	μAdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 vdc, I_B = 0)	 MJ15022 MJ15024	I_{CEO}	 – –	 500 500	μAdc
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_B = 0)		I_{EBO}	–	500	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 0.5 s (non–repetitive)) (V_{CE} = 80 Vdc, t = 0.5 s (non–repetitive))		$I_{s/b}$	 5 2	 – –	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)		h_{FE}	 15 5	 60 –	–
Collector–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)		$V_{CE(sat)}$	 – –	 1.4 4.0	Vdc
Base–Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)		$V_{BE(on)}$	–	2.2	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain – Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	4	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)		C_{ob}	–	500	pF

2. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

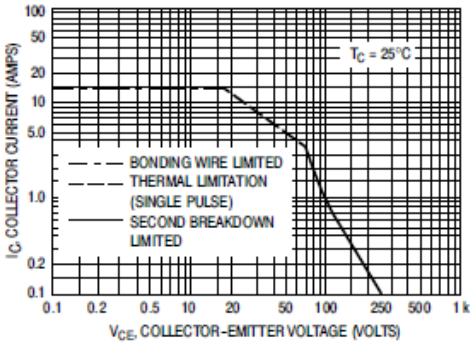


Figure 1. Active–Region Safe Operating Area

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values Ion than the limitations imposed by second breakdown.

http://onsemi.com

MJ15022 Transistor data sheet

Appendix A.6

TOSHIBA TLP504A,TLP504A−2

TOSHIBA Photocoupler GaAs Ired & Photo−Transistor

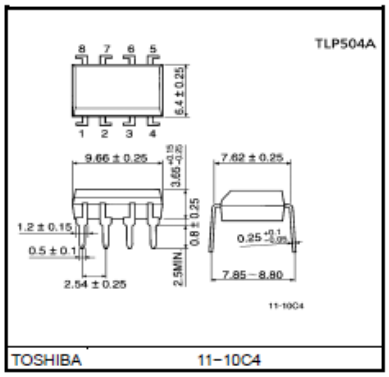
TLP504A,TLP504A−2

Programmable Controllers
AC / DC−Input Module
Solid State Relay

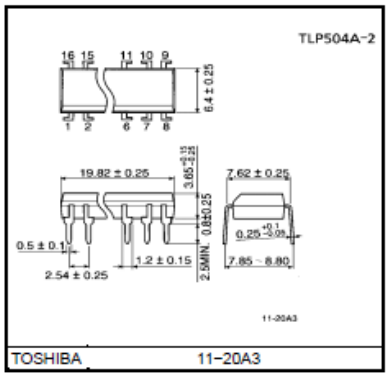
The TOSHIBA TLP504A and TLP504A−2 consists of a photo−transistor optically coupled to a gallium arsenide infrared emitting diode.
The TLP504A offers two isolated channels in a eight lead plastic DIP package, while the TLP504A−2 provides four isolated channels in a sixteen plastic DIP package.

- Collector−emitter voltage: 55 V (min.)
- Current transfer ratio: 50% (min.)
  Rank GB: 100% (min.)
- Isolation voltage: 2500 Vrms (min.)
- UL recognized: UL1577,
  File no. E67349

Unit in mm

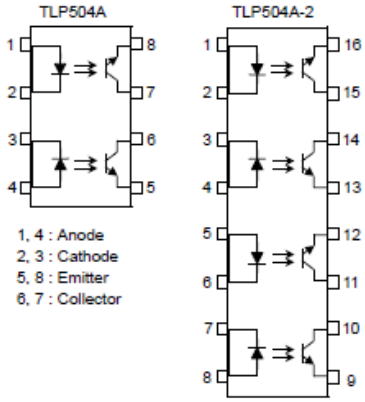


Weight: 0.54 g



Weight: 1.1 g

Pin Configurations (top view)



1, 4 : Anode
2, 3 : Cathode
5, 8 : Emitter
6, 7 : Collector

1, 4, 5, 8 : Anode
2, 3, 6, 7 : Cathode
9, 12, 13, 16 : Emitter
10, 11, 14, 15 : Collector

TLP504 A-2 photo transistor datasheet

TOSHIBA TLP504A,TLP504A−2

Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating		Unit
			TLP504A	TLP504A−2	
LED	Forward current	I_F	60	50	mA
	Forward current derating	ΔI_F / °C	−0.7 (Ta ≥ 39°C)	−0.5 (Ta ≥ 25°C)	mA /°C
	Pulse forward current	I_{FP}	1 (100μs pulse, 100pps)		A
	Reverse voltage	V_R	5		V
	Junction temperature	T_j	125		°C
Detector	Collector−emitter voltage	V_{CEO}	55		V
	Emitter−collector voltage	V_{ECO}	7		V
	Collector current	I_C	50		mA
	Collector power dissipation (1 circuit)	P_C	150	100	mW
	Collector power dissipation derating (1 circuit Ta ≥ 25°C)	ΔP_C / °C	−1.5	−1.0	mW /°C
	Junction temperature	T_j	125		°C
Storage temperature range		T_{stg}	−55~150		°C
Operating temperature range		T_{opr}	−55~100		°C
Lead soldering temperature		T_{sol}	260 (10 s)		°C
Total package power dissipation		R_T	250	150	mW
Total package power dissipation derating (Ta ≥ 25°C)		ΔP_T / °C	−2.5	−1.5	mW / °C
Isolation voltage		BV_S	2500 (AC, 1min., R.H.≤ 60%) (Note 1)		Vrms

(Note 1) Device considered a two terminal device: LED side pins shorted together and detector side pins shorted together.

Recommended Operating Conditions

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	—	5	24	V
Forward current	I_F	—	16	20	mA
Collector current	I_C	—	1	10	mA
Operating temperature	T_{opr}	−25	—	85	°C

TLP504 A-2 photo transistor datasheet

Individual Electrical Characteristics (Ta = 25°C)

	Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
LED	Forward voltage	V_F	I_F = 10 mA	1.0	1.15	1.3	V
	Reverse current	I_R	V_R = 5 V	—	—	10	μA
	Capacitance	C_T	V = 0, f = 1 MHz	—	30	—	pF
Detector	Collector–emitter breakdown voltage	$V_{(BR)\ CEO}$	I_C = 0.5 mA	55	—	—	V
	Emitter–collector breakdown voltage	$V_{(BR)\ ECO}$	I_E = 0.1 mA	7	—	—	V
	Collector dark current	I_{CEO}	V_{CE} = 24 V	—	10	100	nA
			V_{CE} = 24 V, Ta = 85°C	—	2	50	μA
	Capacitance collector to emitter	C_{CE}	V = 0, f = 1 MHz	—	10	—	pF

Coupled Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Current transfer ratio	I_C / I_F	I_F = 5 mA, V_{CE} = 5 V	50	—	600	%
		Rank GB	100	—	600	
Saturated CTR	I_C / $I_{F\ (sat)}$	IF = 1 mA, V_{CE} = 0.4 V	—	60	—	%
		Rank GB	30	—	—	
Collector–emitter saturation voltage	$V_{CE\ (sat)}$	I_C = 2.4 mA, I_F = 8 mA	—	—	0.4	V
		I_C = 0.2 mA, I_F = 1 mA	—	0.2	—	
		Rank GB	—	—	0.4	

Isolation Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Capacitance input to output	C_S	V_S = 0, f = 1 MHz	—	0.8	—	pF
Isolation resistance	R_S	V_S = 500 V	5×10^{10}	10^{14}	—	Ω
Isolation voltage	BV_S	AC, 1 minute	2500	—	—	Vrms
		AC, 1 second, in oil	—	5000	—	
		DC, 1 minute, in oil	—	5000	—	Vdc

TLP504 A-2 photo transistor datasheet