A Supercapacitor Assisted Technique for Reducing Losses in the Input Loop of an Inverter System for Solar PV Applications

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***Abstract*—This paper presents a method of using supercapacitor modules in the input loop, to reduce the input losses of a typical inverter system used in solar applications. It is an extension of the supercapacitor-assisted loss management principle (SCALoM), where supercapacitors act as lossless droppers and energy buffers at the input end with a very low frequency switching scheme with reduced dynamic losses in switches compared to switched capacitor-inverter systems. The technique uses a set of micro-inverters, with the same total power capability as a single inverter, combined with a set of supercapacitor banks switching at a low frequency to reduce the voltage stress and rms current through the H-bridge input stages of the inverters, enhancing the end-to-end efficiency of the overall system. The proposed technique does not require a re-design of the commercially available inverters and adds DC-UPS capability to the system. Preliminary experimental results of the SCA(super capacitor assisted) two-inverter arrangement show stable transient and steady state operations, and the system is up to 2.2% efficient compared to a single central inverter arrangement. With the proposed SCA four-inverter configuration, inverter's overall power load can be further partitioned, and according to the analytical study further improvements in the overall efficiency can be achieved over the SCA two-inverter arrangement .**

***Index Terms*—Supercapacitors, solar inverters, inverter power losses, solar PV systems, inverter efficiency.**

I. Introduction

For medium and high voltage solar PV inputs, commercially available H-bridge based inverters are commonly used. Commercially available H-bridge inverters come in two different forms, namely (i) with a front-end DC-DC converter followed by the DC to AC conversion (inverter) stage and (ii) a single DC-AC conversion stage. The second type is usually used in larger scale solar PV systems where series or parallel connections of inverters are used for grid-level AC systems [1, 2]. Both forms come with a transformer for the galvanic isolation and voltage conversions [2]. Low input range flyback type inverters are of less efficiency in high power density applications due to high MOSFET on-state conduction losses resulted by high RMS currents in the inverter, high switching losses due to hard-switching in such arrangements and high transformer losses due to high flux excursions in the coupled-inductors.

High power density grid-level inverters, without any input side DC-DC converters are more efficient when operated at higher voltage as it reduces parasitic and component level losses caused by the input loop current. To improve the overall efficiency, high power density grid-level systems sometimes use extended high input voltage capable central inverters, [3–8]. However, developing extended input voltage range inverters has been challenging due to many techno-commercial barriers. In such applications as a result of the input side high voltage stresses, high-voltage rated components need to be used. This affects negatively on the component level efficiency of the inverter and manufactures have to look for expensive alternatives such as SiC MOSFETS to limit the power losses at the individual components with additional cost implications. In [9, 10], series inverter arrangements and series DC/DC converter arrangements have been proposed as alternatives, but they have not been developed into industrial solutions , due to instability and high complexity in controlling under dynamic load and input conditions.

Multilevel and string inverter arrangements have been introduced in high power density applications like distributed energy resources (DER). The cascaded H-Bridge (CHB) is a commonly used multilevel circuit topologies in high power density photovoltaic applications [11, 12]. But CHB is suitable for applications where it is possible to provide separate dc-link (connected to a power cell) for each H-Bridge segment [11]. And operating CHB systems efficiently under unbalanced power of the cells under different operating conditions has been challenging.

Multi-level switched capacitor inverter topologies have been proposed which allows the input range of the inverter to be increased which reduces the input loop rms current. But there is a significant trade off in the efficiency gain as they involve inefficient high-frequency switching schemes [13].

This paper introduces a novel technique with the extension of the fundamentals of SCALoM principle to reduce the losses in the input loop of an inverter system. Section II of this paper presents a summary of the key loss elements in a typical inverter, for a given power output and a nominal DC input voltage. In section III, extensive discussion of the novel SCA

(super capacitor assisted) technique has been carried out. In section IV, an analytical study of the impact of the proposed technique on the typical losses in a inverter system has been presented. In section V, results of the laboratory experimental validation of the proposed technique is discussed.

II. TYPICAL LOSSES ASSOCIATED WITH AN INVERTER

For a flyback type H-bridge inverter [1, 2] (transformer located in the DC-DC converter stage), with a nominal AC output of V_{AC} and a DC nominal input voltage of V_{DC}, input current of I_{DC}, and load current of I_{AC}, the key losses in the inverter comprise of (a) copper losses (primary: PTP, secondary: PTP) and the core losses in the transformer, (b) static losses in the switching transistors (on-state conduction: P_{ON}), (c) dynamic losses in the transistor switches (switching: P_{SW}, gate: PG), (d) losses associated with the equivalent series resistance (ESR) of the input DC capacitor (PC) [14–16]. Table I depicts a summary of these losses. There, the transformer losses are calculated assuming that the inverter input DC loop current is equivalent to the transformer primary rms current and the output AC rms current is equivalent to the transformer secondary current.

III. INVERTER LOSS REDUCTION APPROACH WITH SCALOM

Supercapacitors (SC) provide high power capability, due to their very low equivalent series resistance and they come with long life cycles compared to batteries. SCALoM theory [17–19] and the supercapacitor assisted (SCA) techniques [17, 20–23], demonstrate a new design approach for building high efficiency converters with extra-low switching frequency. In renewable energy applications like solar PV, continuous utilization of the generated energy is important to maintain the overall power generation efficiency of the renewable energy system. But in previous SCALoM applications, energy is consumed from the energy source during the charging cycle and in the discharge cycle energy source is idle. This work investigates the possibility of extending the SCALoM loss reduction technique, to a system of solar inverters and multiple supercapacitor banks such that it draws the power continuously from the energy source. Thus, it does not impact the overall end-to-end system efficiency when directly used with a solar PV energy source.

Fig.1 summarizes how a typical power electronic building block (PEBB) can be used in a modified R-C circuit with a SC [17–19], based on the SCALoM theory [18, 19].

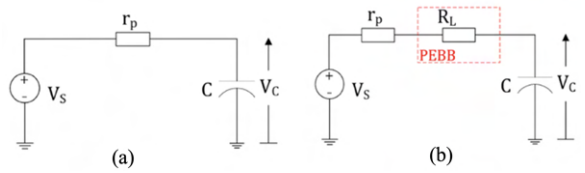

Fig. 1: RC circuit, (a) The basic RC circuit, (b) RC circuit with a PEBB [18].

For a configuration as indicated in the Fig. 1(a), the maximum theoretically achievable charging efficiency of supercapacitor is 50% as the total energy stored during the capacitor is: $E_{\mathrm{C}} = \frac{1}{2}CV^2$ and similar amount of power $E_{\mathrm{r}} = \frac{1}{2}CV^2$ is dissipated through the r_{p} parasitic resistive elements as waste energy. SCALoM principle is based on the fact that as indicated in Fig. 1(b), by adding useful load R_{L} a portion of the energy wasted in r_{p} can be reduced to $E_{\mathrm{r}}^{'} = \frac{1}{2}CV^2\frac{r_{\mathrm{p}}}{(r_{\mathrm{p}}+R_L)}$.

Compared to the possible worst case efficiency of 50% in an R-C circuit, Fig. 2, depicts the efficiency gains in SCALoM approach, where a SC is used instead of a normal capacitor. Here, the useful resistive load (R_L) inserted into the charging loop in Fig. 1(a) can come in the form of a PEBB and a portion of the losses will be usefully consumed by the PEBB.

If the capacitor is pre-charged to a pre-charge factor of k, $k > 0$, there will be further gains of efficiency as indicated in Fig. 2. When the normal capacitor is replaced by a SC, it creates a slow speed circuit (long time constant circuit), which allows the SC bank switching (for charging and discharging) to happen at extra low frequencies, reducing the dynamic losses of the switches in the SCA converter system [17, 18].

As depicted in Fig. 2, the efficiency gains in a SCALoM circuit increase with the $\frac{R_{\mathrm{L}}}{r_{\mathrm{p}}}$ ratio (r_{p}: parasitic resistive components in the circuit). There m is the ratio of DC source voltage/maximum voltage of the SC.

The implementation of the proposed SCA-inverter-technique is indicated in Fig. 3, by having a supercapacitor pre-charged (to VDC_{low}) in series with a loaded inverter as a useful load in the charging loop of the SC and continuing the process until the supercapacitor is charged to VDC_{high}. In the charging cycle as indicated in Fig. 3, a supercapacitor pre-charged to voltage pre-charge factor, $k < 1, m \simeq 0.5$, is operated in series with an inverter, with an input voltage of V_{DC} and a DC source of V_{S}. Here the supercapacitor charge voltage is V_{SC}.

As depicted in Fig. 3, supercapacitor in the charging phase starts with an initial voltage of $V_{\mathrm{SC}} = V_{\mathrm{SC}}(t_1)$ and the charging continues until it reaches $V_{\mathrm{SC}} = V_{\mathrm{SC}}(t_2)$, at which point it changes over to discharge phase as shown in Fig. 4, with the inverter fed by the supercapacitor module. This operation from t_1 to t_2 is given by,

$$\begin{aligned} V_{\mathrm{DC}}(t_1) &= V_{\mathrm{S}} - V_{r_{\mathrm{p}}}(t_1) - V_{\mathrm{SC}}(t_1), \\ V_{\mathrm{DC}}(t_2) &= V_{\mathrm{S}} - V_{r_{\mathrm{p}}}(t_2) - V_{\mathrm{SC}}(t_2), \end{aligned} \tag{1}$$

where: $t_1 < t_2$.

$$V_{\mathrm{SC}}(t_2) = \tfrac{1}{C}\textstyle\int_{t_1}^{t_2} I(t)dt + V_{\mathrm{SC}}(t_1) \tag{2}$$

Here, $V_{r_{\mathrm{p}}}(t_i), V_{\mathrm{DC}}(t_i)$ and $V_{\mathrm{SC}}(t_i)$, $i = 1, 2$ represents instantaneous voltage across parasitic elements, inverter input

TABLE I: Key power loss components of an inverter.

Loss component	Approximate relationships
Transformer Copper loss $(P_{\mathrm{TP}}, P_{\mathrm{TS}})$ [14]	$P_{\mathrm{TP}} = I_{\mathrm{DC}}^2 R_{\mathrm{TP}}, P_{\mathrm{TS}} = I_{\mathrm{AC}}^2 R_{\mathrm{TS}}$
MOSFET switching loss (P_{SW}) [15, 16]	$P_{\mathrm{SW}} = 0.5 I_{\mathrm{DC}} V_{\mathrm{DC}} t_{\mathrm{rise}} f_{\mathrm{PWM}} + 0.5 I_{\mathrm{DC}} V_{\mathrm{DC}} t_{\mathrm{fall}} f_{\mathrm{PWM}}$
MOSFET on-state conduction (P_{ON}) [15, 16]	$P_{\mathrm{ON}} = I_{\mathrm{DC}}^2 R_{\mathrm{DSON}}$
MOSFET gate loss (P_{G}) [15, 16]	$P_{\mathrm{G}} = Q_{\mathrm{G}} V_{\mathrm{GS}} f_{\mathrm{PWM}}$
Input capacitor loss (P_{C})[14]	$R_{\mathrm{C}} I_{\mathrm{rp}}^2$
TP, TS: transformer primary, secondary; f_{PWM}: PWM frequency; $t_{\mathrm{rise,fall}}$: rise, fall time; Q_{G}, V_{GS}=gate charge, gate voltage; $I_{r_{\mathrm{p}}}$=ripple current.	

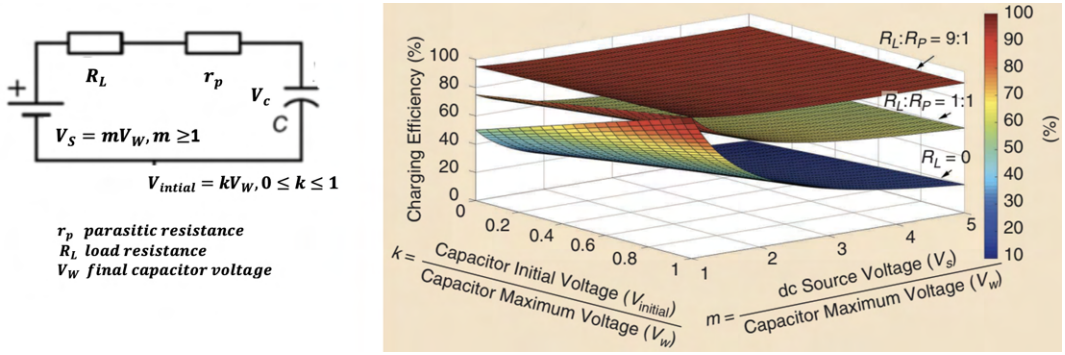

Fig. 2: Supercapacitor charging efficiency variation [18].

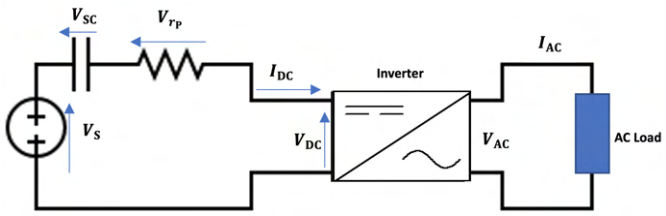

Fig. 3: Charge cycle of the SCA inverter arrangement.

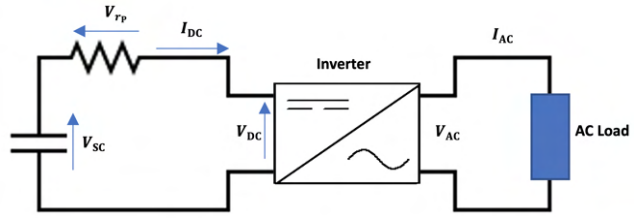

Fig. 4: Discharge cycle of the SCA inverter arrangement.

and supercapacitor respectively, C the supercapacitor capacitance and $I(t)$ the current drawn by the inverter. V_{SC} for the charging and discharging cycles (in Fig. 3, 4) for the supercapacitors is bounded by the input voltage range that the inverter can operate which is $[V_{\mathrm{DC}_{low}}, V_{\mathrm{DC}_{high}}]$. As per the SCALoM principle discussed earlier, the use of the pre-charged supercapacitor in series, significantly reduces the energy losses due to the parasitic components of the charging loop (Fig. 3). i.e. Assuming that the parasitic losses are negligible, (1) can be reduced to:

$$V_{\mathrm{S}} = V_{\mathrm{DC}_{high}} + V_{\mathrm{DC}_{low}} = 2V_{\mathrm{DC}_{avg}}, \tag{3}$$

where, $V_{\mathrm{DC}_{avg}} = \frac{V_{\mathrm{DC}_{high}} + V_{\mathrm{DC}_{low}}}{2}$, $V_{\mathrm{DC}_{low}} = V_{\mathrm{SC}}(t_1), V_{\mathrm{DC}_{high}} = V_{\mathrm{SC}}(t_2)$.

$$f_{\mathrm{SCA}} = \frac{P_{inv}}{\Delta E_{\mathrm{SC}}{}_{t_1}^{t_2}} \tag{4}$$

where, $\Delta E_{\mathrm{SC}}{}_{t_1}^{t_2} = \frac{1}{2} C[\mathrm{DC}_{high}^2 - \mathrm{DC}_{low}^2]$.

Result (3), indicates that by implementing the proposed technique a classical inverter can be successfully operated by a DC voltage source that is two times the rated input voltage of the inverter. As per (4), where, f_{SCA} : SC bank switching frequency, P_{inv} : inverter power, having a supercapacitor bank with a sufficiently large enough capacitance, makes it possible to achieve a very low frequency switching scheme, and the total energy buffered in the SC adds DC-UPS capability into the inverter system for practical operation with fluctuating solar PV power sources.

As shown in Fig. 5 and 6, this approach is further extended to two and four inverter configurations for practical implementation.

IV. IMPACT ON THE KEY POWER LOSSES BY THE PROPOSED TECHNIQUE

The end-to-end-efficiency improvement is based on combining supercapacitor energy storage modules, and a partitioned

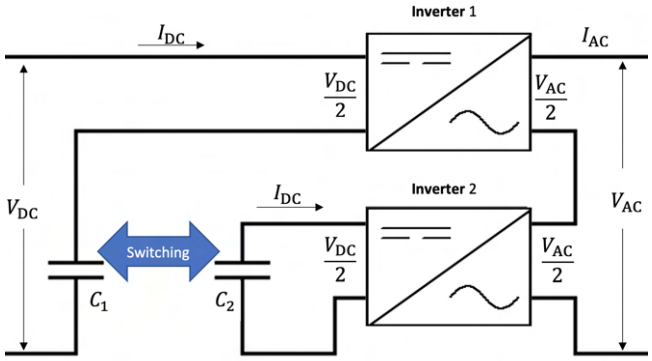

Fig. 5: SCA two-inverter configuration.

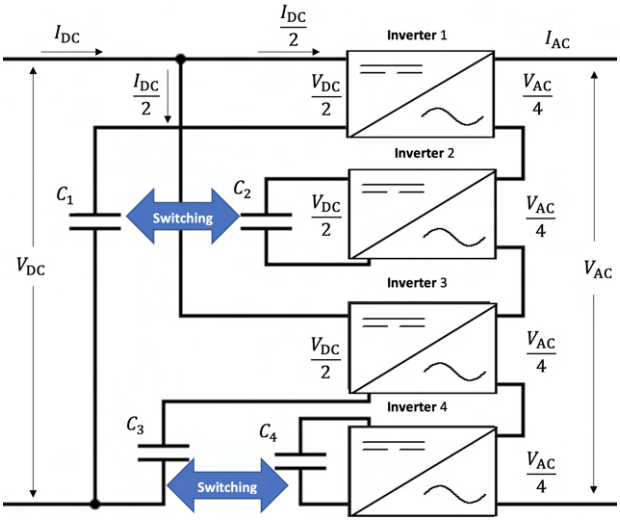

Fig. 6: SCA four-inverter configuration.

(multiple) inverter system to deliver the expected output power, operated by an input power source with a voltage supply that is two times the rated input voltage of inverters. With configuration Fig. 5, voltage stress on the inverter components is reduced by half, and by configuration Fig. 6, current through the inverters too, is reduced by half.

Table II, depicts the reduction of the losses associated with the transformer, transistors and input capacitor compared to the case of a stand-alone inverter in Table I. Considering, Fig. 6, a transformer's rated saturation voltage is given by [24],

$$V_{\mathrm{AC}} = 4.44BANf \tag{5}$$

where, B is the maximum flux density, A is the core cross section, N is the number of turns, and f is the operational frequency. For Fig. 6 arrangement, if the transformer secondary is compared with the single transformer arrangement,

$$\frac{0.25V_{\mathrm{AC}}}{V_{\mathrm{AC}}} = \frac{4.44BAfN^{iv}}{4.44BAfN}, N^{iv} = 0.25N. \tag{6}$$

As per (6), the number of turns in the transformer secondary can be reduced with the four-inverter configuration by four times and, similarly primary turns by two times, leading to a further reduction of the transformer copper losses.

V. IMPLEMENTATION OF THE SCA FRONT END FOR INVERTER SYSTEM AND EXPERIMENTAL RESULTS

Commercially available 24VDC-300W-110VAC, pure-sine wave solar inverters are used in the implementation of the topologies in Fig. 5 and 6. One of the key requirements to use an inverter as the useful load in a SCALoM circuit arrangement is the ability of the inverter to operate within a certain input voltage range, without compromising its normal operation. To determine $V_{\mathrm{DC}_{low}}$, $V_{\mathrm{DC}_{high}}$, efficiency of the inverters under varying input DC voltage and load levels is experimentally studied. As indicated in Fig. 7, in the input voltage range $V_{\mathrm{DC}_{low}}$ = 23VDC, $V_{\mathrm{DC}_{high}}$ = 25VDC, the micro-inverters could be operated without compromising the overall performance.

The two-inverter arrangement in Fig. 5 is implemented using 42F, 54VDC supercapacitor banks and an input voltage source of 48VDC. The steady state and transient behaviours observed are indicated in Fig. 10 and Fig. 11. The combined VAC output of the inverter system is indicated by the yellow line. Light blue and pink lines indicate control signals to switch the capacitor banks C_1 and C_2 such that they are charged and discharged in the VDC range 23-25VDC.

Laboratory implementation of the two-inverter configuration was successful and as indicated in the experiment results in Fig. 10 and 11, combined VAC output of the inverters was stable and no additional harmonic distortions (THD $<$ 0.4 %) was observed due to capacitor bank switching. i.e. Due to very low switching schema of the supercapacitor banks, no additional power quality degradations are not observed.

Preliminary overall efficiency comparison of the two-inverter configuration is conducted under lower load conditions without considering parasitic resistive components associated with an actual site installation. At 104.5W, 24V single inverter arrangement could be operated at 88.8%, at 103.9W while the

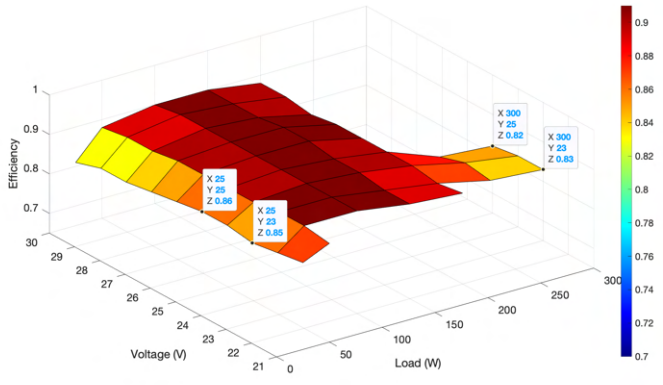

Fig. 7: Input voltage, load efficiency characteristic of the 24VDC inverter.

TABLE II: A comparison of the losses associated with each inverter by partitioning the load.

Losses	Two-inverter (Fig. 5)	Four-inverter (Fig. 6)	Changes
$(P_{\mathrm{TP}}, P_{\mathrm{TS}})$	$P_{\mathrm{TP}}^{ii} = 0.5P_{\mathrm{TP}}, P_{\mathrm{TS}}^{ii} = 0.5P_{\mathrm{TS}}$	$P_{\mathrm{TP}}^{iv} = 0.125P_{\mathrm{TP}}, P_{\mathrm{TS}}^{iv} = 0.25P_{\mathrm{TS}}$	$V_{\mathrm{DC}}^{ii}, V_{\mathrm{DC}}^{iv} = 0.5V_{\mathrm{DC}}, I_{\mathrm{DC}}^{iv} = 0.5I_{\mathrm{DC}}$
(P_{ON})	$P_{\mathrm{ON}}^{ii} < P_{\mathrm{ON}}$	$P_{\mathrm{ON}}^{iv} < P_{\mathrm{ON}}$	$R_{\mathrm{DSON}}^{ii} < R_{\mathrm{DSON}}, R_{\mathrm{DSON}}^{iv} < R_{\mathrm{DSON}}$
(P_{SW})	$P_{\mathrm{SW}}^{ii} = 0.5P_{\mathrm{SW}}$	$P_{\mathrm{SW}}^{iv} = 0.25P_{\mathrm{SW}}$	$V_{\mathrm{DC}}^{ii}, V_{\mathrm{DC}}^{iv} = 0.5V_{\mathrm{DC}}, I_{\mathrm{DC}}^{iv} = 0.5I_{\mathrm{DC}}$
(P_{C})	$P_{\mathrm{C}}^{ii} = 0.5P_{\mathrm{C}}$	$P_{\mathrm{C}}^{iv} = 0.25P_{\mathrm{C}}$	$I_{\mathrm{DC}}^{iV} = 0.5I_{\mathrm{DC}}$
Superscripts ii, iv: parameters of two, four inverter configurations; R_{DSON} =MOSFET on-state drain to source resistance.			

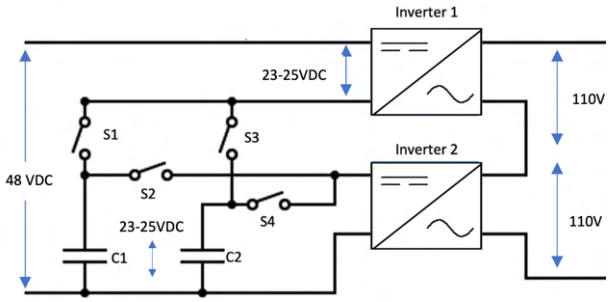

Fig. 8: Switching arrangement of the two inverter configuration.

TABLE III: SCA two-inverter arrangement switching schema.

State	S1	S2	S3	S4
C1 charging, C2 discharging	On	Off	Off	On
C2 charging, C1 discharging	Off	On	On	Off

prototype of the SCA two-inverter could be operated 89%. At 211.9W, 24V single inverter arrangement could be only operated at an efficiency of 87.5%, whereas the SCA two-inverter arrangement operated at an improved efficiency of 89.7% at 207.2W.

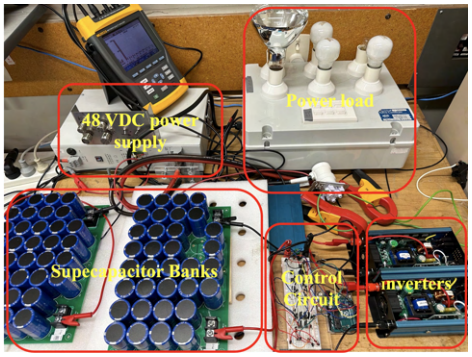

Fig. 9: The experiment implementation of the two inverter configuration.

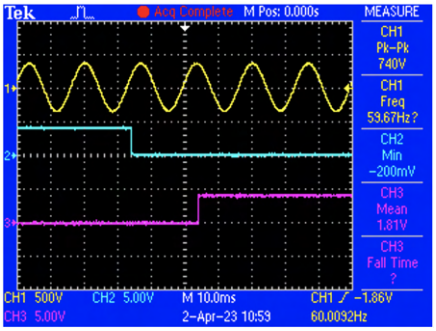

Fig. 10: Two-inverter configuration transient behaviour.

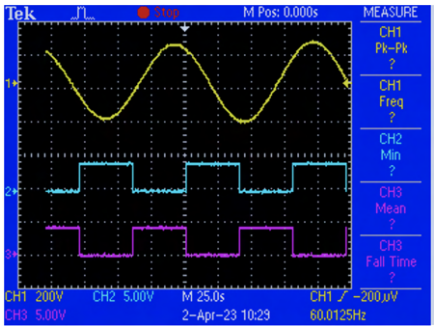

Fig. 11: Two-inverter configuration steady state behaviour.

VI. Conclusion

This paper discusses how a high input voltage range central inverter arrangement in solar PV applications can be partitioned into a set of lower input voltage range inverters based on the SCALoM principle. With the two-inverter arrangement voltage stress on the inverter components is reduced by half using the supercapacitor banks as lossless droppers and energy buffers, with a very low frequency switching scheme. This process does not add dynamic losses typically associated with a high frequency switching converter scheme and as a result it does not compromise the overall performance of the inverter system. With the four inverter arrangement rms current through the inverter components can be further reduced, leading to additional improvements in the overall efficiency as summarized in the Table II.

The proposed SCA two- inverter arrangement was exper-

imentally validated, and the obtained analytical and experimental results of the transient and steady state operation of the prototype indicated stable and efficient operation of the system with DC-UPS capability. Preliminary load tests conducted indicated improvements of the efficiency up to 2.2% at higher load levels. In a further future development, the SCA four-inverter configuration is expected to provide a significant improvement in the efficiency and performance will be validated as per the guidelines of IEC 61683 standard.

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