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# Stability analysis and experimental validation of the supercapacitor-assisted low-dropout regulator

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**Abstract:** The supercapacitor-assisted low-dropout (SCALDO) regulator is a unique new design approach to develop high efficiency, high current and low noise DC–DC converters, where a supercapacitor (SC) is used in the series path of a low dropout (LDO) regulator to act as a lossless voltage dropper. In the published literature, there has been much discussion about the stability of an LDO regulator, where different approaches are applied to frequency compensate depending on the LDO architecture. Given the case that the SCALDO technique is a combination of an LDO regulator and an SC, this study presents an analysis and experimental validation of the stability, based on a 12–5 V SCALDO prototype, proving that the effect of the SC energy recovery method does not make the overall regulator carry a stability issue in general.

## 1 Introduction

### *1.1 Modern DC–DC converter topologies and DC power management*

Energy-efficient power management is a key requirement in the design of modern electronic devices [1, 2]. Therefore, the product manufacturers always strive to come up with optimised DC–DC converters to power these devices to achieve high efficiency. Fast transient response, low noise, and less complexity are also important priorities in developing DC power management solutions for portable products and consumer electronics [2]. Three basic DC–DC converters used in these devices are linear regulators, inductor-based switch-mode converters and switched capacitor converters (charge pumps) [3]. These three techniques can be combined to generate multiple DC power rails in modern electronic products to achieve the best possible performance [3, 4]. On the other hand, non-conventional methods have also been introduced for different applications [5, 6] and these all have various pros and cons, based on their design limitations.

Low-dropout regulators are a special type of linear regulator, which are designed to operate under very low input-to-output voltage differences to achieve high ETEE. Low dropouts (LDOs), with their low headroom voltage, provide very low noise and high current slew-rate capable linear DC power rails. The supercapacitor-assisted low-dropout (SCALDO) regulator, on the other hand, operates based on the principle that an ideal capacitor acts as a series lossless voltage dropper in the series path of a linear (LDO) regulator. Although the SCALDO regulator maintains the same useful characteristics of a linear (LDO) regulator, the major advantage is the high-efficiency operation even at a large input-to-output voltage difference. Therefore, the SCALDO concept is a better alternative to switching converters with the added advantage of DC-UPS capability. Also, this concept has opened the door for another set of SCA (supercapacitor-assisted) techniques useful in wider power electronics area [7–10].

Table 1 compares the performance characteristics of the three conventional DC–DC converter topologies along with the SCALDO regulator.

**Table 1** Comparison of three basic DC–DC converter topologies and the SCALDO regulator

| Conventional topologies | | | | SCALDO regulator |
|---|---|---|---|---|
| Feature | Linear regulators | Switched capacitor converters | Switch-mode converters | |
| conversion type | step-down | step-up/down | step-up/down | Step-down |
| efficiency | low to moderate (limited by $V_{out}/V_{in}$) | moderate to high | highest | High ($V_{out}/V_{in}$ limitation of a linear regulator has been overcome) |
| cost | low | moderate | moderate | Moderate |
| design complexity | low | moderate | moderate to high | Low |
| external components | minimum external components: one or no input/output capacitor | low: a flying capacitor, reservoir capacitors | high: (magnetic components, filters) | Low (one LDO regulator, a supercapacitor and four low-speed switches) |
| noise/EMI | lowest | moderate | highest | Low (similar to a linear regulator) |
| output current | low to high | lowest | highest | Low to high |
| output power | moderate (heat dissipation becomes significant when $V_{out}/V_{in}$ is high) | moderate (due to low output current capability) | highest | High (energy is recovered by a supercapacitor without wasting as heat) |
| dynamic response | best | poor | good | Very good (similar to a linear regulator) |

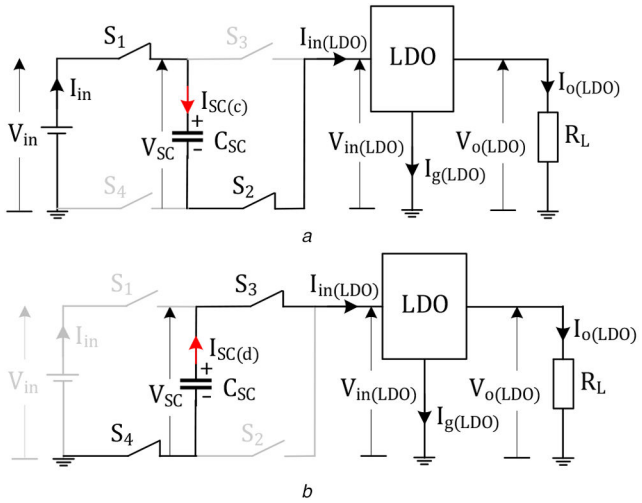



**Fig. 1** *Circuit topology of the single-stage SCALDO regulator*
***(a)*** Charging mode, ***(b)*** Discharging mode

### *1.2 Emergence of the SCALDO technique as a very low-frequency design approach with high current capability*

From 2009 to 2014, as a completely new low-frequency design approach to high-efficiency DC–DC converters, the SCALDO technique was successfully developed with a US patent granted in 2011 [11]. This technique is one of the most developed applications of generic SCA techniques [12]. All SCA techniques are based on the unique supercapacitor-assisted loss management [SCALOM] theory presented in [13]. Wider research interest has been expressed in this method by various groups outside New Zealand, as indicated in [14].

In the basic technique, an array of SCs is used as a voltage dropper element in the series path of an LDO regulator. This concept is based on the loss circumvention principle of a resistor-capacitor loop fed by a DC voltage source [13]. More discussion on the operating principle of this concept is provided in Section 1.3. The energy accumulated in these SCs is recirculated at a very low frequency, increasing the end-to-end efficiency (ETEE) of the regulator by a multiplication factor in the range of 1.33 to 3, compared with the efficiency of a linear regulator circuit designed for the same input-to-output voltage combination. Due to the very low switching frequency, this approach eliminates any RFI/EMI issues. The concept has been successfully matched to different power supply requirements with very good outcomes [12, 15, 16]. One of the latest applications based on this technique is the high-efficiency split-rail DC–DC converter [17].

It is important to note that the SCALDO is not a variation of the traditional charge pump converters, as published in [15]. The unique properties of the SCALDO technique and its applications are listed below.

- Load sees the high quality, low noise output of a linear regulator, while the extra energy accumulated by the series SC in the input side of the regulator is circulated back to the same linear regulator, disconnecting the input energy source and connecting the SC in parallel.
- It operates at a very low frequency in the order of millihertz to fractional Hertz, and does not create RFI/EMI issues.
- It is applicable to load currents in the range of a few milliamperes to tens of amperes. For load currents up to about 10 A, single-chip LDOs are usable. For higher currents, a discrete transistor-based LDO regulator can be used.
- It requires SCs in the range of 1–100 F, with similar can sizes of electrolytic capacitors in the microfarad range and does not add excessive cost to design and manufacturing [17].
- It can be modified to achieve the DC-UPS capability within the converter by oversizing the SC.

### *1.3 Operating principle of the single-stage SCALDO regulator*

This discussion is based on the simplest configuration where a single SC is utilised. This approach has two operating phases, as depicted in Fig. 1, involving both charging and discharging modes. The operation is done based on four low-speed switches ($S_1$–$S_4$), and more implementation details are available in [16].

As shown in Fig. 1*a*, the power source, the SC and the LDO regulator are connected in series in the charging mode. Because of this series connection, the SC acts as a lossless series dropper element between the source and the LDO regulator. The change of voltage (Δv) across the SC is very small due to its large capacitance ($C_{SC}$) when a finite current ($i(t)$) flows for a limited time ($t$), as shown in (1)

$$\Delta v = \frac{1}{C_{SC}} \int_0^t i(t)\mathrm{d}t \tag{1}$$

Due to this effect, the DC is not blocked, and the LDO regulator keeps the output DC voltage regulated for a finite amount of time. Since the ground pin current of a well-designed LDO regulator is close to zero ($I_{g(LDO)} \approx 0$), the output current ($I_{o(LDO)}$) and the source current ($I_{in}$) become equal in the charging mode. As the SC charges, the input voltage of the LDO regulator ($V_{in(LDO)}$) decreases. The SC is kept in this position until $V_{in(LDO)}$ falls to its minimum operating voltage ($V_{min}$). If the ESR of the SC and the resistance of the low-frequency switches are negligible, the voltage of the SC ($V_{SC}$) becomes approximately $V_{in}$–$V_{min}$ at the end of the charging cycle.

When the charging process ends, the SC is forced to switch into discharging mode by disconnecting the power source, as shown in Fig. 1*b*. To maintain the regulation of the LDO, the starting voltage of the SC ($V_{in}$–$V_{min}$) must be higher than $V_{min}$ at the beginning of the discharging phase, satisfying the criterion: $V_{in}$–$V_{min} > V_{min}$. This condition is identified as the $V_{in} > 2V_{min}$ topology requirement of a single-stage SCALDO regulator [16] where the source voltage should be more than twice the minimum working voltage of the LDO regulator. A suitable analogue comparator and logic gates or microcontroller unit can be used to ensure this condition is true always. The SC is allowed to discharge until the input voltage of the LDO regulator drops back to $V_{min}$.

These two operating modes run cyclically maintaining a net-zero charge accumulation in the SC. The switching frequency typically varies from fractional Hertz to a few Hertz. Since the power source is completely disconnected in the discharging mode and $I_{g(LDO)} \approx 0$, the average input current of the source ($I_{in(avg)}$) for a complete period is $I_{o(LDO)}/2$ at the steady-state. Therefore, the approximate ETEE ($\eta_{SCALDO}$) of the single-stage SCALDO topology is given in (2)

$$\eta_{SCALDO} \simeq \frac{V_{o(LDO)} I_{o(LDO)}}{V_{in} I_{in(avg)}} = \frac{V_{o(LDO)} I_{o(LDO)}}{V_{in}(I_{o(LDO)}/2)} = 2\frac{V_{o(LDO)}}{V_{in}}(2) \tag{2}$$

As can be seen from (2), this method gives an efficiency improvement factor of 2, since $V_{o(LDO)}/V_{in}$ is the efficiency of the LDO with the ground pin current neglected. In a 12–5 V case, this approach translates to an ETEE of ~84%, while the load enjoys the low noise high slew rate capable output of a linear regulator [16]. More details about the efficiency advancement of different SCALDO topologies and useful characteristics, such as load regulation, line regulation and transient response, compared with the LDO regulator characteristics, are described in [18].

### *1.4 Requirement of the stability analysis as the next stage of SCALDO research*

Despite the use of a frequency compensated LDO regulator in this technique, the low-frequency switching network at the input side may affect the overall stability. A proper stability analysis is required to investigate the deviations of the stability margins from

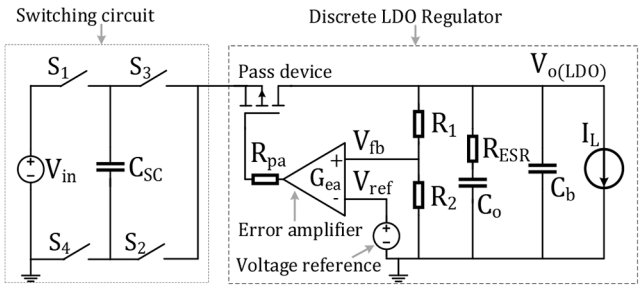



**Fig. 2** *SCALDO regulator in discrete form*

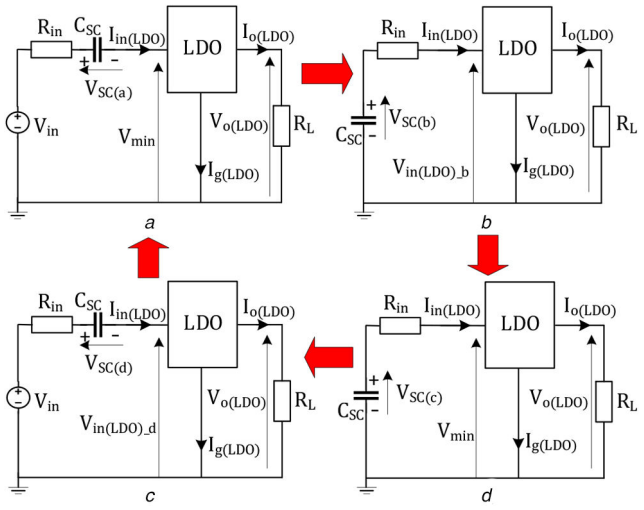



**Fig. 3** *Different stages of a switching cycle*
***(a)*** Termination of the charging mode, ***(b)*** Outset of the discharging mode, ***(c)*** Termination of the discharging mode, ***(d)*** Outset of the charging mode

the LDO regulator after this technique is used for high ETEE operation. Therefore, overall stability margins need to be confirmed, to ensure reliable operation.

Since the SCALDO technique is applicable to large load currents, even up to tens of amperes, the prototype circuit developed in this research is based on a discrete LDO regulator used at the output. Nevertheless, for small load currents, a single-chip LDO regulator can be used. Commencing with an overview of preliminary work published as conference proceedings at different stages [19, 20], this paper makes a significant contribution in the following areas: (i) detailed derivation and analysis of the small-signal model of the SCALDO regulator; (ii) simulated and experimental results concerning the open-loop and load transient responses; (iii) perturbation analysis related to the low-frequency switching; and (iv) quantitative comparison of the theoretical, simulated and experimental results.

## 2 Small-signal modelling of the single-stage SCALDO regulator

### *2.1 LDO stage*

Fig. 2 depicts the case of a typical SCALDO circuit with its LDO stage based on discrete circuit components, where a single SC and four low-frequency switches are used at the input side. The LDO regulator is built with a series-pass device (PMOS transistor), a reference voltage source ($V_{ref}$), an error amplifier, a feedback resistor network ($R_1$ and $R_2$), an output capacitor ($C_o$), a bypass capacitor ($C_b$), and a load. The output capacitor has an ESR of $R_{ESR}$. The ESR of the bypass capacitor is typically kept very small for decoupling purposes, and its ESR/ESL-related poles and zeros occur at relatively high frequencies and their effect on stability is not considered, in general [21–23]. A constant current load ($I_L$) is considered to keep the analysis as simple as possible.

### *2.2 Switching stage*

The SC circulation network of this approach is based on the comparison of $V_{in(LDO)}$ with the $V_{min}$ value, as discussed in Section 1.3. The switching frequency is not constant but depends on the capacitor size, the load current, power source voltage, ESR of the SC, and the resistance of the switches. Given the case of constant load current and a fixed supply voltage for analytical purposes, the switches ($S_1$–$S_4$) controller of this regulator is a frequency-independent system for control loop analysis at the steady-state [19, 20].

### *2.3 Averaged small-signal model*

*2.3.1 Circuit averaging technique:* The conventional approach for small-signal modelling of switch-mode DC–DC converters is the state-space averaging technique in which the switching ripple is averaged out and the low frequencies of the control signal are extracted [24]. Nonetheless, this method cannot be used to model the switching converters near or over the switching frequency due to its limitation of low-pass filtering with a cut-off frequency at the switching frequency [25].

Although the SCALDO regulator is a non-linear system and its operating frequency is in the range of millihertz, the state-space averaging technique is not practical for modelling the converter over a wider range of frequencies. In that case, the circuit averaging method, along with classical control, has been identified as the most practical approach for modelling this technique due to its uniqueness and extra low-frequency operation [19].

*2.3.2 Linearisation of the SCALDO regulator:* In this analysis, the first-order model of the SC [26] with an ideal capacitance and its ESR is used to reduce the mathematical complexity. Also, it is assumed that the four switches are identical with equal resistance ($R_{S1} = R_{S2} = R_{S3} = R_{S4} = R_{SW}$). Since two switches always come in series with the ESR of the SC($R_{SC}$) in both charging and discharging modes, an equivalent resistance of the switching network is defined as follows:

$$R_{in} = 2R_{SW} + R_{SC} \tag{3}$$

The transient events of a switching cycle are illustrated in Fig. 3.

Since the output current is a constant and the quiescent current of an LDO regulator is very low, the input current to the LDO regulator ($I_{in(LDO)}$) is a constant at steady-state. Also, the charge balance of the SC is maintained throughout the switching cycles, as mentioned in Section 1.3. The voltage across the SC at the end of the charging mode ($V_{SC(a)}$) is given as per (4), based on Fig. 3*a*

$$V_{SC(a)} = V_{in} - V_{min} - R_{in}I_{in(LDO)} \tag{4}$$

The initial voltage of the SC at the outset of the discharging phase ($V_{SC(b)}$) is the same as (4) since the voltage of a capacitor does not change instantaneously. Therefore, the input voltage of the LDO regulator at the outset of the discharging mode ($V_{in(LDO)\_b}$) is derived in (5), based on Fig. 3*b*

$$V_{in(LDO)\_b} = V_{SC(b)} - R_{in}I_{in(LDO)} = V_{in} - V_{min} - 2R_{in}I_{in(LDO)} \tag{5}$$

Similarly, (6) and (7) are derived from Figs. 3*c* and *d*

$$V_{SC(c)} = V_{min} + R_{in}I_{in(LDO)} \tag{6}$$

$$V_{in(LDO)\_d} = V_{in} - V_{SC(d)} - R_{in}I_{in(LDO)} = V_{in} - V_{min} - 2R_{in}I_{in(LDO)} \tag{7}$$

Based on the above derivations, voltage waveforms are illustrated in Fig. 4. The charging time, the discharging time, and the time taken for a complete switching cycle are denoted as $t_c$, $t_d$, and $T$, respectively, in this diagram. As shown in Fig. 4, the input voltage of the LDO regulator is a sawtooth waveform, and the amplitude of this waveform is defined in (8)

$$V_{\text{in(LDO)\_amp}} = V_{\text{in}} - 2V_{\text{min}} - 2R_{\text{in}}I_{\text{in(LDO)}} \tag{8}$$

The Fourier series of $V_{\text{in(LDO)}}$ for a given switching frequency (where $f = 1/(T/2)$) can be written as (9)

$$V_{\text{in(LDO)}} = \frac{V_{\text{in}}}{2} + \frac{V_{\text{in(LDO)\_amp}}}{\pi}\sin(2\pi\text{ft}) + \frac{V_{\text{in(LDO)\_amp}}}{2\pi}\sin(4\pi\text{ft}) + \frac{V_{\text{in(LDO)\_amp}}}{3\pi}\sin(6\pi\text{ft}) + \ldots \tag{9}$$

At steady-state $t_c = t_d = T/2$, and the average input voltage of the LDO regulator ($V_{\text{in(LDO)\_avg}}$) can be calculated considering the shaded area in Fig. 4 as per (10)

$$V_{\text{in(LDO)\_avg}} = \frac{(V_{\text{in}} - V_{\text{min}} - 2R_{\text{in}}I_{\text{in(LDO)}} + V_{\text{min}})(T/2)}{2(T/2)} = \frac{V_{\text{in}}}{2} - R_{\text{in}}I_{\text{in(LDO)}} \tag{10}$$

The equivalent circuit model of the single-stage SCALDO topology is shown in Fig. 5, based on (10). When the ripple amplitude ($V_{\text{in(LDO)\_amp}}$) is kept very low, the linearity of the model is maintained as the DC bias point is unchanged in the PMOS transistor. This condition is practically achievable for typical applications. As an example, if $V_{\text{min}}$ is set to 5.95 V as the threshold value of the switching controller in a 12–5 V SCALDO regulator (given that $R_{\text{in}} = 0.19$, $I_{\text{in(LDO)}} = 0.1$ A), the peak values of the fundamental component and the second harmonic of $V_{\text{in(LDO)}}$ become 20 and 10 mV, as per (9).

As with any DC–DC converter topology, the disturbances can be due to changes in the input voltage, reference voltage, and load fluctuations. The effect of input voltage variations can be analysed based on the $v_{\text{o(LDO)}}/v_{\text{in(LDO)}}$ transfer function of the LDO regulator, and it is related to the power supply ripple rejection (PSRR). Since the PSRR of a well-designed LDO regulator is very large at low frequencies [27], the switching ripple (sawtooth waveform which has a frequency typically <1 Hz) of the SCALDO regulator is attenuated, and its effect on the output voltage is negligible. Therefore, it can be considered that the stability of this regulator mainly depends on the $v_{\text{o(LDO)}}/v_{\text{ref}}$ transfer function (where $v_{\text{ref}}$ is the reference voltage perturbation) and the load variations.

Consider that the perturbation is applied at the voltage reference for this equivalent circuit model and the resultant change of the small-signal quantities of the input voltage and the input current are $v_{\text{in(LDO)}}$ and $i_{\text{in(LDO)}}$, respectively as defined in (11)

$$V_{\text{in(LDO)\_avg}} + v_{\text{in(LDO)}} = \frac{V_{\text{in}}}{2} - R_{\text{in}}\left(I_{\text{in(LDO)}} + i_{\text{in(LDO)}}\right) \tag{11}$$

From (10) and (11), the AC components can be extracted as per (12)

$$v_{\text{in(LDO)}} = -R_{\text{in}}i_{\text{in(LDO)}} \tag{12}$$

The linear circuit model of the single-stage SCALDO regulator for small signals is built-in Fig. 6, based on the relationship defined in (12).

### 2.4 Open-loop transfer function

The analytical small-signal model of the SCALDO regulator is depicted in Fig. 7. The following assumptions are made to reduce the complexity of the analytical model.

- The terminal resistance of the source and the drain of the PMOS pass device is neglected.
- The source-drain ($C_{\text{DS}}$) parasitic capacitance is assumed to be very small compared to the other two parasitic capacitances, and it is neglected in this model.
- Only the low-frequency (dominant) pole ($\omega_{p1(\text{ea})}$) of the error amplifier is considered.
- The feedback resistors are not accounted for in the calculation of the output impedance ($Z_{\text{o}}$).

Gate, Drain and Source of the PMOS are represented as G, D, and S, respectively in Fig. 7. The dominant parasitic capacitances are the gate-source capacitance ($C_{\text{GS}}$) and the gate-drain capacitance

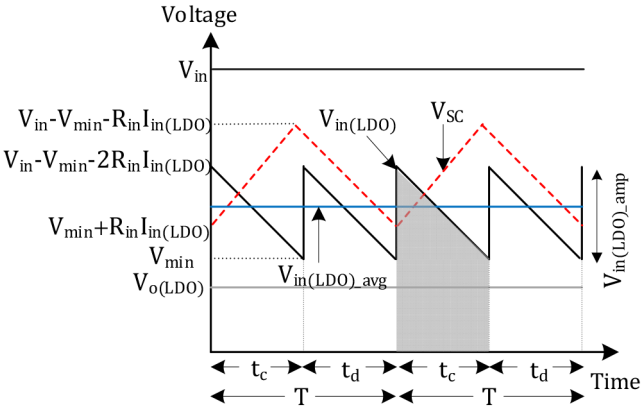



**Fig. 4** *Voltage waveforms of the SCALDO regulator for repeated switching cycles*

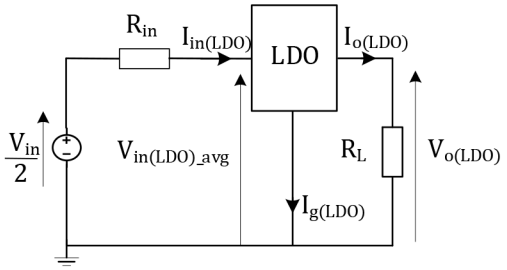



**Fig. 5** *Equivalent circuit model of the SCALDO regulator*

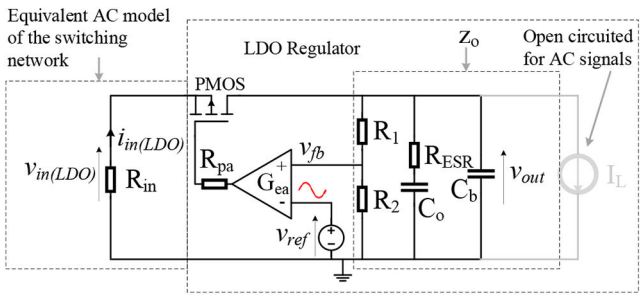



**Fig. 6** *Linear circuit model of the single-stage SCALDO regulator*

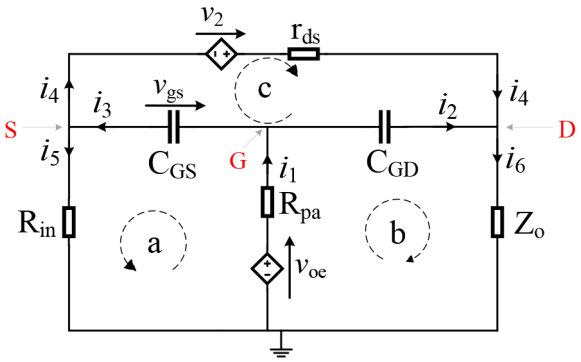



**Fig. 7** *Analytical small-signal model*

**Table 2** Comparison of pole-zero frequencies of the SCALDO regulator with respect to a PMOS LDO regulator

| | | LDO regulator | SCALDO regulator | Remarks |
|---|---|---|---|---|
| DC gain ($A_{DC}$) | | $G_{EA}G_{fb}g_mr_{ds}$ | $G_{EA}G_{fb}g_mr_{ds}$ | |
| Zeros | $\omega_{z1}$ | $-\frac{1}{C_oR_{ESR}}$ | $-\frac{1}{C_oR_{ESR}}$ | $\omega_{z1(LDO)} = \omega_{z1(SCALDO)}$ |
| | $\omega_{z2}$ | not defined for LDO regulator | $\frac{g_mr_{ds}}{(C_{GS}R_{in} + C_{GD}(r_{ds}(1 + g_mR_{in}) + R_{in}))}$ | right-hand-plane zero |
| | $\omega_{z3}$ | not defined for LDO regulator | $-\frac{1}{C_{GS}}\left(\frac{1}{R_{in}} + \frac{1}{r_{ds}} + g_m\right) - \frac{1}{C_{GD}r_{ds}}$ | |
| Poles | $\omega_{p1}$ | $-\frac{1}{C_o(R_{ESR} + r_{ds})}$ | $-\frac{1}{C_o(R_{ESR} + r_{ds})(1 + g_mR_{in})}$ | $\omega_{p1(LDO)} > \omega_{p1(SCALDO)}$ Since: $\frac{1}{(1 + g_mR_{in})} < 1$ |
| | $\omega_{p2}$ | $-\frac{1}{C_{GS}R_{pa} + C_{GD}R_{pa}(1 + R_{ESR}g_m)}$ | $-\frac{1 + g_mR_{in}}{C_{GS}R_{pa} + C_{GD}R_{pa}(1 + g_mR_{in} + R_{ESR}g_m)}$ | $\omega_{p2(LDO)} < \omega_{p2(SCALDO)}$ when $C_{GD} << C_{GS}$ |
| | $\omega_{p3}$ | $-\frac{1}{(R_{ESR}//r_{ds})C_b}$ | $-\frac{1}{(R_{ESR}//r_{ds})C_b}$ | $\omega_{p3(LDO)} = \omega_{p3(SCALDO)}$ |
| | $\omega_{p4}$ | Not defined for LDO regulator | $-\frac{1 + g_mR_{in}}{C_{GS}R_{in}} - \frac{1}{C_{GD}R_{in}}$ | |
| | $\omega_{p5}$ | $-\omega_{p1(EA)}$ | $-\omega_{p1(EA)}$ | $\omega_{p5(LDO)} = \omega_{p5(SCALDO)}$ |
| Unity gain frequency | | $UGF_{(LDO)}$ | $UGF_{(SCALDO)}$ | when $C_{GD} \approx 0$: $UGF_{(LDO)} = UGF_{(SCALDO)}$ |

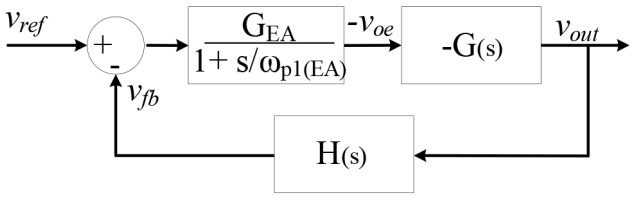



**Fig. 8** *Voltage control loop*

($C_{GD}$). Also, $r_{ds}$ is the output resistance, $v_{gs}$ is the gate-source small-signal voltage, $r_G$ is the gate terminal resistance, and $g_m$ is the transconductance of the PMOS. The small-signal voltage gain of this error amplifier model ($G_{ea}$) is defined in (13) as

$$v_{oe} = \frac{G_{EA}(v_{fb} - v_{ref})}{(1 + s/\omega_{p1(EA)})} \tag{13}$$

where $v_{oe}$, $v_{fb}$ and $v_{ref}$ are the small-signal quantities of the output voltage of the error amplifier, feedback voltage and the reference voltage, respectively. $G_{EA}$ is the gain, $\omega_{p1(EA)}$ is the low-frequency pole and $R_o$ is the output resistance. $R_{pa}$ is the coupled resistance of the error-amplifier output and the gate of the PMOS, as defined in (16)

$$v_2 = -g_mv_{gs}r_{ds} \tag{14}$$

$$Z_o \simeq \left(R_{ESR} + \frac{1}{sC_o}\right)//\left(\frac{1}{sC_b}\right) \tag{15}$$

$$R_{pa} = r_G + R_o \tag{16}$$

One can apply Kirchhoff's Voltage Law (KVL) to loops a, b, and c and Kirchhoff's Current Law (KCL) to nodes D, G, S in Fig. 7 and solve the simultaneous equations to obtain the relationship ($v_{out}/v_{oe}$) in the Laplace domain. This relationship is known as the SCALDO plant transfer function ($G(s) = n(s)/d(s)$) which is split as the numerator ($n(s)$) and the denominator ($d(s)$) in (17) and (18), respectively. For convenience, the impedance of $C_{GS}$ and the impedance of $C_{GD}$ are denoted as $Z_{GS}$ and $Z_{GD}$ in the $s$-domain, respectively. Based on the assumption that $r_{ds}$ is much greater than $R_{in}$ and $R_{ESR}$, the numerator and the denominator can be further simplified. If the poles and zeros are assumed to be real numbers, and they are widely separated, $G(s)$ can be approximated as (19). The angular frequencies of the zeros and poles of $G(s)$ are approximated and listed in Table 2.

### 2.5 Voltage control loop

The voltage control loop is illustrated in Fig. 8 using the error amplifier first-order model and the SCALDO plant transfer function. In this control loop, $v_{ref}$ is considered as a positive term. Therefore, the differential output voltage of the error amplifier is inverted ($-v_{oe}$) according to (13). Also, $G(s)$ is inverted to rectify this effect. The feedback network transfer function ($H(s)$) is the feedback gain of the resistor network ($G_{fb} = R_2/(R_1 + R_2)$). As a result, the open-loop transfer function ($T(s)$) of the single-stage SCALDO regulator is derived in (20). Also, the DC gain of this open-loop transfer function is given in (21)

$$n(s) = z_o[r_{ds}(Z_{GS}(g_m(Z_{GD} - R_{in}) - 1)) - R_{in}(Z_{GS} + Z_{GD})] \tag{17}$$

$$\begin{aligned} d(s) = {} & r_{ds}\big(R_{pa}(Z_o + Z_{GD}) + (Z_{GS} + R_{in})\big(R_{pa} + Z_o + Z_{GD}\big)\big) \\ & + r_{ds}g_mZ_{GS}\big(R_{pa}(Z_o + R_{in}) + R_{in}(Z_o + Z_{GD})\big) \\ & + R_{pa}(Z_{GS} + Z_{GD})(Z_o + R_{in}) \\ & + Z_{GS}Z_o(Z_{GD} + R_{in}) + Z_{GD}R_{in}(Z_o + Z_{GS}) \end{aligned} \tag{18}$$

$$G(s) \simeq \frac{-g_mr_{ds}(1 + (s/\omega_{z1}))(1 + (s/\omega_{z2}))(1 + (s/\omega_{z3}))}{(1 + (s/\omega_{p1}))(1 + (s/\omega_{p2}))(1 + (s/\omega_{p3}))(1 + (s/\omega_{p4}))} \tag{19}$$

$$\begin{aligned} T(s) &= \frac{G_{EA}}{(1 + s/\omega_{p1(EA)})}(-G(s))H(s) \\ &= \frac{G_{EA}G_{fb}g_mr_{ds}(1 + s/\omega_{z1})(1 + s/\omega_{z2})(1 + s/\omega_{z3})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})(1 + s/\omega_{p3})(1 + s/\omega_{p4})(1 + s/\omega_{p1(EA)})} \end{aligned} \tag{20}$$

$$A_{DC} = G_{EA}G_{fb}g_mr_{ds} \tag{21}$$

### 2.6 Analysis of pole-zero frequencies of the SCALDO regulator compared to a standalone LDO regulator

Table 2 lists the poles and zeros of this regulator compared to a PMOS transistor-based LDO regulator [21–23]. This table shows that both regulators share the same quantities for the third pole, DC

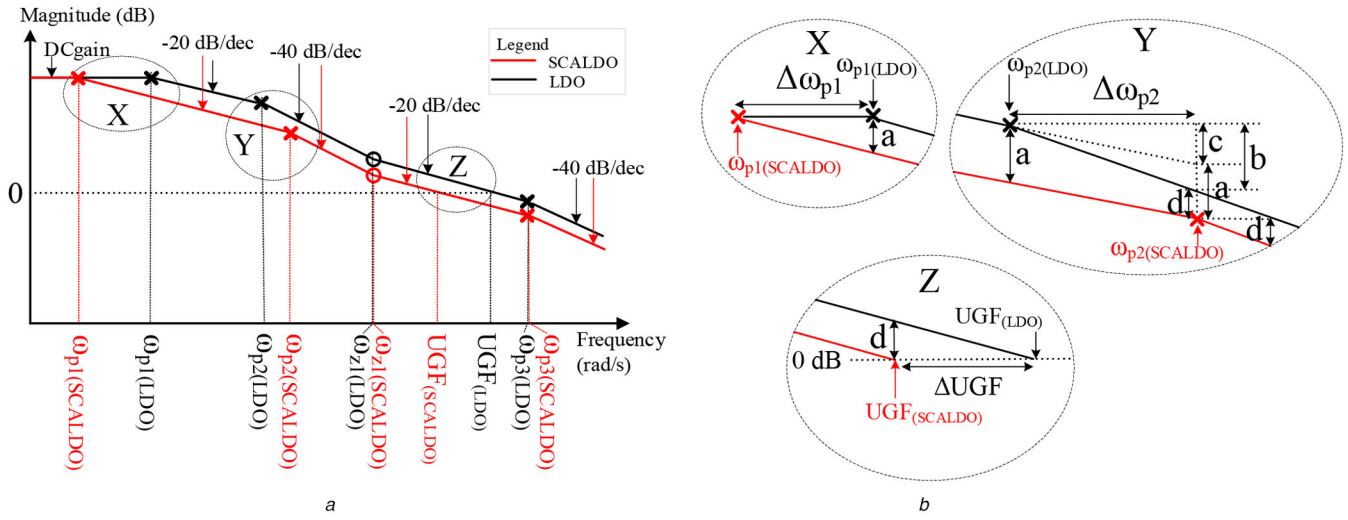



**Fig. 9** *Linear approximation of magnitude plots of SCALDO regulator and LDO regulator*
***(a)*** Comparison of pole-zero locations, ***(b)*** Zoomed areas used to obtain the geometric relationships

gain, and the first zero. Also, the dominant pole of the error amplifier is identical in both designs [19]. Even so, this pole depends on the topology of the error amplifier [28]. In addition, the SCALDO regulator is composed of two high-frequency zeros and one high-frequency pole, and they are based on the parameters of the SC switching network. One high-frequency zero is a right-hand-plane zero. Although the first pole of this regulator falls lower than the first pole of the LDO regulator the second pole could be higher in value when the gate-drain parasitic capacitance is small.

The linear asymptotic approximations of magnitude plots of the LDO and SCALDO regulators are shown in Fig. 9 (For convenience, the subscripts LDO and SCALDO are used in this diagram for poles, zeros, and UGF). Also, the generic method of distribution of poles and zeros of the PMOS based LDO regulator is used to construct this linear asymptotic where $\omega_{p1} < \omega_{p2} < \omega_{z1} < \text{UGF} < \omega_{p3}$ [23]. The high-frequency poles and zeros are neglected to simplify the analysis. The geometric relationships are zoomed and displayed in Fig. 9*b* as X, Y, and Z. Using these geometric relationships, the following equations can be derived:

$$\Delta\omega_{p1} = \log_{10}\left(\frac{\omega_{p1(\text{LDO})}}{\omega_{p1(\text{SCALDO})}}\right) \tag{22}$$

$$\Delta\omega_{p2} = \log_{10}\left(\frac{\omega_{p2(\text{SCALDO})}}{\omega_{p2(\text{LDO})}}\right) \tag{23}$$

$$d = a + c - b = 20\Delta\omega_{p1} + 20\Delta\omega_{p2} - 40\Delta\omega_{p2} \tag{24}$$

$$\Delta\text{UGF} = \log_{10}\left(\frac{\text{UGF}_{(\text{LDO})}}{\text{UGF}_{(\text{SCALDO})}}\right) = \frac{d}{20} = \Delta\omega_{p1} - \Delta\omega_{p2} \tag{25}$$

$$\Delta\text{UGF} = \log_{10}\left(\frac{\omega_{p1(\text{LDO})}\omega_{p2(\text{LDO})}}{\omega_{p1(\text{SCALDO})}\omega_{p2(\text{SCALDO})}}\right) \tag{26}$$

If $C_{\text{GD}} \approx 0$, the right-hand side of (26) can be approximated to (27) using the frequencies defined in Table 2

$$\log_{10}\left(\frac{\dfrac{1}{C_{\text{o}}(R_{\text{ESR}} + r_{\text{ds}})C_{\text{gs}}R_{\text{pa}}}}{\dfrac{(1 + g_{\text{m}}R_{\text{in}})}{C_{\text{o}}(R_{\text{ESR}} + r_{\text{ds}})(1 + g_{\text{m}}R_{\text{in}})C_{\text{gs}}R_{\text{pa}}}}\right) = 0 \tag{27}$$

Therefore, using (26) and (27), the following relationship can be obtained:

$$\text{UGF}_{(\text{LDO})} = \text{UGF}_{(\text{SCALDO})} \tag{28}$$

Equation (28) shows that the gain crossover frequencies of SCALDO and the LDO regulators are the same when $C_{\text{GD}} \approx 0$.

### 2.7 Frequency compensation techniques

The five poles ($\omega_{p1}$-to-$\omega_{p4}$ and $\omega_{p1(\text{EA})}$) together with the right-half-plane zero ($\omega_{z2}$) cause a phase lag in the open-loop transfer function of the SCALDO regulator. Although, a higher value of the unity gain frequency (UGF) gives a faster load transient response, a compromise is made to keep the phase margin at least 45° for better stability. Since $\omega_{p1}$ and $\omega_{p2}$ occur at relatively low frequencies, they can contribute to a maximum of −180° phase shift at UGF. The use of multi-stage error amplifier topology can shift $\omega_{p1(\text{ea})}$ further away from UGF to reduce the phase lag due to the error amplifier. The selection of the optimal value for the bypass capacitor ($C_b$) might also reduce the phase lag of $\omega_{p3}$. Similarly, if the equivalent resistance of the input switching network is reduced, the phase lag due to $\omega_{p5}$ and $\omega_{z2}$ can be reduced. Since $\omega_{z1}$ is the only zero which contributes a phase lead, this regulator should be designed carefully to provide a sufficient phase margin with the aid of the capacitance and the ESR of the output capacitor [20]. For a given output capacitance, the selection of a stable range of its ESR is critical to stabilising the control loop. Typically, the phase margin of a regulator is kept at no <30°; thus, the ESR of the output capacitor can be selected to satisfy the same criteria in the SCALDO regulator too [29]. Other phase margin improvement techniques such as feedforward compensation are also possible in this regulator. Nevertheless, any discussion on these approaches is beyond the scope of this paper.

## 3 Verification

To verify the performance of the technique in terms of its stability, calculated and simulated results are compared with the experimental results in this section. For this process, a 12–5 V discrete prototype was built, including the LDO stage, as shown in Fig. 10. In this prototype, the switches are controlled using an ATtiny261 Microcontroller.

*Calculations*: In this section, the stable range of the output capacitor ESR is calculated to provide a sufficient phase margin using the open-loop transfer function shown in (20) and the circuit component values given in Table 3. The extreme values of the open-loop poles, zeros, and phase margins are also determined for different values of the load current. MATLAB transfer function tools were used for this purpose.

*Simulations*: The open-loop response is simulated, considering the effective resistance of the SC switching stage and load current as variables. The simulated load transient response is estimated to

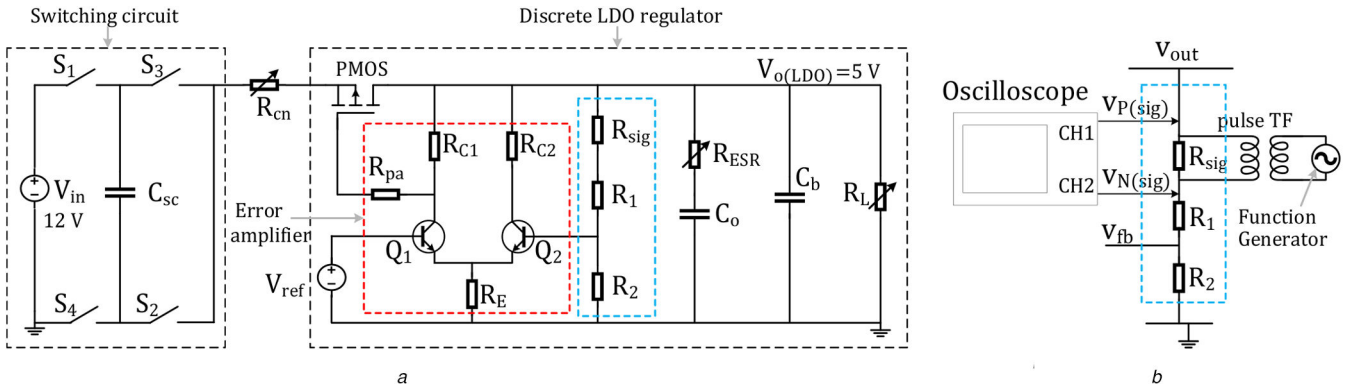



**Fig. 10** *Circuits used to compare the stability performance of the SCALDO technique*
***(a)*** Circuit diagram of the discrete component-based 12–5 V SCALDO regulator, ***(b)*** Signal-injection via an output feedback loop of the LDO stage

**Table 3** Circuit parameters of the discrete SCALDO regulator

| Component | Properties | Range of values of critical parameters |
|---|---|---|
| PMOS (Si2343CDS) | Threshold voltage ($V_{th}$) = -2.38 V | $V_{th}$ = −1.2 to −2.5 V |
| | Channel length modulation ($\lambda$) = 0.34 $V^{-1}$ | $\lambda$ = 0.272 to 0.408 $V^{-1}$ |
| | Gain = 3.15 $AV^{-2}$ | $C_{GS}$ = 880 to 1320 pF |
| | $r_S$ = 0.02 Ω, $r_D$ = 0.013 Ω, $r_G$ = 5 Ω | |
| | $C_{GS}$ = 1100 pF, $C_{GD}$ = 500 pF, $C_{DS}$ = 50 pF | |
| $Q_1$, $Q_2$ (BC546B) | $G_{EA}$ = 25.1 dB | $G_{EA}$ = 23.16 to 26.8 dB |
| $R_{C1}$ = 3.3 kΩ (1%) | $\omega_{p1(EA)}$ = 536 kHz | |
| $R_{C2}$ = 3.3 kΩ (1%) | | |
| $R_E$ = 1.5 kΩ (1%) | | |
| $R_{pa}$ | 18 kΩ (1%) | |
| $C_{SC}$ | $C_{SC}$ = 3.3 F/8.1 V (±5%), ESR ($R_{SC}$) = 90 mΩ | |
| $S_1$, $S_2$, $S_3$, $S_4$ (TLP3543) | on-resistance ($R_{SW}$) = 50 mΩ (each) | |
| $R_1$ and $R_2$ | 2.2 kΩ (±0.1%) | |
| $V_{ref}$ (AD780) | Maximum output voltage drift = 1 mV | |
| | Quiescent current < 1 mA | |
| $R_{sig}$ | 50 Ω (±0.1%) | |
| $C_o$ | 10 µF (±10%) | 9 to 11 µF |
| | $R_{ESR}$ = 400 mΩ at 1 kHz | |
| $R_{ESR}$ | 1 Ω (±0.1%) | 1 to 2 Ω |
| $C_b$ | 1 µF (±10%) | |
| | ESR is negligible from 10 Hz to 1 MHz | |
| $R_{cn}$ | Discrete: 100, 200, 300 mΩ | |

visualise the stability of the regulator due to the disturbances of the load.

*Experiments*: The open-loop response was practically measured using the signal injection method [30, 31] at different values of output current. Phase margins were observed for both output capacitor ESR and the equivalent series resistance of the switching network to determine their effect on stability. The step-load test was conducted and compared with the simulated results. The switching ripple and its frequency spectrum were also analysed to demonstrate the minimal influence of the SC switching network-related disturbances on the stability.

The circuit diagram of the prototype is shown in Fig. 10*a* with a maximum load current of 200 mA, and the theoretical ETEE of 83.3%. The properties of the circuit components are listed in Table 3. A control (variable) resistor ($R_{cn}$) was used to represent the equivalent resistance of the switching network since the resistive component due to the switches, and the ESR of the SC is fixed. Fig. 10*b* demonstrates the experimental setup of the open-loop measurements (signal injection method), and more details are given in Section 3.3.1.

### *3.1 Calculated results*

*3.1.1 Determination of the stable ESR of the output capacitor:* Based on SCALDO open-loop transfer function shown in (20) and the numerical values of circuit components, the graph illustrated in Fig. 11 was developed to determine the stable range of output capacitor ESR, guided by the methods in [23], with a minimum phase margin of 45°. As the stable ESR value falls within 0.6 and 5 Ω for this case, an external 1 Ω resistor is connected in series with the output ceramic capacitor ($C_o$) to make the equivalent ESR ($R_{ESR}$) 1.4 Ω, which falls within the stability margins of Fig. 11.

*3.1.2 Worst-case estimation of phase margin:* With a view of estimating the worst-case stability performance of the technique, six dominant parameters were identified from the open-loop transfer function defined in (20), and their range of values are listed in Table 3 for room temperature, based on the tolerance of the circuit components. Using the corner values of these critical parameters, two extreme cases, along with the nominal phase margin, are shown in Fig. 12. The corner values of the poles and zeros are listed in Table 4.

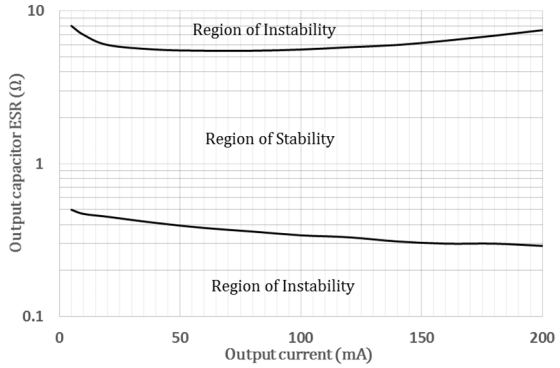



**Fig. 11** *Stable range of the ESR of the output capacitor for the SCALDO prototype*

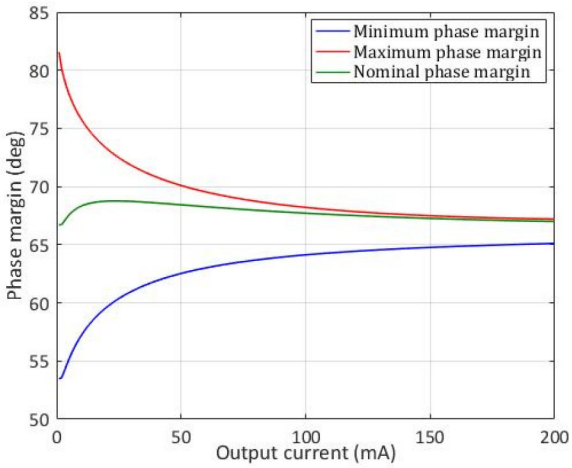



**Fig. 12** *Phase margin variation against the load current*

**Table 4** Corner values of the frequencies of poles and zeros of the SCALDO regulator

| Pole/zero | Load current | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 5 mA | | 50 mA | | 100 mA | | 200 mA | |
| | Min | Max | Min | Max | Min | Max | Min | Max |
| $A_{DC}$ (dB) | 56.37 | 64.90 | 46.37 | 54.90 | 43.39 | 51.89 | 40.35 | 48.88 |
| $\omega_{z1}$, kHz | 7.23 | 17.68 | 7.23 | 17.68 | 7.23 | 17.68 | 7.23 | 17.68 |
| $\omega_{z2}$, MHz | 47.53 | 78.08 | 126.0 | 224.4 | 135.6 | 299.4 | 156.2 | 390.0 |
| $\omega_{z3}$, MHz | 268.2 | 994.7 | 319.9 | 1094.7 | 353.8 | 1160.3 | 404.9 | 1259.4 |
| $\omega_{p1}$, Hz | 15.03 | 29.83 | 97.77 | 213.42 | 159.45 | 360.34 | 249.13 | 583.73 |
| $\omega_{p2}$, kHz | 5.041 | 7.965 | 5.709 | 10.12 | 6.066 | 11.186 | 6.531 | 12.497 |
| $\omega_{p3}$, kHz | 91.57 | 214.84 | 107.45 | 245.29 | 117.10 | 264.38 | 130.78 | 292.15 |
| $\omega_{p4}$, GHz | 0.8582 | 2.8551 | 0.9049 | 2.9453 | 0.9331 | 2.999 | 0.9732 | 3.0772 |
| $\omega_{p1(EA)}$, kHz | 384.5 | 792.3 | 384.5 | 792.3 | 384.5 | 792.3 | 384.5 | 792.3 |

### *3.2 Simulated results*

The simulation model based on MATLAB Simulink is shown in Fig. 13. The switching control algorithm was developed with the aid of the logic blocks.

*3.2.1 Open-loop response:* For the estimation of open-loop response using the Control System Toolbox in MATLAB, a perturbation is fed at the voltage reference, and the control loop is broken at the feedback resistor network. The simulated frequency response of the SCALDO regulator (for $R_{in} = 0.19\ \Omega$) is depicted in Fig. 14. Conversely, the open-loop frequency response of the LDO regulator is obtained in Fig. 15 by using the same simulation model and running directly from a 6 V ideal voltage source without the SCALDO switching circuit. The occurrence of poles and zeros of these two graphs match the derived equations shown in Table 2.

The frequencies of the poles and zeros of the open-loop transfer functions of the two regulators are further compared against the load current and switching network resistance in Table 5. These results show that the simulated values fall within the calculated corner values of the corresponding poles and zeros of the SCALDO regulator. It is interesting to observe that, in Table 5, the frequencies of the high-frequency pole ($\omega_{p4}$) and two zeros ($\omega_{z2}$ and $\omega_{z3}$) decrease as the resistance of the switching network is increased for any given output current. Also, the low-frequency pole $\omega_{p1}$ decreases as the value of $R_{in}$ goes high and it is always lower than the corresponding pole of the LDO regulator. Conversely, the frequency of the second low-frequency pole $\omega_{p2}$ rises when $R_{in}$ is increased, and it is slightly higher than the $\omega_{p2}$ of the LDO regulator. These results match the theoretical comparison made in Table 2.

The output capacitor ESR dependant zero ($\omega_{z1}$) and the error-amplifier dominant pole are independent of the resistive component of the switching network and values are similar for both SCALDO and LDO regulators. Some discrepancies of $\omega_{p3}$ are

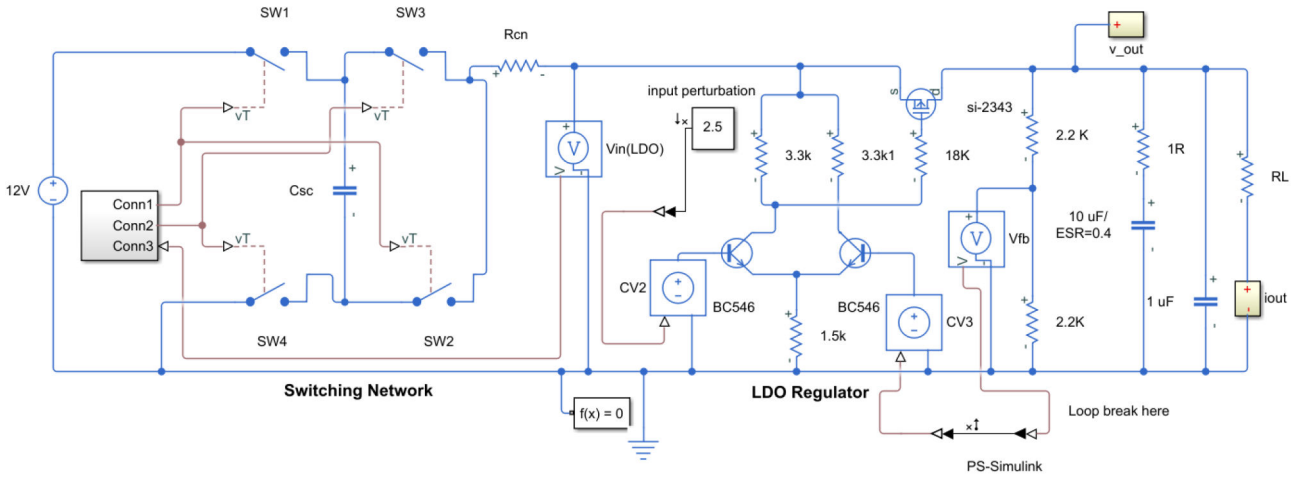



**Fig. 13** *SIMULINK simulation model of the SCALDO regulator*

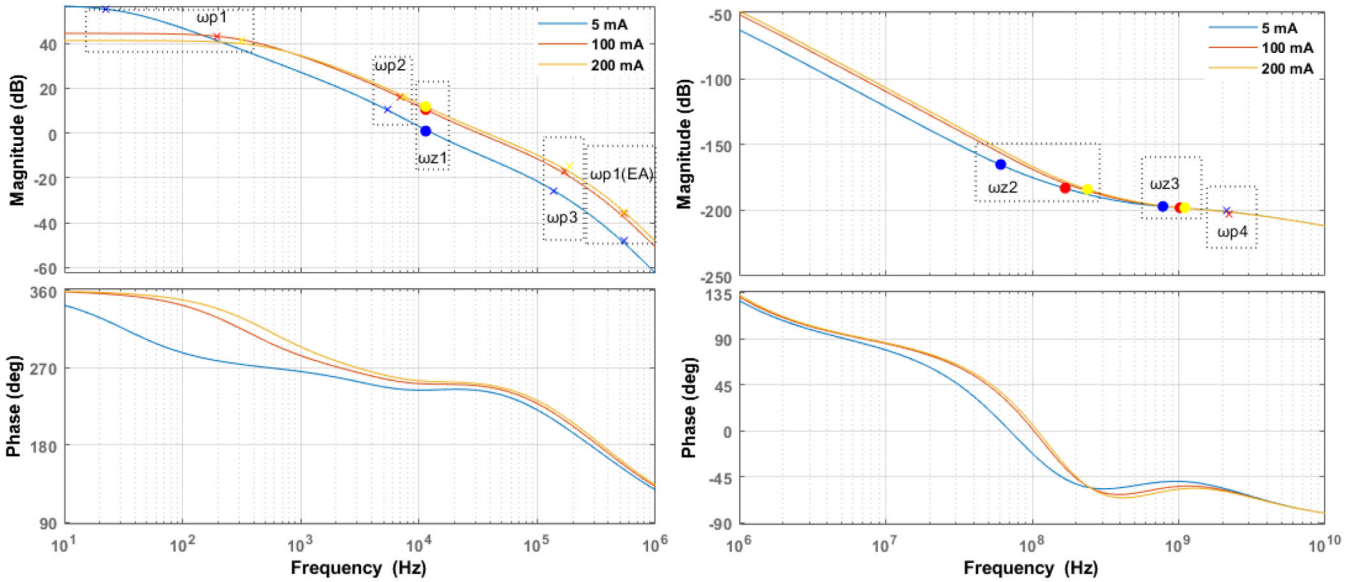



**Fig. 14** *Simulated phase and gain plots of the SCALDO regulator*
***(a)*** 10 Hz–1 MHz, ***(b)*** 1 MHz–10 GHz

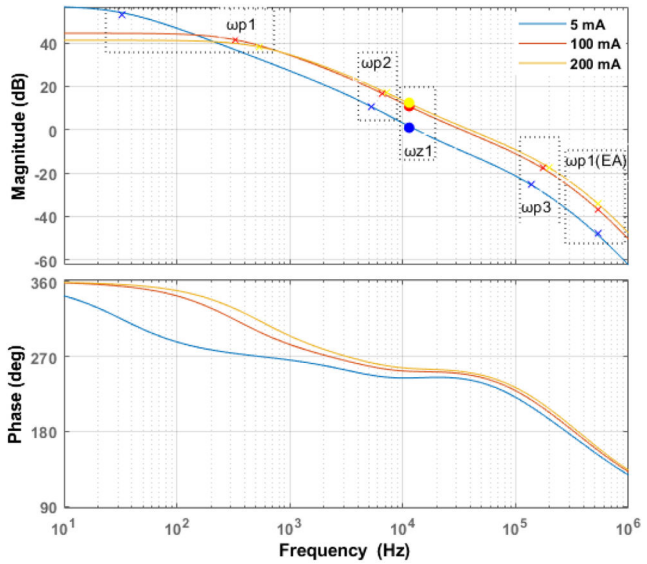



**Fig. 15** *Simulated phase and gain plots of the LDO regulator*

visible in the simulated results compared to the theoretical values since the $R_{in}$ parameter is neglected when simplifying (19) in the theoretical SCALDO model. The effect on the phase margin due to $R_{in}$ is also minimal as the presence of the $R_{in}$ dependant pole, and two zeros, occur well beyond the UGF and the net-zero effect of $\omega_{p1}$ and $\omega_{p2}$. Also, the UGF of the SCALDO regulator decreases when $R_{in}$ is raised and increases when the load current is raised. The UGFs of two regulators at different load currents are very close, as approximated in Section 2.6. Based on these verifications, the simulated results are in very close agreement with the theoretical derivations.

*3.2.2 Load-transient response:* The load transient response is simulated by varying the output capacitor ESR. The selected ESR values for this test fall both inside and outside the stable region, according to the curves shown in Fig. 11. The load current was changed from 5 to 200 mA at a fast slew rate, and the transient response is shown in Fig. 16. As depicted in Figs. 16*a* and *d*, it is evident that the output voltage suffers from ringing when the ESR is out of the stable range. In contrast, the fastest settling time and lowest overshoot for the rising edge of the load current are observed when the output capacitor ESR is 1.4 Ω. These results further indicate that the output capacitor ESR should be within a stable region for a better load transient response.

**Table 5** Simulated frequency values of poles and zeros compared to the resistance parameter of the switching network

| Pole/zero | Load current = 5 mA | | | | Load current = 100 mA | | | | Load current = 200 mA | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LDO only | SCALDO equivalent resistance of the switching network, Ω | | | LDO only | SCALDO equivalent resistance of the switching network, Ω | | | LDO only | SCALDO equivalent resistance of the switching network, Ω | | |
| | | 0.19 | 0.29 | 0.49 | | 0.19 | 0.29 | 0.49 | | 0.19 | 0.29 | 0.49 |
| $A_{DC}$, dB | 56.98 | 57 | 57 | 57 | 44.46 | 44.4 | 44.4 | 44.4 | 41.23 | 41.2 | 41.2 | 41.2 |
| $\omega_{z1}$, kHz | 11.37 | 11.4 | 11.4 | 11.4 | 11.37 | 11.4 | 11.4 | 11.4 | 11.37 | 11.4 | 11.4 | 11.4 |
| $\omega_{z2}$, MHz | N/A | 61.2 | 58.2 | 51.37 | N/A | 189.6 | 168.59 | 140.5 | N/A | 239.1 | 208.25 | 168.75 |
| $\omega_{z3}$, MHz | N/A | 781.5 | 556.99 | 320.74 | N/A | 1018 | 775.43 | 564.3 | N/A | 1132 | 879.6 | 656.57 |
| $\omega_{p1}$, Hz | 32.48 | 22.34 | 22.01 | 21.10 | 330.58 | 196.0 | 188.45 | 175.25 | 530.92 | 317.22 | 304.0 | 280.99 |
| $\omega_{p2}$, kHz | 5.26 | 5.38 | 5.44 | 5.61 | 6.62 | 6.86 | 7.00 | 7.29 | 7.178 | 7.42 | 7.58 | 7.89 |
| $\omega_{p3}$, kHz | 136.06 | 135.5 | 135.3 | 135.18 | 175.44 | 168.5 | 167.33 | 165.18 | 200.14 | 186.98 | 184.56 | 180.25 |
| $\omega_{p4}$, GHz | N/A | 2.1081 | 1.4656 | 0.77568 | N/A | 2.216 | 1.573 | 1.025 | N/A | 2.281 | 1.638 | 1.089 |
| $\omega_{p1(EA)}$, kHz | 540 | 536 | 536 | 536 | 540 | 536 | 536 | 536 | 540 | 535 | 536 | 536 |
| UGF, kHz | 13.02 | 12.91 | 12.84 | 12.73 | 32.78 | 31.43 | 31.51 | 30.39 | 38.83 | 36.92 | 35.97 | 34.38 |
| Phase margin, deg | 64.3 | 64.5 | 64.7 | 65.4 | 69.3 | 68.36 | 68.69 | 69.36 | 70.5 | 70.2 | 70.0 | 69.6 |

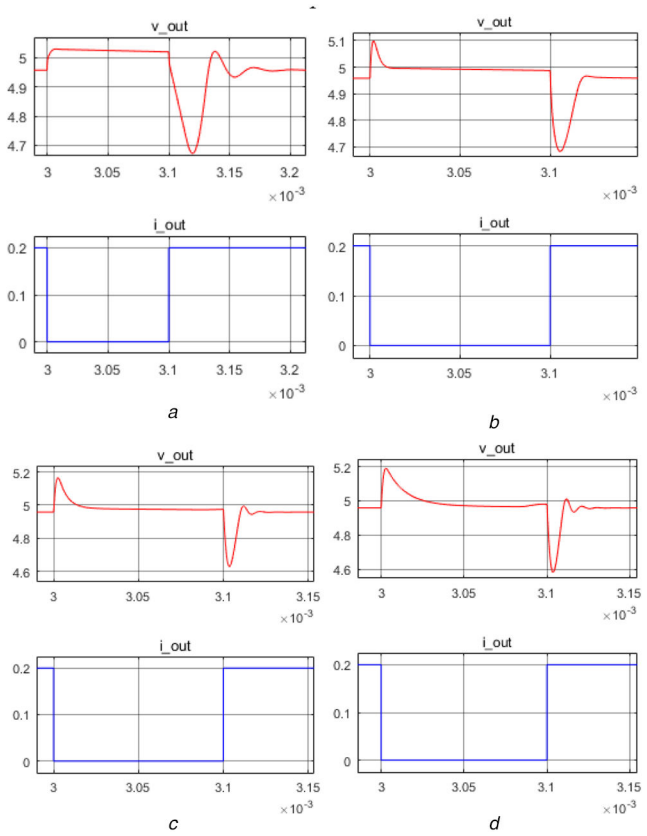



**Fig. 16** *Simulated results of the step load test compared to the output capacitor ESR*
***(a)*** 0.4 Ω, ***(b)*** 1.4 Ω, ***(c)*** 5.4 Ω, ***(d)*** 10.4 Ω. (The time axis: seconds (s) and a single segment: 50 µs)

### 3.3 Test bench results

The experimental setup used to observe the stability of the 12–5 V SCALDO regulator is shown in Fig. 17.

*3.3.1 Open-loop response:* The open-loop frequency response was estimated by feeding small sinusoidal signals to the $R_{sig}$ resistor (see Fig. 10*b*) [30, 31]. The value of $R_{sig}$ was kept small compared to the feedback resistors ($R_1$ and $R_2$) to minimise its influence on output voltage drifts. A pulse transformer was used to inject the perturbations, and the amplitude of this signal was kept below 50 mV to avoid any large-signal disturbances. The frequency range of the injected signal was kept within 100 Hz to 1 MHz, based on the limitations of the measuring instruments. Nevertheless, the frequencies of the dominant poles and the output capacitor ESR dependant zero occur within this frequency band of interest. The measured open-loop gain and phase plots are displayed in Fig. 18.

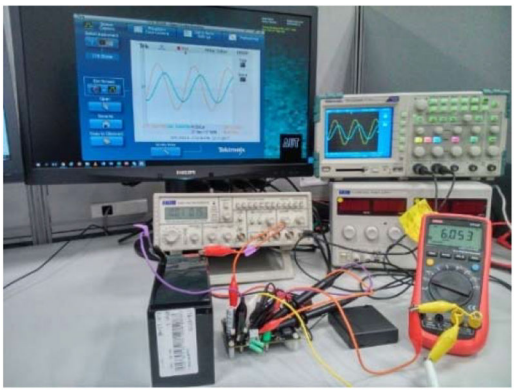
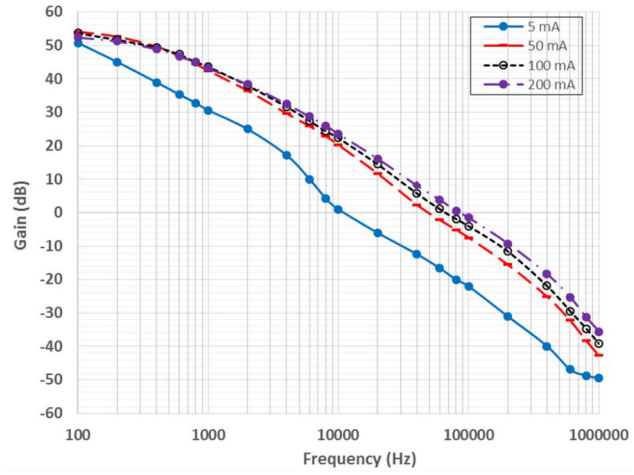


**Fig. 17** *Test setup used for open-loop measurement and step load tests*

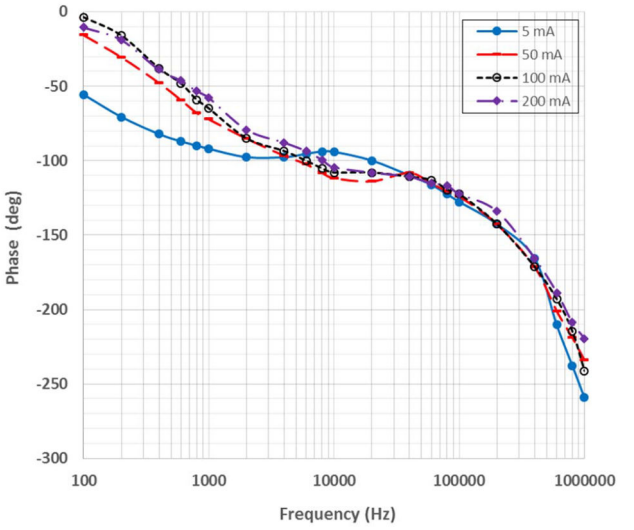
Table 6 summarises the pole-zero frequencies, UGFs and the phase margins derived from the experimental open-loop frequency response curves. This table shows that the DC gain decreases as the load current increases, and this pattern matches the relationship defined in (21) as $r_{ds}$ of the pass device is inversely proportional to the MOSFET output current (the load current of the SCALDO regulator for this case) [21]. The frequency of $\omega_{z1}$ is slightly deviated from its calculated and simulated value (11 kHz) due to the frequency dependence of the ESR and capacitance of the multilayer chip ceramic capacitor used in this prototype. The frequencies of $\omega_{p1}$ and $\omega_{p2}$ are within the calculated margins, and their frequencies increase with the load current. Similarly, $\omega_{p3}$ and $\omega_{p1(EA)}$ fall within the expected corner margins of the calculated and simulated results. Other high-frequency poles and zeros are not visible in the frequency band of measurement.

*3.3.2 Stability margins compared to the output capacitor ESR:* Table 7 shows the phase margin against the ESR value variation, at different output load currents. As can be seen, these values match the calculated results shown in Fig. 11.

In addition to the phase margin measurements, the load-transient response was observed for different values of $R_{ESR}$, and the results are shown in Fig. 19.




*a*




*b*

**Fig. 18** *Measured frequency response*
***(a)*** Open-loop gain plot, ***(b)*** Open-loop phase plot

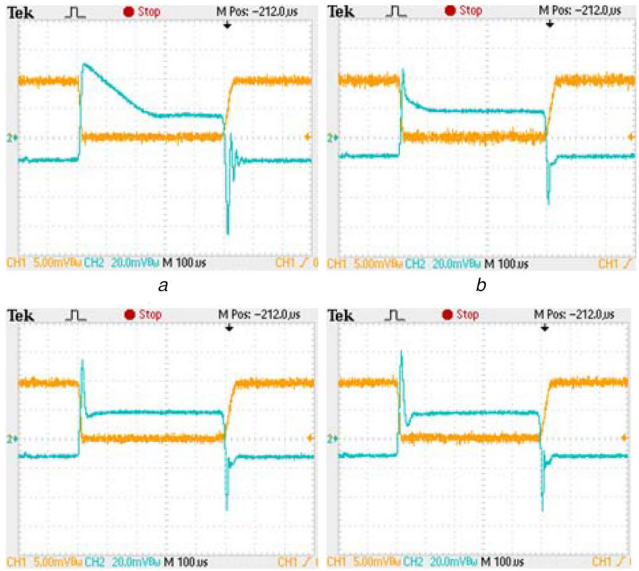
**Table 6** Experimental values of open-loop poles and zeros extracted from phase and gain plots

| Pole/zero | Frequency | | | |
|---|---|---|---|---|
| | $I_{out}$ = 5 mA | $I_{out}$ = 50 mA | $I_{out}$ = 100 mA | $I_{out}$ = 200 mA |
| $A_{DC}$, dB | >50.75 | 54.05 | 53.70 | 52.39 |
| $\omega_{z1}$, kHz | 10 | 20 | 20 | 20 |
| $\omega_{p1}$, Hz | <100 | 200 | 250 | 300 |
| $\omega_{p2}$, kHz | 5 | 8 | 9 | 10 |
| $\omega_{p3}$, kHz | 100 | 200 | 200 | 200 |
| $\omega_{p1(EA)}$, kHz | 400 | 400 | 400 | 400 |
| UGF, kHz | 10 | 50 | 70 | 90 |
| Phase margin, deg | 86 | 68 | 65 | 62 |

This test was done by placing a small shunt resistor (50 mΩ) at the ground return path of the load current and by changing the load current from 5 to 200 mA at a slew rate of 10 mA/μs. Fig. 19*b* shows that there is a minimum overshoot of 32 mV and undershoot of 28 mV in terms of the output voltage, with no oscillations for the step load change when $R_{ESR}$ is 1.4 Ω. Even though Fig. 19*c* gives the fastest settling time for the falling edge, the overshoot and undershoot is higher compared to Fig. 19*b*. On the other hand, when the ESR drops too low ($R_{ESR}$ = 0.4 Ω), severe oscillations are visible before the output voltage settles down and the longest settling time is visible, compared to other cases. Similarly, when the ESR is increased too high ($R_{ESR}$ = 10 Ω), the recorded value of

**Table 7** Summary of phase margins obtained at different ESR values of the output capacitor

| output capacitor ESR, Ω | Phase margin, deg | | | |
|---|---|---|---|---|
| | $I_{out}$ = 50 mA | $I_{out}$ = 100 mA | $I_{out}$ = 150 mA | $I_{out}$ = 200 mA |
| 0.4 | 33 | 25 | 23 | 24 |
| 1.4 | 68 | 65 | 64 | 62 |
| 5.4 | 48 | 48 | 50 | 50 |
| 10.4 | 24 | 28 | 31 | 30 |




*a* *b* *c* *d*

**Fig. 19** *CH1 (DC coupling with 1 mV→20 mA): Load current CH2 (AC coupling): Output voltage Experimental results of the step load test compared to the output capacitor ESR*
***(a)*** 0.4 Ω, ***(b)*** 1.4 Ω, ***(c)*** 5.4 Ω, ***(d)*** 10 Ω

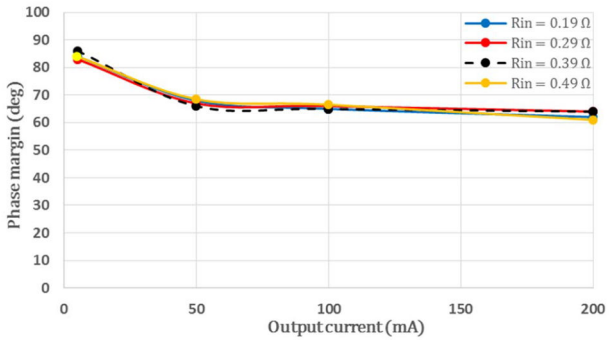



**Fig. 20** *Measured phase margin values compared to the resistive component of the switching network*

the overshoot is 44 mV, and this leads to the more pronounced ringing of the loop in the rising edge. In summary, the best performance is achieved when $R_{ESR}$ is within the stable region. Also, the load transient response shows good agreement with the simulated response shown in Fig. 16 and the calculated results obtained in Fig. 11.

*3.3.3 Stability margins compared to the equivalent resistance of the switching network:* Since the SCALDO regulator uses an LDO stage with an SC and a low-frequency switching network at the input end, it is important to compare the cases of Figs. 12 and 19, with the other cases where different effective series resistances of the switching stage. In Fig. 20, the measured phase margins are displayed against the load current considering the resistive component of the switching network. These measurements were taken by adjusting the $R_{cn}$ resistor in the switching network and

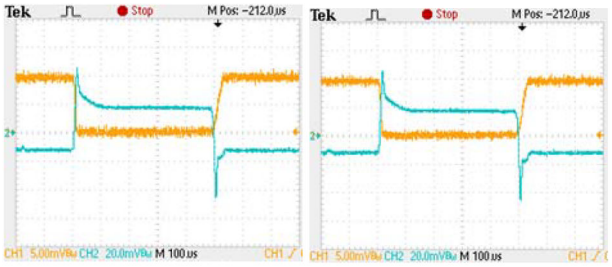



**Fig. 21** *Load-transient response for corner values of the resistive component of the switching network*
***(a)*** $R_{in} = 0.19\ \Omega$, ***(b)*** $R_{in} = 0.49\ \Omega$

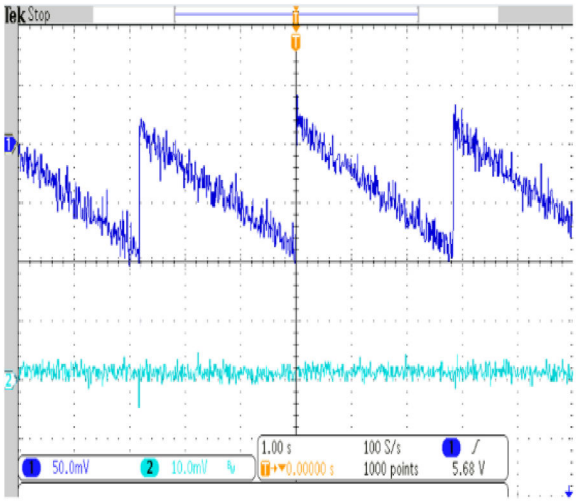



**Fig. 22** *Input and output voltage waveforms of the LDO regulator for 100 mA of load current*

keeping the output capacitor ESR fixed at 1.4 Ω. This diagram shows that there is only minimal influence on the stability due to the variation of the input resistance between the corner values of a typical design. A step-load test was also performed for the corner values of the input resistance, and the observations are displayed in Fig. 21 to compare with Fig. 19*b*. These results clearly reveal the minimal influence of the input series resistance of the SC switching stage on the stability of a SCALDO regulator.

*3.3.4 Switching noise and ripple rejection:* The input switching waveform (fundamental component = 0.357 Hz) of the LDO regulator, together with the output voltage ($V_{o(LDO)}$), was observed using a high bandwidth oscilloscope and the results are displayed in Fig. 22. As shown, the sawtooth input voltage at the LDO stage, due to low-frequency switching of the SC, varies between 6.2 and 6.08 V, while $V_{o(LDO)}$ is regulated at 5.01 V. The low frequency switching related harmonic components and load voltage were analysed using the FFT tool in the MATLAB and the results are displayed in Fig. 23. The frequencies up to the tenth harmonics (the input sawtooth waveform) are displayed in Fig. 23*a*, while Fig. 23*b* shows the related harmonic components at the output up to the fifth component only, since the higher harmonics were obscured by the signal to noise ratio of the oscilloscope.

These measurements also show that an overall efficiency improvement factor of 2 was achieved in this case, due to the SC acting as a near-lossless dropper, ensuring that the DC component of the input voltage of the LDO regulator was maintained at 6.14 V, with a fundamental peak ripple component of 33.5 mV. Harmonic measurements tally with the results derived from (9). These results also indicate that the LDO stage attenuates the fundamental frequency component of the input ripple by at least 50 dB. Therefore, these experimental results match the switching frequency-based disturbance analysis carried out in Section 2.3.2.

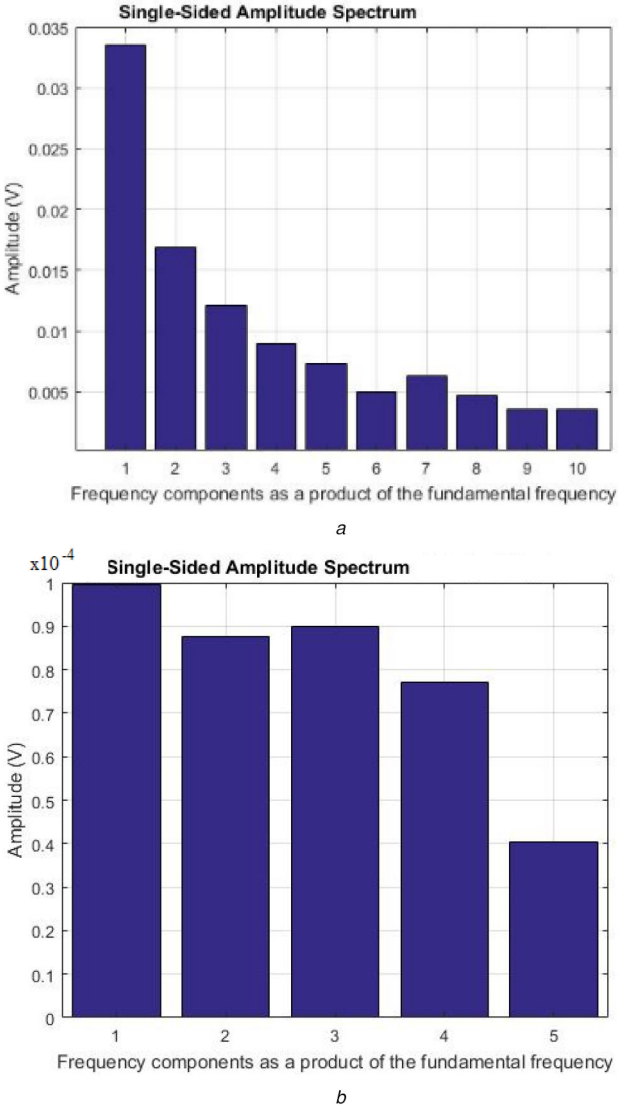



**Fig. 23** *Frequency components as a product of fundamental switching frequency (0.357 Hz)*
***(a)*** $V_{in(LDO)}$, ***(b)*** First five harmonics of $V_{o(LDO)}$

## 4 Conclusion

The stability of the SCALDO technique was analysed for a PMOS pass device based discrete LDO regulator. As with an LDO regulator, the output capacitor ESR could be effectively used to make the control loop stable in a SCALDO regulator, despite the input low-frequency switching stage creating one additional high-frequency pole and two high-frequency zeros in the open-loop transfer function. These results clearly demonstrate that the typical stability calculations applicable to an LDO stage could still be used for the corresponding SCALDO implementations where ETEE is significantly increased, despite the case of a large input-to-output voltage difference.

## 5 References

[1] Manninger, M.: 'Power management for portable devices'. Proc. Int. Conf. European Solid-State Circuits Conf. (ESSCIRC), Munich, Germany, Septmber 2007, pp. 167–173

[2] Iyenggar, A., Tripathi, A., Basarur, A., *et al.*: 'Unified power management framework for portable Media devices'. Proc. Int. Conf. 2007 IEEE Int. Conf. on Portable Information Devices, Orlando, FL, USA, 25–29 May 2007, pp. 1–5

[3] Shen, Z.H., Min, H.: 'Combination method of DC-DC converter and LDO to improve efficiency and load regulation', *Electron. Lett.*, 2011, **47**, (10), pp. 615–617

[4] Vilella, J.C., Garcia, H.M.: 'Design of an On-chip hybrid DC/DC converter', *IEEE Latin Am. Trans.*, 2015, **13**, (7), pp. 2101–2105

[5] Torkan, A., Ehsani, M.: 'A novel nonisolated Z-source DC–DC converter for photovoltaic applications', *IEEE Trans. Ind. Appl.*, 2018, **54**, (5), pp. 4574–4583
[6] Jou, H., Huang, J., Wu, J., *et al.*: 'Novel isolated multilevel DC–DC power converter', *IEEE Trans. Power Electron.*, 2016, **31**, (4), pp. 2690–2694
[7] 'STViQ/3 SMART TViQ', https://www.thortechnologies.com.au/product/stviq3/, accessed Oct 2019
[8] Gunawardane, K., Subasinghage, K., Kularatna, N.: 'Efficiency enhanced linear DC-DC converter topology with integrated DC-UPS capability'. Proc. Int. Conf. 2018 IEEE Int. Conf. on Industrial Technology (ICIT), Lyon, France, 20–22 Feb. 2018, pp. 712–717
[9] Fernando, J., Kularatna, N.: 'Supercapacitor assisted surge absorber (SCASA) technique: selection of supercapacitor and magnetic components'. Proc. Int. Conf. 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, USA, 14–18 September 2014, pp. 1992–1996
[10] Fernando, J., Kularatna, N.: 'Supercapacitors for distributed energy storage in DC microgrids and loads'. Proc. Int. Conf. 2015 IEEE First Int. Conf. on DC Microgrids (ICDCM), Atlanta, GA, USA, 7–10 June 2015, pp. 339–342
[11] Kularatna, N., Fernando, J.: 'High current voltage regulator', US Patent 7,907,430 B2, 2011
[12] Kularatna, N.: 'Supercapacitors improve the performance of linear power-management circuits: unique new design options when capacitance jump from micro-farads to farads with a low equivalent series resistance', *IEEE Power Electron. Mag.*, 2016, **3**, (1), pp. 45–59
[13] Ariyarathna, T., Jayananda, D., Kularatna, N., *et al.*: 'Potential of supercapacitors in novel power converters as semi-ideal lossless voltage droppers'. Proc. Int. Conf. IECON 2017–43rd Annual Conf. of the IEEE Industrial Electronics Society, Beijing, People's Republic of China, 29 Oct.–1 November 2017, pp. 1429–1434
[14] Kwon, O.-S., Son, J.-B., Song, J.-G.: 'Improvement of initial operating characteristics of SCALDO regulator by Pre-charger', *J. IKEEE.*, 2016, **20**, (3), pp. 265–272
[15] Gunawardane, K., Kularatna, N.: 'Supercapacitor-assisted low dropout regulator technique: a new design approach to achieve high-efficiency linear DC-DC converters', *IET Power Electron.*, 2018, **11**, (2), pp. 229–238
[16] Kankanamge, K., Kularatna, N.: 'Improving the End-to-End efficiency of DC-DC converters based on a supercapacitor-assisted low-dropout regulator technique', *IEEE Trans. Ind. Electron.*, 2014, **61**, (1), pp. 223–230
[17] Subasinghage, K., Gunawardane, K., Kularatna, N., *et al.*: 'Extending the supercapacitor-assisted low-dropout regulator (SCALDO) technique to a split-rail DC-DC converter application', *IEEE Access*, 2019, **7**, pp. 124034–124047
[18] Gunawardane, K.K.: 'Analysis on supercapacitor assisted low dropout (SCALDO) regulators', Ph.D, University of Waikato, 2014
[19] Subasinghage, K., Gunawardane, K., Kularatna, N.: 'Pole-zero analysis of supercapacitor-assisted low-dropout (SCALDO) regulator'. Proc. Int. Conf. 2018 IEEE Int. Conf. on Industrial Electronics for Sustainable Energy Systems (IESES), Hamilton, New Zealand, Jan. 31 2018-Feb. 2 2018, pp. 146–151
[20] Subasinghage, K., Gunawardane, K., Kularatna, N., *et al.*: 'Selection of the stable range of the equivalent series resistance (ESR) of the output capacitor for a SCALDO regulator'. Proc. Int. Conf. 2018 IEEE 27th Int. Symp. on Industrial Electronics (ISIE), Cairns, QLD, Australia, 13–15 June 2018, pp. 1359–1364
[21] Lee, B.S.: 'Slyt187 understanding the stable range of equivalent series resistance of an LDO regulator', Texas Instruments, 1999, pp. 1–17
[22] Rincon-Mora, G.A., Allen, P.E.: 'Optimized frequency-shaping circuit topologies for LDOs', *IEEE Trans. Circuits Syst. II: Analog Dig.Signal Process.*, 1998, **45**, (6), pp. 703–708
[23] Rogers, E.: 'Slyt194 stability analysis of low-dropout linear regulators with a PMOS pass element', Texas Instruments, 1999, pp. 1–13
[24] Tan, R.H.G., Hoo, L.Y.H.: 'DC-DC converter modeling and simulation using state space approach'. Proc. Int. Conf. 2015 IEEE Conf. on Energy Conversion (CENCON), Johor Bahru, Malaysia, 19–20 October 2015, pp. 42–47
[25] Wester, G.W., Middlebrook, R.D.: 'Low-frequency characterization of switched DC-DC converters', *IEEE Trans. Aerosp. Electron. Syst.*, 1973, **AES-9**, (3), pp. 376–385
[26] Spyker, R.L., Nelms, R.M.: 'Classical equivalent circuit parameters for a double-layer capacitor', *IEEE Trans. Aerosp. Electron. Syst.*, 2000, **36**, (3), pp. 829–836
[27] Patel, A.P., Rincon-Mora, G.A.: 'High power-supply-rejection (PSR) current-mode low-dropout (LDO) regulator', *IEEE Trans. Circuits Syst. II: Express Briefs.*, 2010, **57**, (11), pp. 868–873
[28] Zendzian, D.: 'U-152 A high performance linear regulator for low dropout applications', Unitrode corporation, 1995, pp. 1–11
[29] SNVA020B, 'AN-1148 Linear regulators: theory of operation and compensation', Texas Instruments, 2000, pp. 1–14
[30] SNVA364A, 'AN-1889 How to measure the loop transfer function of power supplies', Texas Instruments, 2008, pp. 1–9
[31] Middlebrook, R.D.: 'Measurement of loop gain in feedback systems', *INT. J. Electron.*, 1975, **38**, (4), pp. 485–512