Development of a Power Factor Corrected High Current Supercapacitor Charger for a Surge Resistant UPS

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Abstract

The Uninterrupted Power Supplies (UPSs) provide short term power back up to electrical loads when the mains power fail. Usually UPSs employ battery packs as the energy storage device. However the limitations of battery packs can affect the UPS performance.

As an alternative energy storage device, the supercapacitor (SC) technology is well developed over the past 30 years. Due to recent developments, single cell commercial supercapacitors are available up to about 5000 farads. Over the past 10 years, supercapacitor direct current (DC) voltage ratings have gradually increased to about 2.7 V/cell. New lithium based supercapacitor families have DC ratings up to 3.5 V/cell. For the high current applications, the supercapacitors have some advantages over batteries, which are the low effective series resistance (ESR), high power densities and high surge withstand capability.

This thesis is a continuation of the work begun by Kozhiparambil, P. K. on Surge Resistant Uninterrupted Power Supply (SRUPS). The reason for this continual research is due to identify weaknesses in original of SRUPS work with regard to the design of the charger. To reduce the components contain, also achieve common mode transient rejection capability, a flayback mode high current charger with power factor correction has been developed for charging the SC banks.

The prototype circuit includes multiple SC banks to transfer the energy from the 240 V, 50 Hz power line to the load maintaining high isolation level. The loads receive continuous and surge free power from the SC banks, and has electrical isolation from the main power line. An IGBT is used as a switch for the flyback charger, which has the advantage of high current capability.

The experimental results show the design was valid for the SRUPS and it demonstrated the capability to transfer the energy through a flyback charger with power factor correction.

Acknowledgements

This thesis would not be able to be completed without the support and encouragement of others over two years of hard work.

I would like to express my gratitude and appreciation to my academic supervisor, Mr. Nihal Kularatna. Without his wisdom, guidance and insight I would not have been able to complete this thesis to the academic standard required. His time and contribution to the research has been immense and I will always be thankful.

This research follows on from the previous work started by Mr. Parthasaradhy Kumaran Kozhiparambil and I would like to thank him for his invaluable input at the beginning of this research.

On the technical side, the efforts of laboratory technicians, Mr. Stewart Finlay, Mr. Viking Zhou, and Mr. Pawan Shrestha, are most appreciated. Everything I needed in terms of components and equipment was no problem for them.

Of course I could not have got to this point without the love and financial support from my parents who have supported their son's overseas studies for an arduous seven years.

I could not finish without also thanking the special lady in my life, Carol. The time, patience, generosity and love she gave me while we were students together in New Zealand will always be cherished.

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Nomenclature

AC	Altering Current
ADC	Analogue Digital Converter
BDD	Bidirectional Breakover Diode
BJT	Bipolar Junction Transistor
DC	Direct Current
EFT	Electrical Fast Transient
ESR	Effective Series Resistance
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
LED	Light Emitting Diode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOV	Metal Oxide Varistor
PCB	Printed Circuit Board
PIC®	Peripheral Interface Controller
PWM	Pulse Width Modulation
RC	Resistance Capacitor
RCD	Resistance Capacitor Diode
RMS	Root Mean Square
SC	Supercapacitor
SOA	Safe Operating Area
SRUPS	Surge Resistance Uninterrupted Power Supply
UPS	Uninterrupted Power Supply

Chapter One

Introduction

1.0 Introduction

1.1 Introduction to uninterrupted power supply topologies

Business, industry and telecommunication use millions of electrical equipment. They provide control, data processing and communicating systems, which makes the term computer-integrated factory or computer-integrated business happen. For those systems to operate continuously without unexpected interruption, a reliable AC power supply is required.

To control the risk of power interruption, the uninterrupted power supply (UPS) was invented to be the emergency power source that provides the backup power supply to the equipment when the power source, typically the main power source, fails. The first commercial UPS system was invented in the 1950's, which was basic version involving rotating electrical machinery. After years of development, the rotating machinery components in the earlier version of UPS system were replaced by the electrical components. Therefore the physical size of UPS has been decreased, in turn decreasing the cost to approximately $1 per watt (*PQ Assurance Journal*).

By the 1990s, UPS usage had expanded to cover not only industrial systems, but also residential systems. The statistics in 1992 show that three-phase large UPS system only occupied 37% of the UPS market (Katzaro,1993). Comparatively the single-phase system contributed almost two thirds of the UPS market. At this time the electrical transient interference is a major issue in the AC power line, which happens more frequently than a power fail. Therefore, the UPS designs were extended to provide surge protection for occurrences such as surging, transient, and lightning.

Presently, the commercial UPS systems are divided into three basic topologies, off-line, hybrid, and on-line types respectively.

1.1.1Off-line topology

The block diagram of off-line UPS shows in Figure 1.1. The battery takes a charge through the converter, and holds the energy for power backup. In the normal operation, the load is powered directly from the AC power line, the filter on the AC power line provides a basic voltage filtering against the low energy interferences. In the event of power failure, the switch transfers to the standby power source, where the battery will carry the major load current.

The off-line UPS system is usually found in the domestic environment. It is cheap, easy to maintain, and a smaller in size and weight. The off-line UPS presents very low losses during the normal operation, because the battery and inverter normally off and physically disconnected from the power source. The power source carries the most of load current, only small amount charging current goes to the battery against the battery leakage. Therefore regardless of the battery leakage, the power loss on the off-line UPS during the normal operation is approximately zero.

The disadvantage of this type of UPS is response latency and low level surge protection. The transfer time is determined by the sum of detection time and switch transfer. When the AC power fails, an occurrence of voltage glitch is due to transfer time. The quality of line filter and surge suppression available in the off-line UPS are price dependent and may be absent in the low end version which makes them highly unreliable when operated in the environment of high level surge and transient.

When a power failure occurs presenting in Figure 1.2, the off-line UPS switches to the inverter mode and operates in this mode until the main power is recovered again. The system switches from one mode to the other mode in the shortest possible duration, in order to supply uninterrupted power to the load. However the waveform at the middle of Figure 1.2 shows that the sine waveform goes flat, which means the main AC power fails. After a while, this power failure is detected and the inverter starts to operate for providing power to the load. This flat time is significantly demonstrated the response latency during the system switches from one operation mode to the other. The inverter output demonstrates in Figure 1.2 is not smooth sine waveform, contains voltage spikes, brownouts and blackouts. Those influences affect the performance of electrical load that connect to this

inverter, also may damage the electrical load which is sensitive to these voltage interferences.

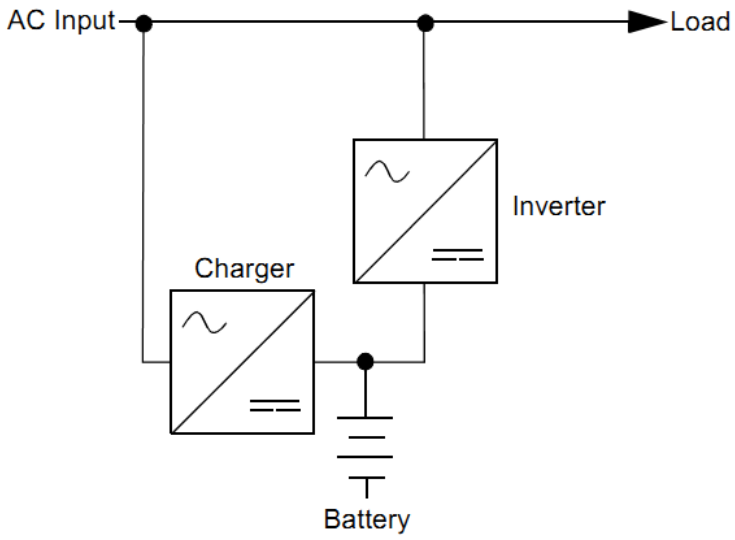


Figure 1.1 Block diagram of off-line UPS (Khare & Kamil, 2009)

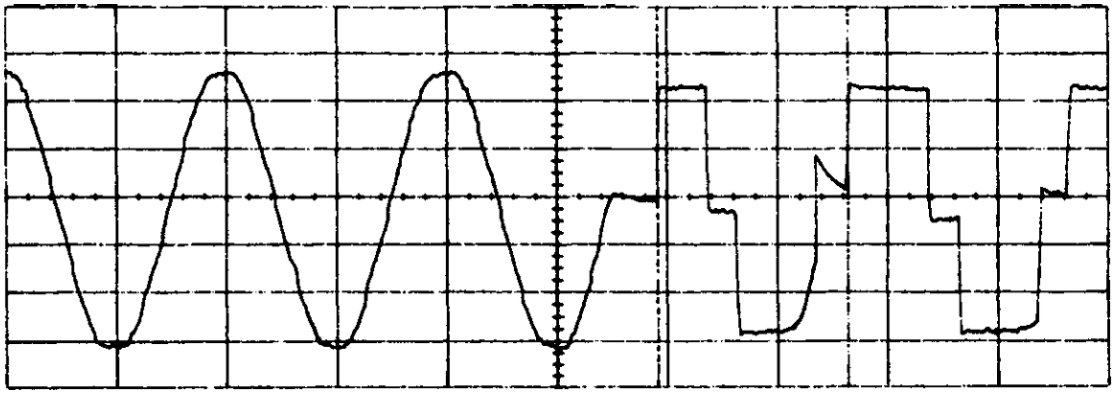


Figure 1.2: An oscillograph of AC output during the transfer process of an off-line UPS (Kularatna, 1998)

1.1.2 Hybrid topology

Principally, the hybrid UPS is developed from the off-line UPS. The transfer switch is replaced by a special saturated transformer that has three windings, two bifilar wind primaries and a secondary. The inductive coupling has the advantage of energy storage and faster transfer. However, this type of UPS is large, heavy, and has high thermal losses due to the local heating of the transformer. Figure 1.3

shows the block diagram of the hybrid UPS.

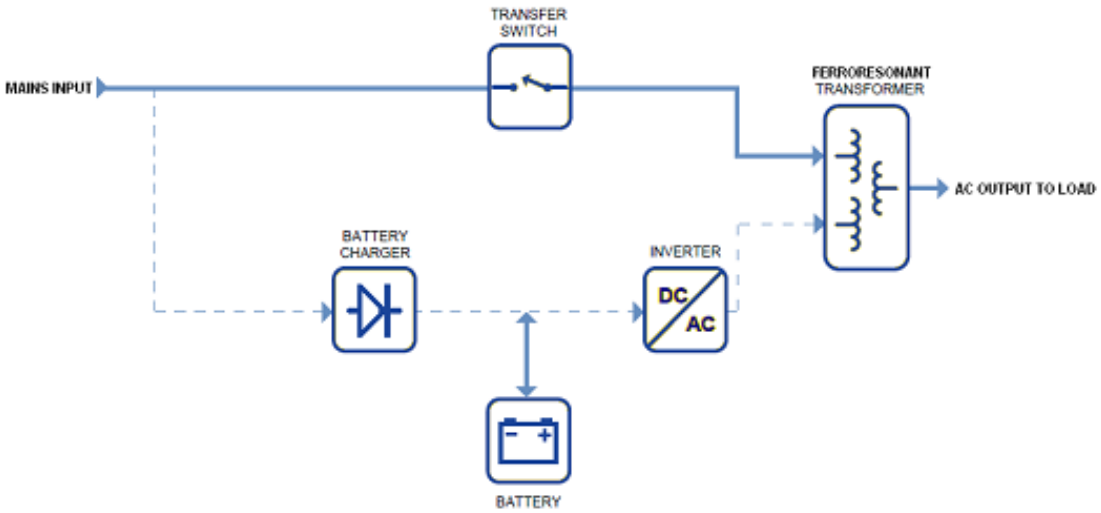


Figure 1.3: Block diagram of hybrid UPS (Kozhiparambil, 2011)

1.1.3 On-line UPS topology

The on-line UPS system is designed for the equipment that operates in the “noisy” environment, or is sensitive to power fluctuation. The block diagram shows in Figure 1.4 the output after the rectifier and inverter is completely isolated from the main AC power source. The rectifier and inverter are always operating, which protect against surges, sags, spikes and transients. The AC input via the rectifier is stepped down to charge the battery, and the inverter boosts the battery power which is then fed into the load. When the main AC power fails, the rectifier simply drops out, and batteries then discharge to the load. When the power resumes, the rectifier carries the most loaded current and batteries start to charge and standby. In the normal operation, the batteries take a small amount of charging current against the self-discharge. The switch free circuit and on-line protection provide the fastest response time and high surge suppression level. However, it has the most complex design, requires a limitation of the charging current to prevent the rectifier from overcurrent, and a cooling system is required for batteries, in order to extend the battery lifetime.

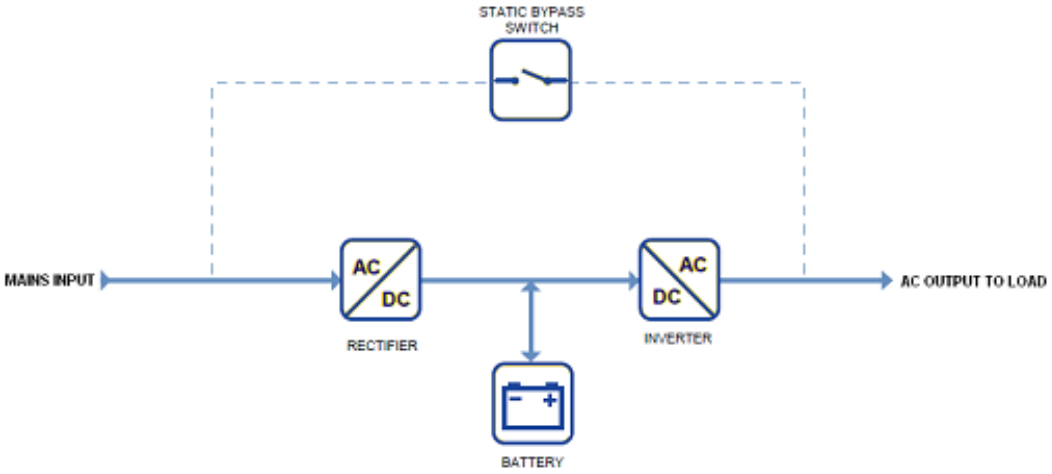


Figure 1.4: Block diagram of on-line UPS (Nesscap Co., Ltd., 2008)

1.2 Research motivation

Three UPS topologies were introduced in the previous section, which were designed to minimize the risk of power fail and surge damage. The circuit devolved from the direct connection to the inductive coupling, and the off-line protection to the on-line protection using a similar battery pack as an energy storage device. The battery is economic and highly reliable, but it has some drawbacks, such as:

- Limitation of the peak charge and discharging current.
- The overcurrent can lead to boiling chemicals that will short or terminate battery service life.
- Rush incoming current may damage the battery.

This research investigates the possibility of using the supercapacitor to be an alternative energy storage device for on-line UPS system, as well as utilizing the supercapacitor surge sustainability to simplify the UPS surge protection design.

1.2.1 Supercapacitor energy storage capability

The supercapacitors are also known as the ultracapacitor. The supercapacitors

(SCs) are high efficient energy storage device that has higher instantaneous power densities than conventional batteries, and higher energy densities than the electrostatic capacitors as depicted in Figure 1.5. The supercapacitors are a non-chemical reaction device, where the energy is stored via an electrostatic process. It allows the supercapacitor to charge and discharge at high rate of current, making it possible to be used as a high current source for the power applications.

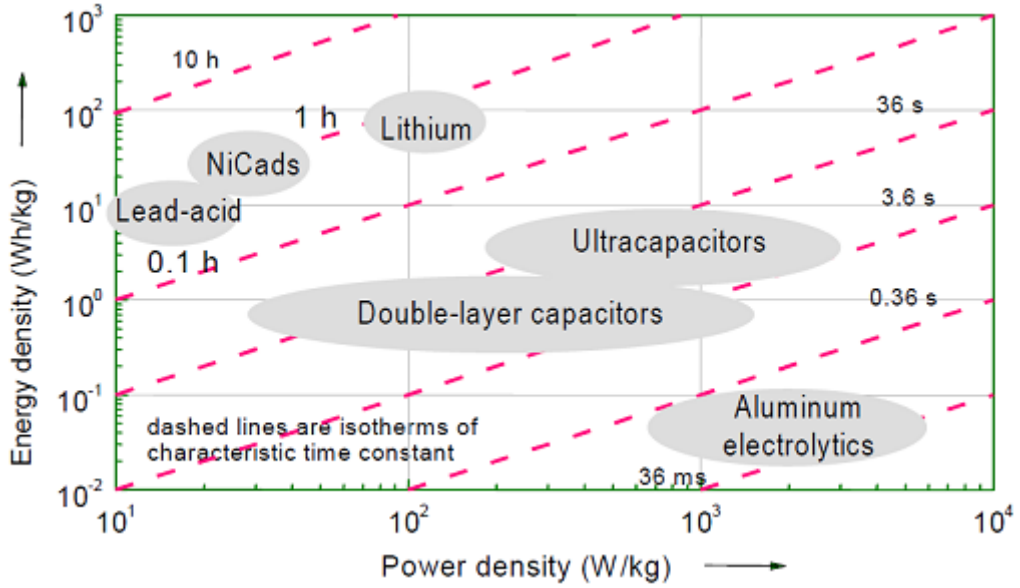


Figure 1.5: Power densities and energy densities of various storage devices (Kozhiparambil, 2011)

The Maxwell Technology proposed approach of a SC module consists of two parallel capacitor packs, where each pack contains 140 cells connecting in series. The SC module is designed to drive a hybrid bus that weighs 9600 kg plus 5400 kg for the passenger mass, which must be satisfied in both conditions of long distance service and fast acceleration. According to the experiment results, the capacitor module in the long term service process presents the utility of high energy storage, which is able to supply over 178kWh. On the other hand, the acceleration experiment required to accelerate from zero speed to 25mph is 295Wh, which demonstrated the capacitor model has the advantage of high peak output current (Miller, 2011) [8]. Therefore, this study will discuss the possibility of the supercapacitor bank as an alternative energy storage device for the on-line

UPS.

1.2.2 Surge protection

1.2.2.1 Conventional surge protection devices

The metal oxide varistors (MOV) and bidirectional breakover diodes (BBD) are the most common electrical surge suppression devices, providing a basic surge protection. These devices have the advantages of low cost and simple structure. However those component are limited on the response time, maximum clamping voltage and repeated pulse current sustainability.

MOVs are nonlinear voltage dependent devices which have an electrical behavior similar to back-to-back zener diodes. It is often used to guard against excessive voltage transients. The devices could conduct heavily when a short duration high voltage transits occurs, and provide a current path to absorb transients energy.

Bidirectional breakover diodes (BDD) consist of two avalanche diodes, which can be switched from the non-conduct state to the conduct state for either polarity of applied voltage. The Figure 1.6 shows the chemical structure, electronics symbol and V-I characteristics. In the non-conduct state, a very small amount of leakage current is exhibited in either direction. The conduction is occurred when the breakover voltage is reached in either polarity across the two terminals. The Bidirectional breakover diode is often used in the high voltage protection circuit, which requires a protection against transients in either positive or negative.

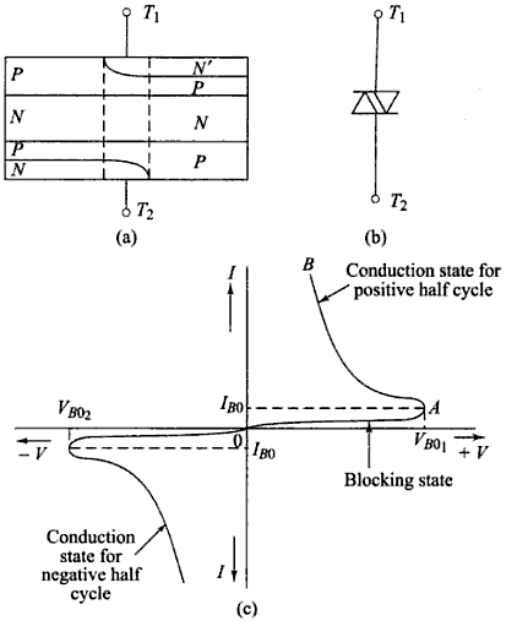


Figure 1.6: (a) the chemical structure of a BDD, (b) BDD electronics symbol, (c) the V-I characteristics (Khanchandani, K. B. & Singh, M. D, 2008)

The major drawback to those two protection devices is, during the shunt period, the occurrence of breakdown causes localized heating. If the heat generation is excessive, the device may melt, burn, vaporize or be otherwise damaged.

1.2.2.2 Supercapacitor surge withstand capability

The journal article published by Nihal Kularatna and his team (Kularatna, Fernando, Pandey, & James, 2011), demonstrated the supercapacitor surge sustainability by testing different commercial brands of supercapacitor families. The result demonstrated that the Cap 0.18F supercapacitor could easily withstand over 200 hits of 6.6 kV repeated surges before the occurrence of failure. Another test sample, Maxwell Boostcap 230F exhibited robust surge sustainability, 600 repeated surges (6.6 kV) could not damage it. Therefore, the test results have allowed others to expend their work, to develop applications of surge protection utilizing the property of supercapacitor surge sustainability.

1.3 Previous research

The master engineering student Kozhiparambil P. K. who proposed an approach

of supercapacitor based surge free on-line UPS. The core concept is that three supercapacitor banks operate independently as energy transfer devices. The capacitor banks provide a complete isolation to the load, and absorb the transients to protect the load from damage. The sizing of the capacitor bank is considered by taking into account their system parameters and properties, such as duty cycle, efficiency, cost, etc.

Figure 1.7 depicts the operation of dynamic supercapacitor banks (SC bank). In normal operation, one of the SC banks, for example SC bank 3, gets charge from the AC power line. Meanwhile, the SC bank 1 operates in the discharge mode. It releases its energy to the inverter, and will return to the charge mode when the terminal voltage is lower than the inverter requirement. The SC bank 2 is kept the full charge and standby, and will replace the SC bank 1 before it disconnects from the inverter. Therefore the SC banks are cycling. If assuming the average rate of charge (from the utility power line) is greater than the rate of discharge (to the inverter), then the inverter could be continuous powered by the SC banks. The load connect to the inverter is powered by the SC banks and completely isolated from the utility power line. Therefore the surges at any given operation modes have no chance to affect the load.

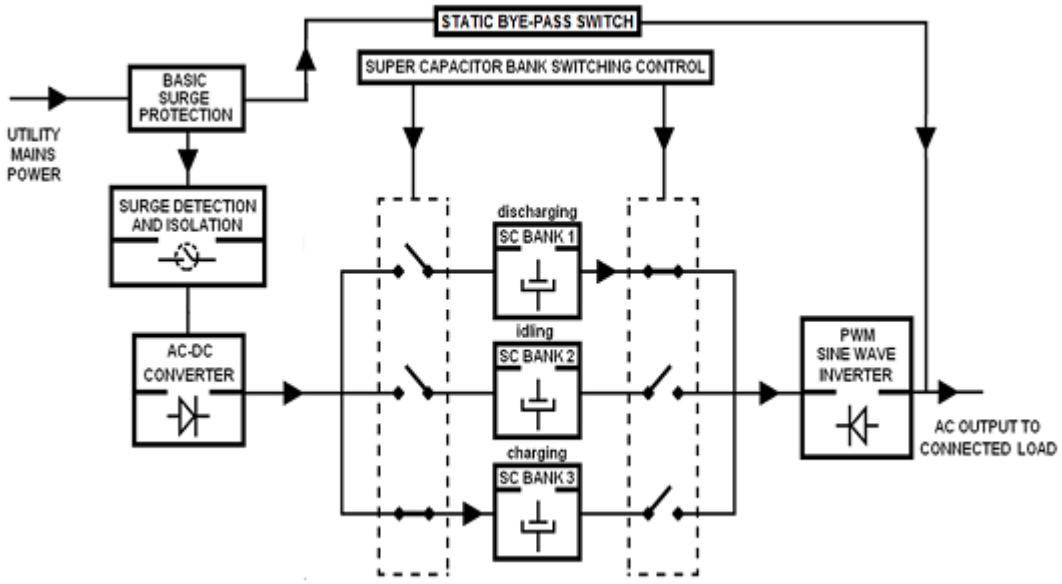


Figure 1.7: The block diagram of a SC based surge free UPS (Kozhiparambil, 2011)

1.4 Development

The UPS approach offered by Kozhiparambil P. K is used a cycling of SC banks to separate the load from the main power, in order to avoid the surge damages. However the charge circuit in this approach is very complicated. Some components are easily damaged by the repeated surges. So the charger could be failed due to component failure. To overcome this problem, this research proposes a technique that employs a flyback type transformer to replace entire charge circuit. It is aimed to develop a simple and reliable charge circuit for charging supercapacitor banks. The new charger must able to supply high rate of charging current with high efficiency, and withstand all level surges that standard is defined by IEEE C62.40. The new proposal of supercapacitor surge free on-line UPS is depicted in Figure 1.8.

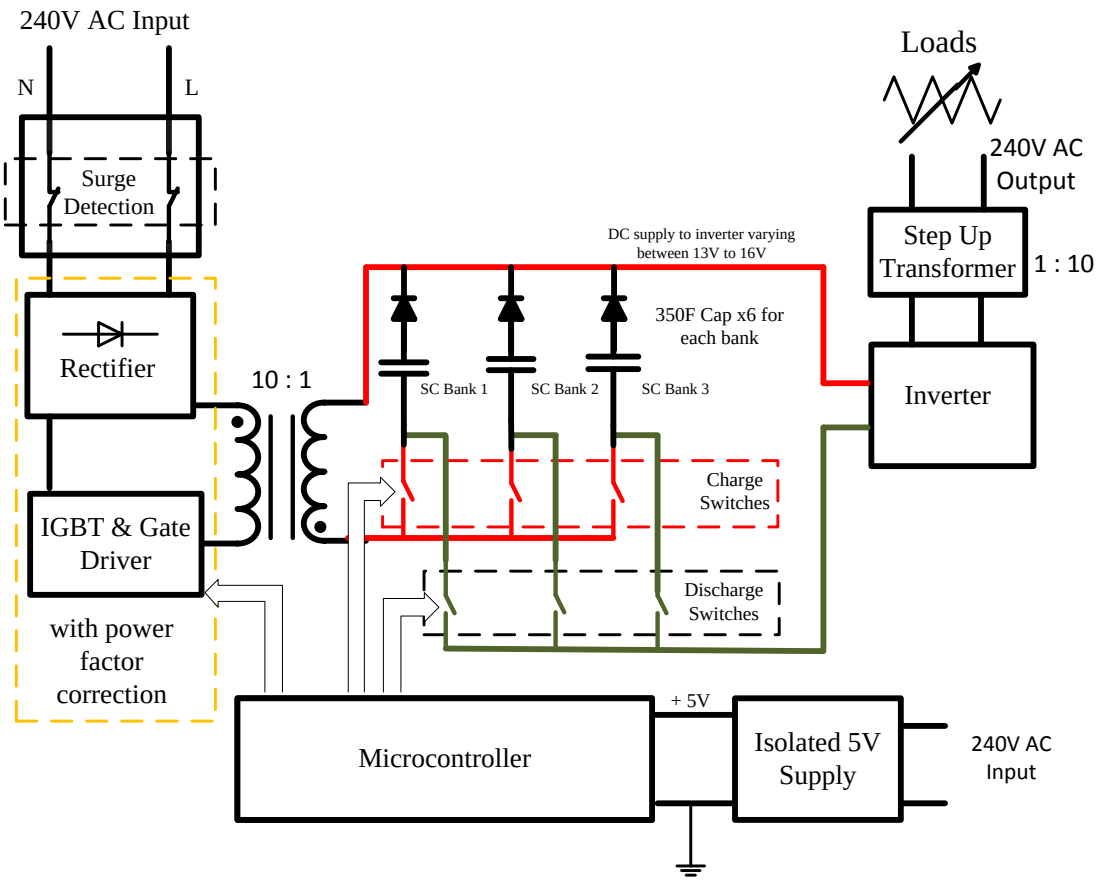


Figure 1.8: Block diagram of a surge resistant UPS with inductive coupling

The switch attached on the primary winding of transformer is switching at certain frequency. The primary winding gats charge during the switch on-period, and then release the energy to the secondary when switch is in off period. The supercapacitor banks connect to the secondary wind gets charge through the weak coupling. The energy transfer via the magnetic coupling makes it possible that the electrical isolation exists between AC main line and the load. The supercapacitor banks are only exposed to transients that propagate through the magnetic coupling. The supercapacitor has the advantage that it is capable of absorbing the surges. The propagation of surges and transients should absorb and vanish at the stage of supercapacitor banks, in order to protect other electrical components on the inverter side. Irrespective of the operation mode, the load has no chance to create a loop for transients in the energy transfer process. Hence the transfer of energy takes place in complete isolation with protection against common-mode transients. Because the valid inverter input voltage is between 12 V to 20 V. Therefore, the supercapacitor banks are design to charge and discharge in a voltage window between 13 V to 16 V.

1.5 Thesis arrangement

Chapter One : Introduction. Introduce to the fundamental of three UPS topologies off-line, hybrid and on-line, which are usually used in the commercial UPS system. Then briefly discuss the advantages and disadvantages of the three UPS topologies, and address the reason why we investigate in the new topology of supercapacitor based UPS.

Chapter Two : Background. It is summering the essential components and their relevant characteristics required for the design project.

Chapter Three : Circuit Description. It discusses the actual circuit and control routines. The procedure of the circuit developing is demonstrated in one step by one step.

Chapter Four : Experiment results. It discusses the measurements and results that can be used to evaluate the performance of project.

Chapter Five: Conclusion and Future Development. It concludes the achievements that have been done in this research, and recommend the future development for a better design approach.

Chapter Two

Background

2.0 Background

2.1 Supercapacitors

Supercapacitor families based on electric double layer effect have entered into a mature stage for usage in many applications, such as electric vehicles, UPS systems, battery-supercapacitor hybrids and cellular phones. The following section will discuss the characteristics of supercapacitor from the different aspects.

2.11 Supercapacitor lifetime evaluation

The lifetime of a supercapacitor is of considerable industrial interest. An investigation by Maxwell discovered that the electrical and thermal stresses are mainly affected by their aging characterization. Two different methods were designed to test the lifetime of the supercapacitor. The first method is power cycling where the devices charge up to rated voltage beginning at zero volts, then discharge from the rated voltage to half rated voltage, and then repeat this process continuously. The second method is where the unit holds the constant voltage and temperature stress.

The references (Kötz, Hahn, & Gallay, 2006) and (Gualous, Louahlia-Gualous, Gallay, & Miraoui, 2009) describe an experiment using a Maxwell BACP350 supercapacitor, which is rated for 2.5 V. The experiment setup consists of four thermocouples that were surface mounted on the body of the supercapacitor as depicted in demonstration mode in Figure 2.1.

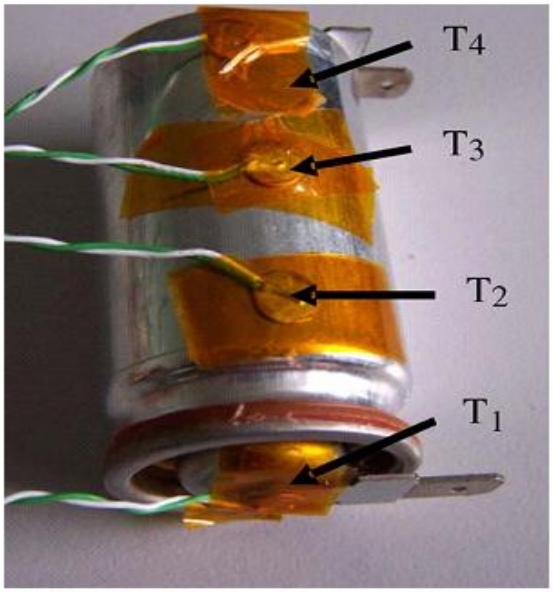


Figure 2.1: The supercapacitor of BCAP350 with four thermocouples (Gualous et al., 2009)

Figure 2.2 graphically demonstrates an energy cycling experiment, where supercapacitors charge and discharge with a quasi-square wave of current. Consequently, the terminal voltage sweeps between its rated voltage (2.5 V) and half rated voltage (1.25 V). The voltage cycling is designed within this voltage window because they can store and provide approximately 75% of its maximum energy, without creating design challenge. (Gualous et al., 2009)

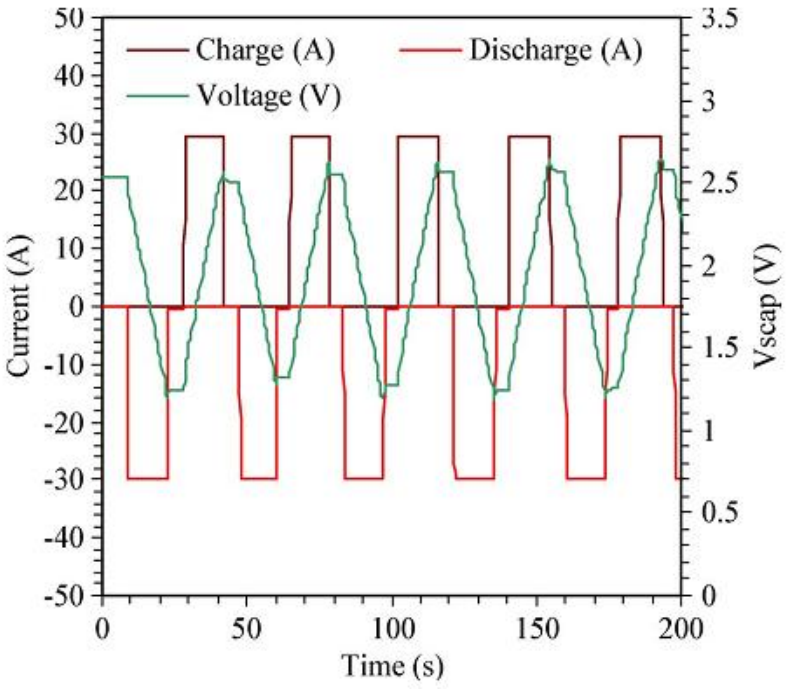


Figure 2.2: Energy cycling test with pulse period of 14 seconds (Gualous et al.,

2009)

Figure 2.3 shows the thermal stresses of the energy cycling experiment. The supercapacitors will get charged and discharged at high current rate, while the temperature increases over time. In the cycling operation, the cell core temperature rises approximately 2ºC more than the ambient temperature. In the steady state (holding the voltage constantly), the core temperature appears 1ºC above the ambient temperature. The small temperature difference makes it evident that the supercapacitor has very low thermal resistance, making it suitable for high power transfer because of lower thermal losses and body heating.

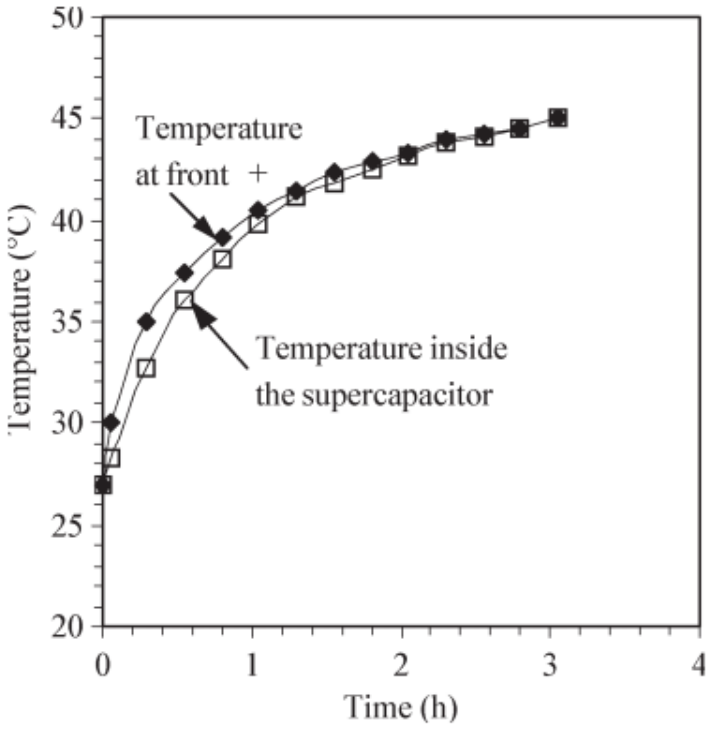


Figure 2.3: Comparison between the core and ambient temperatures (Gualous et al., 2009)

The rate of charging/discharging current is another important parameter to affect thermal drop out behavior. A comparison graph of temperature increases due to the difference of cycling current as depicted in Figure 2.4, illustrates the increasing core temperatures over one hour period. As the results show, in high power applications, a heat sink is necessary, and the design should be based on the rate of charging/discharging current.

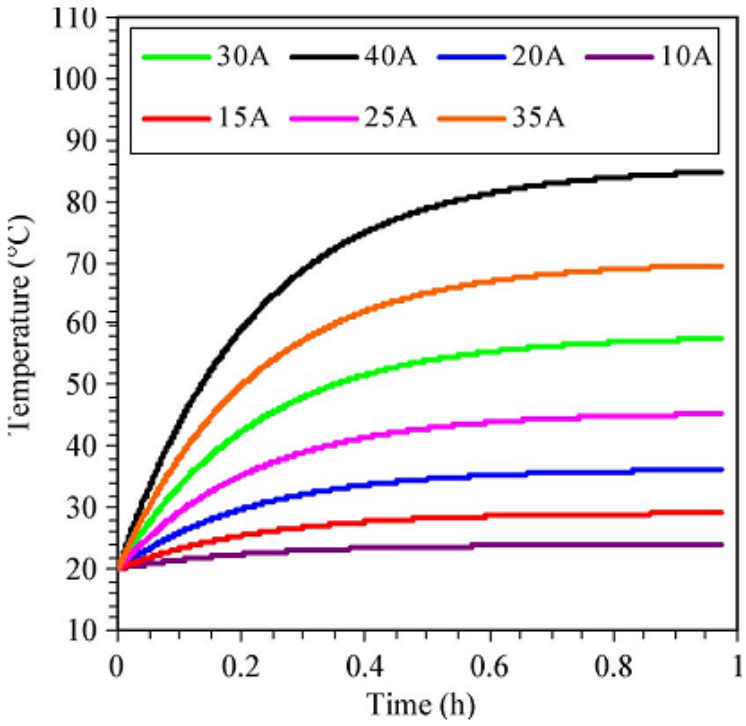


Figure 2.4: BACP350 core temperatures for different cycling current (Gualous et al., 2009)

Although the supercapacitor has very low thermal resistance, for some high current application, it is still a major consideration. A numerical thermal model demonstrated in the flowing section was built by Hamid Gualous, which helps to understand the thermal behavior comprehensively (Gualous et al., 2009). The distribution of heat inside the supercapacitor spreads from the high temperature zone to another zone where the temperature is lower. The heat transformation can be expressed as

$$\nabla^2 T + \frac{P}{\lambda} = \frac{\rho C_p}{\lambda} \frac{\partial T}{\partial t}$$

(2.1)

(Gualous et al., 2009)

Where :

- ∇^2 is the Laplacian operator.
- ρ is the density of capacitor.
- λ is the supercapacitor thermal conductivity
- C_p is the heat-specific capacity.

- P is the local volumetric density.

The physical structure of the supercapacitor can be described as a cylindrical tube, as shown in Figure 2.5. The heat transformation inside this supercapacitor is assumed to be axis-symmetrical, and the heat conduction equation is used in two directions, i.e., in the radial and the axial direction. The conductivity along axial and radial directions are set to be λ z and λ r respectively, and the physical model is given by

$$\rho C_p \frac{\partial T(r,z,t)}{\partial t} = \lambda_r \frac{\partial^2 T(r,z,t)}{\partial r^2} + \frac{\lambda_r}{r}\frac{\partial T(r,z,t)}{\partial r} + \lambda_z \frac{\partial^2 T(r,z,t)}{\partial z^2} + P \quad (2.2)$$

(Gualous et al., 2009)

where:

- $r_i < r < r_o, 0 \leq z \leq L,$ and $0 < t \leq t_f$
- r is the radial coordinate, z is the axial coordinate and
- r_i and r_o are the internal and external radii of the supercapacitor.

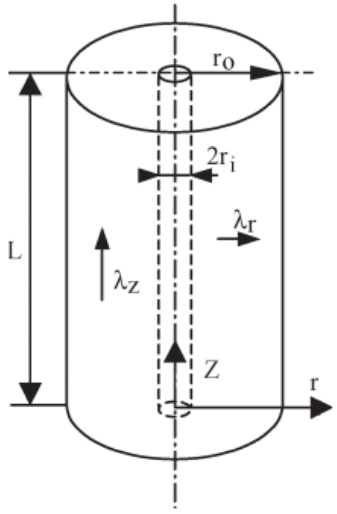


Figure 2.5: Supercapacitor cylindrical structure (Gualous et al., 2009)

The supercapacitor consists of many layers. The thermal resistance in the signal

layer can be written as

$$R_{\mathrm{th}} = \frac{\ln(r_o/r_i)}{2\pi\lambda L}.$$

(2.3)

(Gualous et al., 2009)

However for the multiple-layer supercapacitor, each layer has a different radius; the equivalent thermal resistance along the radial direction is the sum of all the layers. For example, for a four-layer structure, the equation can be written as

$$R_{\mathrm{th}} = \frac{1}{2\pi\lambda_c L}\ln\left(\frac{r_i+e_c}{r_i}\right)+\frac{1}{2\pi\lambda_s L}\ln\left(\frac{r_i+2e_c+e_a+e_s}{r_i+2e_c+e_a}\right) + \frac{l}{2\pi\lambda_c L}\ln\left(\frac{r_i+2e_c+e_a}{r_i+e_c+e_a}\right)+\frac{1}{2\pi\lambda_a L}\ln\left(\frac{r_i+e_c+e_a}{r_i+e_c}\right)$$

(2.4)

(Gualous et al., 2009)

where :

- e_c is the thickness of active carbon.
- e_s is the thickness of separator.
- e_a is the thickness of aluminium.
- λ_c is the active carbon thermal conductivity
- λ_a is the aluminium thermal conductivity
- λ_s is the separator thermal conductivity

Along the axial direction, the thermal conductivity of all the layers is assumed to be the same as the aluminum conductivity. Hence they form a parallel thermal resistance. The expression for the parallel thermal resistance is

$$\frac{1}{R_{\mathrm{th}}} = \sum_{n=1}^{N}\frac{1}{R_{\mathrm{th},n}}$$

(2.5)

(Gualous et al., 2009)

where n is the number of the layer and N is total number of layers. In fact the conductivity of the carbon and the separator is much lower than the conductivity of aluminium. The equation can be simplified, depending only on the conductivity of aluminium.

2.12 Reliability

Reliability and service life are very important considerations when designing commercial applications. The reliability is the subject that relates to the quality of products, which is defined as:

"*The probability that a product performs its intended function without failure under specified condition for a specified period of time. The definition contains three important elements: intended function, specified a period of time, and specified conditions."(Albertsen, 2010)*

For determining the failure of the supercapacitors, an experiment was developed by R. Kötz and his team, where the supercapacitor held at 2.5 V at room temperature. The result as depicted in Figure 2.6 shows, the occurrences of an increase of ESR and reduction of capacitance are during in the server time. On the other hand, the temperature variation is also effect the aging process, which is also discussed by the R. Kötz. An increase of the temperature of 10ºC will result in an accelerated aging factor between 1.7 and 2.5. For more information, please refer to the reference of.

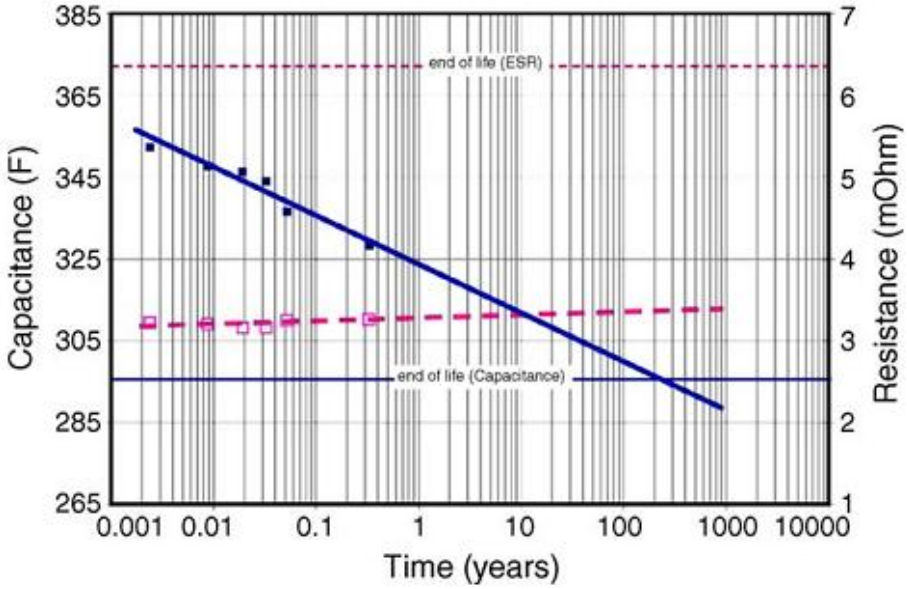


Figure 2.6: Variation of capacitance and ESR versus lifetime (Kötz et al., 2006)

2.13 Energy and Power

Figure 2.7 shows a great development of supercapacitor on the cell voltage, energy storage capability and power supply capability. Because this development, many applications are developed to use supercapacitors as alternative energy storage devices. For general purpose, all the data sheets list the cell mass and dimensions that can be used to calculate energy density. As a voltage device, it evaluates on two aspects, which are specific energy (SE in j/kg, Wh/kg) and energy density (ED in j/L, Wh/L) respectively, and where cell mass (E) and dimensions (L) are used to calculate volume. The expressions are given

$$SE = \frac{CU_{mx}^2}{2M}\,(\mathrm{J/kg}) = \frac{CU_{mx}^2}{7200M}\,(\mathrm{Wh/kg})$$

(2.6)

(Miller, 2011)

$$ED = \frac{CU_{mx}^2}{2Vol}\,(\mathrm{J/L}) = \frac{CU_{mx}^2}{7200Vol}\,(\mathrm{Wh/L})$$

(2.7)

(Miller, 2011)

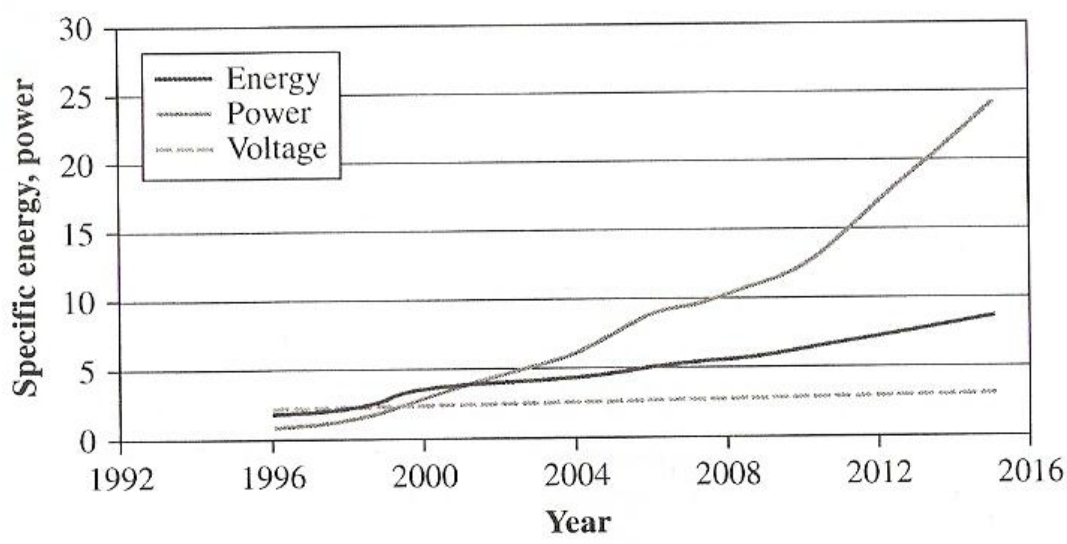


Figure 2.7: Evolution of symmetric supercapacitor cell voltage, energy and power (Miller, 2011)

The power performance of the supercapacitor is also important. Many applications require a high performance instantaneous power supply where the supercapacitor can be used. The most commonly used metric for power is matched load power, P_{ML}, and corresponding specific power defined as 2.9 and 2.10. The table 2.1 highlights the equivalent series resistance (ESR) with different commercial brands. The low ESR is the advantage for high power supply capability, and minor losses during the energy cycling process.

$$P_{ML} = \frac{U_{mx}^2}{4ESR_{dc}}$$

(2.8)

(Miller, 2011)

$$SP_{ML} = \frac{U_{mx}^2}{4(ESR_{dc})M}$$

(2.9)

(Miller, 2011)

Table 2.1 The electrical characteristics of different supercapacitor families (Kularatna et al., 2011)

Parameters as per data sheets	Cap-XX	Nesscap	Maxwell Boostcap
Capacitance	0.18 F	90 F	230 F
Rated DC Voltage	2.3 V	2.7 V	2.5 V
Effective Series Resistance	45 mΩ	0.33 mΩ	2.2 mΩ
Operating Temperature Range	-40 - 70 °C	-40 - 65 °C	-40 - 70 °C
Leakage Current	3.5 µA	0.75 mA	0.45 mA

2.14 Balancing circuits

A supercapacitor module consists of many identical cells, and connecting them in series gives higher net output voltage. In the charging process, voltage distribution in the supercapacitor module is initially a function of capacitance. After a period of time, where each identical cell holds at a particular voltage level, this voltage distribution becomes a function of internal parallel resistance, which represents a leakage current.

A balancing circuit is required to equalize voltages on each identity cell. Without the voltage balancing, the cell voltages during the charging process, where the cell with smaller capacitances will be saturated and tend to overcharge, while the cell with greater capacitances will be charged to lower voltages.

When the capacitor module holds voltages in the steady state, a leakage current is present. The voltages decaying due to leakage current is a function of different resistances, which also cause unequaled cell voltages. The cell voltages discharge in higher rate, which should have lower leakage resistance, and vice versa.

To overcome the problem discussed above, a balancing circuit is developed, and its schematic is demonstrated in Figure 2.8. It employs bypass resistances to

balance terminal voltages of each individual cell, as well as compensation for variation in leakage current. The bypass resistance technology is called passive balancing. It only suits the low duty cycle applications. For the high duty cycle applications, Maxwell Technology recommends an active balancing circuit as depicted in Figure 2.9. It has advantages of performing in a wide temperature range and does compensate while in operation. Because of its fast response, it can be used in high frequency applications.

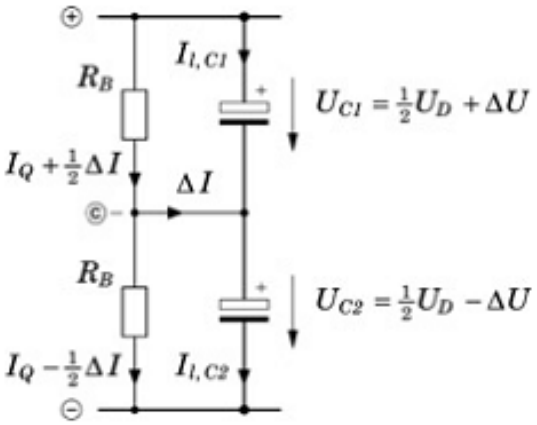


Figure 2.8: The schematic of passive balancing circuit (Ertl, Wiesinger, & Kolar, 2008)

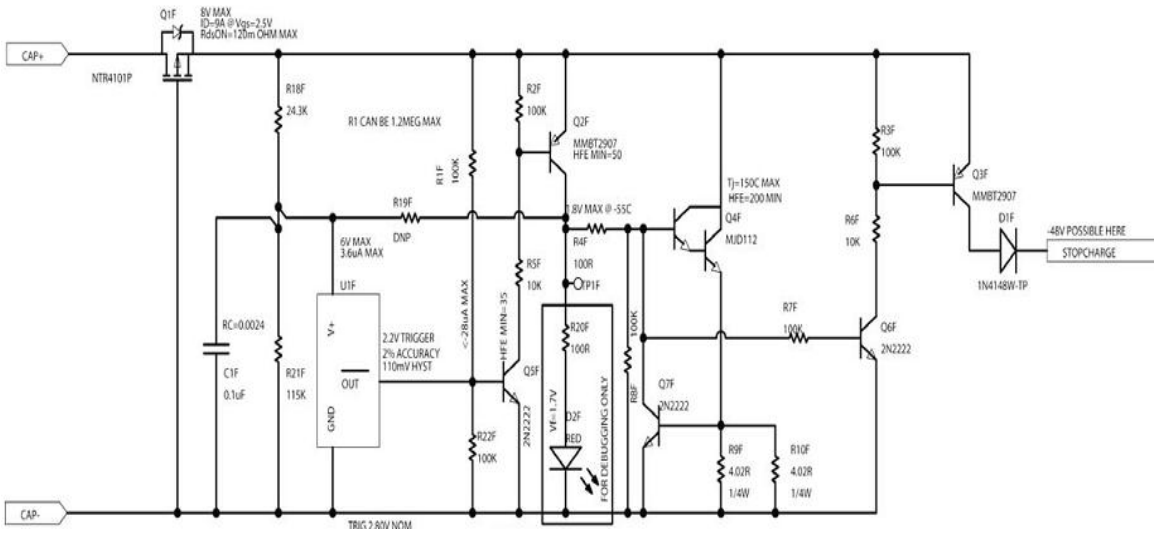


Figure 2.9: The schematic of active balancing circuit (*Maxwell Technology*)

2.15 Modelling

Computer aided modelling is a term for a mathematical model, for simulating circuitry performance under laboratory circumstances. The equivalent model of a supercapacitor helps to understand its performance under certain conditions, and also helps the developer to simulate their project in conditions that are not easy to achieve in practice. The simulation results are very important evidence that confirm the experimental results.

Typically the supercapacitor model is described as a RC circuit. An equivalent circuit in Figure 2.10 shows a first order model. It contains

- A capacitor C
- An inductor XI
- Rs Electrode dynamic representation of ESR (equivalent series resistance)
- A parallel resistance Rp representing as the energy leakage

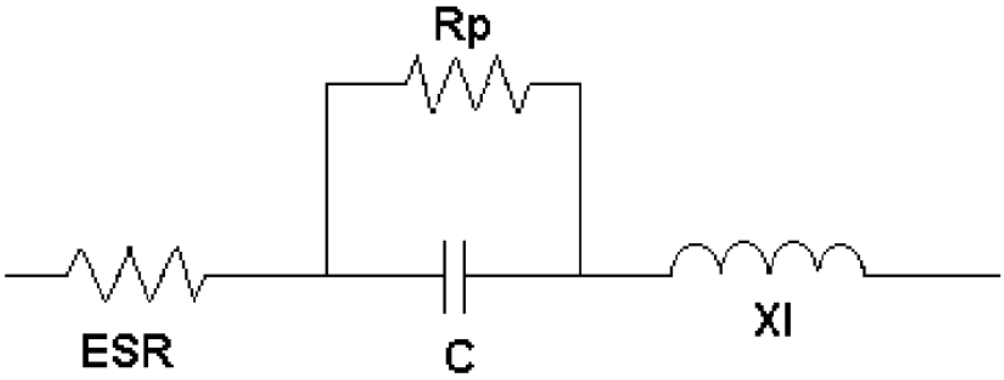


Figure 2.10: The first order supercapacitor model (Illinois Capacitor INC., 2013)

However, this model cannot accurately describe supercapacitor behavior in the high frequency environment. Therefore a complex impedance model developed contains an inductor, a series resistance and the complex impedance, as shown in Figure 2.11.

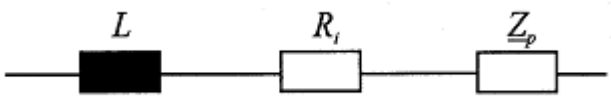


Figure 2.11: Advance equivalent circuit of a supercapacitor (Schiffer, Linzen, & Sauer, 2006)

The equation 2.10 gives the mathematical expression for complex impedance Z_p.

$$\underline{Z}_p(j\omega) = \frac{\tau \cdot \coth(\sqrt{j\omega\tau})}{C \cdot \sqrt{j\omega\tau}}$$

(2.10)

(Buller, Karden, Kok, & De Doncker, 2002)

The leakage current is defined as a gradual loss of stored energy, which is also effected by the temperature variation. A logarithm of the leakage current is plotted in Figure 2.12 versus the reciprocal of the temperature in °K. (The measurements do not exhibit a straight line, which are only able to be used for leakage current estimation.)

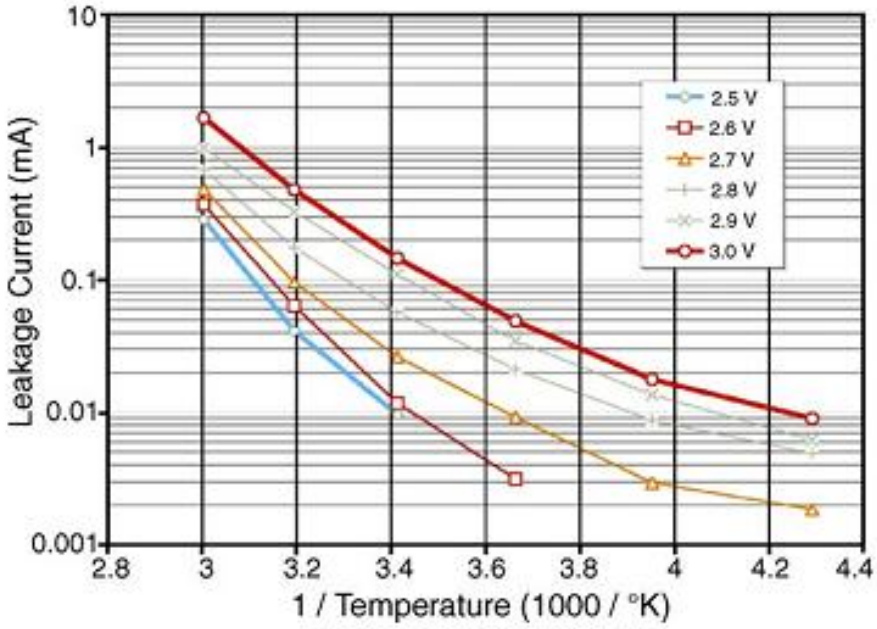


Figure 2.12: Temperatures affect to the behavior of leakage current (Kötz et al., 2006)

2.16 Surge withstand capability

The supercapacitor surge withstand capability was evaluated by Nihal Kularatna and his team. The supercapacitors with different commercial brands have been used for the experiment, which included Cap-xx, Nesscap and Maxwell Boostcap; the electrical characteristics summarized in Table 2.1.

Table 2.2 A summary of test results applicable to the three supercapacitor families (Kularatna et al., 2011)

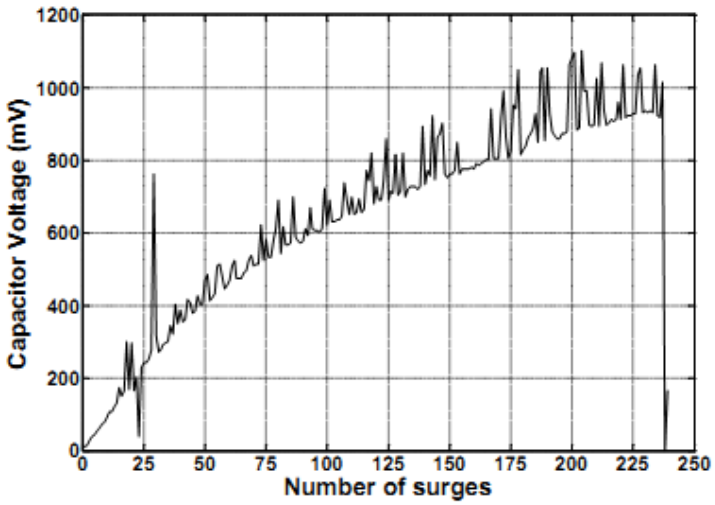
Device data	LSS output peak voltage	Number of surges to destroy the device			
		No pre-charge	Pre-charge voltage =250mV	Pre-charge voltage =500mV	Pre-charge voltage =1.8V
Cap-xx 0.18F, 2.3V	6.6kV	220 to over 250	Over 220	Over 180	Over 160
Maxwell 230F, 2.5V	6.6kV	No pre-charge	Pre-charge voltage =200mV	Pre-charge voltage =1.0V	Pre-charge voltage =2.5V
		Did not fail after 1000	Did not fail after 600; Charge accumulation was not observed	Did not fail after 600; Over the period of 700 repeated surges 0.1V discharge was observed	Did not fail after 600; Over the period of 700surges a discharge of 0.2V was observed
NessCap 90F , 2.7V	6.6kV	No pre-charge	Pre-charge voltage =500mV	Pre-charge voltage =1.0V	Pre-charge voltage =2.0V
		Did not fail after 600	Did not fail after 600; No charge accumulation observed	Did not fail after 600; Slight discharge of 0.15V observed during 700 surges	Did not fail after 600; Discharge of approx 350mV was observed over 700 surges.

Those capacitors have been subjected to three different experiments:

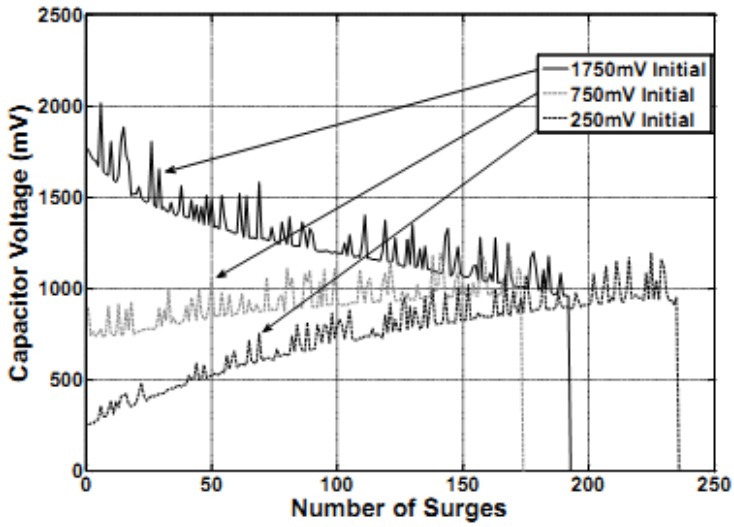
- Uncharged supercapacitor with repeated surges applied.
- Repeated surges applied when the supercapacitors initially hold voltages.
- Repeated surges applied when the supercapacitors operated in voltage cycling.

Figure 2.13 (a) indicates the test sample of 0.18F supercapacitor from Cap-xx could easily withstand over 200 hits of 6.6kV surges before a failure. The surges

has absorbed and resulted in an increase of terminal voltages. In the pre-charging test (in Figure 2.13 b), the supercapacitor initially holding at high voltages (over 1.8V for 1.8F), which keeps discharge when surges applied. While low pre-charging voltages did not show the same effect.



(a)



(b)

Figure 2.13: Waveforms show voltage across Cap-xx (0.18F, 2.3V) after repeated 6.6kV surges (a) uncharged supercapacitor, (b) with initial charge varying from 200mV to 1.8V (Kularatna et al., 2011)

Repeated surges were applied to the supercapacitor of Cap-xx 0.18 F during the

voltage cycling. The Figure 2.14 demonstrates a failure after over 350 repeated surges were applied.

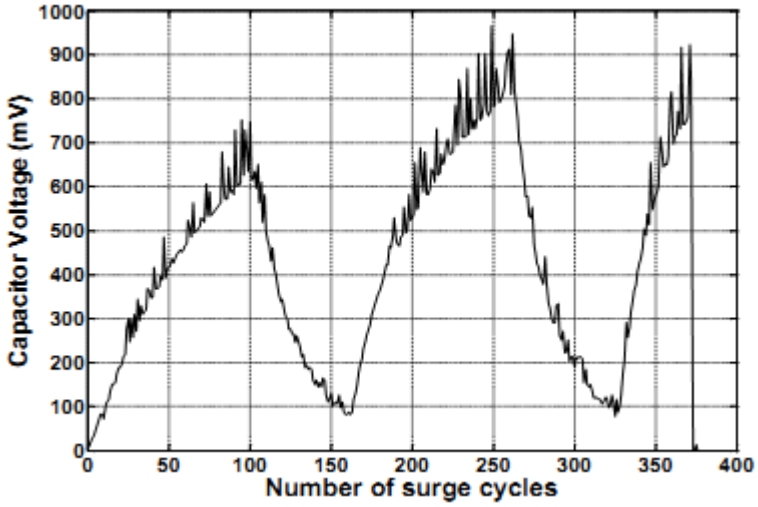


Figure 2.14: Surges are applied to charge the Cap-xx branded SC, after 100 surge applications SC discharges across a 200 Ω resistor. This is repeated until failure (Kularatna et al., 2011)

In summary, the supercapacitors present a robust surge withstand capability. This property can be used for developing the surge suppression system.

2.2 Charge circuit

This research is continual development based on original SRUPS. The major issue of previous design is the usage of a complicated charger. For this weakness, a flyback type charger proposed, which has advantages of minimum components contain and high common mode transient rejection. Therefore, next section will discuss fundamentals of flyback converter topology and transformer design.

2.21 Flyback converter

Low cost and simplify are the major advantages of the flyback topology. The primary specifications for an off-line flyback power supply design are highlighted on the following (Kularatna, 2008):

- Nominal AC input voltage

- Minimum and maximum AC input voltage
- Output voltage
- Maximum output overshoot, full load to no load
- Target efficiency at full load
- Holdup time at nominal AC input voltage and full load at output

Principally, a switch (MOSFET or IGBT is shown as Q1 in Figure 2.15) is used to control the electrical energy storage via the primary winding, where the energy is stored while the switch is on, and the electrical energy is released to the secondary when the switch is off. A diode is on the secondary side that allows the current flow only when the switch is off.

Waveforms show in Figure 2.16, the primary windings get charged as presenting an increase of drain current, during the switch is on. The diode current indicates the energy transfer though the weak coupling to the secondary side, it happen during the switch is off. Switching circuits have parasitic inductance, as well as the transformer and diode have parasitic capacitance. Those will affect the charging circuit performance.

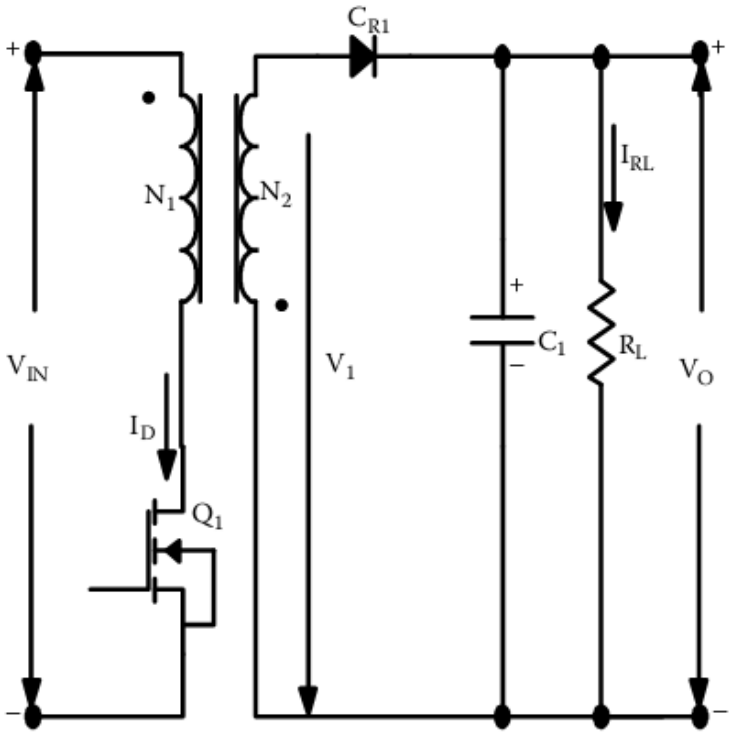


Figure 2.15 A flyback circuit (Kularatna, 2008)

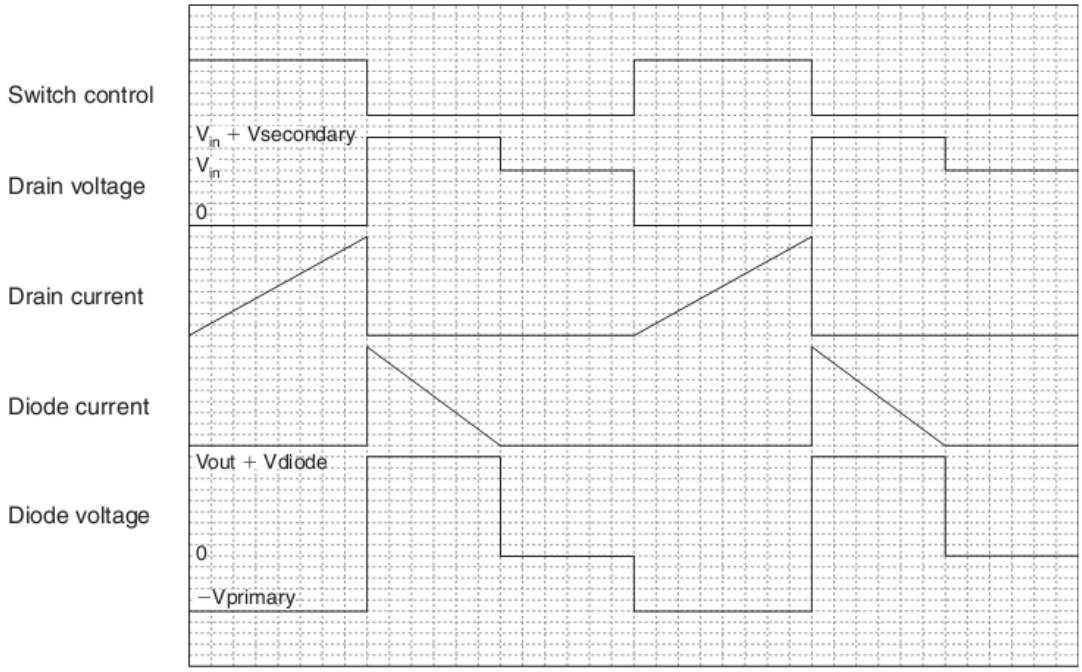


Figure 2.16: Operational waveforms for the flyback circuit in discontinuous mode (Brown, 2007)

2.22 Transformer design

The flyback transformers operate in the flyback mode. Principally, a switch (MOSFET or IGBT) is used to control the electrical energy storage via the primary winding, where the energy is stored while the switch is on, and the electrical energy is released to the secondary when the switch is off. A diode is on the secondary side that allows the current flow only when the switch is off.

To improve the potential of energy storage, the transformer usually employs a ferrite core with an air gap as depicted in Figure 2.17. The energy highly concentrated in the air gap between the core face, because reluctance in the air gap is much higher than magnetic core. The major proportion of magnetic flux is cycling inside the ferrite core. However in practical applications, small amount flux will flow outside the magnetic circuit resulting in flux leakage. The occurrence of high magnetic flux concentrates in the air gap, which is used to improve the inductor saturation.

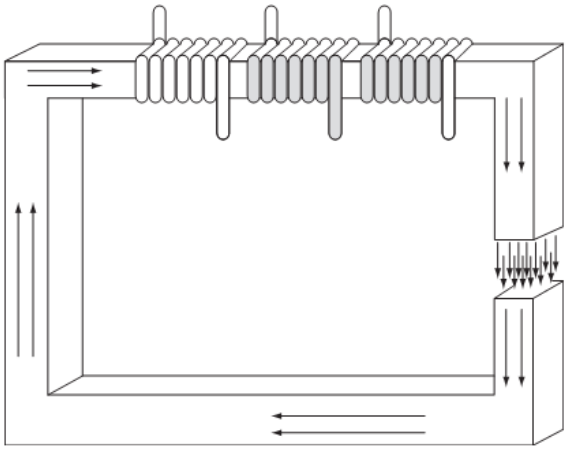
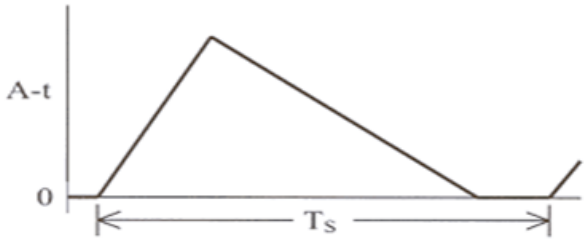


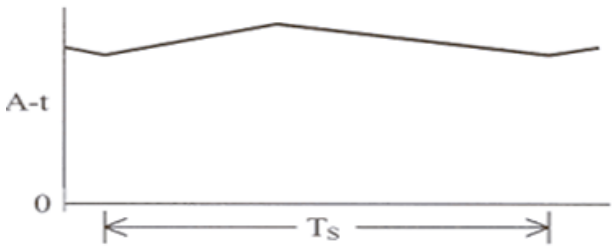
Figure 2.17: A ferrite core with three windings (Brown, 2007)

2.23 Continuous and discontinuous mode

A flyback circuit is able to operate in either continuous or discontinuous mode. In the continuous mode (in Figure 2.18 b), inductor current of all windings never reach zero. In the discontinuous mode, the energy releases from the transformer primary (energy store in the primary inductor) decreases and finally goes to zero, thus the zero current occurs in the all the windings during a part of cycle. The discontinuous current waveforms are depicted in Figure 2.18 (a).



(a) The current waveform in the discontinuous mode



(b) The current waveform in the continuous mode

Figure 2.18: The waveforms of winding current in (a) discontinuous mode and (b) continuous mode (Dixon, 2000)

Both of continuous and discontinuous modes have advantage and disadvantage. The primary advantage of continuous mode is that the current ripple in the conductor is relatively smaller. It requires a simpler smoothing circuit at the transformer secondary side. The peak current compare to discontinuous mode is almost one – half at the same power level. However, a complicated control loop is necessary to keep the current fluctuation in a small window.

The discontinuous mode circuit is used to operate in large peak current. The advantage is that lower thermal stresses drop on the transformer switch, because the current begins from zero and only portion of the input voltage is applied to the switch. The inductor current drop back to the origin at every end of cycle, therefore reserve current across the diode can be negligible, which avoid the diode reserve breakdown. However a requirement of higher inductance of all of transformer windings, because it is efficiently saturated under the high peak current force.

When the flyback transformers are either operated in the continuous or discontinuous mode, the current in each winding is always highly discontinuous, regardless of inductor current mode. However, the continuous mode exhibits lower core loss because of smaller current ripple.

2.4 Transformer equivalent circuit

The equivalent of ideal transformer shows in Figure 2.20, which helps to understand the energy transfer behavior. The resistance and leakage reactance of the transformer are imagined to be external to the winding. The no-load current I_o divides into two parallel branches. The pure inductances X_o carry the magnetizing component I_u, and non-inductive R_o carry the active component I_w.

The magnetizing component I_u is 90° behind the V_1 because of inductance, while the active component I_w is in phase with V_1. Hence the no-load primary input current is the vector sum of I_w and Iu, which lags V_1 by an angle θ. The

vector diagram of primary input current shows in Figure 2.19.

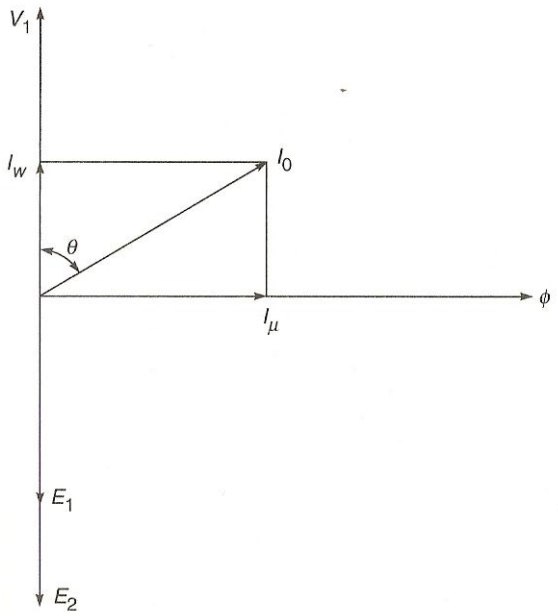


Figure 2.19: Vector diagram of no-load current of ideal transformer (Bharat Heavy Electrical Limited, 2003)

As seen from Figure 2.19, the primary current has two components.

- The active component I_w is in phase with V_1, which is taking the iron-loss plus the copper-loss of primary winding.

$$I_w = I_0 \cos \theta_0$$

(2.11)

(Bharat Heavy Electrical Limited, 2003)

- The magnetizing component is in quadrature with V_1, its expression can be presented as

$$I_\mu = I_0 \sin \theta_0$$

(2.12)

(Bharat Heavy Electrical Limited, 2003)

- The Io is the vector sum of I_w and I_u, hence

$$I_0 = \sqrt{I_\mu^2 + I_w^2}$$

(2.13)

(Bharat Heavy Electrical Limited, 2003)

- R_1 and X_1 represent the transformer input resistance of primary winding. Hence the primary impedance is given by

$$Z_1 = \sqrt{(R_1^2 + X_1^2)}$$

(2.14)

(Bharat Heavy Electrical Limited, 2003)

- R_2 and X_2 represent the leakage reactance of secondary winding, the secondary impedance is given by

$$Z_2 = \sqrt{(R_2^2 + X_2^2)}$$

(2.15)

(Bharat Heavy Electrical Limited, 2003)

And

$$V_1 = E_1 + I_1 (R_1 + jX_1) = E_1 + I_1 Z_1$$
$$E_2 = V_2 + I_2 (R_2 + jX_2) = V_2 + I_2 Z_2$$

(2.16)

(Bharat Heavy Electrical Limited, 2003)

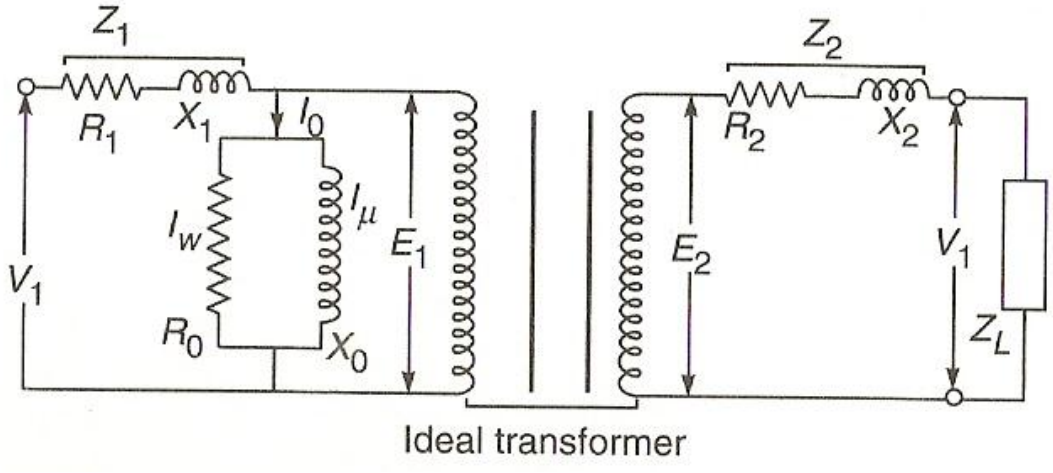


Figure 2.20: A model for an ideal transformer (Bharat Heavy Electrical Limited, 2003)

2.25 Energy losses in the transformer winding

2.251 Hysteresis losses

Hysteresis loop presents energy lost in the core. The large area of hysteresis loop is associated the high energy lost, Figure 2.21 shows the hysteresis loop curves due different ferrite materials. This phenomena occurs because of the flux density B is always lag behind the field intensity H. The loss occurs on every half cycle when the magnetic field reserves the direction, and energy is expended. To reduce the loss, a ferrite core with low hysteresis is required. In general, hysteresis losses will increase with frequency. To accurately calculate the hysteresis losses regarding the high frequency consideration, please refer to references of soft ferrites written by Snelling and 2.21, which the equations are available.

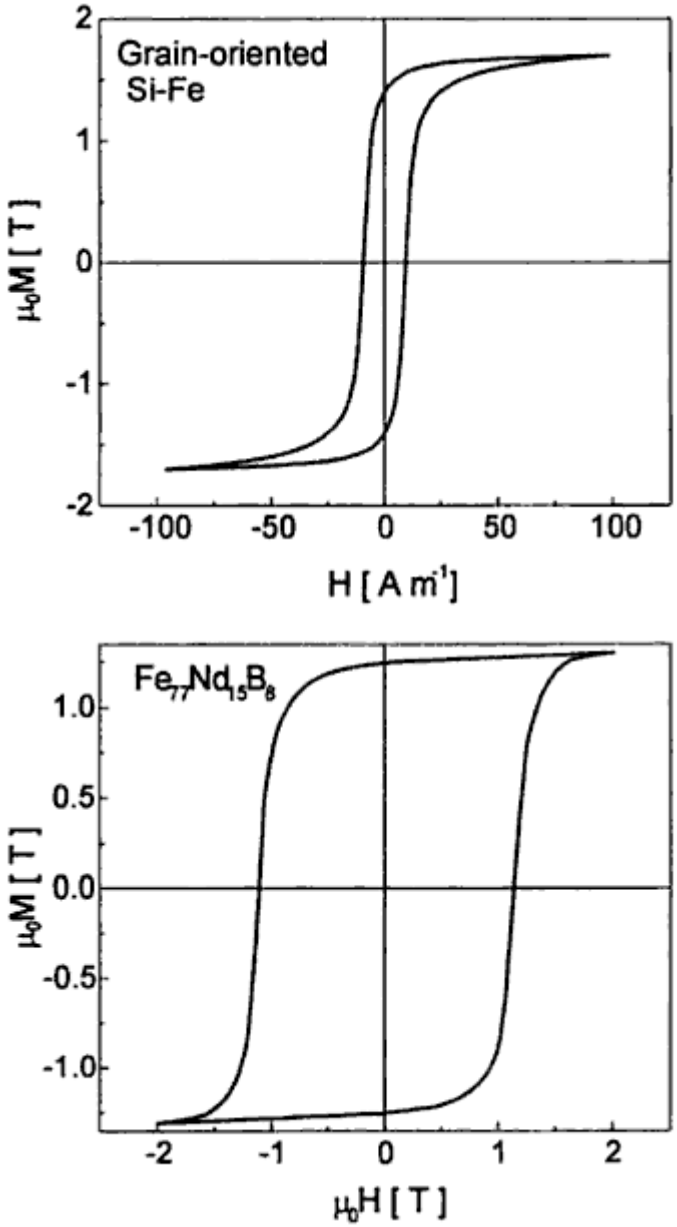


Figure 2.21: Hysteresis loops with different factors (Bertotti, 1998)

2.252 Eddy current losses

Figure 2.22 the symmetrical flied surround an around conductor that is carrying direct current (DC) or low frequency current. The energy losses are due to the DC resistance, which associate to the dimension of cross sectional area of conductors.

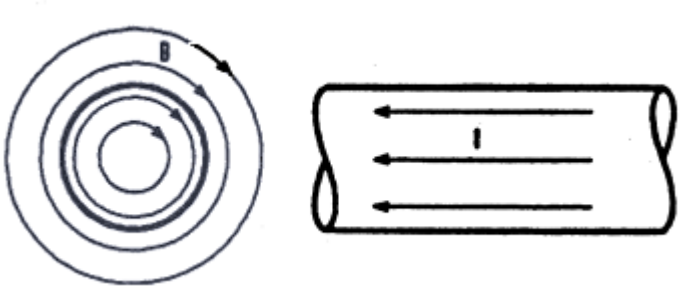


Figure 2.22: Uniform current flows in a conductor at low frequency (Dixon Jr, 1988)

Figure 2.23 depicts what happen when high frequency current flow in the conductors. The dash lines represent the uniform low frequency current distribution, and the circular lines represent the high frequency current distribution. The flow direction of current changes rapidly due to the high frequency, as well as the flux within the conductor is also changed rapidly. The result is that as frequency rises, where the current tends to concentrate towards the conductor skin, with a decrease of current density at the conductor center. Figure 2.24 describes that the current density at conductor center will tail off exponentially and toward zero if the frequency is rising continuously. Hence only potion of conductor carries the total current. In other words the conduct area is much smaller than the same conductor carrying low frequency current.

Figure 2.22: Eddy current at high frequency (Dixon Jr, 1988)

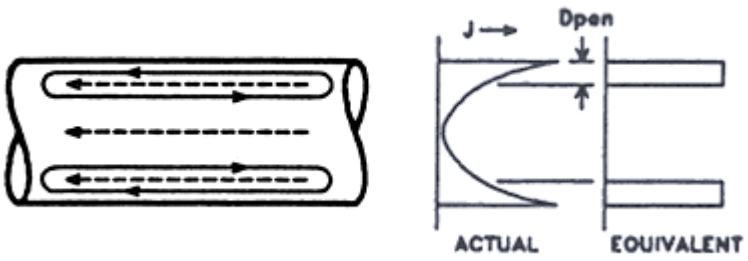


Figure 2.23: Current distributions at high frequency (Dixon Jr, 1988)

Penetration depth is defined as the distance from the surface to where the current density is 1/ e times the surface current density (is the natural log base)

$$D_{PEN} = [\rho/(\pi\mu f)]^{1/2} \text{ m}$$

(2.17)

(Dixon Jr, 1988)

$$D_{PEN} = 7.5(f)^{1/2} \text{ cm}$$

(2.18)

(Dixon Jr, 1988)

The equations of 2.17 and 2.18 are accurate for a flat conductor surface. For the curveted surface the actual penetration depth is smaller than the calculation.

A equivalent circuit mode in Figure 2.24 demonstrates current behavior at high frequency. When the current (I) flow into L_X that represents inductance of the wire at high frequency. The energy store in the external magnetic field L_X will be 0.5 $L_X I$. Point A represents the outer surface of the conductor, and B is internal. The resistance from the surface to the center divides into many concentric cylinders of equal cross section area, which are represented as Ri. The internal inductance Li store energy through the cylindrical sections. The energy store in each section depends on the cumulative current flowing through those elements from the left to the right. The external inductance L_X (represents leakage inductance of the winding) and the source compliance voltage limits the maximum charge radio of the wire, regardless of how fast the switch turns on.

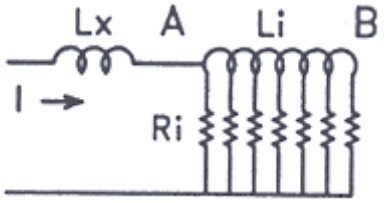


Figure 2.24: Equivalent circuit of a conductor (Dixon Jr, 1988)

2.26 Proximity effect

Proximity effect defines that two close wire carrying equal current in the opposite direction, the magnetic field generated by the wires will cancel each other. This cancellation will results in the concentrated field volume decreases, thus the inductance is reduced.

2.27 Multiple layers

Many transformer applications consist of multiple layers in order to reduce the size of the transformer. Figure 2.25 shows a transformer with multiple layers carrying a low frequency current and the energy density diagrams. At low frequency current (not shown) is uniformly distributed through all windings, because they are much thinner than the penetration depth. The energy diagram shows energy density concentrate and peak at center, and present minor leakages. However at the high frequency, the eddy current losses increase exponentially due to multiple layers.

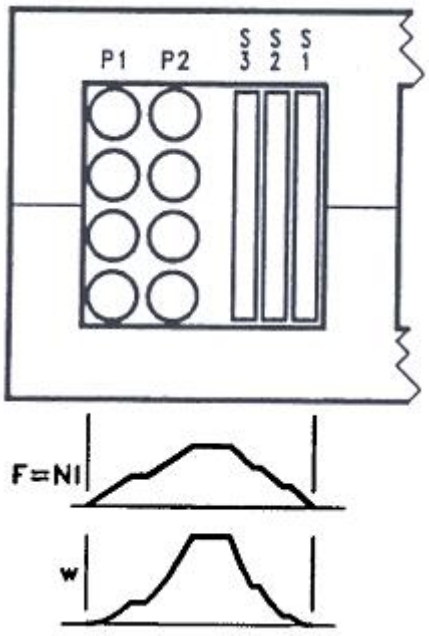


Figure 2.25: Multiple layer windings (Dixon Jr, 1988)

2.28 Litz wires

The first transformer made for this research presented high energy losses. The reason for those losses was due to winging made of solid wires. The resistance of solid wire at low frequency is associated on their across sectional area. Larger cross section area results in the lower resistance. However a charging circuit designed for this research operated at high frequency in the range of 50 kHz. In the high frequency environment, the current is concentrated close to the conductor surface, which results reduction of cross sectional area, while the AC resistance of conductor is increased. The litz wire is used as an alternative conductor to minimize the energy losses that exhibit in the solid wire, as well as to eliminate proximate effect. It consists of many isolated wires, which are stranded and twisted to form a rope. The standard twist configuration is 18 – 36 twists per meter, and typical diameters of the strands are 0.05, .071, 0.1, 0.15, 0.2 and 0.8 mm (Sullivan, 1997). It usually protected by nylon textile or yarn, in order to add the extra strength. The litz wire increases the surface area without increasing the net size of conductor. Figure 2.26 shows both wires have almost same net diameter, but litz wire provides larger surface area. The overall eddy current loss at high frequency represent as

$$P_{loss} = F_r I_{ac}^2 R_{dc}$$

(2.19)

(Sullivan, 1997)

Where :

- F_r is a factor relating to DC resistance to AC resistance which accounts for all winding losses.
- I_{ac} is root mean square (rms) value of sinusoidal current.
- R_{dc} is DC resistance of winding.

The approximation effect can be expressed as

$$F_r = 1 + \frac{\pi^2 \omega^2 \mu_0^2 N^2 n^2 d_c^6 k}{768 \rho_c^2 b_c^2}$$

(2.20)

(Sullivan, 1997)

Where :

- ω is the radian frequency of AC current.
- ρ_c is the resistivity of copper conductor.
- N is the number of turns.
- n is the number of strands.
- B_c is the breadth of the window area of the ferrite core.
- K is a factor of net field distribution.

The resistance of litz wire winding is independent of the number of layers, assume the DC resistance of litz wire is similar to the solid wire, it can be expressed as

$$\frac{4\rho_w \iota_w}{\pi d^2} = \frac{4\rho_w \iota_{w\iota}}{n\pi d_\iota^2}$$

(2.21)

(Sullivan, 1997)

Obtain the number of strands, equation is rearrange as:

$$n = \frac{\iota_{w\iota}}{\iota_w}\left(\frac{d}{d\iota}\right)^2$$

(2.22)

(Sullivan, 1997)

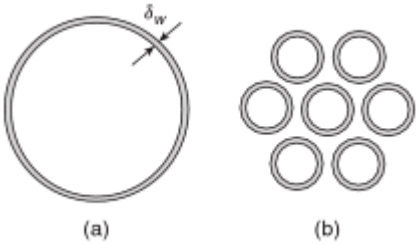


Figure 2.26: The litz wire has larger surface area than a round solid wire, (a) solid wire, (b) litz wire (Sullivan, 1997)

2.29 Snubbers

Snubber is a protection circuit where the circuit configuration is very simple. Two typical arrangements are the resistor–capacitor (RC) damping network and the resistor–capacitor–diode (RCD) snubber. They are usually placed across the switches to limit the clamping voltage on the switches, as well as to improve the switching performance. The main purposes of the snubber are:

- Limit or eliminate voltage or current spike across switches
- Limit the clamping voltage on the switches
- Reduce total loss due to switching

2.291 Resistor-capacitor snubber design

The resistor-capacitor (RC) snubber consists of a resistance (R_s) and capacitor (C_s), which is connected across the switch in parallel, the Figure 2.27 demonstrates a typical RC snubber circuit. For the RC snubber must obey $C_s > C_p$. Cs usually chooses as twice the sum of the output capacitance of the switch and the estimated mounting capacitance. R_s is selected so that $R_s = E_o/I_o$. Hence the voltage across the RC network due to the initial current flowing in R_s is no greater than the clamped voltage. The power dissipation in Rs can be estimated from peak energy stored in C_s:

$$U_p = \frac{C_s E_0^2}{2}$$

(2.23)

(Severns, 2006)

The capacitance of C_s charge and discharge at the switching frequency, the average power dissipation in R_s can be expressed as:

$$P_{diss} \approx C_s E_a^2 f_s$$

(2.24)

(Severns, 2006)

The equation above is to estimate power dissipation, but the actual power dissipation may slightly higher than this calculation.

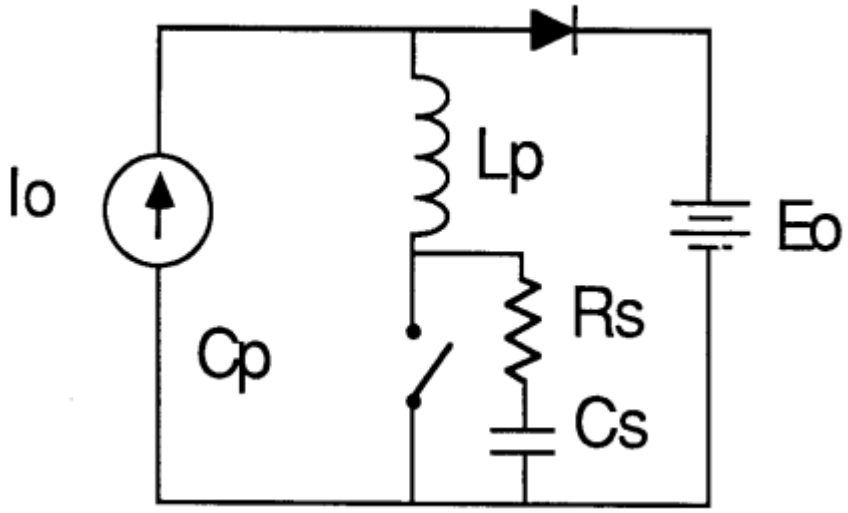


Figure 2.27: Snubber circuit using Resistor-Capacitor network (Severns, 2006)

2.292 Resistor-capacitor-diode snubber design

The resistor-capacitor-diode (RCD) in Figure 2.28 snubber has several advantages over the basic RC snubber. It minimizes losses in both switching and snubber circuit. It allows the load line to pass well within the safe operating area (SOA). It also takes the shunt capacitance C_p into the snubber circuit design, the total capacitance of snubber is sum of C_p and C_s. However the disadvantage is that the initial charging current into the capacitor Cs is relatively larger, because effective resistance of diode (D_s) is much lower than C_s. During the charge period of C_s, the effective value for RS is essentially zero.

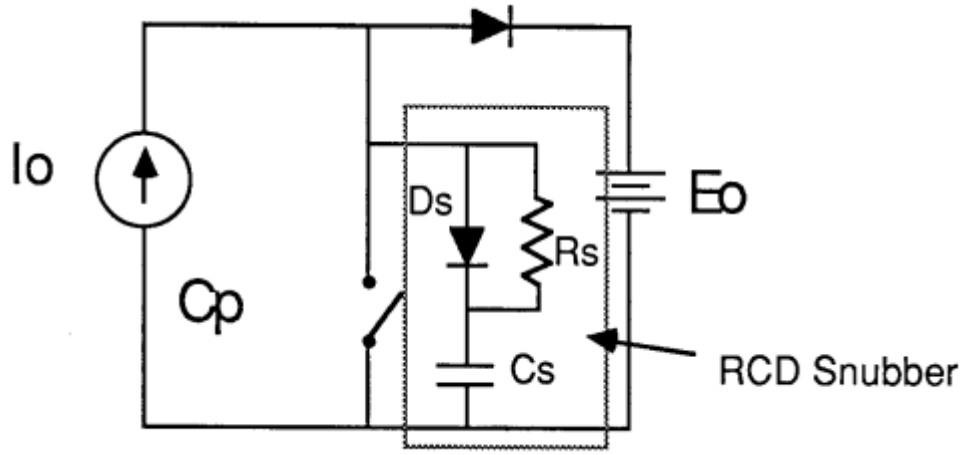


Figure 2.28: Resistor-Capacitor-Diode snubber circuit (Severns, 2006)

Figure 2.29 shows a pure (assuming the inductance Lp is zero) turn-off waveforms for RCD snubber circuit. The snubber capacitor C_s takes charge when the switch is sudden off. It is resulting a gradually increase voltage across the switch, in order to protect the switch from the overvoltage damage.

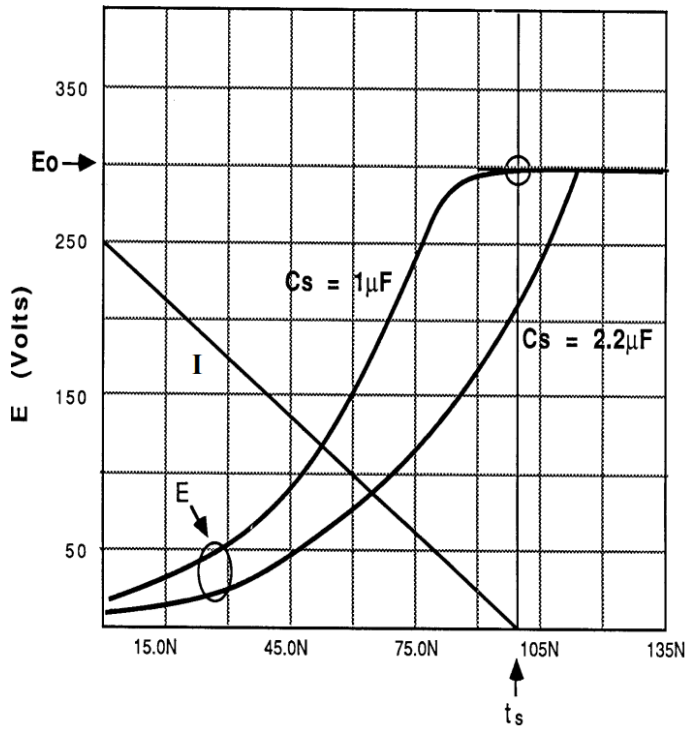


Figure 2.29: V-I characteristics of RCD snubber (Severns, 2006)

The requirement is to balance the switch loss and snubber loss by optimizing the

value of C_s and C_n. To choose a large C_s brings the negative consequence of increasing the snubber loss. In Figure 2.30 describes the relationship of switching loss and snubber loss by using different sizes of C_s. To obtain the minimum net losses for a snubber circuit, is to balance the switch losses, for more information, please refer to snubber for power circuit written by Rudy Severns (Severns, 2006).

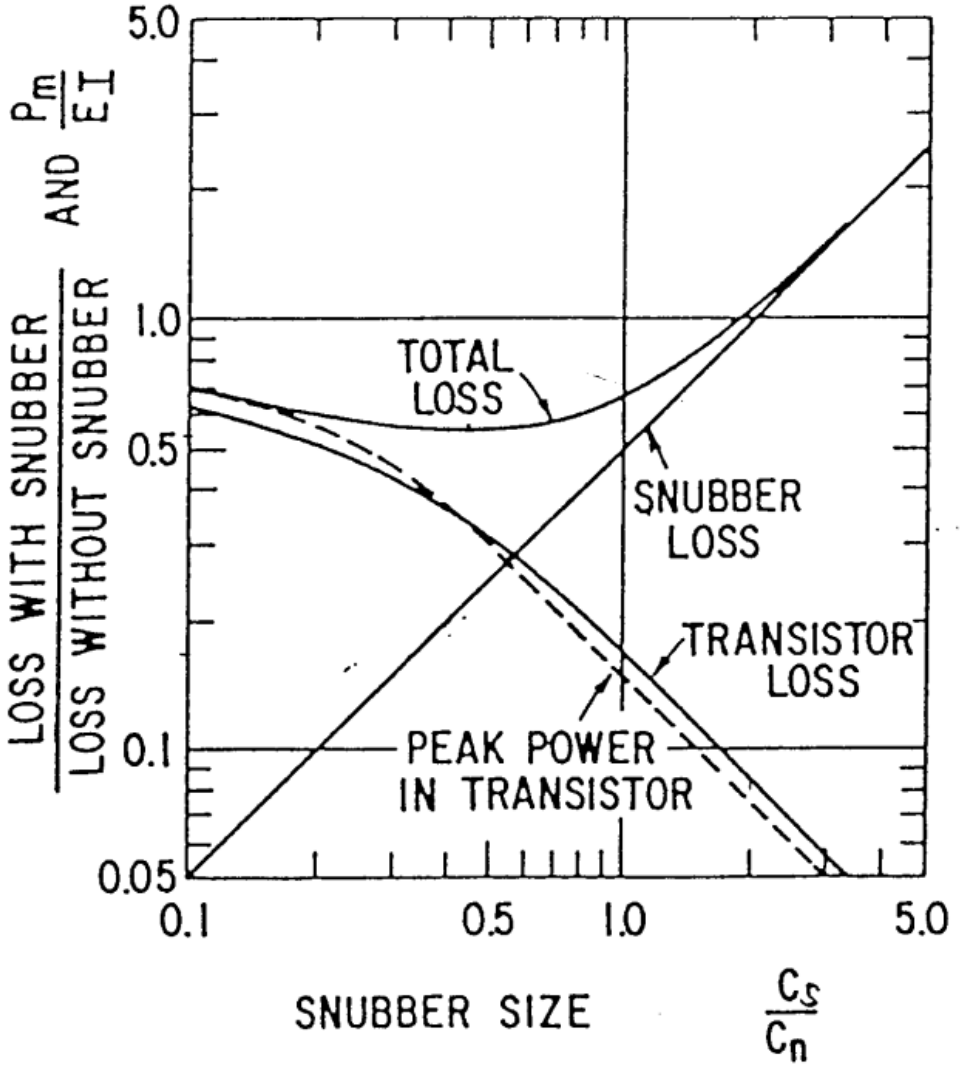


Figure 2.30: The net losses versus snubber sizes (Severns, 2006)

Figure 2.31 shows a comparison of voltage waveforms between RC network snubber and RCD snubber. Note that both snubber circuits use same value of components. The RCD has an advantage of lower net loss, but the overshoot voltage is higher than the RC snubber.

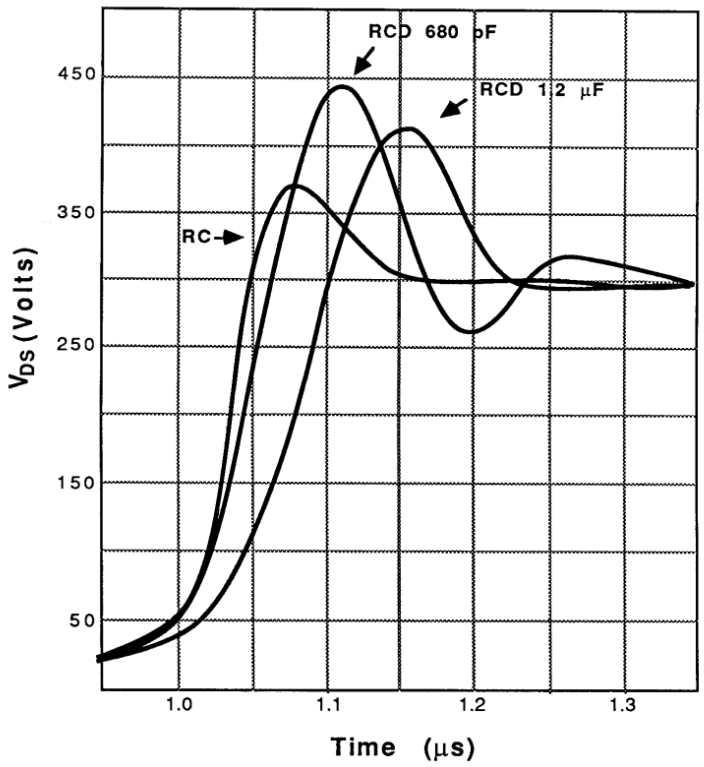


Figure 2.31: Comparison waveforms between RC snubber and RCD snubber (Severns, 2006)

2.3 Power factor correction

The power factor is very important to the power applications. In the switching power supplies, the typical input circuit and its associated waveforms are shown in Figure 2.32. As the result, the rectifier can only conduct when the AC line voltage exceeds the voltage on the input filter capacitor. Hence a current draws during a small fraction of the half cycle duration. Improving the poor power factor, the correction circuits are intended to increase the conduction angle, the corrected current waveform is shown in Figure 2.33. The net result is that the peak and RMS current drawn from the line is reduced.

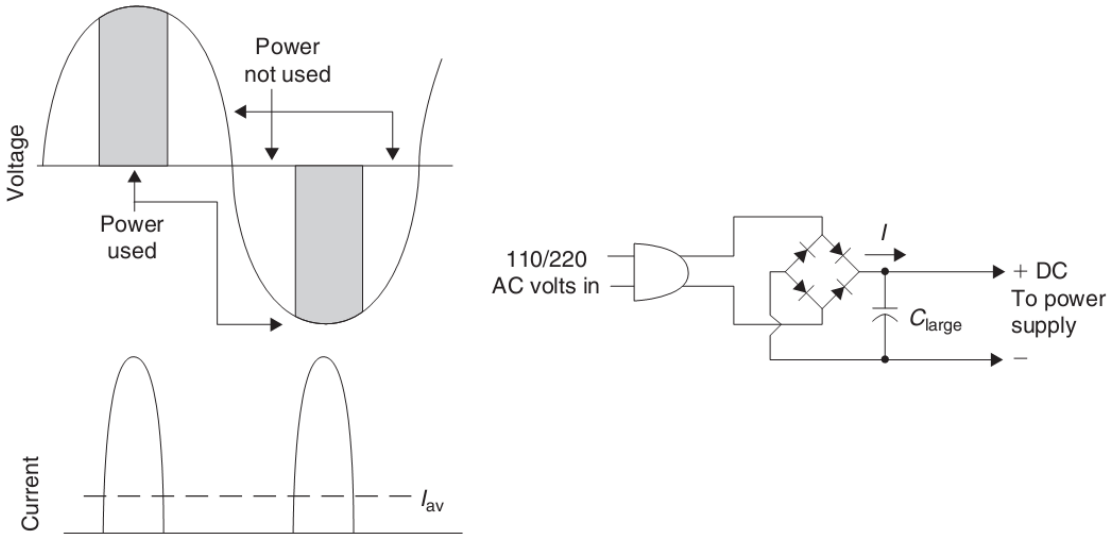


Figure 2.32: The waveforms of a capacitive input filter (Brown, 2007)

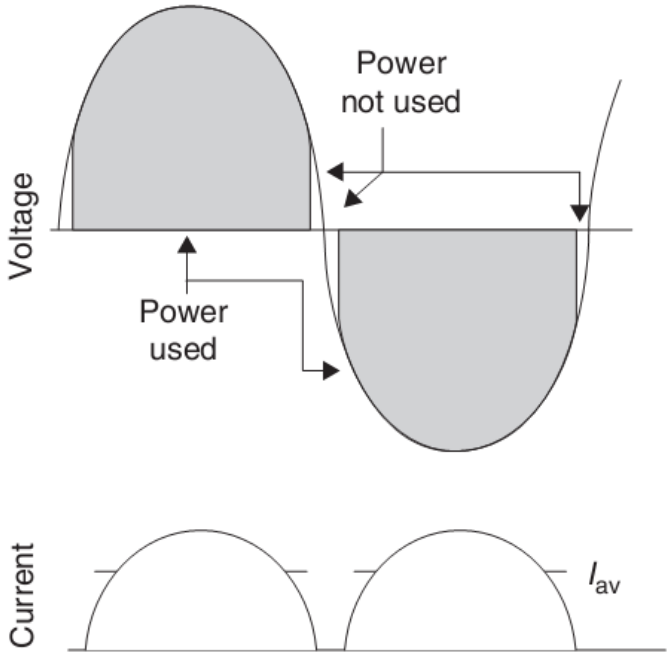


Figure 2.33: Power factor corrected input (Brown, 2007)

2.4 Insulated gate bipolar transistors

MOSFETs operate as switches, which are commonly used in the power applications. However, the on-resistance of such devices increases with increasing drain-source voltage capability. The practical voltage capability due to this limitation is below a few hundred volts (Kularatna, 1998).

To combine the advantages of power MOSFETs and BJTs, a new device of

insulated gate bipolar transistor (IGBT) is developed. It has voltage-controlled gate, high-speed switching and low saturation voltage. Its symbol, circuit structure and V-I characteristics are plotted in Figure 2.34.

For the purpose of quick design a switch in power applications, the available devices are listed in the table for comparison.

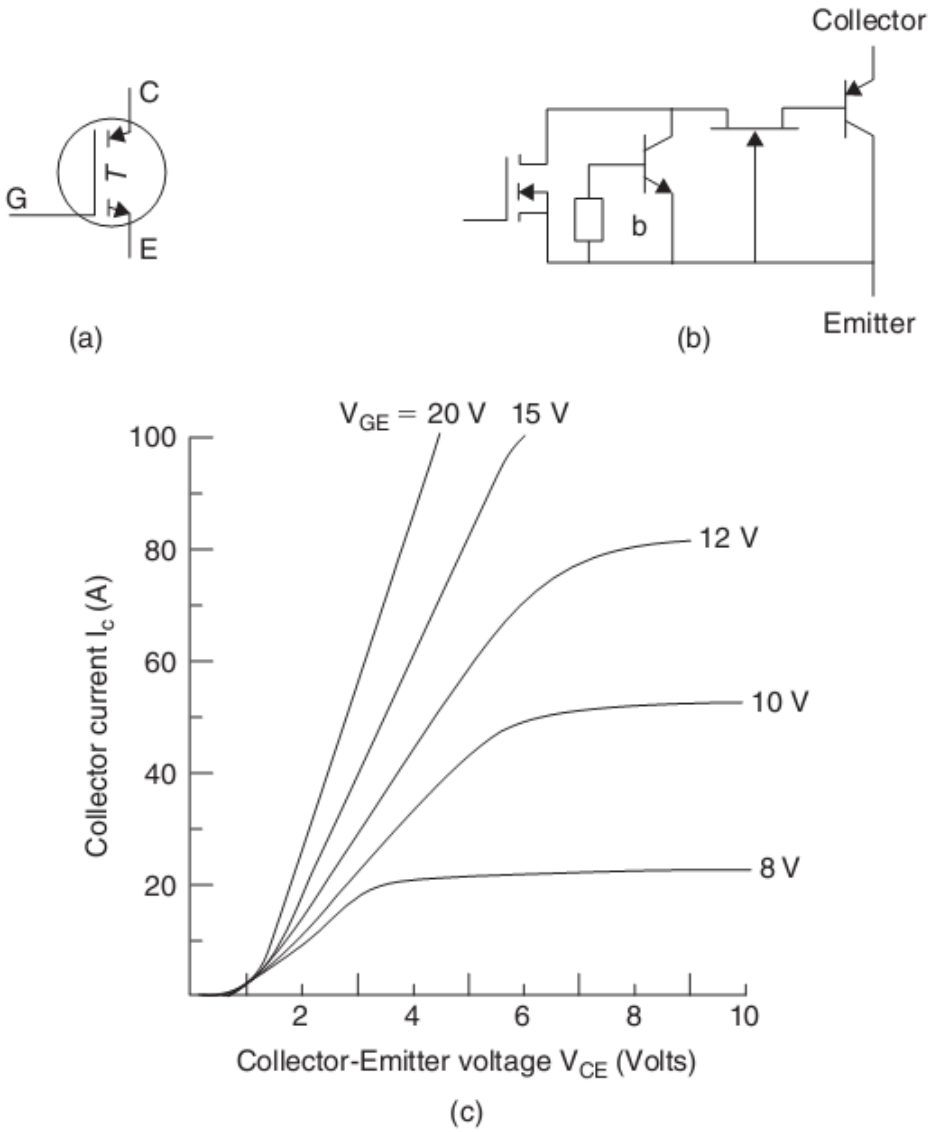


Figure 2.34: IGBT (a) Symbol (b) Equivalent circuit (c) typical output characteristics (Brown, 2007)

Table 2.3 Characteristics of IGBT, power MOSFETs, bipolars and darlingtons (Brown, 2007)

	Power MOSFETs	IGBTs	Bipolars	Darlingtons
Type of Drive	Voltage	Voltage	Current	Current
Drive Power	Minimal	Minimal	Large	Medium
Drive Complexity	Simple	Simple	High (large positive and negative currents are required)	Medium
Current Density for Given Voltage Drop	High at Low Voltage—Low at High Voltages	Very High (small trade-off with switching speed)	Medium (severe trade-off with switching speed)	Low
Switching Losses	Very Low	Low to Medium (depending on trade-off with conduction losses)	Medium to High (depending on trade-off with conduction losses)	High

2.5 Surge waveforms

To develop a surge resistant UPS using supercapacitor technology, the system must test in the surge environment for evaluating the surge withstand capability. Therefore, Understanding surge characteristics and its commercial standards help to design a proper test for evaluating.

The purpose of IEEE surge standard is recommendations for testing surge withstand capability where the equipment connects to low voltage AC power line. The standard is defined by collecting practical data over 30 years, initially started in 1980. It categorizes the environment where the surge hazards are frequently occurred, and demonstrates the respective surge waveforms.

The surges occurring in low-voltage AC power circuits originate from two major sources, lightning and switching. For identify the surge resources, they are simplified by considering different stresses that will be referred to as “scenarios I and II”, will discuss in the following section.

Scenario I is usually found in the household environment. As a first step toward a reduction of the complex database on surge occurrences for Scenario I, the concept of location categories is proposed, as depicted in Figure 2.35. Location

category A applies to the installation at some distance from the service entrance. Location category C applies to the external part of the structure, extending some distance into the building. Location category B is in between location categories A and B.

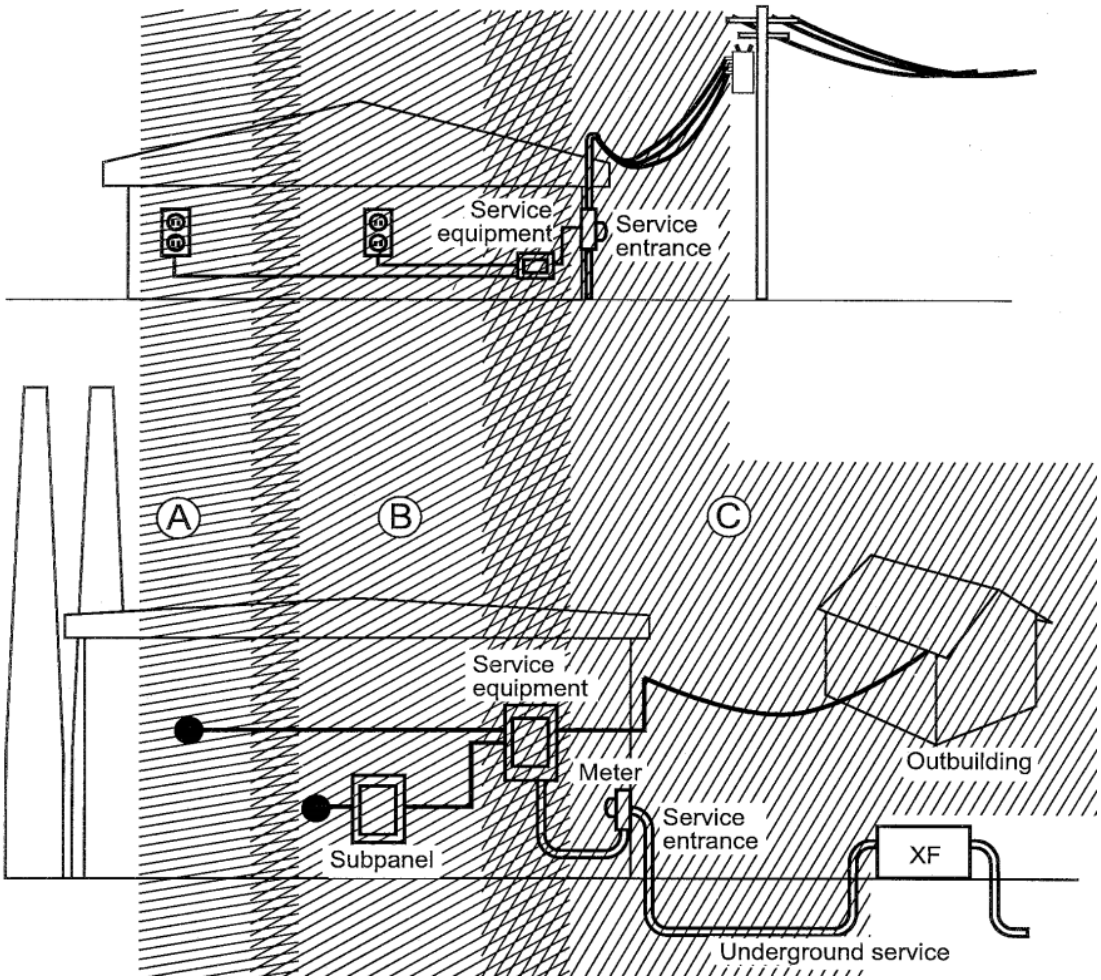


Figure 2.35: Proposal of location categories A, B and C in Scenario I (IEEE Std C62.45-2002)

Scenario II is proposed to describe the direct flash to the structure, or the flash hit on earth where is very close to the structure.

The UPS designed in this research is referred to the environment that proposed in Scenario I. The emergency power supply and protection is offered to the household equipment. According to this concept, the switching surges are commonly happened in this area. Therefore in the following section, a study is to discuss the different voltage waveforms, regarding to the switching surges. The

two seminal surges, ring wave and combination wave were deigned as standard surge testing waveforms. However, there are no specific models that are reprehensive of all surge waveforms, which are simplified and extracted into two typical waveforms for evaluating the surge withstand capability of the equipment.

2.51 Combination wave

The combination wave of open-circuit voltage and short-circuit current are shown in the Figure 2.36 and 2.37 respectively. The voltage amplitude across an open circuit is applied by a 1.2/50 μs voltage wave, and an 8/20 μs current wave into a short circuit. The tolerances are proposed by the IEEE Std C62.45-2002, the front time is 1.2 μs ± 0.36 μs, and duration is 50 μs ± 10 μs. The exact waveform that is delivered is defined as :

- The front time for voltage waveforms is 1.67 ($t_{90} - t_{30}$), where t_{90} and t_{30} are the time of the 90% and 30% amplitude points on the leading edge of the waveform.
- The current waveform is defined as 1.25 ($t_{90} - t_{10}$), where the t_{90} and t_{10} are the time of the 90% and 10% points on the leading edge of the waveform.
- The effective source impedance is specific as 2.0 Ω ± 0.25 Ω.

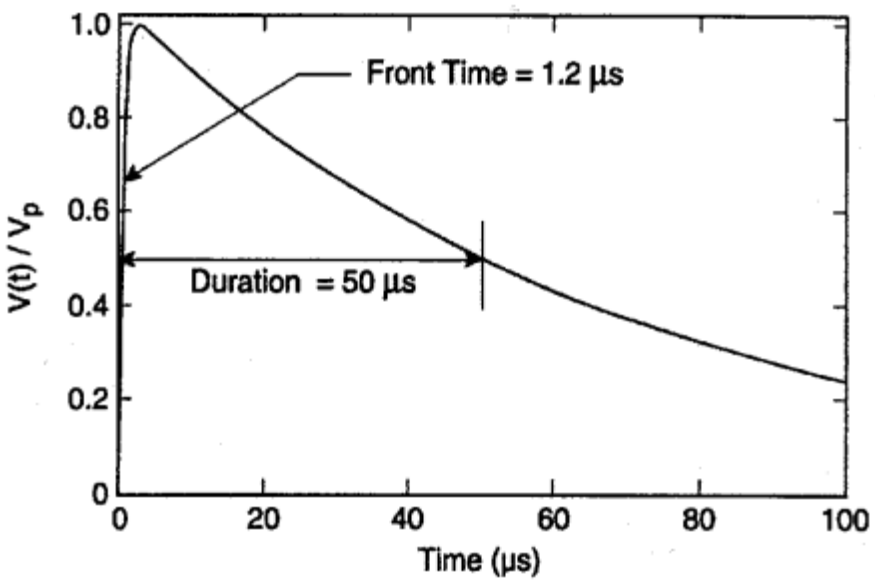


Figure 2.36: Combination wave open-circuit voltage (IEEE Std C62.45-2002)

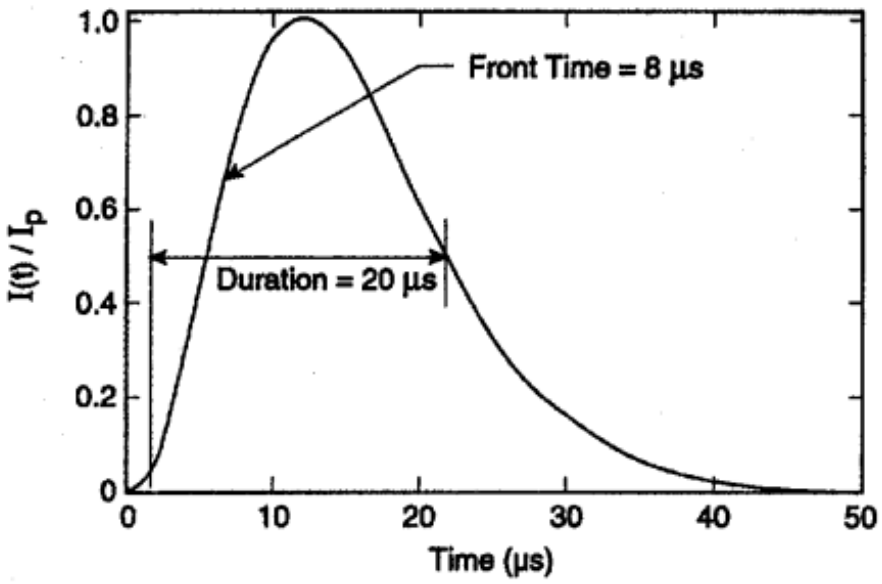


Figure 2.37: Combination wave short-circuit current (IEEE Std C62.45-2002)

2.52 100 kHz ring wave

The open-circuit voltage waveform of 100 kHz ring wave is plotted in Figure 2.38. The primary parameters are defined by the 0.5 µs rise time and 100 kHz ringing frequency. However, the tolerance may apply, according to IEEE Std C62.45-2002, the variation of rise time is between $\pm 0.15\ \mu s$, and the variation of the ringing frequency is between ± 20 kHz. The amplitude will decay so that the amplitude ratio of adjacent peaks of opposite is as follows:

- The ratio of the second peak to the first peak is between 40% and 90%.
- The ratio of the third to the second peak is between 40% and 80%, and also the fourth peak to the third is the same. It is unnecessary to set the voltage amplitude beyond the fourth peak. Because the amplitude decays the following peaks are much smaller than the initial peak. Hence the voltage stress from the following peaks can be ignored.
- The frequency is defined as the first completed cycle, which accounts from the first and third zero-crossing after the initial peak.
- The ratio V_p/I_p is specified as 12 Ω for simulation of Location Category B environments or 30 Ω for simulation of Location Category A environments. If the peak open-circuit voltage chooses to be 6 kV, the

short current will be 500 A and 200 A respectively.

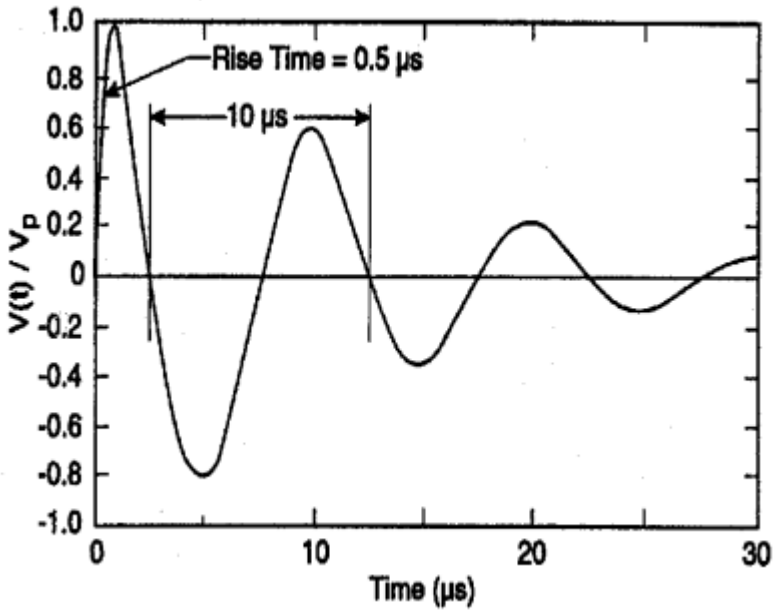


Figure 2.38: 100 kHz ring waveform (IEEE Std C62.45-2002)

2.53 The electrical fast transient burst

The electrical fast transient burst (EFT) Burst waveform consists of repetitive bursts. Each burst contains many individual unidirectional pulses. The voltage levels are defined by IEC 61000-4-4:1995, which include five test-severity levels, from 0.5 kV to 4 kV, the open-circuit voltage waveform is demonstrated in the Figure 2.39. The current waveform is defined when the generator is connected to a load of 50 Ω, and the frequency is varying between 1 MHz and 100MHz.

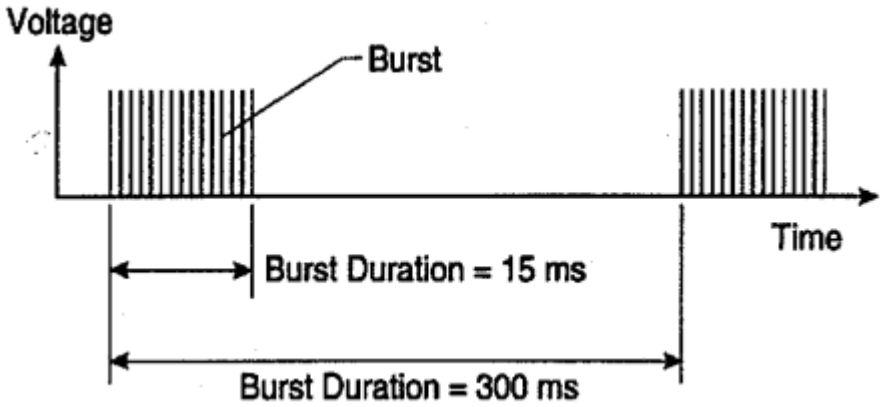


Figure 2.39: The waveform of the EFT burst (IEEE Std C62.45-2002)

2.34 The surge modes

- Common mode noise: The common mode noise shows in Figure 2.40, which is the harmful electrical interference appearing either in the common wire or the ground wire, which is an almost deadly interruption to the electronic equipment operation and component. The voltage amplitude of the noise can be as high as 6 kV.

- The normal mode noise: It (shows in Figure 2.41) occurs between the line and neutral conductors. The most normal mode disturbances result from load switching, occasionally coming from outside, such as lightning.

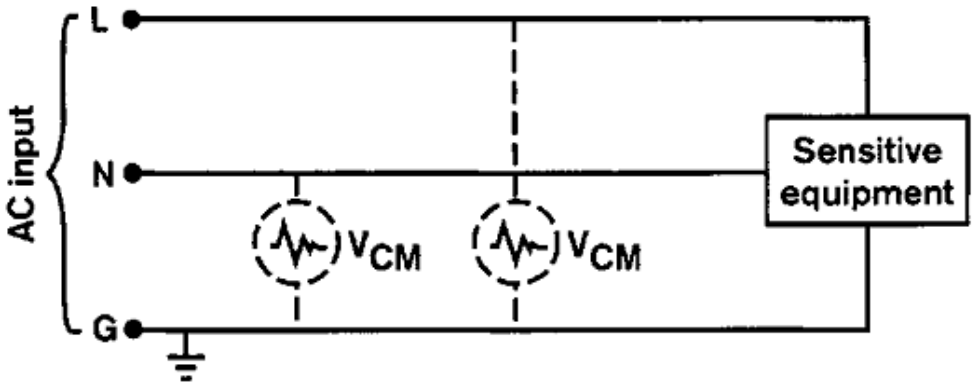


Figure 2.40: Common mode (CM) noise (Paul, 2001)

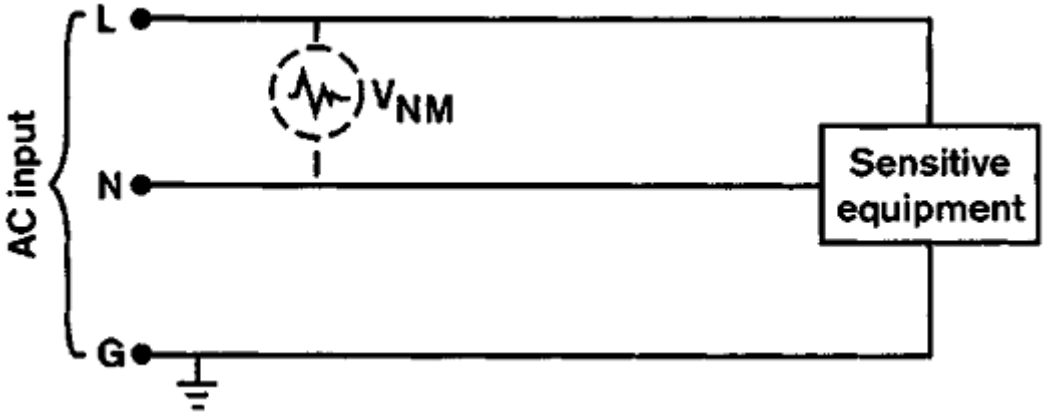


Figure 2.41: Normal mode (NM) noise (Paul, 2001)

- Low voltage and high voltage surges: the low voltage surge is defined that

the voltage peak is less than 2 kV. The high voltage surge is defined that the voltage peak is within the range from 2 kV to 6 kV.

- Voltage spike and oscillatory decaying noise, depicted in Figure 2.42 and 2.43. The term voltage spike refers to a voltage overshoot disturbance that has a fast rising time in the order of 1 ns to 10 μs, and occupy a board frequency spectrum from 4 kHz to 5 MHz. The oscillatory decaying noise has a frequency range from 400 Hz to 5 kHz.

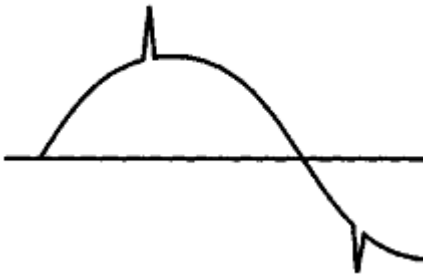


Figure 2.42: Voltage spikes (Paul, 2001)

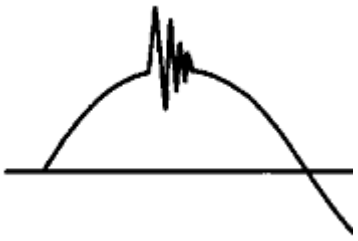


Figure 2.43: Oscillatory decaying disturbances (Paul, 2001)

Chapter Three

The circuit description

3.0 The circuit description

3.1 Overview of supercapacitor based on-line UPS system

The supercapacitor banks are operating as the energy transfer device, which provides the complete isolation of the inverter side from the charger side. The operation state of the energy transfer circuit is voltage dependent, which is controlled by a PIC microcontroller. The circuit is dynamic, where three supercapacitor banks are cycling in the operational states of charge, discharge and idle respectively. For any given states of the circuit operation, there is always one supercapacitor bank connecting with the inverter for supplying energy to the load. The block diagram of SRUPS please refers to Figure 1.7.

A flyback type transformer provides the magnetic coupling, and converts half waveform alternating current (AC) into pulse charging current, which is used to charge the supercapacitor banks. Assuming all of the SC banks are initially empty or hold at very low voltages, at the system start-up the voltage sensors (microcontroller voltage sensor) detect the exact timing of voltage level of each SC banks, and charge them to the upper voltage limit, which is 16 V (V_{max}). After being fully charged from all three SC banks, the first SC bank is set to discharge, by connecting to the inverter, while the other two SC banks are set to idle. The first SC bank will stop discharge when the voltage level reaches the lower limit of 13 V (V_{min}). The second SC bank replaces the first bank to discharge, and the first SC bank connects to the main source for charging. The third SC bank will discharge when the second SC bank runs out of energy. The cycled SC banks are always one kept in the state of charge, another one is in the state of discharge, and the third bank is kept on standby fully charged, which is used in the event of a failure or a heavy load connect to the power supply system.

The advantage of this system is that only SC banks are exposed to the transients when it propagates through the magnetic coupling. The load in this system is completely isolated at any operation state. The active surge detection attached at the very beginning of the system input ensures that the transients propagate through the windings under the limit of SC banks surge sustainability, otherwise it

disconnects when the transients are exceeding.

3.2 Microcontroller

The analog-to-digital converter (ADC) is used to measure the actual terminal voltage of each supercapacitor bank. The voltage signals convert into the 10-bit digital signals. Those binary measurements are taking in the determination of supercapacitor operation mode in either charge, discharge or idle. The available reference voltage between V_{cc} and V_{dd} is 5 V. Therefore the resolution of ADC can be written as (Microchip, 2005):

$$\frac{1}{1024} \times 5V = 4.8mV \tag{3.1}$$

This resolution is sufficient to give a less than one percent inaccuracy measurement. The 20 ADC readings are taken in a short period and averaged. Averaging the measurements is done to reduce the risk of misreading that is usually taken from the unregulated noises. The optical couplers separate the supercapacitor bank and the input pins of microcontroller in high isolation level, preventing the transient effect that may occur across the supercapacitor bank. In fact that latency is added due to the propagating through the optical coupler, but it does not disturb the control sequent. A summarizing table 2 demonstrates the supercapacitor bank operational states in each particular condition.

Table 3.1 Supercapacitors switching sequent in the condition of terminal voltages

Current State	Previous State	Following State	Description	Voltage at Start	Voltage at End
Charge	Discharge	Idle	SC connect to main supply	15V	20V
Idle	Charge	Discharge	SC Bank is kept on standby	20V	20V
Discharge	Idle	Charge	SC Bank connect to the inverter	20V	15V

3.3 The principle of the transformer design

The transformer used in this research operates in the discontinuous and unsaturated mode. Knowing the ferrites core cannot store infinite flux. For the proper design, the peak flux should less than the upper limit of the ferrite core against the saturation. Principally the large size of core is associated with large flux capability, therefore, to choose the core size is taking the consideration on the total volt-amp rating of the component and a core characteristic size parameter a_{ch}

$$S_{tot} = \sum_{alll\ winding} V_{rms} I_{rms} = A a_{ch}^{r}$$

$$\Rightarrow\ a_{ch} = \left(\frac{S_{tot}}{A}\right)^{1/r} \tag{3.2}$$

(Bossche & Valchev, 2005)

Where

- A is a coefficient for ferrites, for the general propose $A = (5 - 25) \times 10^{6}$ if a_{ch} is in [m]
- a_{ch} is the largest dimension of the ferrite core
- S_{tot} is the total volt-amp rating of the ferrite core

Figure 3.1 shows the possible range of the scaling parameter a_{ch} , as function of the total V-A rating S of the component, it can be used as a fast approach for obtaining the core size. The coefficient γ is depended on the core material varying in a range 2.8 < γ <3.2. For a fast approach, the value of r is usually to be γ = 3.

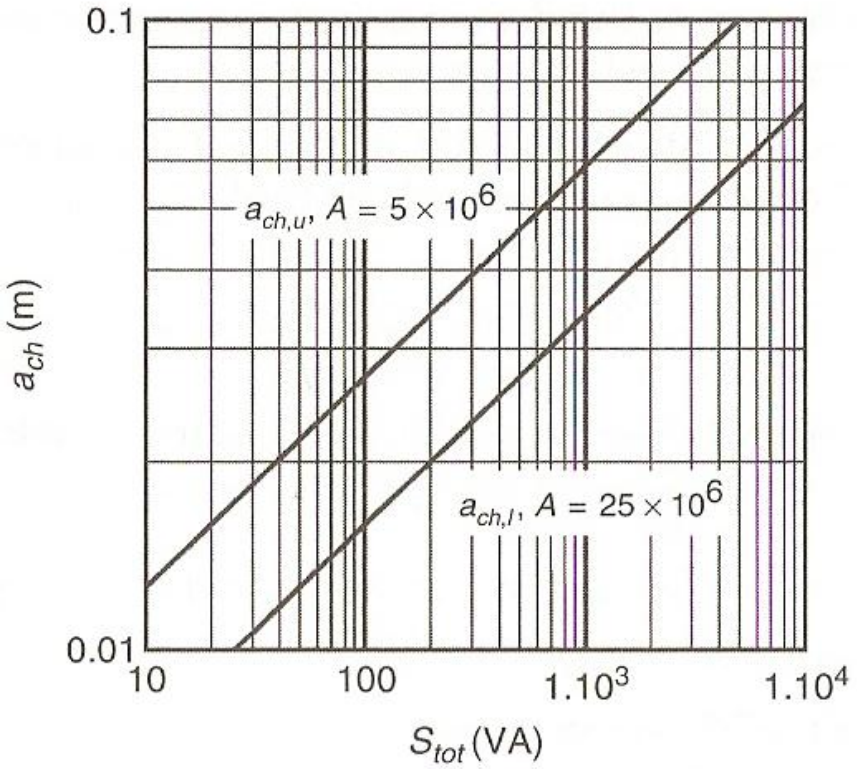


Figure 3.1: Core size estimation for a non-saturated thermally limited ferrite core design (Bossche & Valchev, 2005)

Find the peak induction B_{pg} from the graph waveform, in the datasheet of ferrite core, the peak induction is usually given, and also demonstrates with corresponding parameters, such as the core loss at a given frequency. In general the peak-to-peak induction is multiplied the peak induction by 2. However, in the practice, the peak-to-peak induction is different when the transformer operates in the different modes. A symmetrical waveform shows in Figure 3.2, in the situation of a, the transformer operates in the forward mode, the flux flows in both directions, hence the peak-to-peak induction is twice large than the peak induction. In the situation of b, the induction fluctuates in a small region, hence the peak-to-peak induction is less than the peak induction. In the situation of c and d, the peak-to-peak induction is equal to the peak induction. In this research, the transformer operates in the discontinuous mode, which the induction waveform should similar as the situation of d. Notice that the saturation induction is the maximum allowed with a particular ferrite core, the operational peak induction designed should not excessed this upper limited.

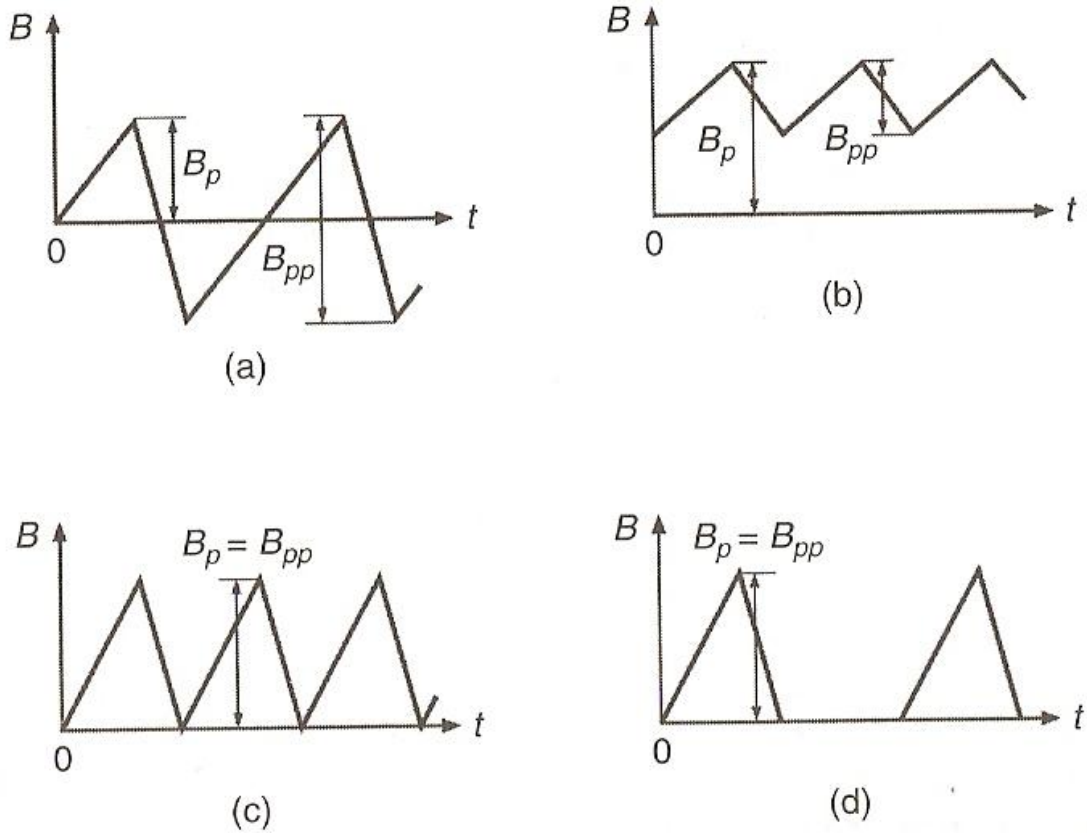


Figure 3.2: Typical waveforms and corresponding peak induction B_P (Bossche & Valchev, 2005)

The winding turn is calculated in the consideration of arbitrary voltage waveform. For a given voltage waveform, the integral of the voltage waveform S, depicted in Figure 3.3, is equivalent to the peak-to-peak flux linkage Ψ_{pp}. The equation can be expressed as:

$$\int_{t_1}^{t_2} V(t)dt = \Psi_{pp}, \quad \Psi_{pp} = N\Phi_{pp} \tag{3.3}$$

(Bossche & Valchev, 2005)

Where

- Ψ_{pp} is the peak-to-peak magnetic flux linkage [Wb]
- N is the number of turns

- Φ_{pp} is the peak-to-peak magnetic flux

The peak-to-peak magnetic flux Φ_{pp} is equal to the product of the peak-to-peak induction and the cross section area of the core, the equation can be written as:

$$\Phi_{pp} = A_e B_{pp}$$

(3.4)

(Bossche & Valchev, 2005)

The number of turns of primary winding can be calculated by substituting the equation above into the equation of flux linkage, the primary turns can be presented as:

$$N_1 = \frac{\Psi_{pp}}{\Phi_{pp}} = \frac{\Psi_{pp}}{A_e B_{pp}} = \frac{\Psi_{pp}}{2} \frac{1}{A_e B_{pg}}$$

(3.5)

(Bossche & Valchev, 2005)

As considering the transformer operates in the AC environment, the equation can be modified to

$$N_1 = \frac{V_1\sqrt{2}}{2\pi f A_e B_{pg}} = \frac{V_1}{4.44 f A_e B_{pg}}$$

(3.6)

(Bossche & Valchev, 2005)

Where

- V_1 is the RMS value of the voltage across the primary winding
- f is the excitation frequency
- A_e is the effective cross section area of the core

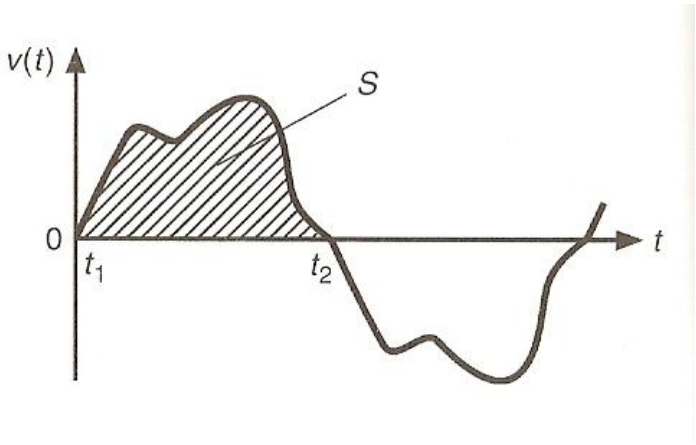


Figure 3.3: The arbitrary voltage waveform across the transformer winding (Bossche & Valchev, 2005)

3.4 Insulated gate bipolar transistor driver

IGBT is able to conduct and block the current by switching the gate drive, so designing a proper gate drive is extremely important to the performance of the IGBT. The switching frequency of this project is 50 kHz, which requires the IGBT drive to have a fast response without the high frequency issue. For providing the hard-switch that the IGBT operates in the switch mode, only changing between two extremes either conducts or cut-off, the gate drive waveform must ensure that has fast switching rate (dv/dt). The conduction of IGBT can be made when appropriate voltage (generally +15 V) is applied to the gate. The current is cut off when the gate voltage is lower than the threshold. Note that the turn off voltage threshold is less than 0 V, therefore the IGBT gate drive must be able to switch between positive and negative power trails.

The MC33153 is an integrated IGBT gate driver, which is used for this research. This device offers the features of high current output stage, protection circuit and negative gate drive capability. It has reasonable good switching characteristics, which the output rise and fall time is approximately 17 ns respectively, making the possibility of drive frequency in 50 kHz.

For the high frequency application, the optimization of switching characteristics is very important to the gate driver design. Typically a signal resister is used to bridge between the pulse-width modulation (PWM) output and the gate of IGBT.

However the resistor value selected must be a compromise in turn-on abruptness and turn-off loss. The signal resistor configuration is usually found in the low frequency applications. An optimized gate drive output stage is offered in Figure 3.4. Two resistors and a turn-off diode are allowed to optimize the turn-on and turn-off separately.

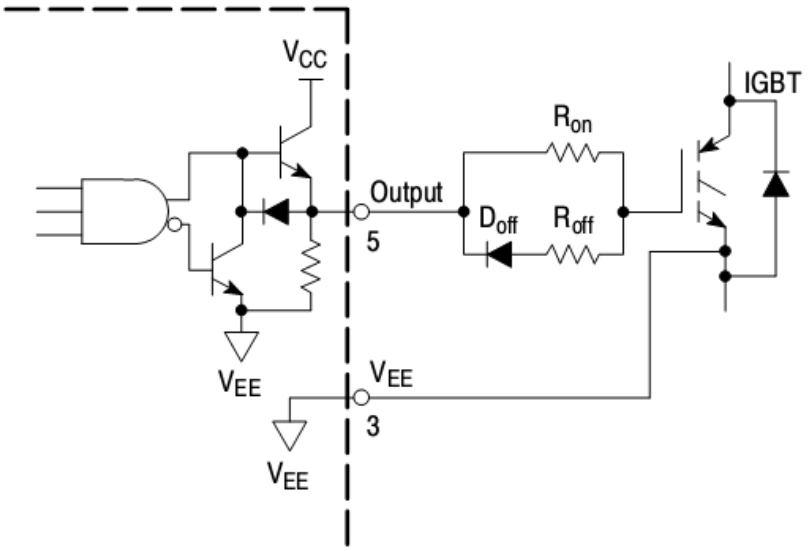


Figure 3.4: Using a separate resistor for turn-on and turn-off (ON Semiconductor, 2011)

The available of negative drive depicted in Figure 3.5, can be used to drive IGBT in off-state. The voltage difference between the V_{cc} and V_{ee} must be within a voltage window of 20 V, so the supply voltage is set to be +15 V/ – 5 V.

The gate driver is negative triggered. Hence an optical coupler is used as interfacing to provide a voltage level shifting, and a high level isolation is offered to protect the circuit that connects to this gate driver. The PWM signal via the optical coupler must have minor influence on propagation delay. Therefore a high speed gate driver optical coupler (FOD3181) is used rather than the one that is used for the ADC coupling. The gate driver also offers a feature of fault detection, where the entire system will shut down when a high priority signal of the device fault is raised on the pin 7 of the integrated circuit.

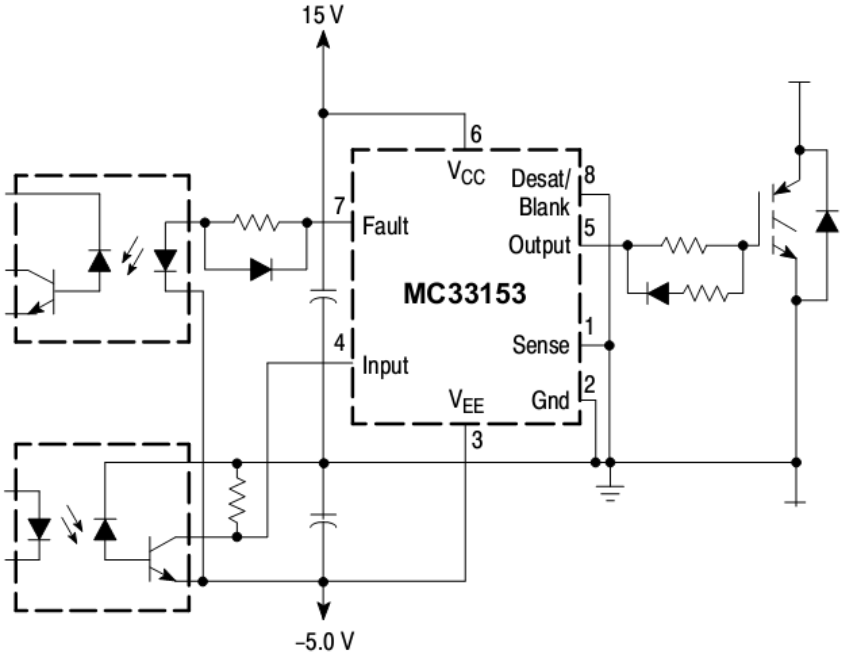


Figure 3.5: The gate driver is negative triggered and offers a positive/negative drive (ON Semiconductor, 2011)

The feature of saturation protection as demonstrated in Figure 3.6, is to prevent the IGBT from the damage of overcurrent. The diode connect to the IGBT must has high voltage capability. The blanking capacitor must connect to the Kelvin Ground. The flux generated in the core tends to reach the saturation when the transformer primary winding is overloaded from excessive voltage. Consequently, the high current generates in the transformer primary winding, as well as passing through the switch. An increase of voltage drop on the switch due to the high current flow is detected by the desaturation comparator. When the voltage signal is higher than the upper limit, then a system turn off signal is sent by the desaturation comparator, which is in order to protect the primary winding of the transformer from the overcurrent.

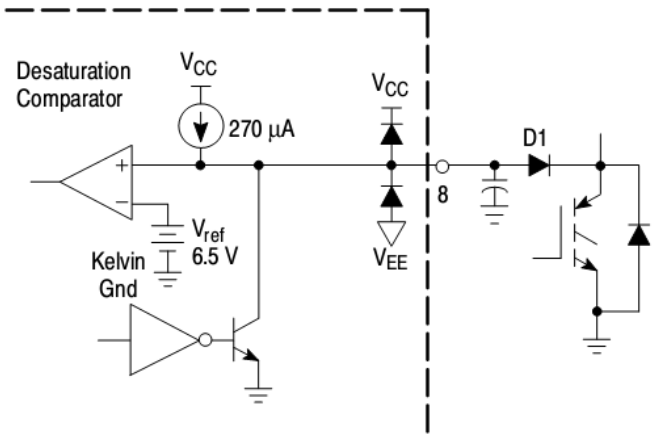


Figure 3.6: Desaturation circuit with support components (ON Semiconductor, 2011)

3.5 The charge circuit

The flyback charge circuit is shown in Figure 3.7. The full sine waveform via the rectifier is converted into half waveform with peak to peak voltage of 120 V. The converted half waveform passing through the primary winding generates the magnetic flux. The IGBT attached on the primary winding is operated as a switch. The switch frequency is 50kHz that is controlled by the microcontroller and amplified by the IGBT driver. The IGBT driver enlarges and transfers the voltage level of PWM drive signal to be +15/-5 V, which is able to drive the IGBT in state of hard-turn on and off. The IGBT also offers the feature of power correction, making the high efficiency power supply possible.

The operation sequence of flyback type charger, where the primary winding is charged during the switch is on. The electrical energy charge creates the magnetic flux, and a small fraction of magnetic flux is stored in the primary winding and most of the flux is stored in the ferrite core around the area of air gap. When the switch is off, the magnetizing inductance of the transformer primary releases their energy to the secondary via weak coupling. While a high speed recovery diode (MUR1620CT) attached on the secondary winding allows the current flow from one direction this is not reversible. Therefore, the pulse current appear in the secondary winding is used to charge the supercapacitor bank. The high speed recovery diode has relatively low voltage drop out, approximate to 0.9 V. The low drop out is ensures that the majority of charge energy is concentrated on the

supercapacitor banks. The other advantage is fast recovery that has minimum energy losses due to the occurrence of reverse current.

Multiple charge and discharge cycles occur in the one cycle of input source, due to the switching frequency being much faster than the frequency of AC input. The design calculation is taking into consideration the worst conditions. The maximum charging current is used to design the switching frequency and the number of turns of transformer windings. Therefore the average charging current is lower than the design current, the transformer is actually operated in the discontinuous mode.

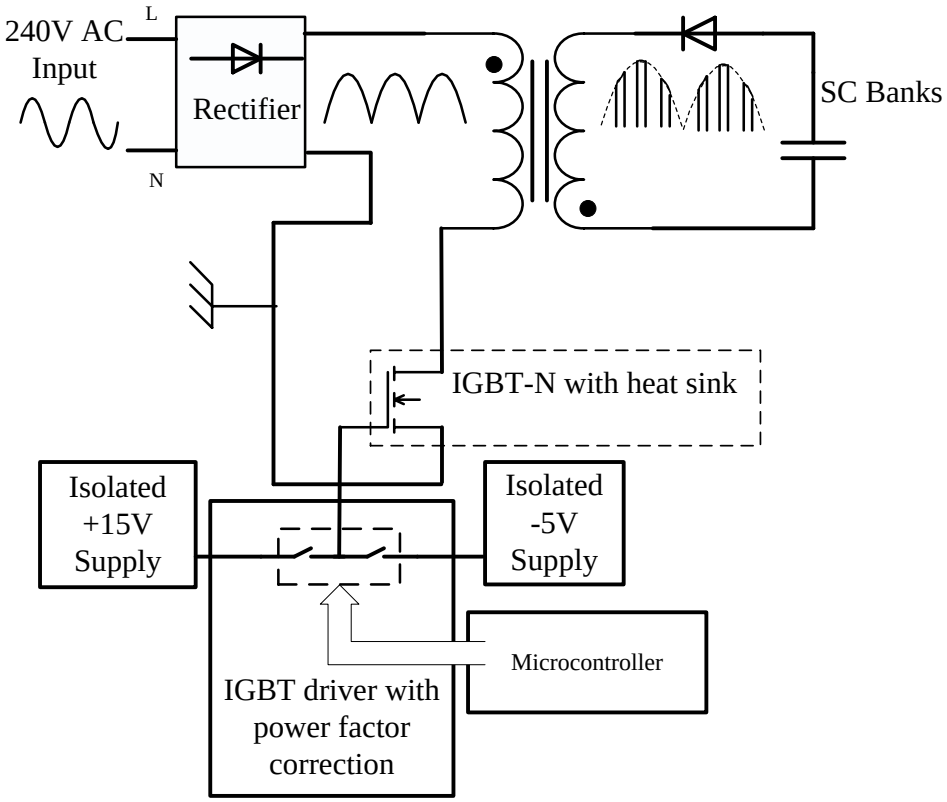


Figure 3.7: The block diagram of the charging circuit

3.6 PWM inverter

A pre-made PWM inverter is used to boost the voltage level and convert DC into 240 V AC that is supplied to the load. The DC voltage supply to the inverter is required to remain within a voltage window of 20 to 12 V. Therefore minimum

terminal voltage when supercapacitor banks discharge is set to be 13 V. The disadvantage of this inverter is that there is no output power corrector. A varying input voltage will cause the amplitude fluctuation of output voltage.

3.7 The circuit control routines

The control circuit utilizes a PIC® 16F690 microcontroller for controlling and monitoring circuit. The feature of ADC is used to sense the actual voltages that develop across the supercapacitor banks. The digital outputs are generated to switch the supercapacitor banks either in charge, discharge or idle mode. The PWM signal generated by the microcontroller is used to drive the IGBT for charge and discharge the primary winding of flyback transformer. The flow chart below is the routines operating inside the firmware of the microcontroller. The actual code write in C language and presents in the Appendix.

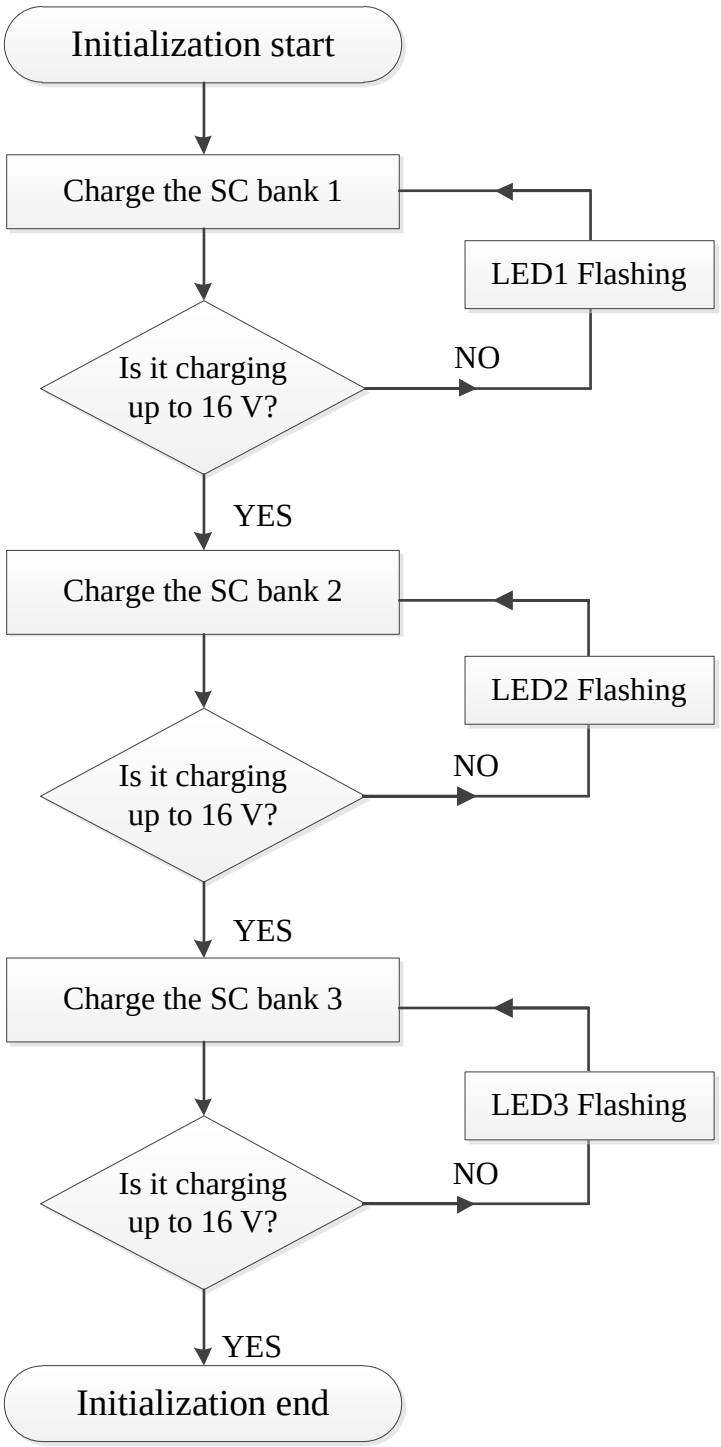


Figure 3.8: The flow chart of the supercapacitor based on-line UPS initialization routine

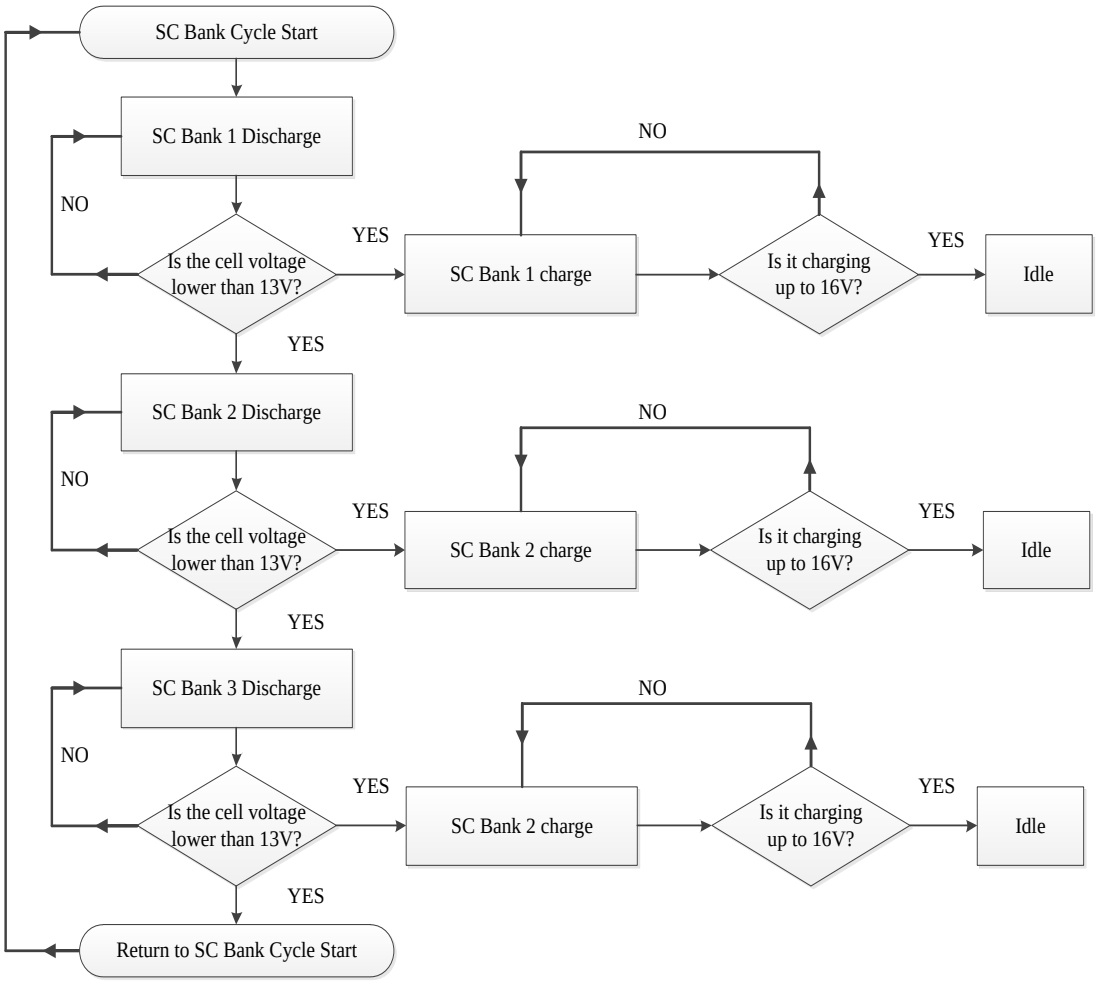


Figure 3.9: The flow chart of supercapacitor banks switching routine

Chapter Four

Implementation

4.0 Results

A prototype supercapacitor on-line UPS system was built for testing. The measurements obtained are in order to evaluate the system performance, and furthermore can be used to optimize the design for a better approach. The following tests and measurements were carried out the supercapacitor on-line UPS system.

- To measure the actual PWM output generated by microcontroller for driving the IGBT
- To measure the current and voltage waveforms on both side of transformer
- To test the switch circuit to verify the performance of switching circuit
- Recording the charge time when the supercapacitor bank charge from 0 V to 16 V
- Recording the charge time when the supercapacitor banks are cycling in the voltage window between 13 V to 16 V
- Recording the time when the supercapacitor banks discharge via the inverter with different loads

All measurements were read off by the Tektronix TPS 2024 digital storage oscilloscope with four isolated inputs which is shown in Figure 4.1. The all current waveforms obtained were measured off the voltage across a 0.05 Ω resistor. An insolation transformer (Figure 4.2) was used avoiding the short circuit issues.

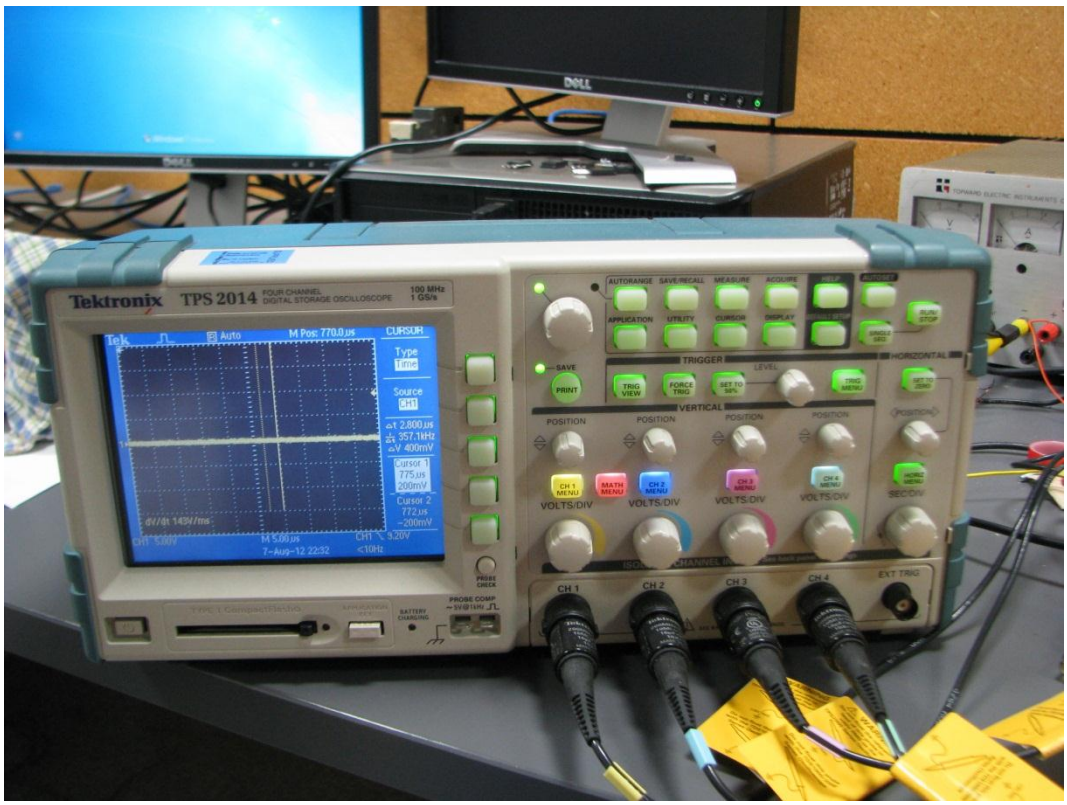


Figure 4.1: Tektronix TPS 2024 digital oscilloscope

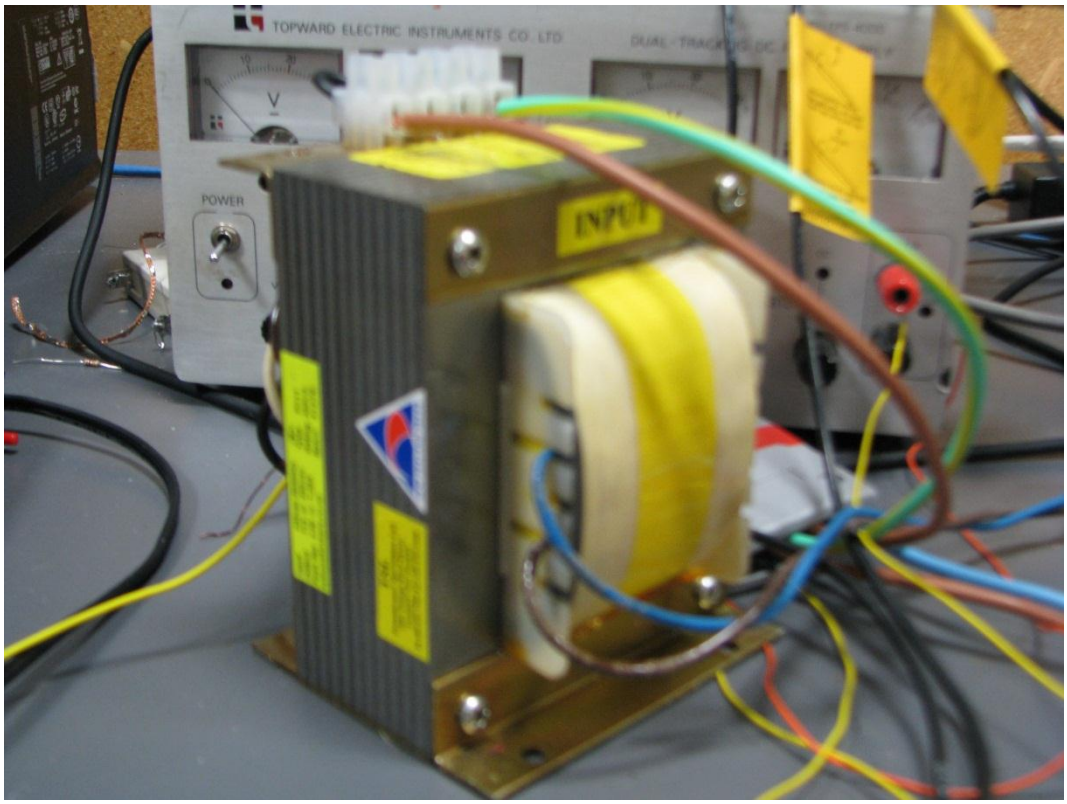


Figure 4.2: Isolation transformer

4.1 Insulated gate bipolar transistor driver testing

The PWM signal generated by the microcontroller was in frequency of 50 kHz with 20 % duty cycle. In the datasheet, IGBT requires a negative voltage for hard turn off. An IGBT gate driver used to shift the PWM voltage level, providing between +15V to -5 V, which the open circuit voltage waveform was shown in Figure 4.3.

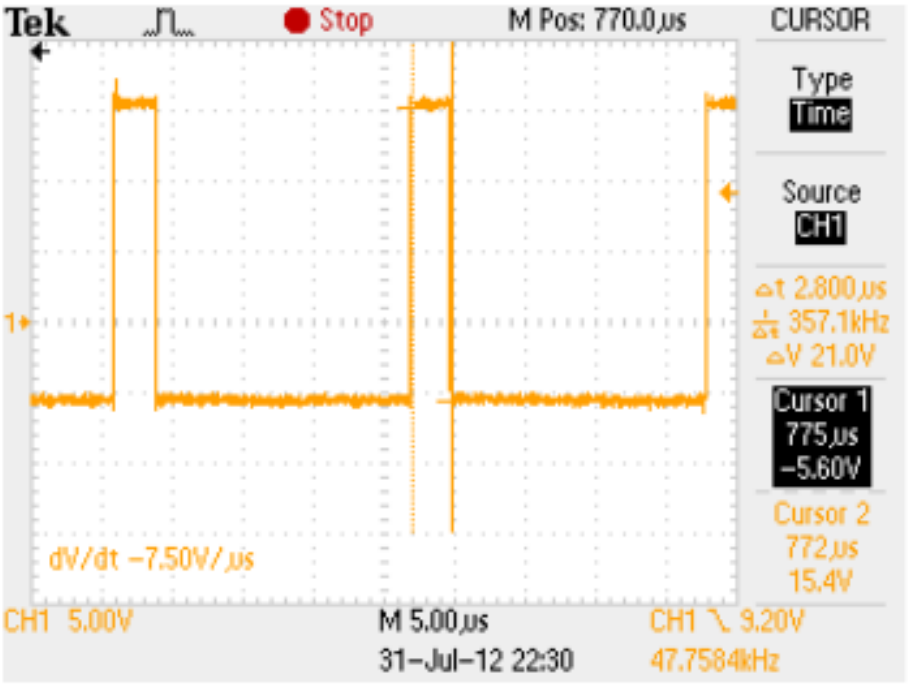


Figure 4.3: The open circuit waveform of PWM drive supplied by the IGBT driver

In the project, a high speed optical coupler separated the microcontroller and IGBT driver, which provides 5000 V isolation for protecting the microcontroller. However, this optical coupler is interfered the propagating signal in the result of 500 ns delay. In this project, this propagation delay can be neglect.

The open circuit PWM waveforms, depicted in Figure 4.3, were perfect square waveforms. However, when an IGBT connected to the driver, the PWM voltage waveforms were out of the shape, which demonstrated in Figure 4.4. The pulse width was extended by 2 ns, which is very important. It means that the IGBT will turn on for 2 ns longer. So this extra time should add into the calculation of charge period.

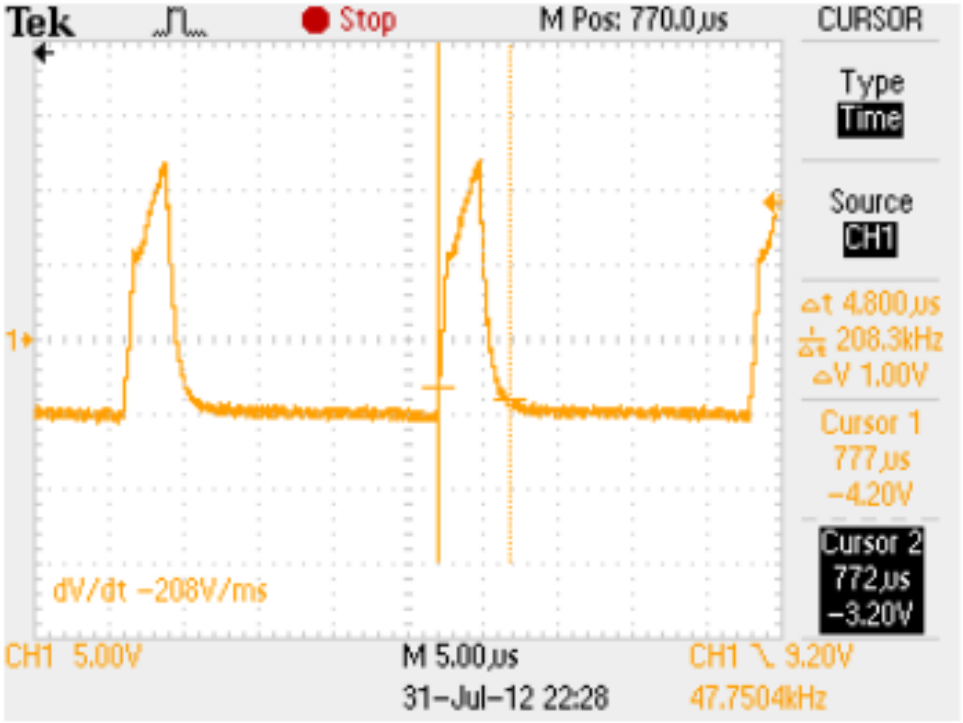


Figure 4.4: Actual waveforms of PWM output

4.2 Flyback charger testing

The measurements as shown in Figures 4.5 and 4.6 indicate transformer primary side and secondary side. Figure 4.5, the 240V, 50 Hz AC supplied across the primary winding, purple waveforms indicate the voltage on the transformer primary side, and the primary current is shown in blue. As result the current peaked when the supply voltage reached the maximum amplitude. On the secondary side, the supercapacitor bank got charge, it indicates as an increase terminal voltage (purple waveforms) in Figure 4.6. The secondary current is pulse current, shown in the bottom of Figure 4.6.

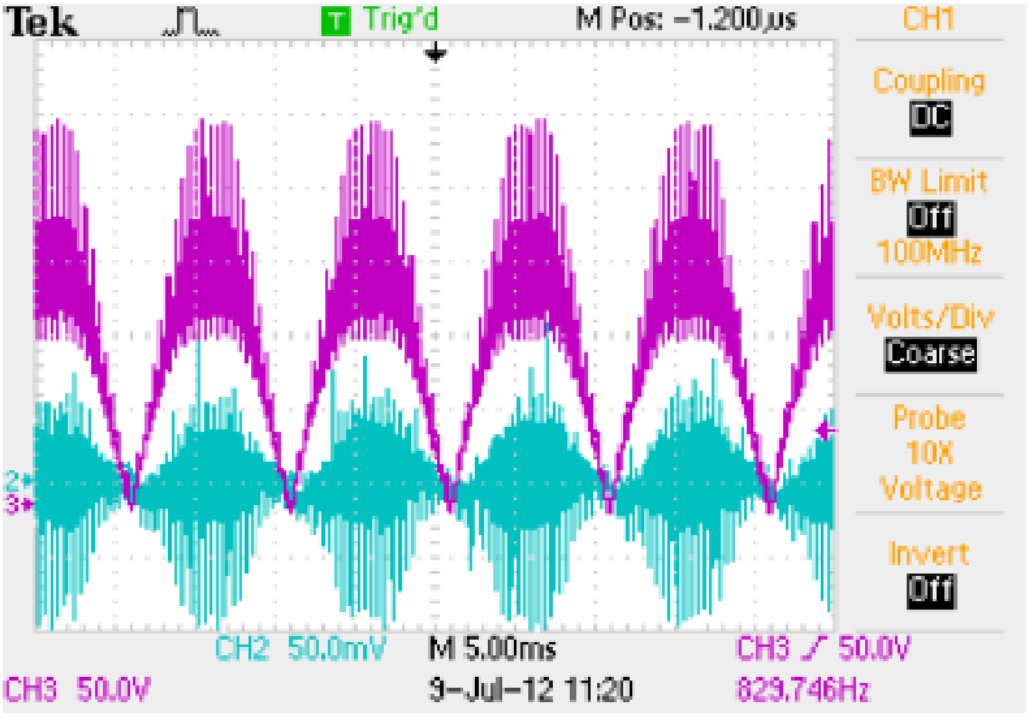


Figure 4.5: The voltage (purple) and current (blue) waveforms of the transformer primary winding

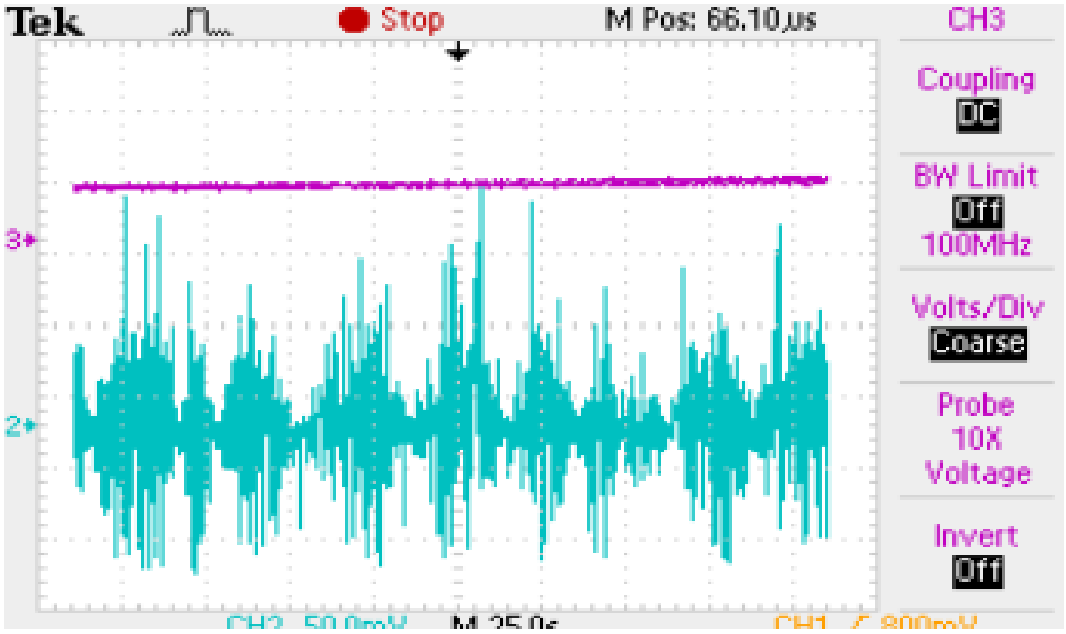


Figure 4.6: The voltage (purple) and current (blue) waveforms of the transformer secondary winding

Figure 4.7 demonstrated one complete PWM cycle. The IGBT was conducting when a positive voltage (yellow waveform) supplied to the IGBT gate. The

primary winding charged in the result of increase of primary current, which displayed in the blue waveform. The green waveforms indicate the voltage across the primary winding during the IGBT is conducting. When the IGBT was cut off, the energy stored in the primary winding was released to the secondary, which was used to charge the supercapacitor banks. The purple waveform demonstrated that the supercapacitor got charged at the IGBT off period and then the terminal voltage was decaying after a pulse charge. This measurement was verified that the energy transformation was very similar to the flyback converter.

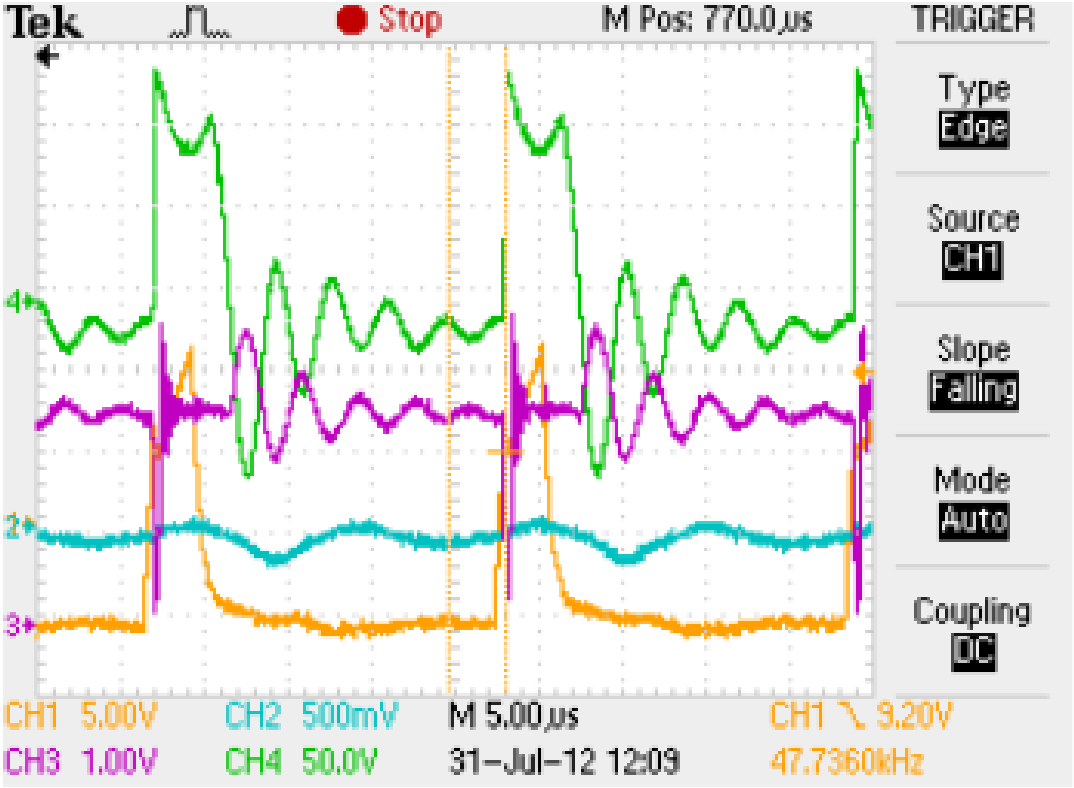


Figure 4.7: Flyback charger waveforms

Where

- The voltage across the primary winding of the transformer is representative as the green waveform.
- The current via the primary winding of the transformer is representative as the blue waveform. The amplitude waveform obtained is the voltage across a 0.05 Ω resistor, can be converted into the current measurements by using the equation of $= V/R$.
- The terminal voltage of supercapacitor bank is representative as the purple

waveform.

- The yellow waveform is PWM output for driving the IGBT either in conduction or cut-off mode.
-

4.3 Switch circuit testing

The measurements were carried out to confirm the supercapacitor bank control routine operated correctly. Figure 4.8 and 4.9 show voltage waveforms of each supercapacitor bank in the start-up routine and normal operation routine. In the start-up routine, all of supercapacitor banks charged to 16 V. In normal operation routine, the supercapacitor banks were cycling within a voltage window between 13 V to 16 V.

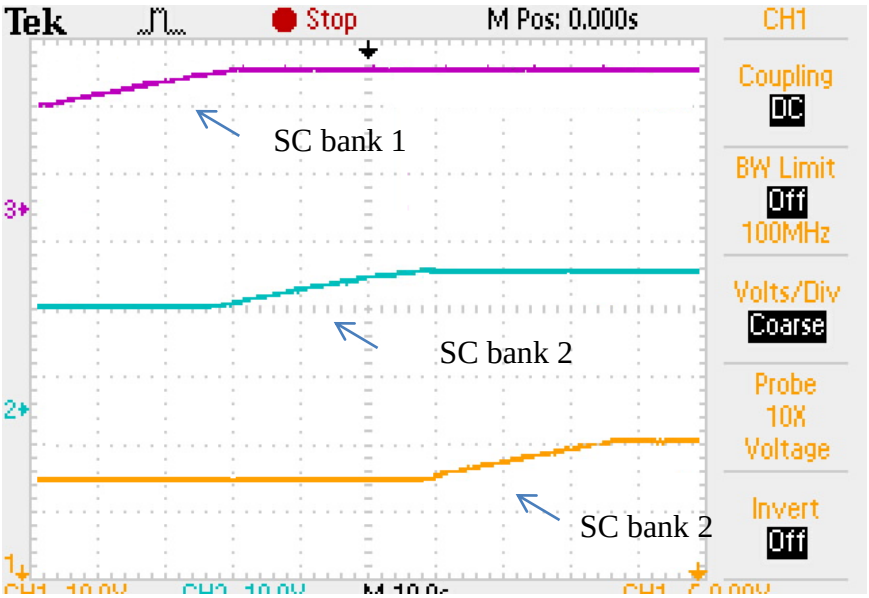


Figure 4.8: Charge the SC banks individually in the start-up mode

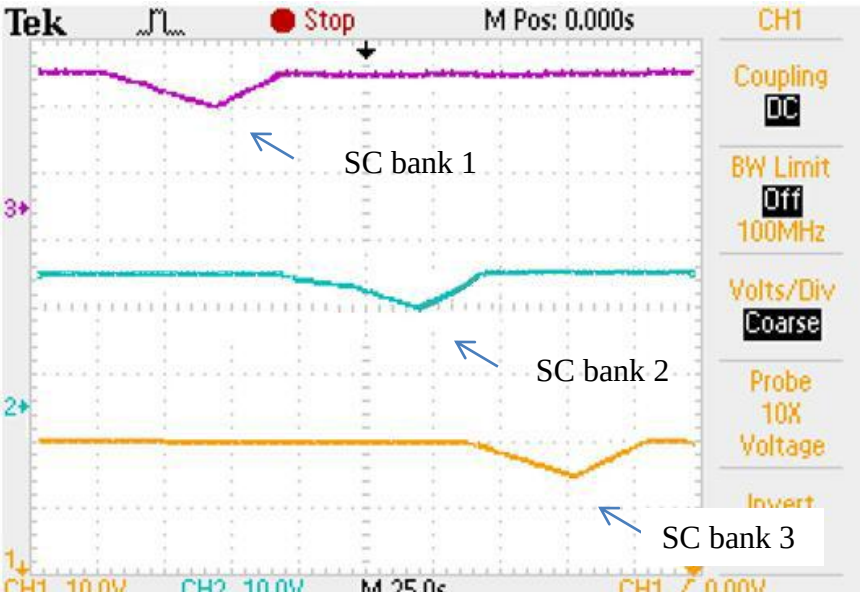


Figure 4.9 Switching the SC banks in a cycling mode during normal operation

4.4 Measurement summary for evaluating SRUPS performance

Figure 4.10 shows the charging time of one supercapacitor bank during the start-up. The charge period was started when the supercapacitor bank held 0 V, and then charged up to 16 V. Figure 4.11 shows the charging time of one supercapacitor bank during the normal operation, the charge started when the supercapacitor held voltage below 13 V, and then stopped when it reached at 16 V.

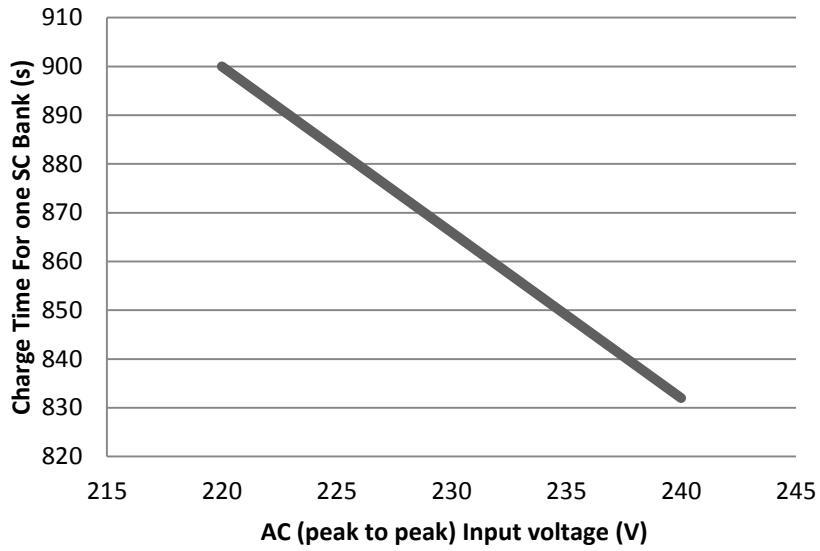


Figure 4.10: Charge time is differ with voltage source

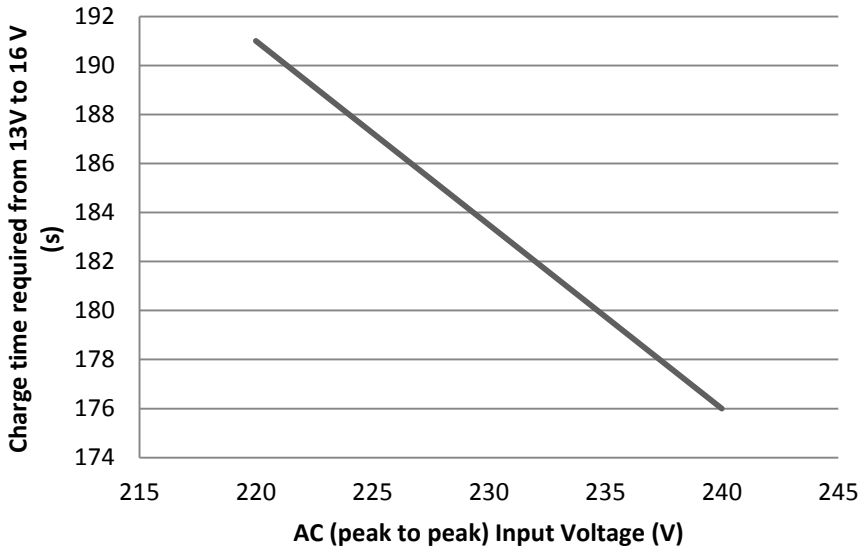


Figure 4.11: The charge time required for cycling operation

Power factor corrected waveforms show the in Figure 4.12. The input AC main is 240 V at 50 Hz, representing as the purple waveform. The dot line waveform is the charging current, which was peak at the 5.95 A. the flat spaces indicated there was no charge current when the voltage was lower than supercapacitor bank terminal voltages.

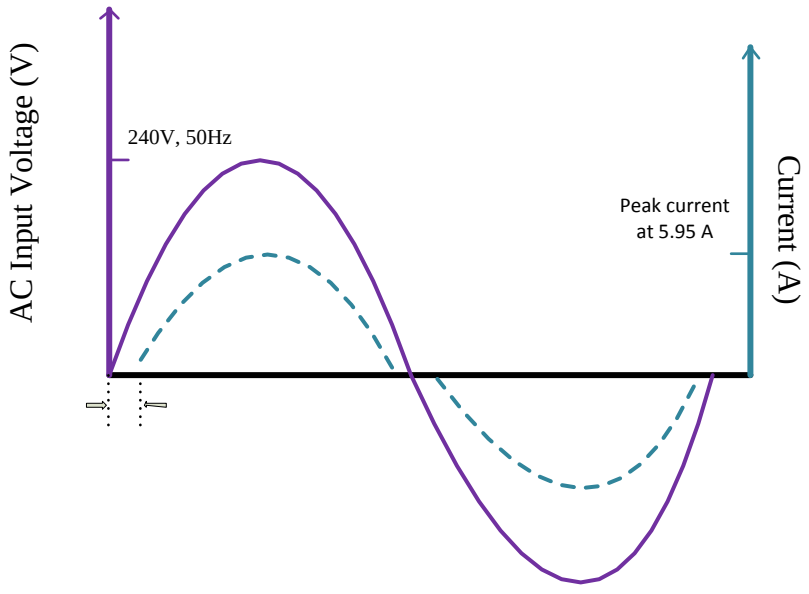


Figure 4.12: Power factor concerted waveforms

Chapter Five

Conclusion and future development

5.0 Conclusion and future development

5.1 Conclusion

A flyback charger developed for the surge resistant uninterrupted power supply is workable. The charging circuit contains few components, which is much simpler than original design. Supercapacitor banks get charge via the charger, and only the devices expose to the common mode surges. The property of supercapacitors presents a high transient resistant capability, where the common mode surges are absorbed and vanished. Loads are always powered by the supercapacitor banks via a PWM inverter, have no chance connect to the main power line, therefore, the high level insolation is possible. The power factor correction available in this design is to enhance the charger performance, providing energy transformation in high efficiency. To achieve high reliability, a desaturation circuit is used to avoid the transformer saturation.

5.2 The future development

Due to the limitation of time, all the measurements obtained were under the non-surge condition. There are primary requirement for the future development, this circuit should be tested with surge applied for evaluating the surge withstand performance. The test could start with applying single surge, and then apply surges repeatedly.

In anticipation of driving a heavy load, the flyback charger should be required and improved the RMS charging current. The high current charger is to ensure that the SC banks are cycling in the continuous mode, where the average charging current must capable of sustaining the load current. The increase of the charging current can be made from refining the flyback current with batter materials and optimizing circuit design.

The transformer is another aspect that affects the energy transfer. The transformer used in this project is handmade, which presented large flux leakage. And for the shortage of materials, the litz wire is used for the transformer secondary winding

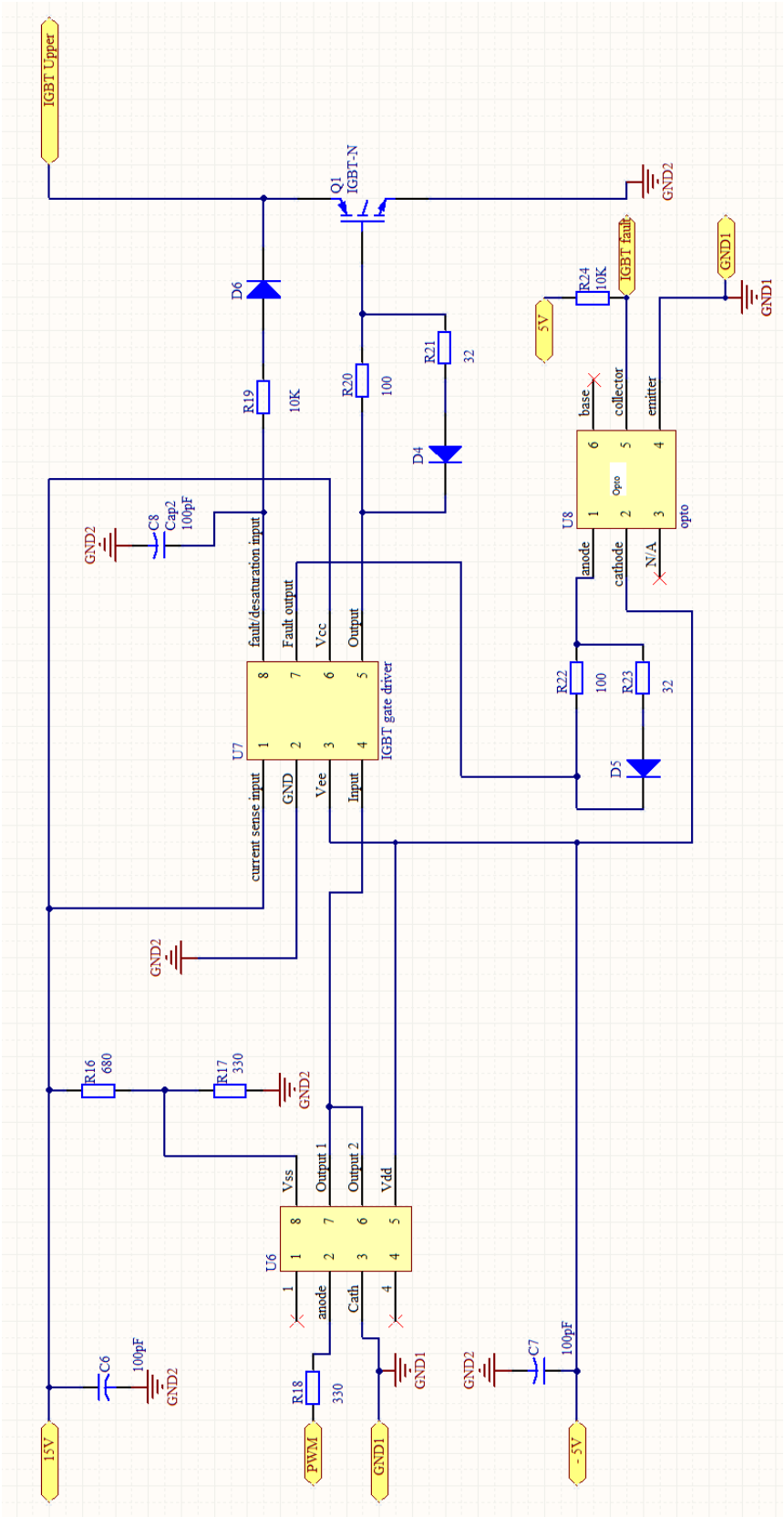
is in low quality. Because original litz wire I had was shorter than the required, I twisted 10 solid wires together in form a handmade litz type wire. In the future development, a transformer with proper design should improve on reducing the flux leakage and batter performance in high frequency operation.

This circuit is formed by three blocks, the control circuit, supercapacitor bank switches and inverter respectively. The copper wires were used to link those circuits together. The disadvantage is the unexpected energy losses due to long connections. In future development, the circuit should be assembled on the single printed circuit board (PCB). On the other hand, the inverter used, which has no feedback to cooperate with control circuit. In future improvement, the inverter should synchronize with entire circuit control. Entire circuit operates with a control loop that can be improved SRUPS performance effectively.

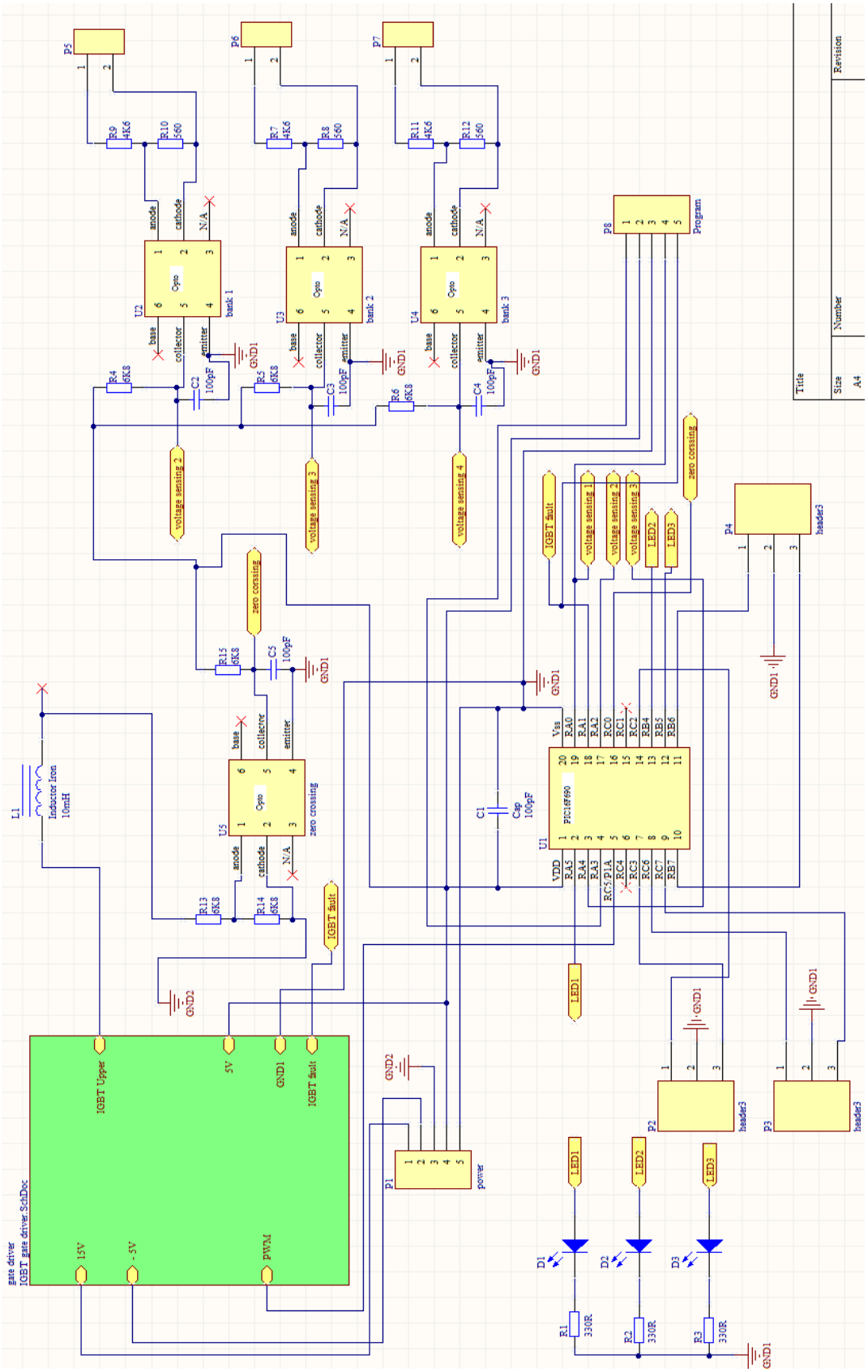
The commercial SCs are still limited by their cell voltage. The SC bank used in this project consists of 6 individual supercapacitor cells, which is connected in series to meet the input voltage level for the inverter. This compromise is required for the external connection to bridge the SC cells, which contributes the extra resistances to the charge circuit. The energy losses are generated due to this extra series resistance. One strong suggestion to have a larger capacity SC bank is to use the SC module sold by Maxwell or Nesscap, provided the prices are affordable. However the SC module contains electronic circuits to balance cell voltage, in the cases, the surge might have negative effect on these balancing circuits.

Appendices

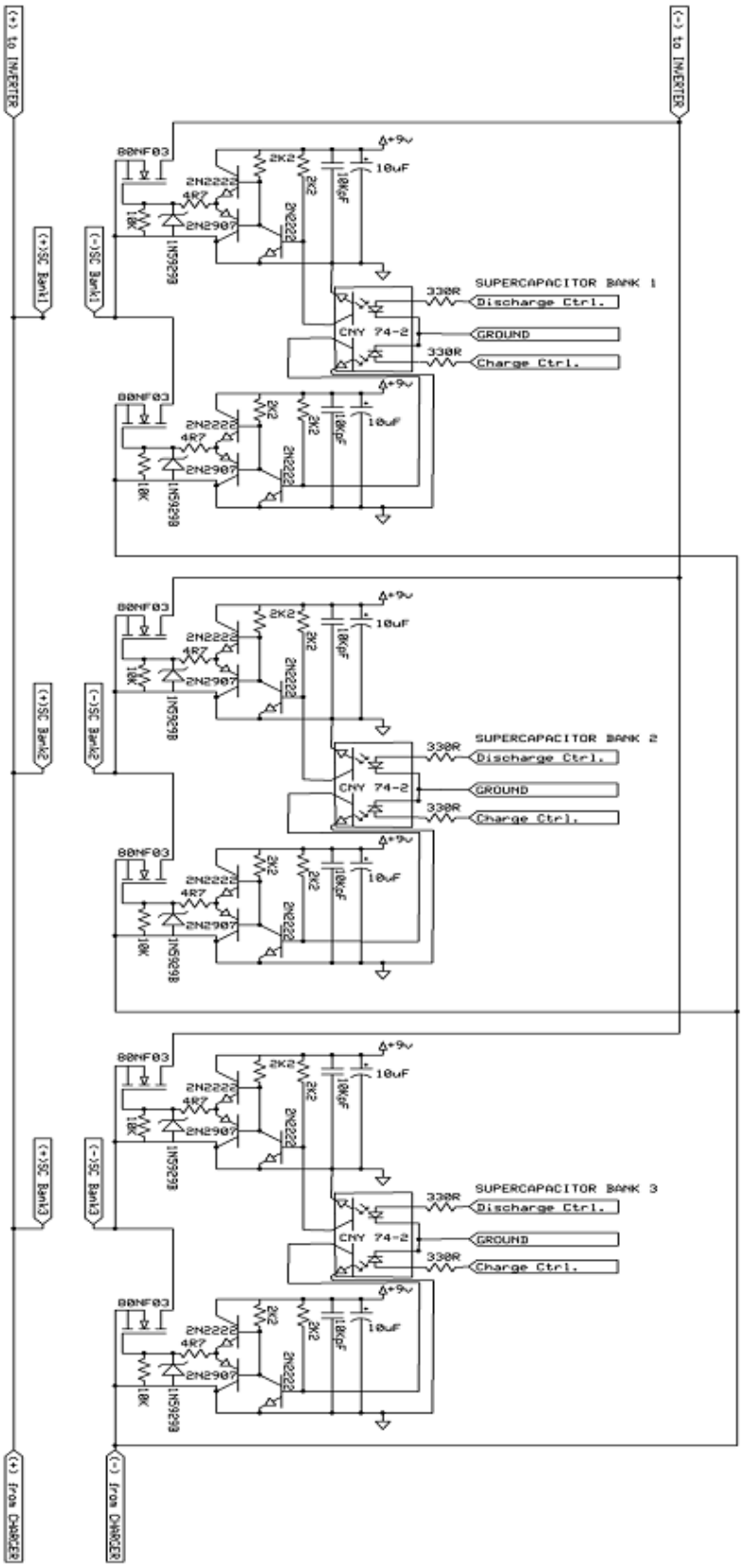
IGBT driver circuit



Flyback charger control circuit



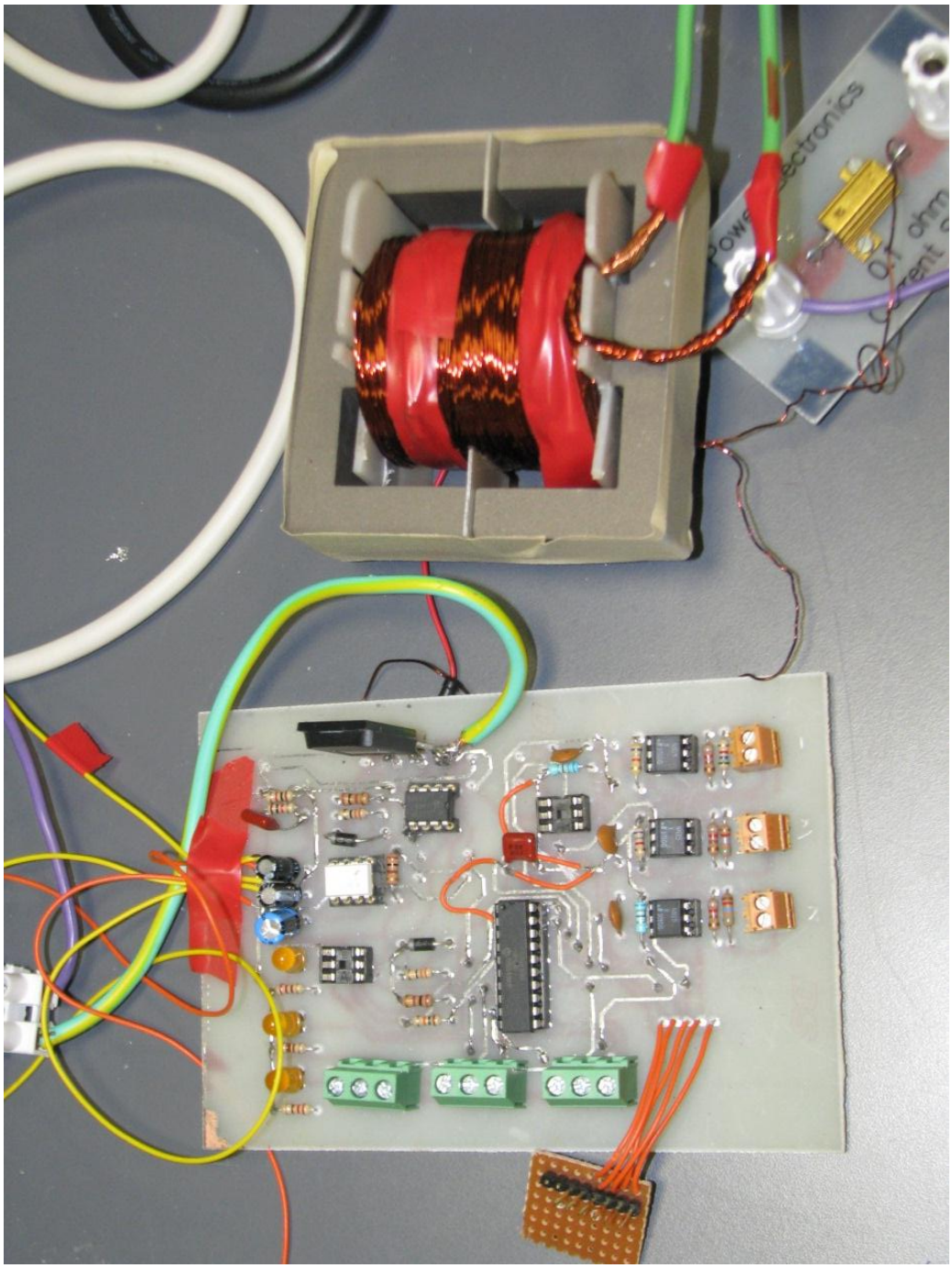
Bank switching circuit



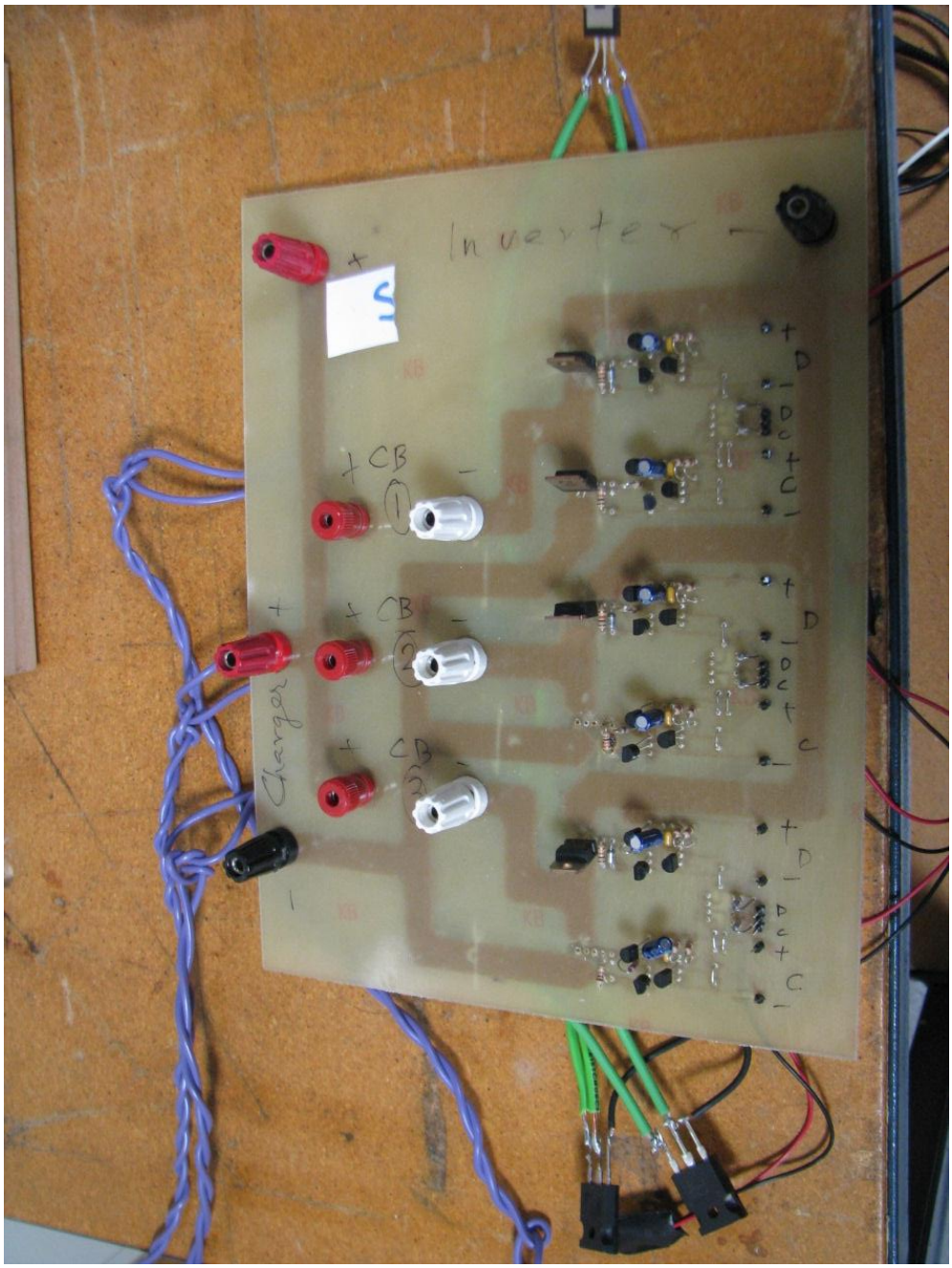
Photograph of circuits

PWM Inveter with stupup transformer and loads

Flyback charger



Supercapactior banks switching circuit



Supercapacitor bank

Microcontroller coding

```
#include <pic.h>
#include <stdlib.h>
#include <htc.h>
#include <math.h>

#define on 1
#define off 0
#define set 1
#define clear 0
#define pwm CCP1CON
#define pwm_fre PR2
#define pwm_duty CCPR1L
#define pwm_pin RC5
#define pwm_on 0b00001100
#define pwm_off 0

//defined switch control output pins
#define BANK1_CHARGE          RC2
#define BANK1_DISCHARGE       RC3
#define BANK2_CHARGE          RC7
#define BANK2_DISCHARGE       RC6
#define BANK3_CHARGE          RB6
#define BANK3_DISCHARGE       RB7

//defined LED output pins
#define BANK1_DISP     RA5
#define BANK2_DISP     RB4
#define BANK3_DISP     RB5
#define DEAD_DISP      RC1
```

```
#define ON_MOSFET 1
#define OFF_MOSFET 0
#define HIGH_READING 295        //0.17V//35
#define LOW_READING    786      //3.84V

//defined variables
unsigned int a;
unsigned int b;
short unsigned int pTMR1 @ 0x0E;          //16 bits of timer1 are named as pTMR1
short unsigned int i;                     //Used in loop
short unsigned int j;
unsigned char final_voltage_reading;
unsigned char voltage_reading[10];
unsigned short int bank1_final_voltage;
unsigned short int bank2_final_voltage;
unsigned short int bank3_final_voltage;
unsigned char timer1_overflow;
unsigned int average_voltage;

// Initial conigfuartions
__CONFIG(INTIO & WDTDIS & PWRTEN & MCLRDIS & UNPROTECT & BORDIS );

unsigned short int read_adc(void)
{
    unsigned short int temp_adc_results;          //Used in read_adc function
    temp_adc_results = 0;
    GODONE = 1;
    while(GODONE);
    temp_adc_results = (ADRESH<<8)+ADRESL;
    return temp_adc_results;                      //Return 8 bit ADC value
}//read_adc
```

```
unsigned short int average_adc_value(void)
{
   unsigned short int voltage = 0;
   unsigned char i;
   for (i=0;i<10;i++)
     {
          voltage +=read_adc();
     }
          voltage /=10;
   return voltage;
}

void delay_a_sec(void)
{
     TMR1ON = on;
     while (timer1_overflow<3);
     TMR1ON = off;
     timer1_overflow = 0;
}

void delay_long(void)
{
     TMR1IE = set;
     TMR1ON = on;
     while (timer1_overflow<5);
     TMR1IE = clear;
     TMR1ON = off;
     timer1_overflow = 0;
}

void delay_a_bit(void)
{
```

```
    for(j=0;j<10000;j++);
}

void select_zero_channel(void)
{
                                        //AN4 (RC0) is zero crossing
   ADCON0 = 0B10010001;                  //Bit 7 = 1 (Right justified)
                                        //Bit 6 = 0 (Reference bit VDD)
                                        //Bit 5,4,3,2 = 0100 (AN4)
                                        //Bit 1=0 ADC off yet
                                        //Bit 0 = 1 ADC enable

}//select_switch_channel

//Function which used select the proper capacitor bank for ADC
void select_bank1_sense_channel(void)
{
                                        //AN0 (RA0) Bank 1 voltage
   ADCON0 = 0B10000001;                 //Bit 7 = (Right justified)
                                        //Bit 6 = 0 (Reference bit VDD)
                                        //Bit 5,4,3,2 = 0000 (AN0)
                                        //Bit 1 = 0 ADC off yet
                                        //Bit 0 = 1 ADC enable
}//select_voltage_sense_channel

void select_bank2_sense_channel(void)
{
                              //AN2 (RA2) Bank 2 voltage
   ADCON0 = 0B10001001;                     //Bit 7 = 1 (Right justified)
                                            //Bit 6 = 0 (Reference bit VDD)
                                            //Bit 5,4,3,2 = 0010 (AN2)
                                            //Bit 1=0 ADC off yet
                                            //Bit 0 = 1 ADC enable
```

```
}//select_voltage_sense_channel

void select_bank3_sense_channel(void)
{
                                        //AN3 (RA4) Bank 3 voltage
   ADCON0 = 0B10001101;                 //Bit 7 = 1 (Right justified)
                                        //Bit 6 = 0 (Reference bit VDD)
                                        //Bit 5,4,3,2 = 0011 ( AN3)
                                        //Bit 1=0 ADC off yet
                                        //Bit 0 = 1 ADC enable
}//select_voltage_sense_channel

void select_IGBT_fault_channel(void)
{
                                            //AN1 (RA1) IGBT
   ADCON0 = 0B10000101;                     //Bit 7 = 1 (Right justified)
                                            //Bit 6 = 0 (Reference bit VDD)
                                            //Bit 5,4,3,2 = 0001 (AN1)
                                            //Bit 1=0 ADC off yet
                                            //Bit 0 = 1 ADC enable
}//select_voltage_sense_channel

/////// Bank-States Disp /////////////////
void bank1_status_charge(void)
{
     BANK1_DISP = on;
     delay_a_sec();
     BANK1_DISP = off;
     delay_a_sec();
}

void bank2_status_charge(void)
```

```
{
   BANK2_DISP = on;
   delay_a_sec();
   BANK2_DISP = off;
   delay_a_sec();
}

void bank3_status_charge(void)
{
   BANK3_DISP = on;
   delay_a_sec();
   BANK3_DISP = off;
   delay_a_sec();
}

/////////dicharge/////////

void bank1_status_discharge(void)
{
   BANK1_DISP = on;
}

void bank2_status_discharge(void)
{
   BANK2_DISP = on;
}

void bank3_status_discharge(void)
{
   BANK3_DISP = on;
}

////////////idle//////////////
```

```
void bank1_status_idle(void)
{
   BANK1_DISP = off;
}
void bank2_status_idle(void)
{
   BANK2_DISP = off;
}

void bank3_status_idle(void)
{
   BANK3_DISP = off;
}

void bank1_status_dead(void)
{
      DEAD_DISP = on;
}

void bank2_status_dead(void)
{
      DEAD_DISP = on;
}

void bank3_status_dead(void)
{
      DEAD_DISP = on;
}

void init (void)
{
```

```
VRCON    = 0;              // Turn off voltage reference Peripheral

OSCCON = 0b01100000;       // 4 MHz
//OSCCON = 0b01110000;     // 8 MHz

ANSEL = 0b00011111;        // AN0-4 are analog input
                           // AN0:IGBT Fault,
                           // AN1:bank1, AN2: bank2, AN3: bank3
                           // AN4: zero crossing
ANSELH = 0;                // all digital I/O

// set Port A
TRISA = 0b00010111;        // RA0,1,2,4 are input
PORTA = 0;

// set PortB
TRISB = 0;                 // portB are outputs
PORTB = 0;

//set Port C
TRISC = 0b00000001;        // RC0 is input as zero corssing
                           // RC5 output for pwm
PORTC = 0;

//timer0
OPTION = 0b00000000;       // disable portA weak pull up
                           // interupt on the rising edge
                           // internal clock
                           // increment on low to high
                           // prescale 1:2
//timer1
T1CON = 0b00110000;        //prescle 1:8 16 bit timer=0.262sec/cycle
TMR1IF = clear;
```

```
    TMR1IE = 1;

    // pwm
    T2CON = 0b00000000;     // prescle 1:1
    pwm_fre = 20;           // 50kHz
    CCP1CON = pwm_on;       // bit7-6: signal output, P1A
                            // bit5-4: lower bits are zero
                            // bit3-0: PWM mode; P1A, P1C active-higt
    pwm_duty = 18;          // duty cycle (min 14)
    TMR2IF = clear;         // interrupt flag
    TMR2IE = 1;
    TMR2ON = 1;

    // interruputs
    T0IE = 1;               // timer0 overflow enable
    T0IF = clear;           // clear timer0 flag

    GIE = 1;

//self testing///
    BANK1_DISP ^= 1;
    BANK2_DISP ^= 1;
    BANK3_DISP ^= 1;
    delay_a_sec();

    BANK1_DISP ^= 1;
    BANK2_DISP ^= 1;
    BANK3_DISP ^= 1;
    delay_a_sec();

    BANK1_DISP ^= 1;
    BANK2_DISP ^= 1;
```

```
    BANK3_DISP ^= 1;
    delay_a_sec();

    BANK1_DISP = 0;
    BANK2_DISP = 0;
    BANK3_DISP = 0;
}


void main (void)
{
    timer1_overflow = 0;

    init ();

    select_bank1_sense_channel();
    delay_a_bit();
    bank1_final_voltage = average_adc_value();
    while(bank1_final_voltage>HIGH_READING)
//If the capacitor is not charged do this while loop
    {
        bank1_status_charge();
        BANK1_CHARGE = ON_MOSFET;
        bank1_final_voltage = average_adc_value();     //until it is charged
    }
    bank1_status_idle();
    BANK1_CHARGE = OFF_MOSFET;
    delay_a_bit();

    select_bank2_sense_channel();
    delay_a_bit();
    bank2_final_voltage = average_adc_value();
    while(bank2_final_voltage>HIGH_READING)
```

```
//If the capacitor is not charged do this while loop
    {
        bank2_status_charge();
        BANK2_CHARGE = ON_MOSFET;
        bank2_final_voltage = average_adc_value();          //until it is charged
    }
    bank2_status_idle();
    BANK2_CHARGE = OFF_MOSFET;
    delay_a_bit();

    select_bank3_sense_channel();
    delay_a_bit();
    bank3_final_voltage = average_adc_value();
    while(bank3_final_voltage>HIGH_READING)
    {
//If the capacitor is not charged do this while loop
        bank3_status_charge();
        BANK3_CHARGE = ON_MOSFET;
        bank3_final_voltage = average_adc_value();     //until it is charged
    }
    bank3_status_idle();
    BANK3_CHARGE = OFF_MOSFET;
    delay_a_bit();

//All the capacitors are charged now start discharging capacitor 1


    while (1)
    {
        select_bank1_sense_channel();
        bank1_final_voltage = average_adc_value();
        select_bank3_sense_channel();
```

```
        bank3_final_voltage = average_adc_value();

    while((bank1_final_voltage<LOW_READING)  |  (bank3_final_voltage>
HIGH_READING))
        {
            select_bank1_sense_channel();
            bank1_final_voltage = average_adc_value();
            if (bank1_final_voltage<LOW_READING)
            {
                bank1_status_discharge();
                BANK1_DISCHARGE = ON_MOSFET;
                bank1_final_voltage = average_adc_value();
            }

            select_bank3_sense_channel();
            bank3_final_voltage = average_adc_value();
            if (bank3_final_voltage> HIGH_READING)
            {
                bank3_status_charge();
                BANK3_CHARGE = ON_MOSFET;
                bank3_final_voltage = average_adc_value();
            }
            else
            {
                BANK3_CHARGE = OFF_MOSFET;
                bank3_status_idle();
            }
        }

    BANK1_DISCHARGE = OFF_MOSFET;
    bank1_status_dead();
    delay_a_bit();
```

```
////////////////////////////////////////////////////////////////////

    select_bank2_sense_channel();
    bank2_final_voltage = average_adc_value();
    select_bank3_sense_channel();
    bank3_final_voltage = average_adc_value();

    while((bank2_final_voltage<LOW_READING)                    |
(bank1_final_voltage>HIGH_READING))
    {
        select_bank2_sense_channel();
        bank2_final_voltage = average_adc_value();
        if(bank2_final_voltage < LOW_READING)
        {
            bank2_status_discharge();
            BANK2_DISCHARGE = ON_MOSFET;
        }

        select_bank1_sense_channel();
        bank1_final_voltage = average_adc_value();

        if(bank1_final_voltage>HIGH_READING)
        {
            bank1_status_charge();
            BANK1_CHARGE = ON_MOSFET;
        }
        else
        {
            BANK1_CHARGE = OFF_MOSFET;
            bank1_status_idle();
        }
    }
```

```
    BANK2_DISCHARGE = OFF_MOSFET;
    bank2_status_dead();
    delay_a_bit();

////////////////////////////////////////////////////////////

        select_bank3_sense_channel();
        bank3_final_voltage = average_adc_value();
        select_bank2_sense_channel();
        bank2_final_voltage = average_adc_value();

        while((bank3_final_voltage<LOW_READING)                    |
(bank2_final_voltage>HIGH_READING))
        {
            select_bank3_sense_channel();
            bank3_final_voltage = average_adc_value();

            if(bank3_final_voltage < LOW_READING)
            {
                bank3_status_discharge();
                BANK3_DISCHARGE = ON_MOSFET;
            }

        select_bank2_sense_channel();
        bank2_final_voltage = average_adc_value();

        if(bank2_final_voltage>HIGH_READING)
        {
            bank2_status_charge();
            BANK2_CHARGE = ON_MOSFET;
        }
        else
        {
```

```
                BANK2_CHARGE = OFF_MOSFET;
                bank2_status_idle();
            }
            }
            BANK3_DISCHARGE = OFF_MOSFET;
            bank3_status_dead();
            delay_a_bit();

}

}

void interrupt isr (void)
{

    if (TMR1IF)
    {
        TMR1IF = clear;
        timer1_overflow++;
        return;
    }

    if (T0IF)
    {
        T0IF = clear;
        return;
    }

}
```

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