Pulse-Shaping Feed-Forward-Compensated Generator

Sinduja Seshadri, *Student Member, IEEE*, Jonathan Scott, *Senior Member, IEEE*

***Abstract*—A typical electrical stimulator has a battery, step-up converter, voltage regulator, pulse generator with a micro-controller providing the clocking signal. This outputs a step response with a specified amplitude and pulse-width. In this work, Single-Ended Primary Inductance Converter (SEPIC) and Cúk converter are built to output a step response without the requirement of a voltage regulator and a pulse generator. The transfer function of both instruments predict a step response that will overshoot but settle to steady-state. This is true when the drive is of a fixed duty cycle. We show that the overshoot can be reduced or completely removed by sending an irregular pulse waveform to the drive, determined from the transfer function of the converters. Sufficiently adjusting the duty cycles of drive pulses forces the converter to rapidly reach steady-state value. As a result, a programmable converter delivers a well-formed pulse of specific length without the need for additional circuitry.**

keywords: pulse generator, pulse-shaping, biomedical, Cúk, SEPIC

I. Introduction

A neuromodulation system delivers pulses to the electrode inserted in a patient. Electrical charge is applied to effect stimulation of the neural tissue. This charge is of the form of a pulse defined by its pulse-width, amplitude and occurs at varying specified frequencies. Each applied stimulus provides the patient with relief.

The neurostimulator package contains three primary components: a centralised implantable pulse generator (IPG), one or more leads and one or more electrodes (for stimulating and recording signals) [1]. The IPG houses a battery and other circuitry which generates the desired pulses. Usually, the output voltage required is greater than the battery voltage and is typically accomplished by a Switched Mode Power Supply (SMPS). The electrodes receive the pulses through an analog circuitry connected to the output stage. A typical structure of an electrical stimulator is shown in Fig. 1 modified from [2].

The output voltage of a SMPS can be maintained at the desired voltage for an arbitrary length of time specified at the input of the switching element. Thus, the SMPS can deliver the required voltage to the electrode in the form of a pulse directly, instead of the circuitry in the output stage in Fig. 1. In this manuscript, we propose such an IPG design, shown in Fig. 2, that eliminates the analog pulse generating circuitry in Fig. 1 for electrode stimulation.

We investigate with Cúk and SEPIC as the 'VOLTAGE REGULATOR SMPS' in Fig. 2. Typically a boost converter steps up the battery voltage and an LDO drops this voltage before it reaches the pulse generator. Cúk and SEPIC, on the other hand, produce an output voltage that can be greater or smaller than the battery voltage as stipulated by the user.

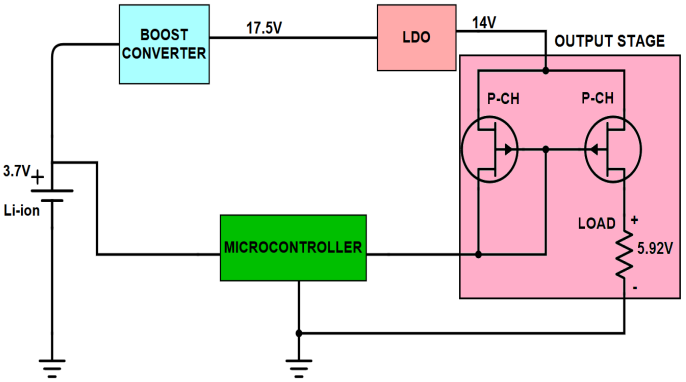

Fig. 1. Block diagram of a typical embedded electrical stimulator modified from [2]. The battery is usually a 3.7V Li-ion cell which is stepped up to 17.5V by a boost converter and fed into the low-dropout (LDO) regulator. The 15V output of the LDO is connected to the input of the current mirror array which switches according to input pulse current for a set period of time, specified at the microcontroller. A 5.92V output is in the form of a pulse observed over the stimulating electrodes, modelled as a resistive load ($\sim$1kΩ).

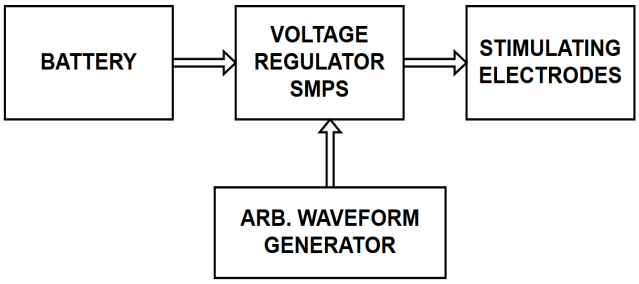

Fig. 2. Block diagram of the proposed IPG design. The SMPS provides the desired output voltage by programming a set of pulses with arbitrary duty cycles to the clock input.

The output pulse reaching the electrodes is produced by the step response of Cúk and SEPIC with respect to the gate drive. The gate drive is a pulse train which can be specified to a length of time. The output pulse will be of the same duration as the input pulse train and the step response from SMPS is directly delivered to the electrode. However this step response is inexpedient in neuromodulation applications.

The transfer function of both SMPS predict an overshoot

due to Cúk's two and SEPIC's three complex conjugate pairs of poles. The high-order, underdamped transfer functions of these converters would normally result in a very unsuitable pulse, showing overshoot and long decay times. This may require additional circuitry to compensate for the overshoot.

We show that the overshoot can be regulated without requiring additional circuitry. Observing the location of poles, we can empirically control the overshoot by sufficiently varying the duty cycles of the input pulse train. Adjusting the duty cycle of the drive allows for Cúk and SEPIC to deliver a shapely pulse for the requisite duration.

This paper is organised as follows: Section II discusses a brief review of literature; Section III outlines the design of the SMPS pulse generators; Section III-B explains the expected behaviour from the converters; Section IV shows the results of our proposed pulse generator and conclusions close the paper.

II. State of the art

The IPG design shown in Fig. 1 is a popular design in literature because efficient SMPS regulation demonstrated measurable extension of battery life. For example, Jalilian et al. (2004) [3] developed a gastric and colonic neurostimulator by utilising a MAX686, which is a DAC controlled boost inverter, to extend the longevity of the device. The switching converter produced a DC voltage between 4V and 10V from input voltages as low as 0.8V. The analog switches generated 1000 chronic colonic stimulations at varying DC voltages, indicating an IPG life of 1.3 years at a usage rate of two times per day. As a result, improving the efficiency of the SMPS stage has persisted as a strong area of research [2], [4]–[7].

The IPG design in Fig. 1 is implemented using SPICE simulator and the results are produced in Figs. 3 and 4. Effect

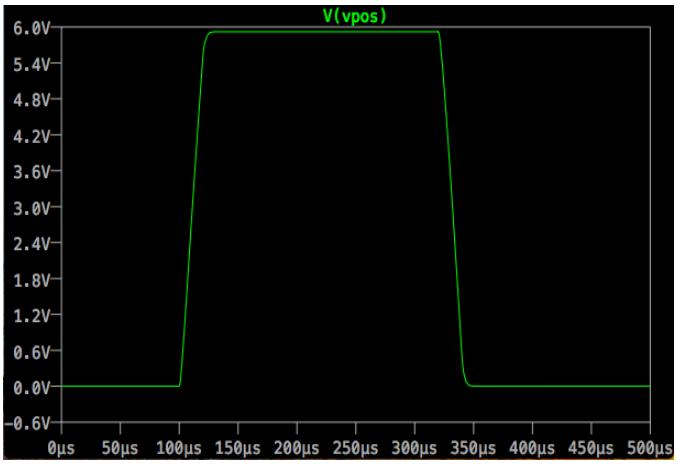

Fig. 3. The output pulse has an amplitude of 5.9V and a pulse-width of 200μs, which is the stimulation period.

of current design is not measured against battery life of the IPG. The aim of this work is to present an alternate design to the existing topology to demonstrate that the same results may be produced with much less circuitry.

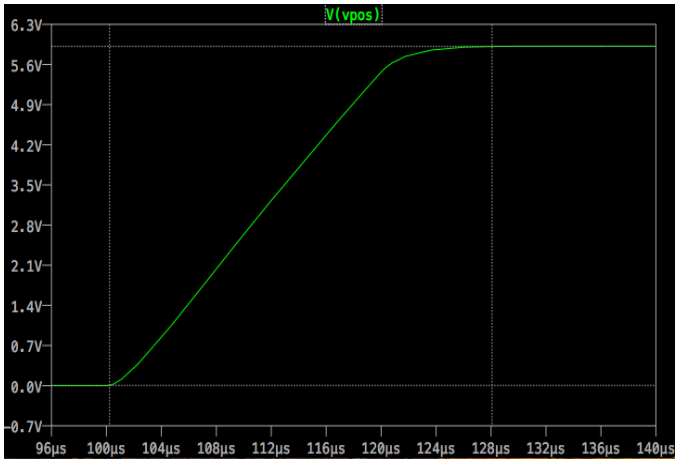

Fig. 4. The settling time $\approx 28\mu s$ which is the time taken to reach steady state value. The grey lines span from $100\,\mu s$ to $128\,\mu s$, the time it takes for the pulse to rise and settle to steady state.

III. Methodology

A. Converter designs

The converters are built in an open loop configuration. Cúk and SEPIC, shown in Figs. 5 and 6 respectively, are both operating in continuous conduction mode and under steady-state conditions. Both converters use an N-channel MOSFET and a Schottky diode as switches. TSM2N7000K transistor has an input gate capacitance of 7 pF which is very small and useful for obtaining a fast switching frequency such that little energy is wasted by the driver stage. The SR1100 offers a higher switching capability compared to a silicon diode.

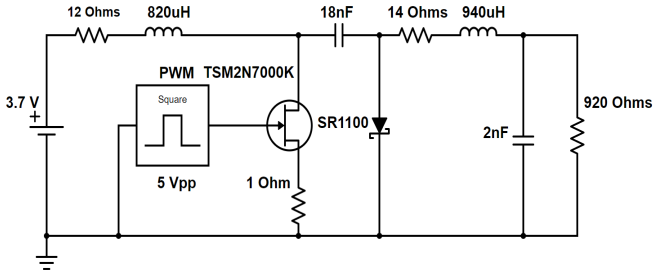

Fig. 5. Cúk converter with the values of components calculated from the dynamic and steady-state model presented in [8] and [9]. The model includes the parasitic resistances of the inductors along with the 1 Ω resistor to measure drain current. The electrode-tissue impedance is characterised as a resistive load of 920 Ω. The source is a Li-ion battery and the PWM is an Agilent 33220A arbitrary waveform generator that drives the gate.

The output voltage of Cúk and SEPIC will overshoot before settling to steady state, Figs. 9 and 10. We require a pulse similar to Fig. 3 for the converters to operate as an effective pulse generator. If the gate drive is a fixed duty cycle square pulse train, the output will overshoot before steady state voltage is reached. To correct the overshoot we can dynamically adjust the duty cycles of the pulse train (i.e. send an arbitrary pulse

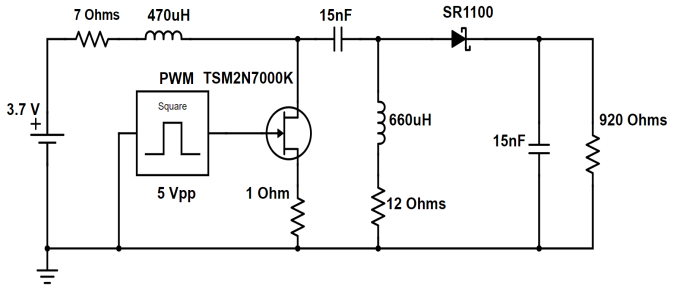

Fig. 6. SEPIC with the values of components calculated from the dynamic and steady-state model presented in [8] and [9]. The model includes the parasitic resistances of the inductors along with the 1 Ω resistor to measure drain current. The electrode-tissue impedance is characterised as a resistive load of 920 Ω. The source is a Li-ion battery and the PWM is an Agilent 33220A arbitrary waveform generator that drives the gate.

wave) determined empirically from the trajectory of poles of their respective transfer functions.

B. Step response from transfer function

The duty cycle to output voltage transfer function for the Cúk and SEPIC are given by (1). Cúk and SEPIC's numerator and denominator constituents are given by (2) and (3), respectively [8].

$$H(s) = \frac{num(s)}{den(s)}. \tag{1}$$

The $num(s)$ and $den(s)$ are:

$$\begin{aligned} num(s) &= (C_1L_1(V_{in}+V_{out}))s^2 - (DL_1(I_{in}+I_{out}))s \\ &\quad + (D')(V_{in}+V_{out}), \\ den(s) &= (C_1C_2L_1L_2)s^4 + \frac{C_1L_1L_2}{R}s^3 \\ &\quad + (C_2L_1D^2 + C_2L_2(D')^2)s^2 \\ &\quad + \Big(\frac{L_1D^2}{R} + \frac{L_2(D')^2}{R}\Big)s + (D')^2, \end{aligned} \tag{2}$$

$$\begin{aligned} num(s) &= -(C_{11}L_{11}L_{22}(I_{in}+I_{out}))s^3 \\ &\quad + (C_{11}(L_{11}+L_{22})D'(V_{in}+V_{out}))s^2 \\ &\quad - (L_{11}D(I_{in}+I_{out}))s + D'(V_{in}+V_{out}), \\ den(s) &= (C_{11}C_{22}L_{11}L_{22})s^4 + \frac{C_{11}L_{11}L_{22}}{R}s^3 \\ &\quad + (C_{22}L_{11}D^2 + C_{11}L_{11}(D')^2 + C_{11}L_{22}(D')^2)s^2 \\ &\quad + (C_{22}L_{22}(D')^2)s^2 + \Big(\frac{L_{11}D^2}{R} + \frac{L_{22}(D')^2}{R}\Big)s \\ &\quad + (D')^2, \end{aligned} \tag{3}$$

where D is the duty cycle for the ON state and $D' = 1 - D$ for the OFF state. C_1, L_1, C_2, L_2 represent Cúk's components and C_{11}, L_{11}, C_{22}, L_{22} represent SEPIC's components. The pole-zero map is constructed using component values from Figs. 5 and 6; the following eight values for the duty cycle:

$$D = [0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9],$$

and for each duty cycle, the output voltage V_{out}, is cycled from 2 V to 9 V.

The transfer functions are plotted in Figs. 7 and 8. Fig. 7 shows the Pole-Zero plot for the Cúk converter. Fig. 8 shows only the poles for the SEPIC as the zeros mimic the plot from [8]. Cúk produces two complex conjugate pairs of poles while SEPIC has three complex conjugate pairs.

The movement of poles suggest that the step response will overshoot and settle to steady-state. Each data point in the curve of the overshoot is a voltage V_{OS}, which is a different value to the steady-state voltage V_{SS}. If we sufficiently adjust the duty cycle of the drive to equal the duty cycle of V_{OS}, the overshoot should minimise. Cúk's dominant poles' proximity suggests that we have to provide a longer duration of drive pulses with varying duty cycles compared to SEPIC's dominant pole locations. The typical response curve will transform to a clean step response without the overshoot.

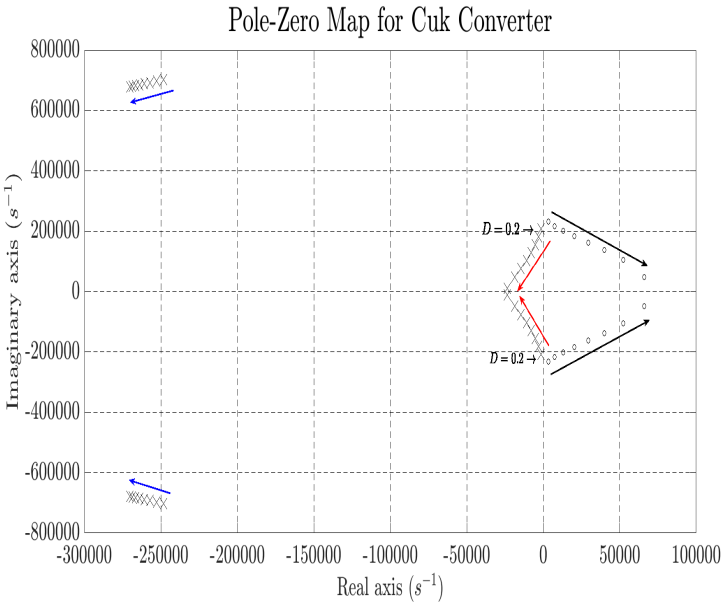

Fig. 7. The transfer function produces two complex conjugate pairs of poles with varying duty cycles. Poles denoted by the red arrow are dominant poles. Poles indicated by the blue arrow do not affect system stability. The diagonal trajectory of the dominant poles suggest that the output of the converter is going to overshoot before settling to steady-state. Also the poles are very close in proximity to each other.

IV. Results and Discussion

There are two sets of waveforms for each converter with the following parameters. The first waveform is the result of sending a drive of fixed duty cycle. The second waveform is the result of sending a drive of varying duty cycles to correct the overshoot. Each waveform is set to reach V_{SS} of 8 V. The drive is a burst of pulses, 320 μs long and occurs every 16 ms. All pulses in the drive of the first set of waveforms have 70 % duty cycle. To correct the overshoot in Cúk, the first 45 μs of the drive has varying duty cycles and the remaining 275 μs is fixed at 70 %. Similarly for the SEPIC, varying duty cycle drive is 21 μs long and 300 μs of the burst is of fixed

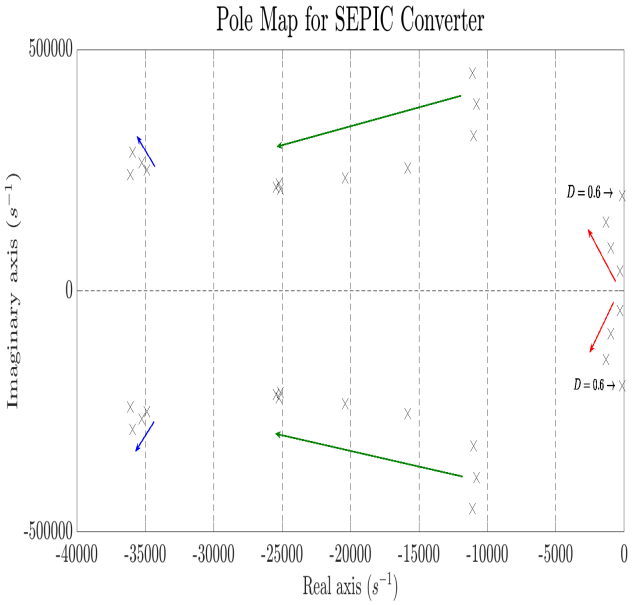

Fig. 8. The transfer function produces three complex conjugate pairs of poles with varying duty cycles. Poles marked by the red arrow are dominant poles. Poles indicated by the green and blue arrows do not affect system stability. The loosely spaced apart diagonal trajectory of the dominant poles suggest that the output of the converter will overshoot before settling to steady-state.

duty cycle. The original and corrected responses are shown in Figs. 9, 11, 10 and 12.

Trajectory of the poles determine the sharpness of the step response. Observe in Fig. 11, the overshoot is not completely suppressed in the Cúk converter, while the overshoot is non-existent in the SEPIC, Fig. 12. The acute diagonal configuration of Cúk's poles indicate that muzzling the overshoot is a non-trivial endeavour. Figs. 10 and 12 demonstrate the contrary argument for SEPIC poles' locations. Proving the relationship between the transfer function and the input pulse waveform that suppresses the overshoot is analytically difficult.

The settling times for SEPIC: $t_{s,pre} = 60\,\mu$s, $t_{s,post} = 28\,\mu$s; Cúk: $t_{s,pre} = 120\,\mu$s, $t_{s,post} = 50\,\mu$s; where the subscripts pre and $post$ refer to before and after varying the duty cycles of the drive. SEPIC has a better response time than Cúk and the settling time is comparable to existing IPG design simulation from Fig. 4.

Table I: Simulated results of existing IPG design

V_{SS} (V)	t_s (s)
3.92	28.0μ
4.24	28.0μ
4.57	28.0μ
4.72	28.0μ
5.04	28.0μ
5.37	28.0μ
5.53	28.0μ
5.92	28.0μ
6.32	28.0μ
6.63	28.0μ

Table II: Measured results of SEPIC

V_{SS} (V)	Duty cycle	V_{OS} (V)	$t_{s,pre}$ (s)	$t_{s,post}$ (s)	$t_{s,pre-post}$ (s)
3.92	0.50	1.44	64.4μ	30.4μ	34.0μ
4.24	0.52	1.44	64.4μ	28.0μ	36.4μ
4.56	0.54	1.56	64.4μ	31.6μ	32.8μ
4.72	0.55	1.64	64.4μ	28.4μ	36.0μ
5.04	0.57	1.60	60.4μ	30.8μ	29.6μ
5.36	0.59	1.64	60.0μ	30.0μ	30.0μ
5.52	0.60	1.64	59.6μ	29.2μ	30.4μ
5.92	0.62	1.56	58.0μ	30.4μ	27.6μ
6.32	0.64	1.52	58.4μ	31.2μ	27.2μ
6.64	0.65	1.44	58.8μ	30.8μ	28.0μ

The results shown in Table I and Table II are comparable. The settling times of SEPIC varies between $28\,\mu s$ to $31\,\mu s$, similar to t_s of existing IPG design. Furthermore, SEPIC's settling times are only possible *after* correcting for the overshoot. While V_{OS} is not large, the settling time is twice as slow. Adjusting the duty cycles to suppress the overshoot makes SEPIC a viable candidate for further exploration in the application for medical implants.

V. Conclusion

We showed a programmable converter delivered a pulse of specific length with no overshoot. Varying the duty cycles of drive pulses controls the output waveshape and forces the converter to rapidly reach steady-state value. Empirically determining the pulse-width required to cancel the overshoot produced the desired step response. This pulse generator can provide insight into optimising the operation of electronics in implanted systems.

Acknowledgement

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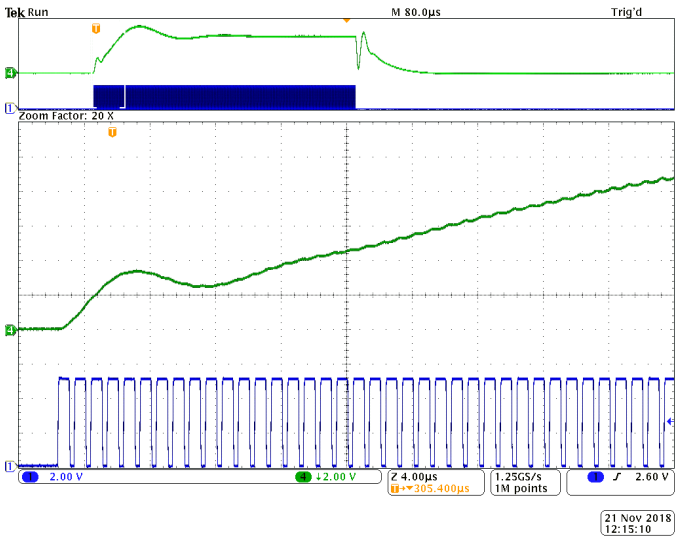

Fig. 9. Cúk converter shown with gate drive and output response. The pulses in blue are the drive and the curve in green is the output response. The top window shows the capture of the full output response and there is ringing at the start of the output response which has an amplitude of 3.7 V. This represents the inductor charging before boosting to 8 V. There is also ringing at the end of the green waveform which is a result of the LC-LC filter network in the converter. The bottom window is a close-up capture of the initial set of drive pulses. The duty cycle of the drive is 70 %. Note: output is inverted to show positive voltage.

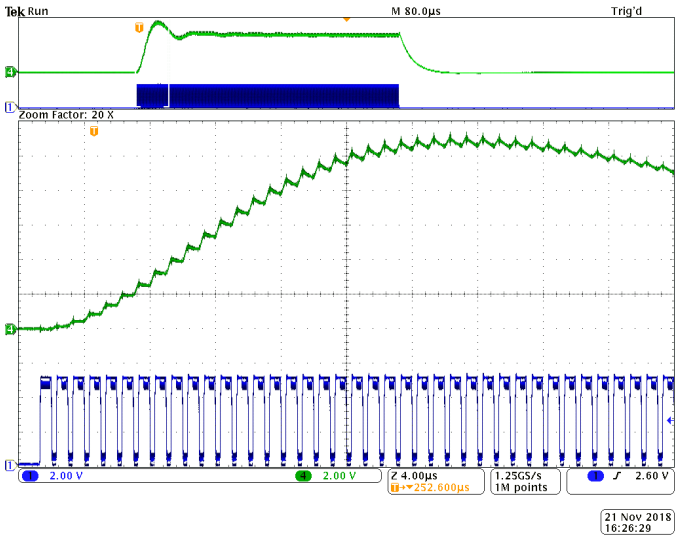

Fig. 10. SEPIC converter shown with gate drive and output response. The pulses in blue are the drive and the curve in green is the output response. The top window shows the capture of the full output response and there is no ringing at the start or at the end of the green waveform as the diode breaks the LC-LC filter loop. The bottom window is a close-up capture of the initial set of drive pulses. The duty cycle of the drive is 70 %.

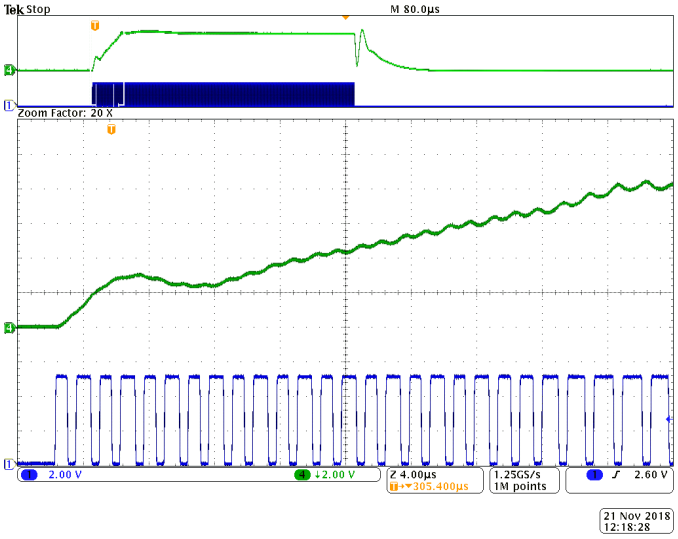

Fig. 11. Cúk converter shown with gate drive and output response. The pulses in blue are the drive and the curve in green is the output response. The top window shows the capture of the full output response. The overshoot is significantly smaller than Fig. 9. There is still ringing at the start of the output response with an amplitude of 3.7 V. This represents the inductor charging before boosting to 8 V. There is still that ringing at the end of the green waveform as a result of the LC-LC filter network in the converter. The bottom window shows a close-up portion of the initial set of drive pulses. The duty cycles range from $60 - 71\,\%$ for $45\,\mu$s. Once the output pulse approaches V_{SS}, the duty cycle is fixed at 70 %. Note: output is inverted to show positive voltage.

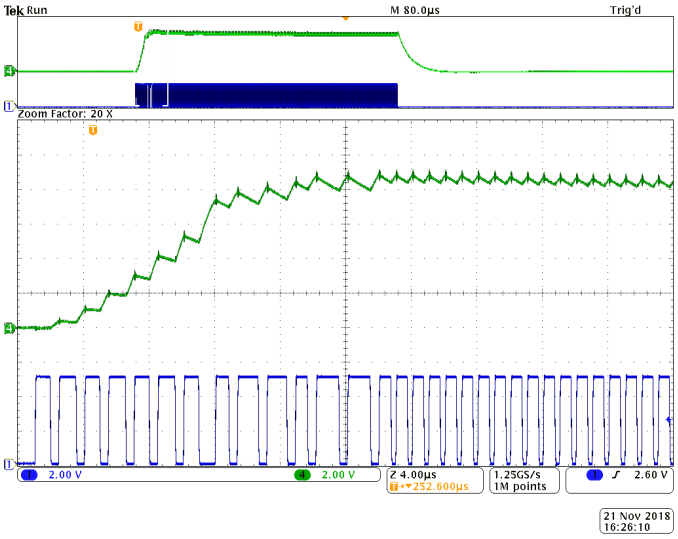

Fig. 12. SEPIC converter shown with gate drive and output response. The pulses in blue are the drive and the curve in green is the output response. The top window shows the capture of the full output response which has no overshoot. There is also no ringing at the start or at the end of the green waveform as the diode breaks the LC-LC filter loop. The bottom window is a close-up capture of a portion of the initial set of drive pulses. The duty cycle ranges from $57 - 74\,\%$ for $21\,\mu$s. Once the output pulse approaches V_{SS}, the duty cycle is fixed at 70 %.