Efficiency Enhancements to a Linear AC Voltage Regulator: Multi-transformer and Multi-winding Designs

A thesis submitted

for the degree of

Doctor of Philosophy

in Engineering

by

Priyanwada Nimesha Wijesooriya

The University of Waikato
Te Whare Wānanga o Waikato

June 2020

The University of Waikato

Abstract

Utility companies are expected to distribute electricity that conforms with international or national standards related to RMS voltage fluctuations. However, RMS voltage variations sometimes exceed acceptable limits and this demands consumer-end voltage regulators. Commercial AC regulators such as (i) servo-driven variacs, (ii) ferro-resonant, (iii) transformer tap changers, (iv) solid-state types, have their own advantages and limitations. Common issues include (a) slow response time, (b) low efficiency and flattened-output waveform, (c) tap dancing and related switching issues, (d) harmonics and RFI/EMI at the output, respectively.

The linear RMS AC voltage regulator is a patented technique developed in the late 1980s to address most of the above issues. It is a solid-state, single-phase system that employs a line-frequency transformer with its primary connected in series with an AC-operable variable impedance based on power transistors. The secondary winding is placed in series with the varying AC input, so that the induced secondary voltage acts as a correction signal to maintain the output at the desired value. A feedback circuit varies the effective impedance of the transistor-array, thus, manipulate the induced secondary voltage to regulate the output.

This is a linear technique that allows seamless transition between boost to buck mode. However, this comes at the cost of lower efficiency at high AC input, particularly when line voltage goes beyond the nominal value.

Commercial partner, Thor Technologies, Australia, wanted the team to modify their servo-driven AC regulator (PS-10), based on our technique with efficiency in the range of $90-95\%$ and the response time improved by about 10 times.

During development of a commercial prototype, the author implemented two potential solutions: (i) multi-transformer and (ii) multi-winding transformer based techniques to overcome the reduced efficiency during buck-mode operation, an issue inherent to the basic linear AC technique.

Thesis was aimed at improving the power stage of the linear technique while maintaining the already developed analog control loop with true RMS regulation capability. thesis presents two alternative transformer solutions to reach efficiencies in the range of $90-95\%$ on a laboratory prototype of 500 VA. Experimental results were validated by constructing a theoretical model for the two transformer configurations, supported by an equivalent circuit analysis using MATLAB and LTSpice software.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Scope

This thesis encompasses the implementation details of linear RMS AC voltage regulator with an enhanced efficiency compatible with commercial standards. It includes a brief summary on various power quality issues in power lines and solutions to mitigate such issues. There is also a discussion on different RMS voltage regulation techniques that can be fixed at the consumer premises in response to voltage fluctuations with a performance comparison between these designs. This thesis presents a detailed discussion on the two potential solutions for efficiency enhancement of the linear regulator; multi-transformer and multi-winding designs including experimental results validated by an analytical approach using transformer equivalent circuit models using MATLAB and LTspice simulations.

1.2 Background and motivation

Electric power quality that involves voltage, frequency and the waveform of the supply, is a significant factor that affects the performance of electrical devices used by both domestic and industrial customers [1–3]. Power quality quantifies electrical boundaries that allow electrical equipment to function in its intended manner without degrading performance or life-expectancy [3]. Any power-related disturbance that compromises either attribute is called a power quality issue. In general, power quality can be identified as the compatibility between the electric power supply and the equipment that is being powered.

Power quality can be affected by number of reasons throughout different phases of power generation to distribution. Following paragraph briefly describe a common architecture of an electric power network.

1.2.1 Power Distribution and Power Quality

Electricity is generated at different types of power plants such as fossil-fuel (coal, diesel), renewable power (geothermal, hydro-electricity, solar power, tidal, wind power) and nuclear power. According to the International Atomic Energy Agency (IAEA), the world's total electricity production by energy source is given in Figure 1.1. When the power is generated by electromechanical generators of these power plants, it is being transmitted at very high voltages (110 to 220 kV), to intermediate electrical substations through the transmission network. At this substation, the voltage is stepped down to medium voltage levels ranging from 33 kV to 66 kV phase-to-phase with the use of substation transformers. The power distribution begins at this point through the distribution network to the individual customer

utilities. Figure 1.2 shows a block diagram of the New Zealand electric power grid from generation to distribution [4]. When the electrical power is being distributed to the residential or commercial customers, the voltage is further lowered by step-down distribution transformers to the mains voltage which conforms the specified limits of voltage standards set by the country.

Power quality issues can be categorized as (i) RMS voltage fluctuations, (ii) transient surges, (iii) harmonics, (iv) noise, (v) short or long term blackouts. More detail on electromagnetic disturbances in the power distribution lines is provided in Chapter 2.

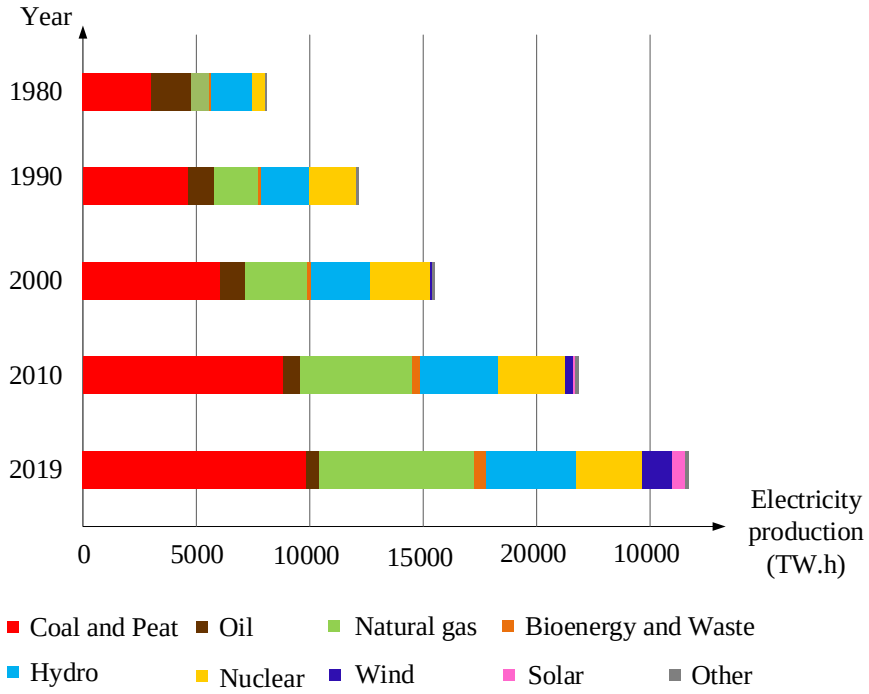


Figure 1.1: World's total electricity production by energy source. Data extracted from [5]

During the transmission and distribution process, the power quality can be significantly affected by different types of loads connected to the network, environmental conditions, human activities or imbalanced loading [1, 2, 6]. On the other hand, increasing demand for electrical energy and the proliferation of electronic devices can cause electromagnetic disturbances in the power distribution lines thus, degrade the power quality of the electric supply at the customer premises. The consequences of poor power quality can be sudden and unexpected [1, 2, 7]. It results in device malfunction and premature failure.

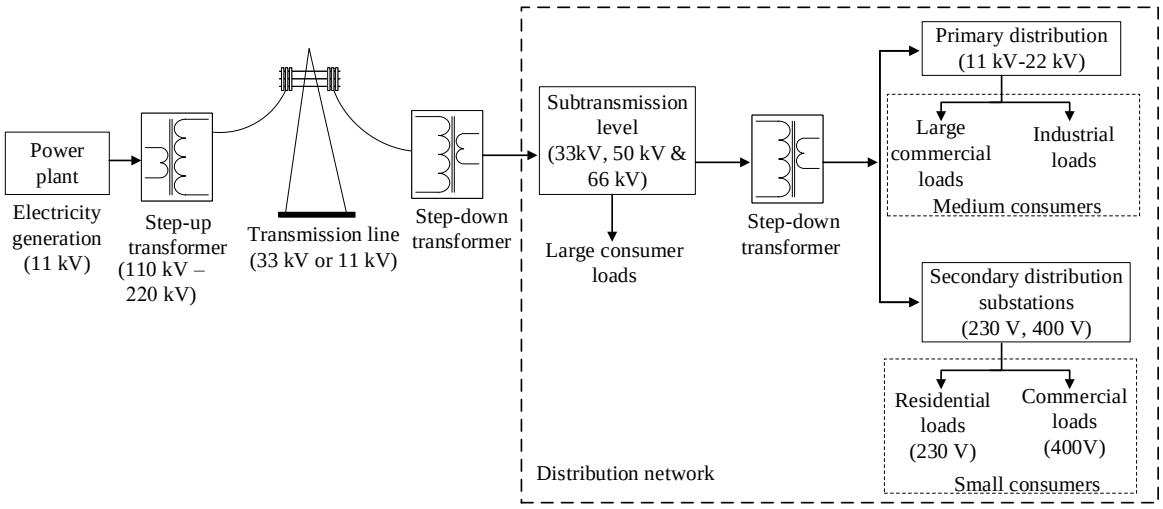


Figure 1.2: Electric power grid in New Zealand [4]

Regional Variation of Electrical Supply

There are regional variations to the voltage and frequency of the mains supply. Most of the countries and regions in Europe, Asia, Australia and New Zealand use 50 Hz, 220 or 230 V single phase, or 400 V three-phase for residential and low-user industrial customers. Countries like United States of America uses 60 Hz, 120 V or 120/240 V split-phase systems domestically and three-phase for large customers. Table 1.1 shows a comparison of standard mains voltage and frequency of different countries and regions around the globe [8, 9].

Table 1.1: Mains voltage and frequency

Country	**Geographical area**	**Residential voltage (V)**	**Three-phase voltage (V)**	**Frequency (Hz)**
Canada	North America	120	120/208	
		120	240	
		240	277/480	60
		240	347/600	
USA	North America	120	120/208	60
		277/480		
		240	120/240	60
		240	240 and 480	
Mexico	North America	220	220/480	60
Argentina	South America	230	380	50
Colombia	South America	110	220/240	60
Brazil	South America	127	220	60
		220	380	
Austria, Denmark, Italy, Sweden, United Kingdom France,Germany	Europe	230	400	50
Norway	Europe	230	230/400	50
New Zealand, Australia, Samoa	Oceania	230	400	50
Vanuatu	Oceania	220	400	50
Fiji	Oceania	240	415	50
Russia	North Asia	230	380	50
Japan	Asia	100	200	50
		200	415	60
Bangladesh, Vietnam	Asia	220	380	50
Sri Lanka, India, Singapore, Malaysia, Maldives	Asia	230	400	50
China, Hong Kong	Asia	220	380	50
North Korea	Asia	110	380	60
		220	380	50
South Korea	Asia	220	380	60
Ethiopia, Burkina Faso, Guinea, Namibia	Africa	220	380	50
Sudan	Africa	230	400	50
Kenya, Nigeria	Africa	240	415	50
South Africa	South Africa	230	400	50
United Arab Emirates	Middle East	220	400	50
Kuwait, Oman, Qatar	Middle East	240	415	50
Syria	Middle East	220	380	50

RMS variation of the supply voltage

Ideally, the wave shape of the voltage and the current distributed through the power grid should be a pure sinusoid without any harmonics or waveform distortions as illustrated in Figure 1.3. Usually, the voltage and the current of the utility supply is referred to the root mean square (RMS) value of the associated waveform. Assuming a periodic sinusoidal waveform V_t, of amplitude V_p, angular frequency ω and period T, the RMS value is given

$$V_{\text{RMS}} = \sqrt{\frac{1}{T}\int_{0)}^{T}(V_t)^2 dt} = \frac{V_{\text{p}}}{\sqrt{2}} = 0.707V_{\text{p}} \tag{1.1}$$

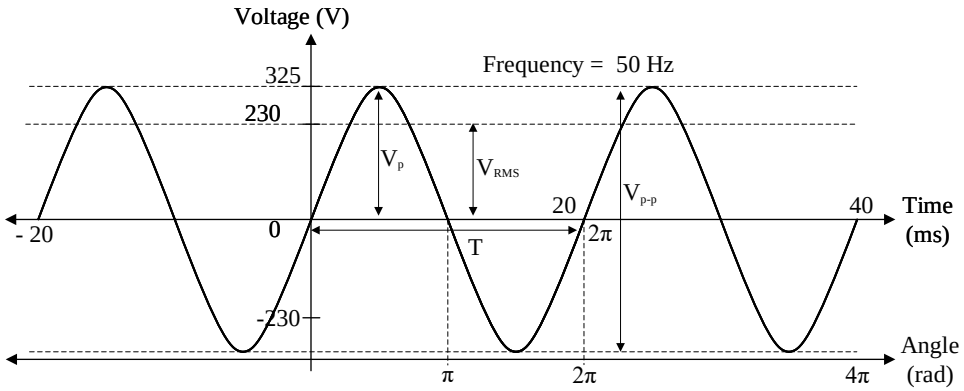


Figure 1.3: Ideal AC waveform of a typical 230 V supply

RMS voltage variation is a common power quality phenomenon seen at the consumer end [1, 7]. According to the definition in IEEE Std 1159$^{\text{TM}}$ – 2019 regarding recommended practice for monitoring electric power quality, RMS voltage variations can be categorized as voltage dips, swells, over-voltages and under-voltages depending on the magnitude and duration of occurrence which is summarised in Figure 1.4.

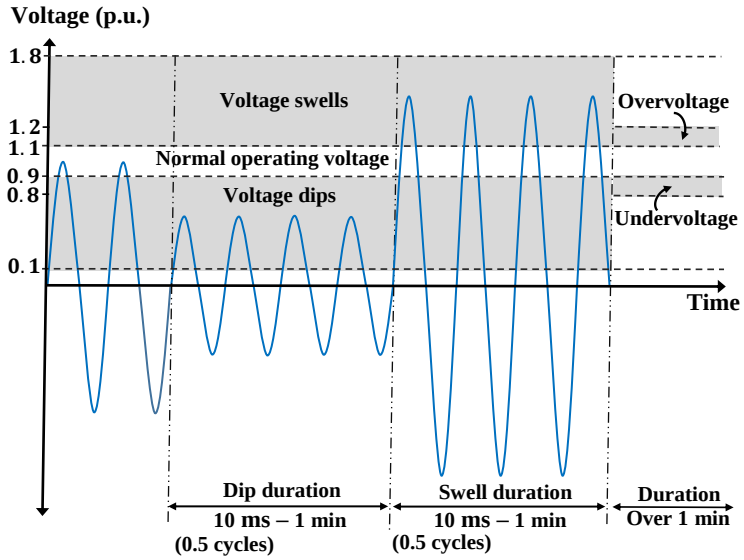


Figure 1.4: RMS voltage variations adapted from IEEE Std 1159$^{\text{TM}}$ – 2019.

Most modern equipment used in residential homes or industrial plants include sophisticated electronics such as computers, process controllers, adjustable speed drives, robotics, and programmable

logic controllers, is sensitive to voltage fluctuations. During a sag, processor-based equipment such as computers or data loggers may experience intermittent lock-up and garbled data. Besides, these low voltages can reset electromechanical relays or contactors in motor starters and shut down production lines and dependant systems. Consequences could include process delays, damaged products, wastage, and additional cost for repairing the damages before restarting the process [1, 2, 10].

Voltage swells are more destructive than sags. Overvoltages can break-down systems or power supply components and require costly repairs or equipment replacement [2, 10]. To mitigate RMS voltage variations, AC voltage regulators can be connected at the consumer end to achieve a constant voltage supply at the premises [1].

1.2.2 RMS AC voltage regulators and their common issues

A variety of AC voltage regulators are currently in use at the consumer endpoint to correct incoming RMS voltage variations. Commercially available AC voltage regulators can be divided into four common types: (1) servo-driven variacs, (ii) ferro-resonant regulators, (iii) transformer tap changers, (iv) solid-state regulators. The following paragraphs describe these traditional RMS AC voltage regulators and the significant drawbacks of these systems that motivated the authors to develop a unique technique to address those issues.

In *servo-driven variacs*, the active turns ratio of an autotransformer is continuously varied by a servo mechanism to achieve a constant output voltage for varying line voltages [11–13]. Although the mechanical system delivers reliable operation, it makes the regulator bulky and heavy. Unlike digital control systems, the mechanical moving parts are slow to respond and require regular maintenance to ensure consistent performance.

Ferro-resonance of a saturable inductor (coupled to a transformer winding) and a capacitor can be used to drive an inductor core into magnetic saturation to maintain a constant output voltage; hence, the name *ferro-resonant regulator*. Unfortunately, transformer operation in the saturation region is not efficient and results in a clipped sinusoidal output and high no-load power consumption [14, 15].

Transformer tap changers employ a feedback controller and a transformer with multiple taps in the secondary winding. In response to a fluctuating input line voltage, the taps are switched to regulate the output voltage. The switching is usually achieved by contactors or mechanical relays that may trigger arcing across taps if the input line voltage fluctuates rapidly [16, 17].

Solid-state regulators are popular due to their compact design and energy-efficient operation [18–20]. These products use thyristors or IGBTs under different operational principles. One such technique is a transformer-winding mechanism implemented by thyristor phase control, discussed in [20, 21]. Other types of switch-mode regulators, such as electronic transformers or DC-to-AC inverter-based regulators, commonly utilize a switching PWM scheme to regulate the output. However, due to the high-frequency operation of the switching devices, the output sinusoid is distorted with harmonics and RFI/EMI related defects which require additional filter circuits that increase the price of the device significantly [18, 22–24]. Moreover, most of these solid-state techniques are only capable of operating either in boost- or buck-mode as given in [19, 25–28]. Due to this single mode operation, these solid-state devices are not favourable in situations where the AC utility power supply possesses frequent voltage variations that fluctuate below the nominal value and increases beyond that. A detailed description of various AC voltage regulator types are provided in Section 2.2.

In many developing countries due to infrastructure limitations of the AC utility power supply, most of the above types are not well-positioned. Examples in Sierra Leon and Sri Lanka [29, 30] provide details. The extreme voltage variations in such countries motivate the development of reliable and low-cost products with easy manufacturability, which motivated the second author of the thesis to develop a low-cost RMS AC voltage regulator.

The linear AC regulator was originally developed in late 1980's aiming to overcome the typical issue of flattened sine wave in a ferro-resonant AC regulator [14] and the slow response time of $1-2$ s typical of servo-driven variacs which carries a bulky auto-transformer with a servo mechanism. Since the technique is based on a continually varying AC impedance generated by a power transistor array, it does not create the typical RFI/EMI issues common to switching type solid-state regulators.

Table 1.2 summarizes the operating principles of the different regulator designs and their pros and cons.

Table 1.2: Different families and techniques of AC voltage regulators

Basic technique used	Advantages	Disadvantages
Servo-based voltage regulators [11–13, 31, 32] Servo motor based autotransformer/transformer with a voltage feedback. Effective turns ratio of the transformer is changed in order to induce desired output voltage	• Very accurate output voltage regulation • High efficiency • Simple construction • Tolerant to device overloading, line frequency changes and power factor • Safety due to electrical isolation • Relatively inexpensive	• Bulky and heavy • Slow response due to mechanical moving parts • Can get stuck at the lowest input voltage and create an over-voltage when the line voltage returns to normal • Mechanical drive components require regular maintenance and replacement
Ferro-resonant regulators [14, 15, 33] A precisely gapped transformer is used in resonance with a capacitor to create a resonant circuit, while core saturation is used for regulating the output voltage	• Reliable • Simple design • Can withstand few cycle outage at the input side • Differential mode transients can be tolerated	• Flattened top non-sinusoidal output due to transformer core-saturation • Sensitivity to input voltage frequency fluctuations • Low efficiency • High no-load power consumption
Transformer tap changers [17, 34–36] Transformer with multiple taps and a feedback to automatically change the taps	• High efficiency • Simple construction • Low cost	• If input voltage fluctuates frequently, tap dancing can occur • Arcing in taps create problems with inductive loads • During tap changes, voltage transients can appear at the output

Solid state types **Subtype 1: Thyristor-based regulator** [20, 37] A series secondary winding or an autotransformer is used with thyristor phase control to maintain the RMS voltage at a constant level	• High efficiency • Fast response • Wide input range • Compact design	• Could cause problems with inductive loads • Complex circuitry • RFI/EMI problems (in switching technique based ones) • Reliability issues due to environmental conditions such as high common mode transient surges • Unidirectional operation (Boost or buck mode operation)
Subtype 2: High-frequency switch-mode RMS voltage regulator [16, 22–25, 28, 38–40] High frequency switched AC voltage regulator based on PWM control algorithm to regulate the output voltage		
Subtype 3: Series power transistor array based linear AC regulator [41] A power transistor-array connects in series to a transformer primary winding to regulate incoming voltage	• Harmonic-free, RFI/EMI free output waveform • Low cost • Fast response • Wide input range • Input and output electrically isolated • No core saturation issues and no mechanically moving parts • Insensitive to environmental conditions	• Efficiency drops due to heat dissipation across the semiconductors when input voltage exceeds nominal value

1.2.3 Essentials of the linear AC voltage regulator

This technique makes use of a two-winding transformer in which the primary is connected in series with a variable AC impedance as shown in Figure 1.5(a) [41, 42]. A traditional feedback circuit is used to monitor the output AC voltage and to convert that to an equivalent DC value using an RMS/DC converter IC. This equivalent DC voltage is compared with a DC reference value to control the impedance of a series semiconductor array placed across a rectifier bridge as shown in Figure 1.5(b). A constant voltage is maintained at the regulator output by varying the array impedance, hence manipulating the transformer primary winding to induce a corrective voltage in the secondary winding that is connected in the input-output load path.

This technique is fundamentally different to all of the previously described techniques due to the following properties [41–43]:

(a) A simple line-frequency step-down transformer with two windings is used

(b) A series-connected power transistor array works in a linear mode, so does not require high-frequency switching, thus eliminating RFI/EMI issues

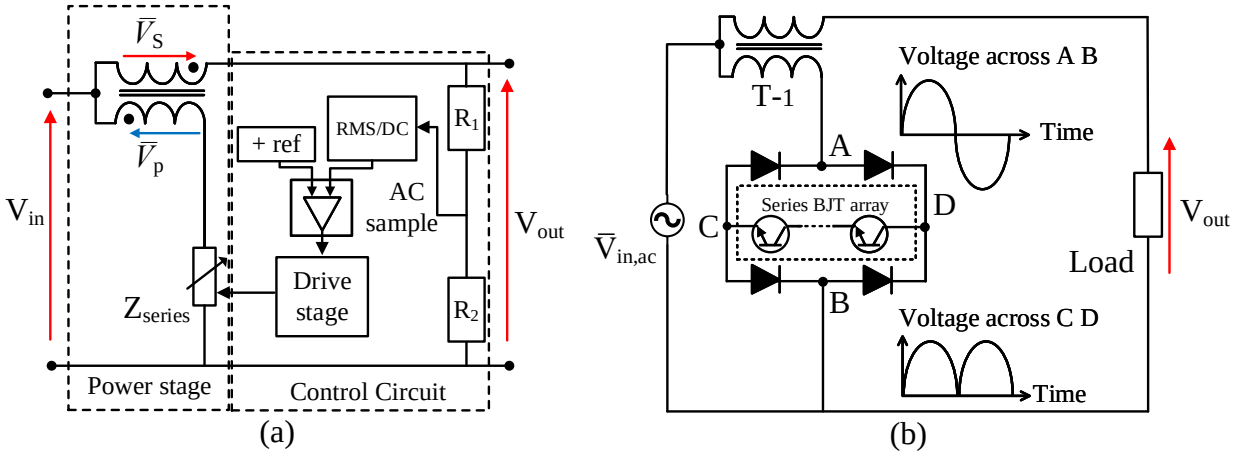


Figure 1.5: Basic block diagrams of linear AC regulator; (a) conceptual implementation (b) variable impedance

(c) The transistor array is connected to a transformer primary winding whose effective impedance is electronically controlled from near zero to a very high value, thus eliminating the need to physically change the winding configuration between boost to buck modes.

However, when the input voltage reaches the nominal value and goes beyond that, the required regulation is maintained by increasing the array impedance. This results in significant ohmic losses in the semiconductor array which leads to a decline in device efficiency at higher input voltages. To enable the linear regulator to be developed into a commercially useful prototype, this reduced efficiency issue needs to be addressed. The design team introduced two viable solutions to enhance efficiency at higher input line voltages enabling development of a commercially useful prototypes of 250 VA output capacity.

This thesis presents implementation details of two proposed solutions for efficiency enhancement of the linear AC regulator; (i) multi-transformer and (ii) multi-winding transformer regulator including analytical and experimental results validated by simulations.

1.3 Thesis outline

Following is a brief summary of the chapters that outline the thesis structure.

- Chapter 1 presents the background of the research and the motivational factors that led to develop linear RMS AC voltage regulator.
- Chapter 2 presents a brief introduction to various power quality issues in the utility power lines followed by several international standards to implement system compatibility. In addition, different types of conventional RMS AC voltage regulators are discussed and few examples are presented.
- Chapter 3 discusses the implementation details of the basic linear AC regulator including the design details of the series AC impedance employed by power transistor array and the digital feedback control circuit including the AC sampling block, electrical isolation unit, RMS/DC converter stage, delay start unit and the op-amp based amplifier circuit including a DC reference source.

- Chapter 4 describes the buck-boost capability of the regulator due to impedance variation of the series array and the drawbacks of this basic implementation of the linear AC technique.
- Chapter 5 discusses the series dual-transformer regulator developed for improving the efficiency of the base technique. It also includes experimental data and equivalent circuit analysis to validate the experimental data using MATLAB and LTspice software simulations.
- Chapter 6 provides a comprehensive description of a commercially useful technique to enhance the efficiency of the base technique using a multi-winding transformer followed by experimental data. It also includes an equivalent circuit analysis to model the design and validate the experimental data by performing a set of computer simulations.
- Chapter 7 details concluding remarks and future development.

1.4 Publication summary

1.4.1 Journal papers

- P.N. Wijesooriya, N. Kularatna and D. A. Steyn-Ross, "Efficiency enhancement to a linear AC voltage regulator: Multi-winding versus multi-transformer design," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, 2020 Jun 18; 1(2), pp. 192-199
- P.N. Wijesooriya and N. Kularatna, "A Review of AC Voltage Regulators," Multidisciplinary Digital Publishing Institute (MDPI), submitted 2020 Nov 29

1.4.2 Peer-reviewed conference papers

- P.N. Wijesooriya, N. Kularatna, J. Fernando, and D.A. Styne-Ross, "Series transistor array-based linear AC regulator: Role of multiple buck-boost transformer in efficiency improvements", Proc. of the International Symposium of Industrial Electronics (ISIE), 2017, Edinburgh, UK, pp. 1699 – 1704.
- P.N. Wijesooriya, N. Kularatna, J. Fernando, and D.A. Styne-Ross, "Two-transformer-series approach in developing a transistor based-AC voltage regulator for consumer-end applications", in 43rd anuual conference of the IEEE Industrial Electronics Society (IECON), 2017, Beijing, China, pp. 6437 – 6444.
- P.N. Wijesooriya, N. Kularatna, J. Fernando, and D.A. Styne-Ross,"Fast acting linear AC voltage regulator for consumer applications: Implementation options", in IEEE International Conference on Industrial Elelctronics for Sustainable Energy Systems (IESES), Hamilton, New Zealand, 2018, pp. 277 – 282.
- P.N. Wijesooriya, N. Kularatna, J. Fernando, and D.A. Styne-Ross,"Linear AC Voltage Regulator: Implementation Details of a Multi-Winding Approach", Proc. of the IEEE 27th International Symposium on Industrial Electronics (ISIE), 2018, Cairns, QLD, Australia, pp. 421 – 426.
- P.N. Wijesooriya, N. Kularatna, and D.A. Styne-Ross,"Use of multiple transformer windings for efficiency enhancement in the series transistor-array based linear AC voltage regulator", Proc. of Applied Power Electronics Conference and Exposition (APEC), 2018, Anaheim, CA, USA, pp. 2414 – 2419.

Chapter 2

Power Quality Issues and RMS AC Voltage Regulators

2.1 Power quality

Ideal utility power supply is expected to have a reasonably constant RMS voltage with no anomalies of waveshape. Several factors including the proliferation of electronic products and increasing demand for electricity, cause electromagnetic disturbances on the utility power lines. Power quality is an important aspect in electrical grids which determines the efficiency, reliability and security of electrical systems and equipment, whereas it has now become a key issue for electricity companies, industrial sites and equipment manufacturers for the following main reasons [1, 3, 6].

- *Growing of businesses* – Competitive growth of industries requires continuous and quality electricity-supply, with higher costs for installation and monthly energy bills. In addition, unexpected costs may arise due to power quality disturbances and related problems.
- *Proliferation of electronic equipment* – Use of sophisticated equipment adds numerous advantages to the consumers although, most of them are vulnerable to power quality disturbances while some of them generate disturbances and feed to the electric grid. Therefore the equipment manufacturers have to abide by relevant standards and recommendations specified by certain authorities/government for system compatibility.
- *Opening up of the electricity market* – Electricity generation has now been decentralized and electricity consumers can choose between potential suppliers. Thus the energy market has now been competitive over supplying quality and continuous electricity supply for low- medium- and large-scale electricity consumers.

2.1.1 Overview of power quality issues

The level of electromagnetic disturbances in the utility power lines determine the quality of the supply and has been officially identified by the international community and set up standards to qualify and quantify the disturbing electromagnetic phenomena. According to the standard of IEEE recommended practice for monitoring electric power quality (IEEE Std. $1159^{TM} - 2019$), power quality anomalies have been classified as (i) transients, (ii) short and long duration RMS variations, (iii) voltage/current imbalances, (iv) waveform distortions, (v) voltage fluctuations (vi) power frequency variations [1, 3, 7, 44]. Table 2.1 provides a general classification of electromagnetic phenomena in the utility supply.

Table 2.1: Categories and characteristics of power systems Electromagnetic Phenomena; data extracted from IEEE Standard- 1159^{TM} – 2019

Categories	Typical spectral content	Typical duration	Typical voltage magnitude
1.0 Transients			
1.1 Impulsive			
1.1.1 Nanoseconds	5 ns rise	$<$ 50 ns	
1.1.2 Microsecnds	1 μs rise	50 ns – 1 ms	
1.1.3 Milliseconds	1 ms rise	$>$ 1 ms	
1.2 Oscillatory			
1.2.1 Low frequency	$<$ 5 kHz	0.3 – 50 ms	0 – 4 pu
1.2.2 Medium frequency	5 – 500 kHz	20 μs	0 – 8 pu
1.2.3 High frequency	0.5 – 5 MHz	5 μs	0 – 4 pu
2.0 Short duration RMS variation			
2.1 Instantaneous			
2.1.1 Sag		0.5 – 30 cycles	0.1 – 0.9 pu
2.1.2 Swell		0.5 – 30 cycles	1.1 – 1.8 pu
2.2 Momentary			
2.2.1 Interruption		0.5 cycles – 3 s	$<$ 0.1 pu
2.2.2 Sag		30 cycles – 3 s	0.1 – 0.9 pu
2.2.3 Swell		30 cycles – 3 s	1.1 – 1.4 pu
2.2.4 Voltage imbalance		30 cycles - 3 s	2% – 15%
2.3 Temporary			
2.3.1 Interruption		$>$ 3 s – 1 min	$<$ 0.1 pu
2.3.2 Sag		$>$ 3 s – 1 min	0.1 – 0.9 pu
2.3.3 Swell		$>$ 3 s – 1 min	1.1 – 1.2 pu
2.3.4 Voltage imbalance		$>$ 3 s – 1 min	2% – 15%
3.0 Long duration RMS variation			
3.1 Interruption, sustained		$>$ 1 min	0.0 pu
3.2 Undervoltages		$>$ 1 min	0.8 – 0.9 pu
3.3 Overvoltages		$>$ 1 min	1.1–1.2 pu
3.4 Current overload		$>$ 1 min	
4.0 Imbalance			
4.1 Voltage		steady state	0.5 – 5%
4.2 Current		steady state	1.0 – 3.0%
5.0 Waveform distortion			
5.1 DC offset		steady state	0 – 0.1%
5.2 Harmonics	0 – 9 kHz	steady state	0 – 20%
5.3 Interharmonics	0 – 9 kHz	steady state	0 – 2%
5.3 Notching		steady state	
5.3 Noise	broadband	steady state	0 – 1%
6.0 Voltage fluctuations	$<$ 25 Hz	intermittent	0.1 – 7% 0.2 – 2 P_{st} [1]
7.0 Power frequency variations		$<$ 10 s	$\pm$0.10 Hz

Note: [1] - Flicker severity index P_{st} as defined in IEC 61000 – 4 – 15 : 2000 and IEEE Std. 1453^{TM}
The quantity *pu* refers to *per unit*, which is dimensionless. Nominal condition is considered to be 1.0 pu, corresponds to 100%. (pu = actual value / nominal value).

Transients

Transients, commonly referred to as surges, are signals of high magnitude with finite life. Transients are characterized by the following attributes; ***rate of rise***, ***peak amplitude***, ***duration***, ***rate of occurrence***, ***energy potential***, ***primary frequency*** and ***other spectral components*** [7]. Based on significance of each attribute, transients are characterized into two subclasses such as impulsive and oscillatory.

Impulsive transients

An impulsive transient is sudden and it transmit an excessive amount of power that the voltage/current or both go up or down from the nominal condition. These unidirectional spikes are characterized by peak value, rise time, decay time (or duration) and its spectral content. An example of impulsive transient would be electrostatic discharge or lightning.

Due to the high frequency components superimposed on the transient waveform, the shape can be changed quickly by circuit components, thus, exhibit significantly different characteristics when propagating through the power system. In addition, they damp quickly by resistive circuit elements. Sometimes these transients propagate a long distance through the utility lines, there's a tendency to damage electric equipment located far from the point that originated the impulsive transient [45].

A waveshape of an impulsive transient as illustrated in Figure 2.1(a) is described as $1.1/65\ \mu s$, 4000 V can be elaborated as an impulsive transient rises to 4000 V in 1.1 μs before the voltage decays to 50% of its peak value in 65 μs later [7, 46, 47]. The numbers of the particular waveshape denotes,

- 1.1 μs – rise time (from 10%–90% of peak) in microseconds
- 65 μs – duration of the signal from start to 50% peak in microseconds
- 4000 V – peak amplitude

Lightning strikes are a common cause for impulsive transients and can damage distribution transformers, consumer end-products along with surge protection devices including the arrestors. A lightning current transient (surge) having the same waveshape as described above is illustrated in Figure 2.1(b) [7, 46, 47].

Oscillatory transients

As illustrated by Figure 2.1(c), oscillatory transient of voltage or current, rapidly changes its polarity several times and eventually decay within a fundamental frequency cycle [7, 46]. An example would be capacitor bank energizing or a cable switching. The oscillations (also known as ringing) are characterized by magnitude, duration and spectral content. Based on the spectral content, oscillatory transients are categorized under three frequency subclasses such as low, medium and high.

- Low-frequency - Transients under 5 kHz falls into this subclass. Power electronic devices produce oscillatory transients of magnitude up to 0.1 pu due to commutation and operation of RLC snubber circuits which lasts for few cycles of their fundamental frequency with few repetitions per cycle. Oscillatory transients with fundamental frequency less than 300 Hz originates from transformer energizing, series capacitor switching and system resonance. Consequences can be tripping of variable speed-drives , relays or contactors.
- medium-frequency- A transient with spectral content within 5 kHz – 500 kHz with duration in microseconds. As a result of back-to-back capacitor energizing, power line cable switching and traveling waves resulting from lightning, medium-frequency oscillatory transients are produced. In addition, due to exciting of resonance circuits in power systems by impulsive transients, oscillatory transients can be produced as a secondary effect.
- High-frequency- These types of transients ($>$ 500 kHz) always generates due to switching on secondary systems, local ferro-resonance and lightning-induced ringing. As a result, low voltage power supplies can fail.

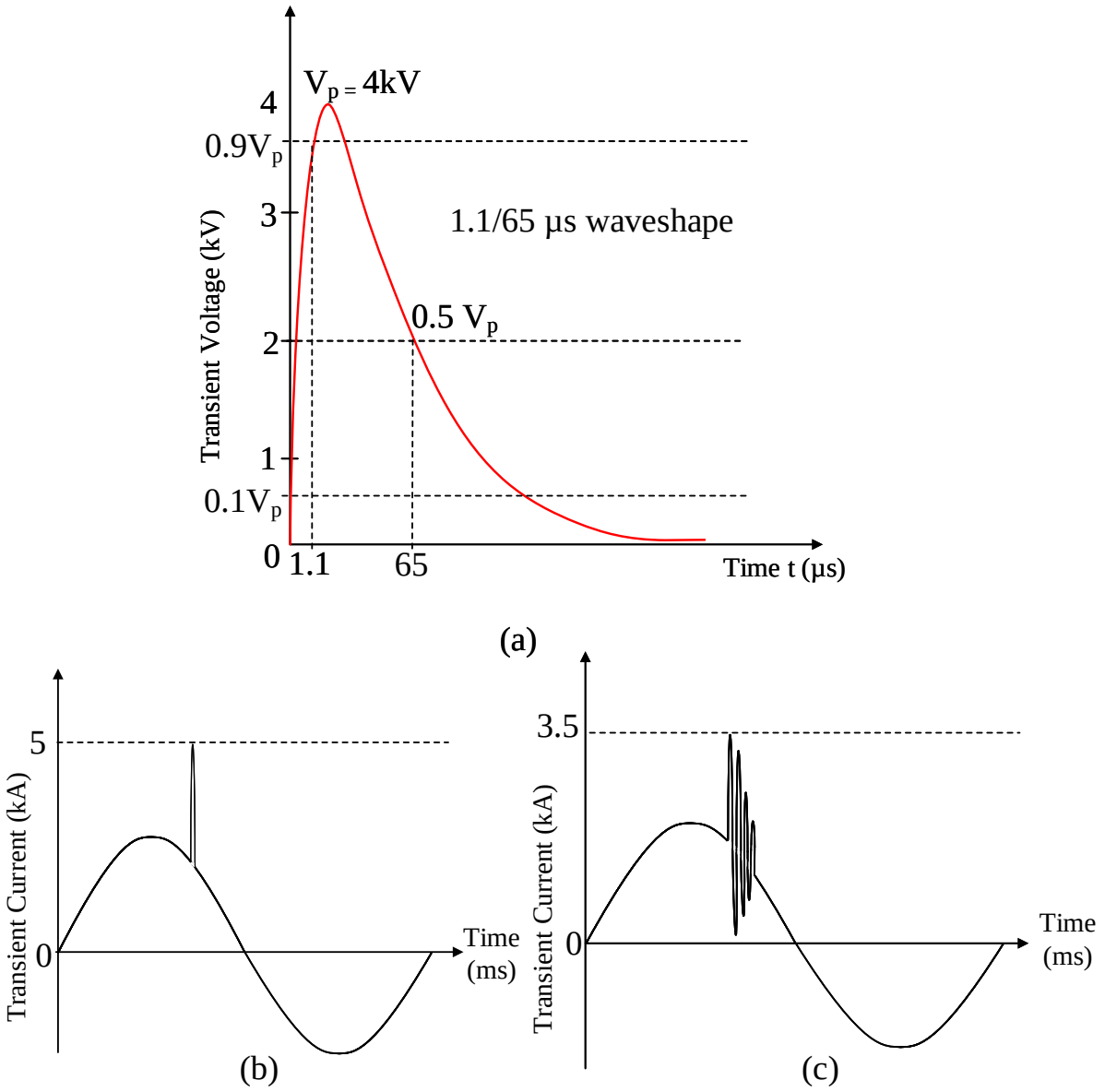


Figure 2.1: Transients; (a) Characteristic parameters of transients (b) Impulsive transient due to lightning (c) Oscillatory transient caused by back-to-back capacitor energizing

Classification of transients based on their mode is a very common practice. This classification is usually used in a three-phase system with separate neutral conductor and they are namely common and normal mode transients.

- common mode transients: these type of transients are measured between current-carrying conductor and the neutral (ground).
- normal mode transients: usually occur between two phase conductors

Short and Long Duration RMS Variation (Voltage Sags, Swells, Interruptions, Overvoltage and Undervoltages)

Among many power quality anomalies, short- and long-term RMS variation is a common occurrence. Continuous variation of loading and extension of the power grid to cater growing demand are the main

factors that contribute to above problem [1, 48]. In fact, over-voltages reduce the life span of electronics circuits and under-voltages reduce the device efficiency whereas, very low voltages create unexpected system shut-down. With proliferation of microprocessor-based equipment for industrial sites, residential homes, commercial and office environments, the equipment become more sensitive to voltage fluctuations. Increasing the clock frequency (from 4 MHz to 100 MHz) to speed up the circuit response, decreasing the supply voltages (to 3 VDC for microprocessor-based control circuit) and reduction in ride-through times of power supplies enhance the vulnerability of the equipment to voltage fluctuation [3, 6, 10].

RMS voltage variations are characterized by two parameters such as its depth (ΔU) or magnitude (U) and duration (ΔT) [7, 49, 50].

- **Voltage/current Dips (Sags), interruptions and undervoltages**:
  As illustrated in Figure 2.2, a *dip* is a sudden reduction of the voltage or current at a point in an electric network between 10% – 90% of nominal voltage for a duration between 0.5 cycles to 1 minute [7, 49].

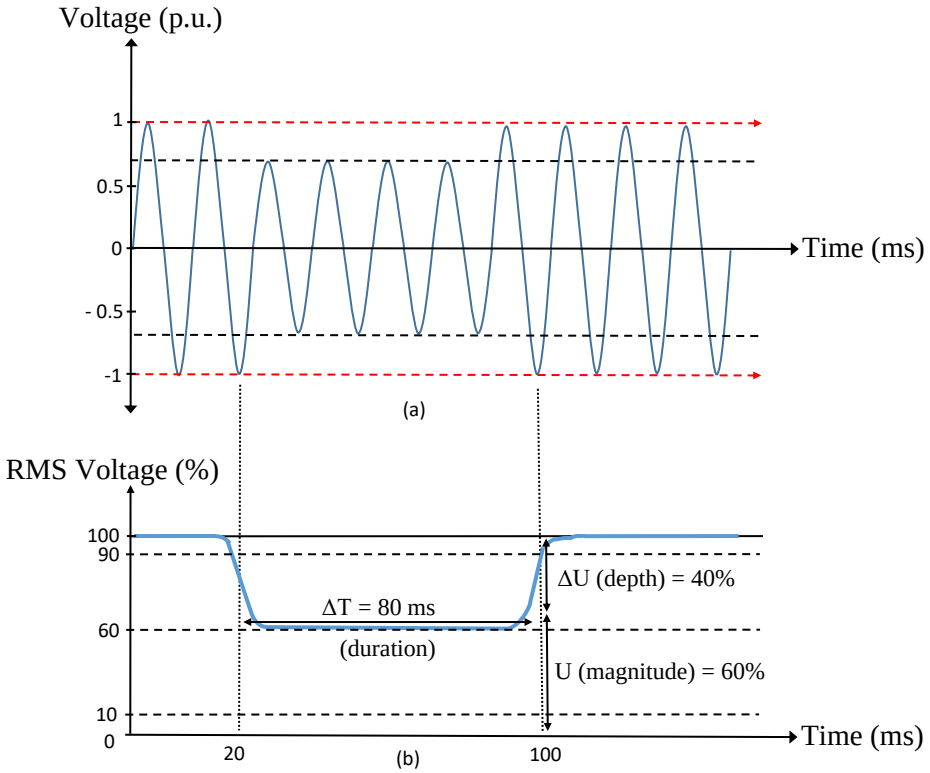


Figure 2.2: Characteristic parameters of a voltage dip in utility supply; (a) AC sinusoidal waveform (b) RMS waveform

Voltage dips usually occur due to faults in transmission (HV) or distribution (LV and MV) networks or on the installation. The duration of dips due to network faults usually depends on the operating time of the power conditioning devices and at the fault clearance, the isolation of faulty line by the operation of circuit breakers. Faults on the transmission and distribution lines are mainly due to human activity such as transportation accidents (planes or short distance air crafts crash into transmission lines), animal contacts (nesting habitats of large animals), falling or contacting of tree limbs or contamination of insulators.

A dip of magnitude in between 80 to 90% of nominal voltage which is longer than 1 minute is known as an *undervoltage*. They occur due to switching on of large inductive loads (asynchronous

motors, arc furnaces, welding machines or boilers) or switching off capacitor banks, faulty voltage regulation and overloaded circuits [2, 7, 51].

Short and long interruptions are a special type of dips of magnitude less than 10%, characterized by one parameter only: the duration. For short interruption the duration is less than a minute and for long interruption (sustained interruption) the duration can last over a one minute. These types of voltage interruption are permanent in nature and require manual restoration. The causes could be due to slow variation of loads connected to the network. Sustained interruption in urban areas are not very often as the network lines lying underground; in rural sites with overhead lines exposed to the environment and other causes of disturbances would often create interruption for longer duration. The most damage happens to the processor based equipment results in system shut down or garbled data [2, 7, 51].

- **Voltage Swells and overvoltages**:

  A sudden decrease in current flow will result in sudden increase in voltage across an inductive or capacitive source impedances that will be seen as a swell by the load. *Swells* are defined as RMS voltage or current increases to between 110% – 180% of nominal voltage for a duration between a half cycle to a 1 minute and is illustrated in Figure 2.3 [2, 7] .

  Voltage swells are less common than dips or interruptions but could be more destructive. Swells of magnitude between 110 and 120% of nominal voltage that will last for more than 1 minute are known as *overvoltages* [7]. Switching off of heavy loads, switching of capacitor banks, badly dimensioned power sources and unregulated distribution transformers (mainly during off-peak hours) cause voltage swells and overvoltages in the utility lines [2, 6, 7]. In addition, single line-to-ground faults in one phase will experience temporary high voltage by unfaulted phases (i.e. ungrounded or floating ground delta systems). An abrupt interruption of current due to sudden change of operation of huge inductive loads create swells as per formula: $V = Ldi/dt$.

  Figure 2.4 provides a visual representation of different types of RMS voltage variations defined by IEEE Std. 1159-2019 [6, 7, 51].

Consequences of voltage dips, interruptions and swells on electric equipment

Voltage dips, interruptions and swells in the power lines disturb many sensitive electric equipment connected to the network. Following paragraphs describe the main consequences of these phenomena on commonly used electrical equipment in industry and normal house holds [6, 52].

- **Computer equipment:**

  Voltage dips have been identified as the most common cause for power-rated computer system failure. During a sag, processor based equipment such as computers, measurement apparatus or data loggers may experience intermittent lock-ups, garbled data and data loss in volatile memory (i.e. RAM). These equipment are sensitive to voltage dips with depths greater than 10% of nominal voltage and are mostly affecting data processing centres, banks and telecommunication centres.

  In presence of voltage swells or over-voltages, power supply components can be fatally damaged requiring costly repairs or equipment replacement. In such situations, data loss or complete break down of systems can happen [3, 6, 10].

  ITIC (CBEMA) Curve - Revised 2000

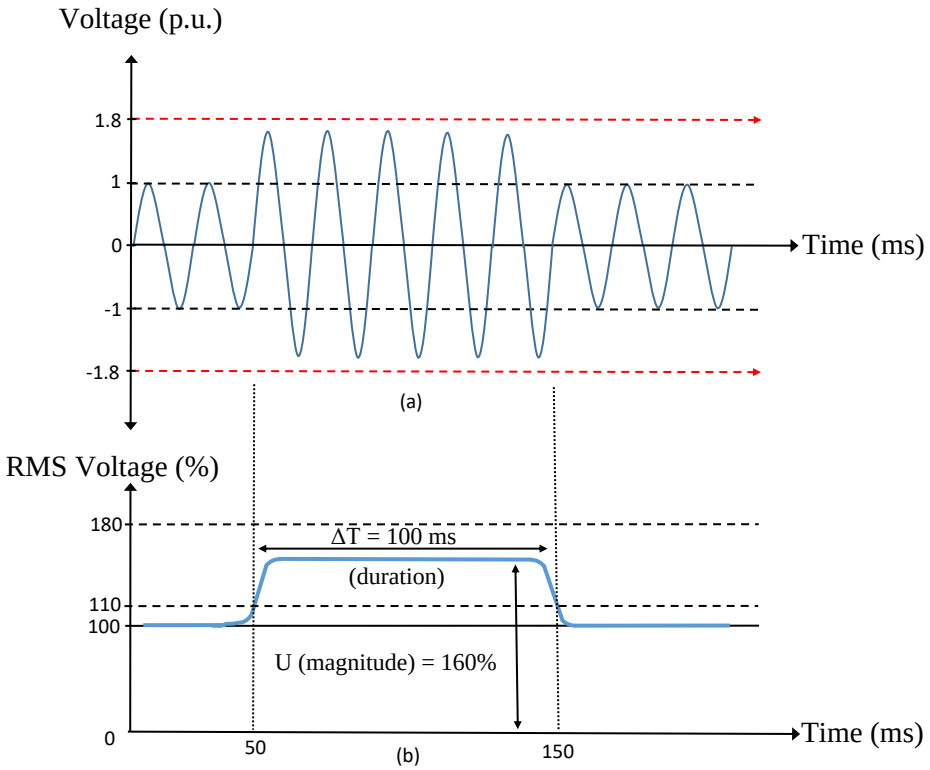


Figure 2.3: Characteristic parameters of a voltage swell in utility supply; (a) waveform of the AC supply (b) RMS waveform

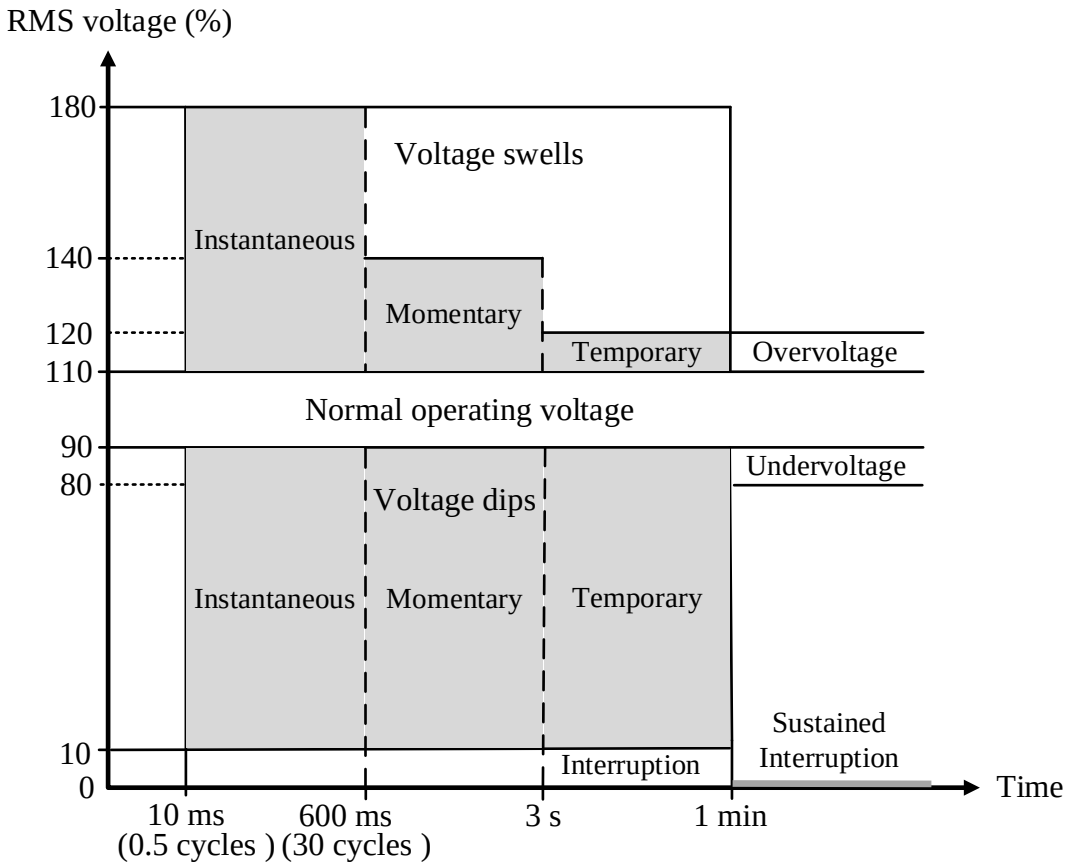


Figure 2.4: Definition of voltage disturbances according to IEEE Std. 1159-2019

A voltage-tolerance curve was presented in 1970s by Computer Business Equipment Manufacturers Association to test the immunity of the computer equipment for voltage disturbances known as CBEMA curve [46, 48, 51, 53]. Eventually, Information Technology Industry Council (ITIC) developed the original CBEMA curve to generate power quality variation data for IT equipment to understand the device immunity for such voltage disturbance and to determine how the power quality issues affect the device. Figure 2.5(a) illustrates voltage-tolerance curves according to CBEMA and ITIC recommendations.

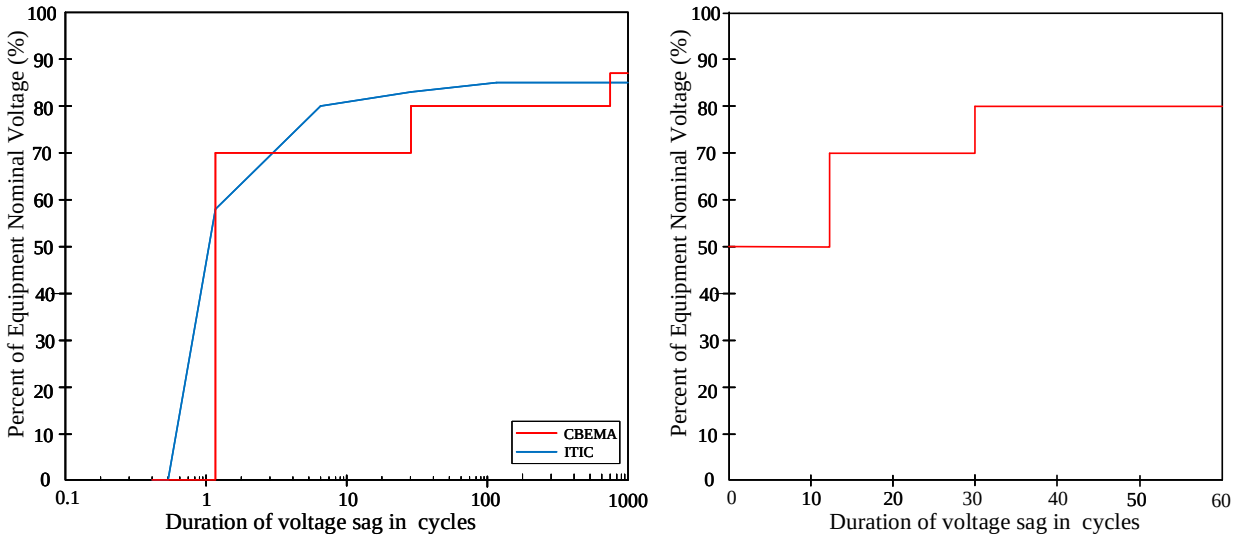


Figure 2.5: Voltage tolerance curves (a) CBEMA and ITIC (b) SEMI F47-0706

- **Lighting and safety systems:**
  Lighting devices such as incandescent lamps and fluorescent tubes derate prematurely due to voltage dips. Voltage dips lower than or equals to 50% with a duration of 50 ms will extinguish discharge lamps which require several minutes to be cooled-down before turn them on again. Voltage swells can cause flickering of lighting equipment, screens and safety systems which make false alarms or burn the electronics inside [6, 51]. Due to faults in the lighting and safety systems, hospitals, public or high-rise buildings and air ports are mostly affected.
- **Synchronous motors, asynchronous motors and adjustable speed drives (ASD):**
  Motors and adjustable speed drives play an important role in domestic and commercial application such as industrial process control, actuation (vehicles, fans, pumps, compressors, elevators, robots and machinery) and energy conservation of utility devices (such as fans and pumps by speed control when necessary).
  During a dip, the motor torque suddenly drops and slows down and will eventually stalls. When the voltage recovers, the motor tends to re-accelerate following an interruption and during the restarting may overheat the motor due to sudden increase of current [54].
  However, over-currents and voltage drops will result in electro-dynamic forces in the motor coils which may cause insulation failures and abnormal mechanical stress on the couplings. Thus lead to premature ageing and breakdown of motor as well as wear and fusion of contactors. Over-currents may cause tripping of protective devices of the installation causing process shut-down [6, 10, 51].

ASDs usually trip out in the presence of a dip of magnitude greater than 15%. Due to insufficient voltage supply, the motor slows down and the control circuit either malfunction or stop functioning which cause unwanted operation of the motor. The over-currents (swells) during the voltage recovery phase would recharge the drive filter capacitor and sometimes lead to phase imbalances too.

- **Actuators/ Robotics:**
  The control devices (contactors, circuit breakers, electromechanical or solid state relays) are sensitive to voltage dips of depth greater than 25% of the nominal voltage. These devices usually has a minimum voltage value (drop-out voltage); thus for lower voltages, the actuators malfunction or stop-working. Low voltages and interruptions reset electromechanical relays or contactors in motor starters and programmable logic controllers (PLC) affecting the process controllers (actuators or robotics), medical equipment, electronic ballast [3, 6, 10]. Consequences could include shut down of production lines, process delays, damaged/defected products, wastage and cost for repairing the damages before restarting the process [48, 51, 55, 56].
- **Semiconductor fabricating equipment:**
  Voltage sag is a main disturbance in semiconductor fabrication plants as semiconductor wafer production is very sensitive to voltage sags and could cost hundreds of thousands dollar worth loss per one event of sag [10, 46]. SEMI F47-0706 is standard that implemented in 2000 and revised in 2006 to define voltage sag immunity requirements for semiconductor fabrication facilities. This standard is applicable to single- two- and three phase manufacturing equipment used for semiconductor manufacturing. Figure 2.5(b) illustrates voltage-tolerance criteria for SEMI F47 standard [2, 46, 48, 57].

Voltage/current imbalance

Voltage/current imbalance is defined as the ratio of the magnitudes of negative-sequence components to the positive-sequence components of voltage or current waveform, expressed as a percentage as given by the following formula [2, 7].

$$voltage\ imbalance = \frac{|V_{\text{neg}}|}{|V_{\text{pos}}|} \times 100\%$$

Based on ANSI C84.1-2016, measuring instruments often use another definition for imbalance such as, the ratio of the maximum single phase deviation from the average voltage/current of the three phase supply to the average voltage/current of the three phase supply, expressed in percent as below [2, 7];

$$voltage\ imbalance = \frac{maximum\ deviation\ from\ average}{average\ voltage} \times 100\%$$

Typical voltage imbalances present in the three-phase lines are less that 5%, however current imbalances occur in a much higher rate. Common cause for current imbalance is one over-loaded phase on a three-phase system which has an occurrence rate of greater than 2%. Voltage imbalances can occur due to the following reasons [2, 58].

- blown fuses in one phase of a three-phase capacitor bank
- blown fuses on a three phase capacitor bank
- use of single phase line regulators - minor voltage imbalances

- single-phasing conditions - severe voltage imbalances of greater than 5%.

Waveform distortion

waveform distortion is a steady-state deviation from an ideal sine wave of the fundamental frequency characterized by the spectral content [7]. There are five main types of waveform distortion present in the network such as, (i) DC offset, (ii) harmonics, (iii) interharmonics, (iv) notching, (v) noise.

DC offset

the presence of DC voltage or current in an AC power system is called DC offset. As an effect of half-wave rectification or any geomagnetic disturbances can create a DC offset. Consequences could be transformer saturation and associated heating that can damage the insulation. Figure 2.6 illustrates a steady-state DC offset where its magnitude can vary between 0 to 0.1% of the nominal value [46].

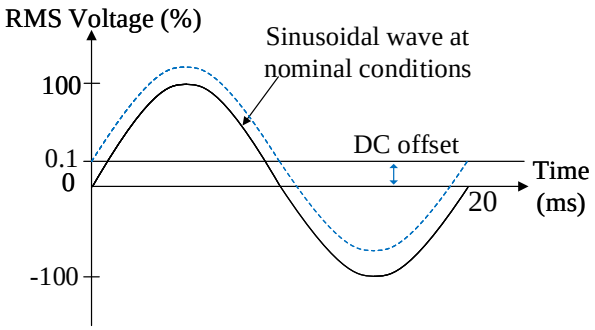


Figure 2.6: DC offset

Harmonics

Harmonics are mainly produced by non-linear loads by drawing a current of a different waveform than the supply voltage waveform. As a result high frequency current and voltage waveforms which are superimposed on the fundamental frequency (50 or 60 Hz), the pure sinusoid waveshape of the supply voltage or current will distort [7, 59, 60].

As defined by ANSI/IEEE Std. 519-1992 (IEEE recommended practices and requirements for harmonic control in electrical power systems), harmonics are steady-state periodic functions where the magnitude and phase angle can be computed using the Fourier analysis as below, [61–64];

$$y(t) = Y_{(0)} + \sum_{h=1}^{\infty} Y_h \sqrt{2} \sin(2\pi h f + \varphi_h)$$

where,

Y_0 - value of the DC component, where applicable,

h - an integer that represent the harmonic order ($h > 1$),

Y_h - RMS value of the harmonic order h,

f - fundamental frequency,

φ_h -initial offset of the harmonic component

Positive and negative half cycles of line voltage and current waveforms are usually identical; therefore only the odd harmonics are significant in the harmonic spectrum [62, 65].

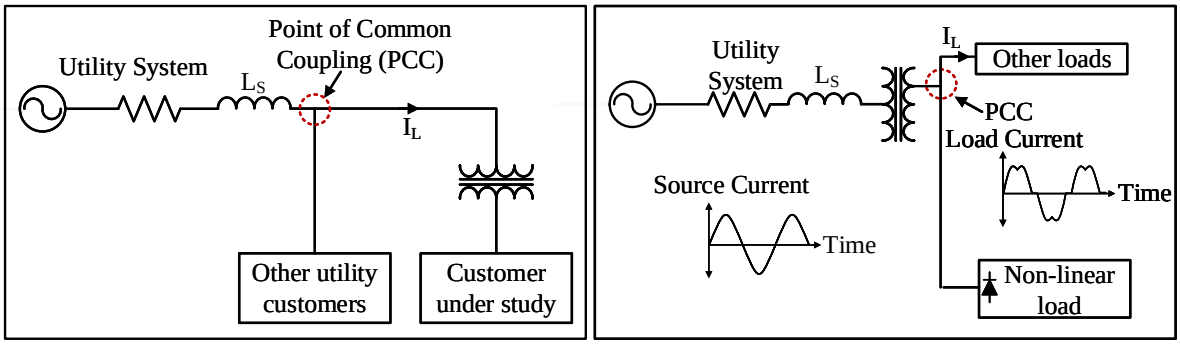
Total harmonic distortion (THD) is the common method to measure distortion of a power system waveform and is calculated as follows [6, 62];

$$THD = \sqrt{\sum_{h=2}^{\infty} \left(\frac{Y_h}{Y_1}\right)^2} = \frac{\sqrt{Y_2^2 + Y_3^2 + Y_4^2 + ... + Y_h^2}}{Y_1}$$

Total demand distortion (TDD) or root-sum-square (RSS) is a measure of harmonic currents between an electric power end-user and a power source, which indicates the impact of harmonic distortion in the system. The harmonic values are measured based on a point of common coupling (PCC), which is a common point that each end-user receives power from the power source as illustrated in Figure 2.7 [66, 67].

$$TDD = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + ... + I_h^2}}{I_L}$$

$I_1, I_2, I_3, ...I_h$ are harmonic currents; I_1 refers to the current of fundamental frequency whereas $h = 2, 3, 4, ...$ refer to harmonic frequencies. I_L is defined as the maximum demand load current (fundamental frequency component) at PCC.



(a) (b)

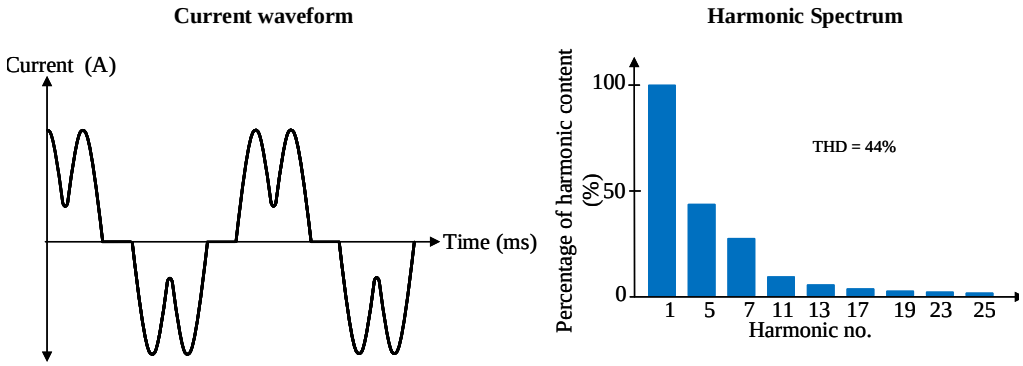
Figure 2.7: Point of Common Coupling (PCC) (a) basic microgrid with PCC (b) harmonic distortion at PCC (sourced from [64, 67])

Unlike other power quality issues such as surges or voltage variations which are occasionally appear in the power line and decay with time, harmonics are periodic, thus, the distortions appear repeatedly in the waveform unless they are filtered using filtering circuits or power factor correction method [6, 60, 62]. Harmonics are easily generated by commonly used electric equipment which can be categorized in to two general categories such as saturable devices and power electronic devices [62, 68]. Following are a list of common harmonic generators,

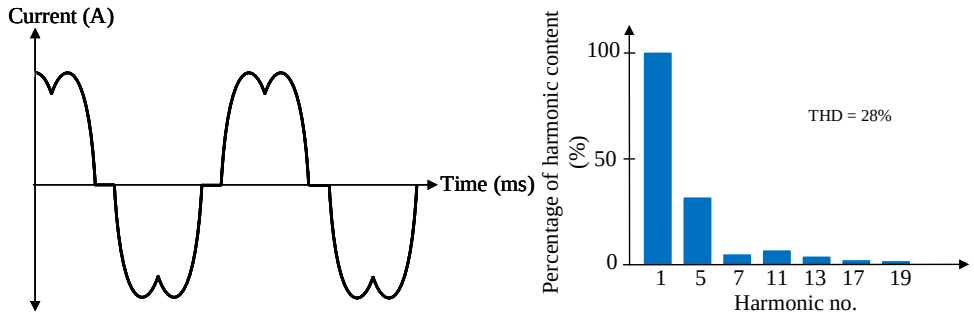
- Industrial loads : Electric equipment using power electronic components such as variable speed drives, rectifiers (diodes or thyristor based), battery chargers, switch mode power supplies, Inverters
- Loads using electric arcs: arc furnaces, welding machines, fluorescent lamps
- Staring of motors that use electronic starters and power transformer energizing (transformer saturation and inrush)

- Domestic loads: Electric equipment with power inverters or switch mode power supplies such as television power supply, microwave ovens, computers, printers, photocopiers, induction cookers, dimmer switches, fluorescent lamps.

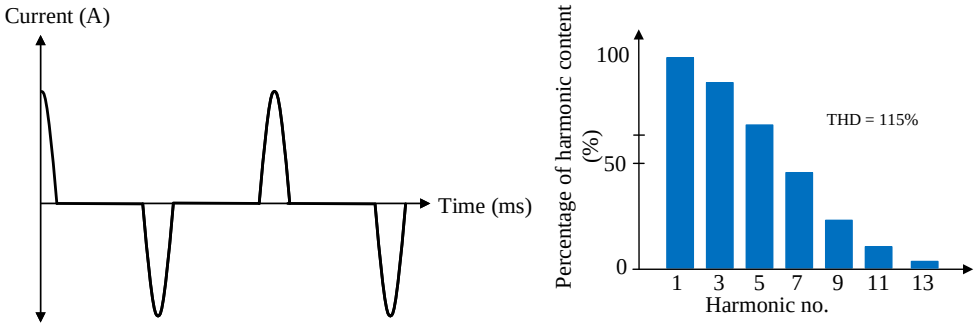
Saturable devices generate harmonics due to iron core saturation. For economic reasons transformers and motors are designed to operate just above the knee of the saturation curve, the magnetizing current rich in third harmonic where the third harmonic current is approximately 30% of the fundamental. Fluorescent lamps with magnetic ballasts generate harmonics due to the arc and the ballast where the third harmonic is dominant with a 3^{rd} harmonic current of $15-30\%$ of the fundamental [62]. Figure 2.8 shows characteristic waveforms generated by different harmonic generators.



(a) Adjustable speed drive



(b) Rectifier/ battery charger



(c) Data processors, electronic ballasts and other types of non-linear loads

Figure 2.8: Characteristics of different harmonic generators: data extracted from [6]

Power electronic devices employing non-linear circuit components such as switch mode power supplies (SMPS), inverters, PWM converters and electronic lighting ballasts draw current from the power line during portions of the applied voltage waveform. Therefore, the typical current/ voltage waveform exhibits a distorted wave shape as in Figure. 2.8(c). Due to this non-sinusoidal power consumption of the non-linear loads, the supply line voltage and current waveforms get distorted, thus, the other loads connect at the PCC receives a degraded voltage/ current what started out as a sinusoidal waveform as illustrated in Figure 2.7(b). This distorted power supply causes significant damages to electric equipment as discussed later in this section.

Out of power electronic loads, switch mode power supplies are widely used, thus, contribute most to the harmonic generation at the supply line. Following paragraphs briefly describe the ways of harmonic generation from the SMPSs.

Figure 2.9 indicates the logical arrangement of a typical switching power supply showing its input rectifier stage, followed by the PWM switching stage. As depicted in Figure 2.9(b), despite the case of having a input sinusoidal AC source of 50 Hz, the current drawn by the rectifier stage makes it non-sinusoidal. With almost all modern appliances are internally DC operated, this non-linear input current causes the input AC source voltage distorted by harmonic components (typically with a flattened top sine wave [69, 70].

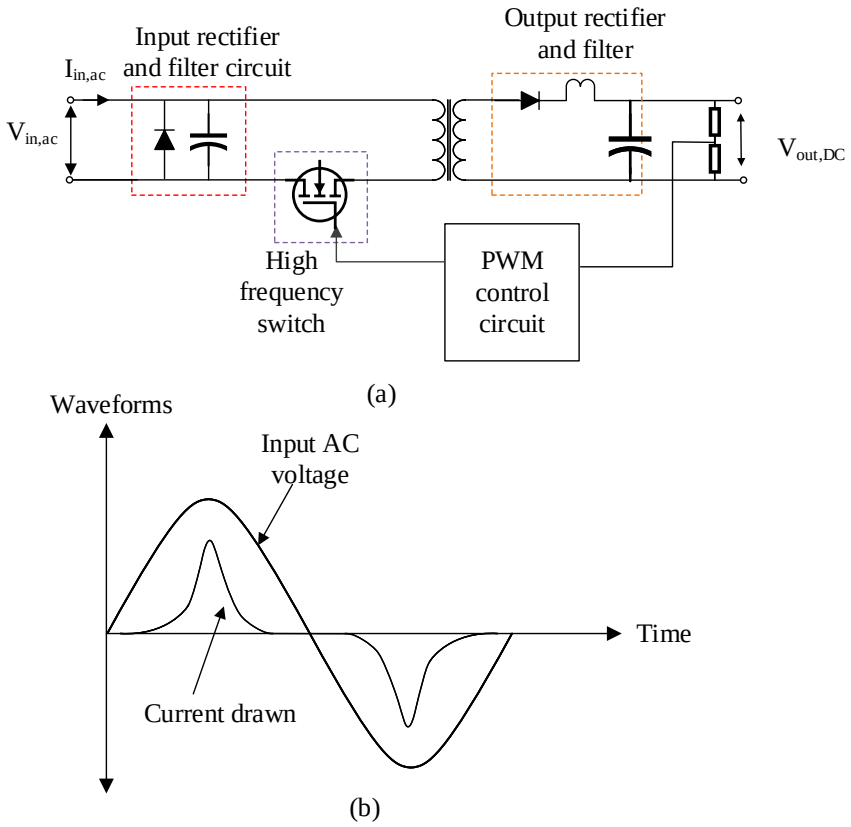


Figure 2.9: Simplified digram of a switch mode power supply (a) basic circuit (b) current and voltage waveform across A-A

The large inductor used to limit the DC current ripple, is incapable of change its inductor current suddenly, thus, has a high rise and fall time as shown in Figure (b). If Φ is the angle of rise and fall time

(t_r), and the duty cycle is T, $\Phi = 2\pi t_r/T$. Fourier transforms the load current, I_d obtains,

$$i = I_d[c_1 sin(\omega t) + c_3 sin(\omega t) + c_5 sin(\omega t) + ...] \tag{2.1}$$

According to (2.1), the rectifier current contains odd harmonics [69].

Figure 2.10 shows a typical single-phase inverter circuit with MOSFETs as the switching element. These switching elements that are being used in SMPS such as MOSFETS, SCRs, IGBTs and power BJTs are highly non-linear. For the half-bridge inverter shown in Figure 2.10 has a duty cycle of 50% where Q_1 and Q_2 switch on for $T/2$ alternatively. The Fourier transform of the voltage across the load, V_o is given by,

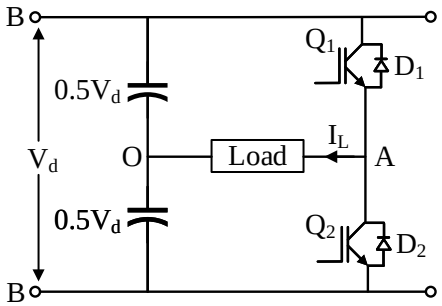


Figure 2.10: MOSFET based basic single-phase inverter

$$V_o = \frac{E}{2} + \frac{2E}{\pi} sin(\omega t) + \frac{2E}{3\pi} sin(3\omega t) + ...] \tag{2.2}$$

According to (2.2) we obtain that output load voltage include $3^{rd}, 5^{th}, 7^{th}$ and other higher order harmonic components superimposed on the fundamental component and distort the output waveform as shown in Figure 2.9 (b) [69, 71]. This distorted waveform is fed into the mains supply from the output side of the switch mode power supply and distribute through the network unless the high frequency components are filtered using additional circuits. Reliable SMPS units usually include such filter circuits which makes them more expensive.

Harmonic Limits

Tables 2.2 and 2.3 indicate the limits of total harmonic distortion for voltage and current waveforms of the power system as per IEEE Std. 519 [64]. The harmonic limits specify the maximum amount of harmonic current/voltage that the user can inject into the utility supply.

Table 2.2: IEEE Std. 519-1992 Harmonic Voltage Limits as given in [7]

Bus voltage at PCC	**Individual Voltage Distortion (%)**	**Total Voltage Distortion, THD (%)**
69 kV and below	3.0	5.0
69.001 kV through 161 kV	1.5	2.5
161.001 kV and above	1.0	1.5
Note: High-voltage systems can have up to 2.0% THD where the cause is an HVDC (High Voltage Direct Current) terminal that will attenuate by the time it is tapped for a user.		

Table 2.3: IEEE Std 519-1992- Harmonic Current Limits for General Distribution Systems (120 V through 69 kV)

Maximum Harmonic Current Distortion in Percent of I_L						
Individual Harmonic Order (Odd Harmonics)						
I_{SC}/I_L	< 11	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	TDD %
< 20[2]	4.0	2.0	1.5	0.6	0.3	5.0
$20 < 50$	7.0	3.5	2.5	1.0	0.5	8.0
$50 < 100$	10.0	4.5	4.0	1.5	0.7	12.0
$100 < 1000$	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonic limits above.						
Current distortions that result in a DC offset, e.g. half-wave converters, are not allowed.						
[1] All power generation equipment are limited to these values of current distortion, regardless of actual I_{SC}/I_L.						
Where, I_{SC} - maximum short-circuit current at PCC. I_L - maximum demand load current (fundamental frequency component) at PCC. TDD - Total demand distortion, harmonic current distortion in % of maximum demand load current (15 or 30 min demand).						

Consequences of harmonics

System harmonics lead to increasing of peak and RMS values of the waveform and changes to the frequency spectrum of voltage and current [6, 60]. The following paragraphs briefly describe the effects of harmonics on frequently used electric equipment.

- **Protective devices:**
  Harmonics influence mis-calculation of the RMS value of the current/voltage using the peak value of the waveform. Thus unwanted operation of protective devices can happen even when the operation is normal. Thermal control devices are frequently affected by this phenomena [6].
  Harmonics cause unwanted tripping of circuit breakers due to exceeding voltage peak values which leads to unwanted operation of protected equipment. Loss of productivity, energy loss, defected products, accelerated ageing of equipment are some of the bad effects.
- **Power factor correction capacitors:**
  Presence of harmonics in the utility power line generate harmful effects to the power factor correction capacitors. As the capacitive reactance is inversely proportional to the frequency (as per $X_c = 1/(2\pi fC)$), at higher order harmonics, the capacitive reactance decreases, drawing a high current supplied by the distorted voltage. This over-current can damage the capacitor bank which require costly repairs or replacement [59, 60].
  Another important effect is resonance between the capacitance of the power factor correction capacitor and the equivalent network inductance. If a series resonant circuit is created by the resonance harmonics, a current amplification will occur and damage the network components. And if a parallel resonant circuit is supplied by the resonance harmonics, an over-voltage will be created [6, 60].
- **Motors and transformers:**
  Harmonics affect motors in three different ways [60, 72]:
  - Reduce motor efficiency: harmonics in the power line increase eddy current and hysteresis losses while high content of harmonics lowers the power factor causing raised power bills

  - Reduce the life span of the motor (windings, bearings, lubricants): due to overheating of the motor as a result of increasing losses may damage winding insulations and lose the lubricity of bearing grease. Also, harmonics can trigger bearing currents causing arcs inside the bearings that increases the frictional losses.
  - Pulse torque: As the positive-sequence harmonics ($7^{th}, 13^{th}, 19^{th}, ...$) help the motor turn in the direction of the fundamental frequency by increasing the torque, the negative-sequence harmonics ($5^{th}, 11^{th}, 17^{th}, ...$) try to turn the motor into opposite direction (braking) which is known as pulse torque. These torque pulsation cause mechanical stress (shaft torsion), vibrations and acoustic noise.

  Transformers on the other hand have similar effects due to harmonic content in the supply lines which cause iron and ohmic losses that reduce the transformer efficiency. Overheating of the transformer may cause damages to the windings which could be very dangerous depending on the transformer application (i.e. transmission or distribution transformers). Further mechanical vibrations and noise could be disturbing and lead to noise pollution.

- **Power and telecommunication cables:**
  In the presents of third harmonic (and multiples of 3), current flowing through the phase conductors add in the neutral line creating the neutral overloaded and over heated. Thus the power cables generate dielectric and ohmic losses resulting degrading and economic loss. The above phenomena create over-current in the telecommunication lines too.
- **Power electronics and utility devices:**
  Due to harmonics, the operation of low power consuming utility devices such as remote control, hi-fi systems, low-voltage switch boards, television and computer screens get disturbed and power electronic systems using thyristors, diodes and other types of semiconductor switches subject to commutation and synchronization problems.

Interharmonics

High frequency components of voltage or current that are not integer multiples of the fundamental frequency (50 or 60 Hz) are called interharmonics [2, 6, 7]. They can locate between harmonics and appear as a wide-band spectrum.

Interharmonics are generated mainly due to operation of devices whose control is not synchronizes with the system frequency. Few examples of such devices are pulse-width modulated inverters, static frequency converters, cyclo-converters, induction motors and arcing devices. Power line carrier signals and the remote control frequencies used by the power distributor can be considered as interharmonics.

Effects of interharmonics are visual flicker in monitors (Cathode ray tubes), interference with power-line carrier signals and low frequency torsional oscillations in motors [6, 7].

Notching

Notching is a periodic voltage disturbance that occur during commutation of current between phases due to normal operation of power electronic devices [7]. Notching is a steady-state phenomena which involves with high frequency components, thus similar to harmonic distortion. As the higher-order frequency component that occur with notching are quite higher than system harmonics, such frequencies cannot be measured using typical harmonic measurement instruments [2].

Notching occurs when current commutates from one phase to another, during which a momentary short circuit may occur between two phases. The main source for notching is three phase converters that produce continuous DC current. Arcing of power conductors also creates notching and communication equipment can be affected by that. Voltage notching can cause frequency and timing errors on power electronic circuits. Figure 2.11 illustrates a voltage notching situation [7].

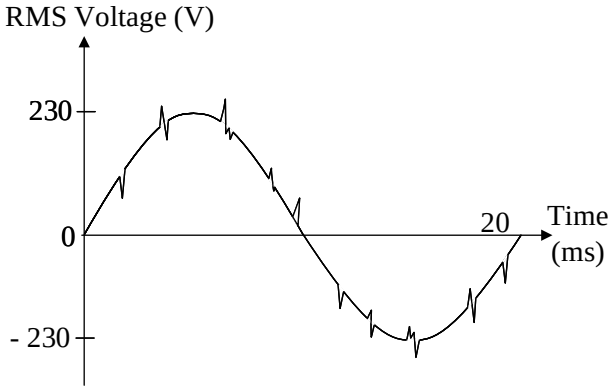


Figure 2.11: Voltage notching in the main supply line due to converter operation

Noise

Noise is unwanted electrical signals with broadband spectral content lower than 200 kHz, superimposed on the power system voltage or current in phase conductors, neutral conductor or signal lines. Power line noise could be due to improper grounding, operation of switch-mode power supplies, arcing devices, control circuits, power electronic equipment and loads with solid-state rectifiers [2, 7]. The frequency and magnitude levels of noise depends on its source. The typical magnitude of noise is less than 1% of the system voltage. Microcomputers and programmable controllers often see noise as a problem.

Voltage fluctuations

As illustrated in Figure 2.11 voltage fluctuations are defined as systematic or random variation of voltage envelop within a specified range of voltage magnitude 0.95 pu to 1.05 pu (or $95\% - 105\%$ of nominal value) [7, 73]. A varying current drawn by the system will result in dropping the system voltage. When the loads exhibit rapid variations of operation continually, voltage fluctuations occur [73]. Such variation is detectable by the human eye as flicker of lamp illumination [2,7,73]. Even very low magnitude voltage fluctuation as small as 0.25% of frequencies in the range of 6 to 8 Hz is able to produce visual effect of lamp flicker which annoys the human eye [7, 73].

Other than flicker of lamps, voltage fluctuations cause tripping of relays, interfere with communication equipment and in worst case, prevent some other loads to be switched on due to insufficient supply voltage. Stall of induction motors can be another consequence of voltage variations.

Voltage fluctuations are generally caused by sudden changes of real and reactive power drawn by certain types of loads [73]. Arc furnaces, arc welders, equipment with motor starts (air conditioners, fans), motor drives with cyclic operation (mine hoists, rolling mills) and equipment with rapid motor speed

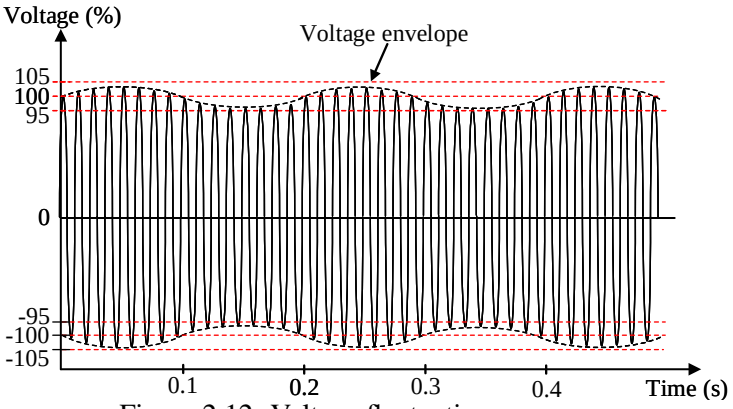


Figure 2.12: Voltage fluctuation

changes (wood chippers, car shredders) cause voltage fluctuations in the transmission and distribution lines.

Power Frequency Variation

Deviation of system frequency from its specified nominal value (50 or 60 Hz) are known as power frequency variations. Main cause is poor speed regulation of the generator at the generation power-plant. Due to faults on the bulk power transmission system, such as disconnecting of bulk loads or large sources of generation going off-line cause huge deviation to the power frequency.

Rotating machines and processes that the timing is based on power frequency would be affected by deviation of frequency in the supply lines but such issues are significantly minimized by implementing modern interconnected power systems.

2.1.2 Electromagnetic compatibility

The above section describes the existing power quality issues in the utility line and how they affect on consumer electronics. Electromagnetic compatibility is the ability of an electrical equipment to function in a satisfactory level in its electromagnetic environment without disturbing it. The aim of electromagnetic compatibility is that to monitor the immunity of an electrical equipment and to control the level of emissions of electromagnetic disturbances by individual equipment to ensure that the total emissions in an environment does not exceed an intolerable value [46, 73]. Thus, a set of standards have been declared by different standard-making authorities that guide the product manufacturers and industrial and domestic customers for manufacturing and consumption of electrical equipment with increased performance while maintaining a safe electrical system. Table 2.4 shows related standards for different power quality anomalies in the utility line [46, 61, 73].

Standardization Bodies

On behalf of consumers and manufacturer of electric goods, it is important that electric equipment comply with a set of standards and regulatory approach for product design, emissions, safety and immunity for system compatibility. There are several organizations that put-up such standards and influence system compatibility which have been briefly described in Table 2.5 [46].

Table 2.4: Standards related to system compatibility

Power Quality Category	Standard or reference document
Immunity	
Voltage sags and interruptions (cycles to second)	ITIC curve; SEMI F47 Curve; IEC 61000-4-11, 61000-4-14 and 61000-4-34
Low RMS variation (seconds to minute)	ITIC curve, SEMI F47 Curve, ANSI/IEEE C84.1
Steady-state variation (seconds to minute)	ANSI/IEEE C84.1
Voltage swells	ITIC curve
Voltage imbalance	NEMA MG-1, ANSI/IEEE C84.1, IEC 61000-4-27
Voltage distortion	IEEE 519
Common mode noise	IEEE P-1100
Normal mode noise	IEEE P-1100
Switching transients	IEEE C62.45, IEC 61000-4-4 and 61000-4-5
RFI	IEC 61000-4-3, 61000-4-6
Frequency variation	IEC 61000-4-28
Emissions	
Current distortion	IEEE 519, IEC 61000-3-2 and 61000-3-4
Voltage fluctuations	IEEE 1453, IEEE 141; IEC 61000-3-3, 61000-3-7 and 61000-3-11, AS 4376, AS 4377
Low-frequency magnetic field	IEC 61000-2-7
Survivability	
Lightning transients	UL 1449, IEEE C62.45, IEC 61000-4-5
Overvoltage	ANSI/IEEE C84.1
All types	
Event quantification	IEEE 1159, IEC 61000-4-30

Table 2.5: Standardization organizations

Organization	Comments
ANSI (American National Standard Institute)	Set-up standards
IEEE (Institute of Electrical and Electronic Engineers)	Predominately setting of electrical standards
IEC (International Electrotechnical Commission)	Standardized nomenclature and ratings of electrical apparatus and machinery to common use and provide rules, guidelines and characteristics
NEMA (National Electric Equipment Manufacturers Association)	Publish standards, application guides, white papers and technical papers for electric utilities such as enclosures, motors, magnet wire, AC plugs
UL (Underwriters Laboratories)	Put-up standards (i.e. fire safety and industrial control equipment, electrical and electronic products)
FCC (Federal Communications Commission)	Mandatory compliance for radiated-emissions related equipment and regulate interstate communications by radio, TV, wire, satellite and cable
CSA (Canadian Standard Association)	Enforces standards in multiple industries (i.e. electrical, mechanical, industrial, public safety, construction)
ULC (Underwriters Laboratory of Canada)	Safety testing, certification and inspection organization which makes standards for product safety
CENELEC (European Committee for Electrotechnical Standardization)	Create standards and specifications in the area of electrical engineering
ETSI (European Telecommunication Standards Institute)	Produce globally acceptable standards for information and communication technologies

2.1.3 Solutions for improving power quality

Poor power quality disturbs and degrades the steadiness of the supply voltage, smoothness of its sinusoidal shape and changes its frequency which lead to change in performance of consumer electronics and even destruction of equipment and dependent processes. Therefore while improving power quality

of the supply lines there are several mitigation techniques that can be adapted to control the generation of PQ anomalies in utility lines, prevent developing the electromagnetic disturbances to intolerable levels and distributing them through the network [6, 46, 52]. The solutions can either be facility level by implementing proper network installation up to the specified standards or equipment level specially when connecting polluted loads (possible disturbance generators). Power quality monitoring is vital at this point to learn various generators of disturbances, their propagation path and other loads that can be sensitive to the disturbance [6, 57].

Table 2.6 present a summary of consequences and mitigation techniques of several power quality issues in the supply lines.

Table 2.6: Mitigation solutions of power quality issues

Type of Disturbance	**Consequences**	**Mitigation Techniques** (special equipment and modifications)
Transient over-voltages	locking of drives, unwanted tripping, destruction of switchgear, fire, operating losses	surge-protective devices, surge arrestor, surge diverter, controlled switching, pre-installation resistor, line choke, static automatic compensator
Voltage sags and under-voltages	process shutdown/ malfunction, data loss, opening of contactors, locking of drives, stalling or slow down of motors, Extinguishing of discharge lamps	UPS, real time reactive compensator, dynamic voltage restorers, RMS voltage regulators, soft starters, increase the short circuit power, modify the discrimination of protective devices
Interruptions		UPS, mechanical source transfer, zero-time set, shunt circuit breaker, remote management
Voltage fluctuations	lamp flicker, tripping of relays, malfunction of communication equipment, stall of induction motors	electromechanical reactive power compensator, real-time reactive compensator, power conditioners, tap changer
Harmonics	overloads, unwanted tripping, improper ageing, diminish energy efficiency and productivity	anti-harmonic-choke, passive or active filters, hybrid filters, line choke, Increase the short-circuit power, de-rate the equipment
Inter-harmonics	flicker and interruption of metering signals	series reactance
Noise	malfunction of programmable logic controllers and degraded performance of micro-computers	isolation transformers, line conditioners and noise filters
Voltage imbalance	inverse motor torque and overheating of asynchronous machines	balance the load, shunt electronic compensator, electronic voltage regulator, increase the short-circuit power

2.2 RMS AC voltage regulators

RMS Voltage variation is one of the most common power quality anomaly that can be harmful to equipment safety and the productivity of industrial plants. In a practical scenario although many precautions and measures have been taken, voltage fluctuations and RMS variations cannot be completely removed from the supply line; but the severity of the occurrence can be reduced [3].

In order to reduce the RMS variations in the transmission and distribution lines, utility companies have taken several measures including the addition of regulating devices to the transmission network such as static synchronous compensator (STATCOM), dynamic voltage restorers (DVR) or fault current controllers (FCC). These devices cannot be controlled by the end-users and are not responsible for "within-facility" issues. RMS AC voltage regulators, an important family of power conditioners, can be installed by any electricity end-user are intended to reduce line-voltage fluctuations and RMS variations of AC mains at customer premises [10, 44, 55]. There are four main types of AC voltage regulators available in the market as follows [19, 20, 35, 36, 74].

- servo-based voltage regulators
- ferro-resonant regulators
- transformer tap changers
- solid state regulators

2.2.1 Servo-based voltage regulators

A simple construction of voltage regulator using an auto-transformer or a transformer, with an in-built servo-mechanism is a low cost solution for protecting sensitive electronics in industrial plants from olden times [11,32]. The primary objective of this type of voltage regulator is that changing the transformer effective turns ratio (primary to secondary number of turn counts, N_p/N_s); where different techniques were used in achieving this [11, 12, 31]. Following are few of the different servo-based regulator approaches.

Figure 2.13 shows a basic design of a servo-based regulator to achieve a boost and a buck type correction to the output. An auto-transformer's turns ratio is continuously changed by the servo mechanism to deliver a constant AC voltage output by moving a wiper along the auto-transformer winding according to a feedback signal. The feedback control block is capable of measuring the change of input or output voltage with reference to a predefined value and delivers an error signal to control the servo mechanism to achieve necessary regulation. Required electrical isolation can be introduced for the regulator by utilizing separate windings for the primary and secondary side [12, 31]. PS-10 smart power station developed by Thor Technologies, Perth, Australia is a commercially available servo-based voltage regulator and its functional block diagram is illustrated in Figure 2.14

Figure 2.15 illustrates an improved version of a servo-based voltage regulator utilizing a buck-boost transformer. The secondary winding of a two-winding buck-boost transformer is placed in the input/output load path in order to achieve the boost (or buck) mode regulation by adding (or subtracting) the induced secondary voltage to (from) the input line voltage. The primary winding of the buck-boost transformer is extended by connecting in series to a variable auto-transformer from which the buck-boost transformer is being powered. The turns ratio of the auto-transformer is adjusted by a servo-mechanism according to the feedback signal from the input/output sensing unit, thus maintains a constant output voltage [11]. Due to the buck-boost transformer arrangement, the servo mechanism only produce the

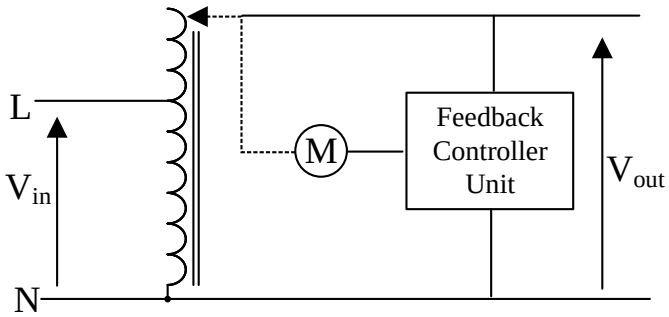
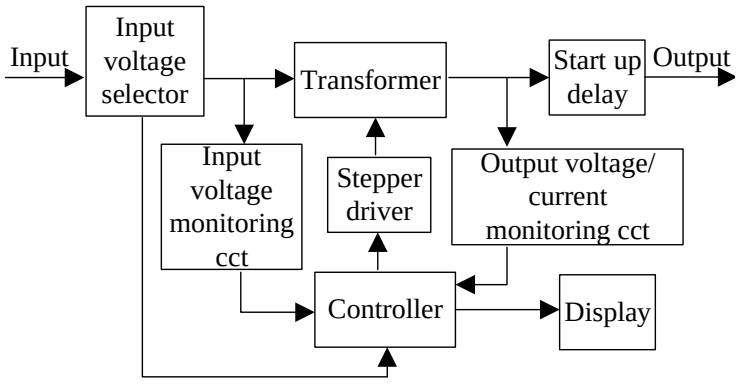


Figure 2.13: Basic diagram of a servo driven variac

error voltage corresponding to the difference between the input and the output voltage which requires less mechanical work with compared to the previously described method.

Figure 2.16 illustrates another configuration of changing the transformer turns ratio by altering the physical orientation of the transformer windings relative to each other using a servo mechanism, thus named as servo induction voltage regulator (magnetic induction voltage regulator) [35,75]. As illustrated in Figure. 2.16(a), the transformer windings are positioned cylindrically around a fixed axis, where the primary winding, the outer most coil is fixed stationary and the secondary is placed inside the primary, supported by bearings to rotate back and forth in an arc, less than 360°. A feedback controller measures the input and output voltages and produces an error signal. The servo motor rotates the secondary coil at an angle proportional to this error signal and change the relative position of the two windings, thus induce a secondary voltage to achieve the desired output voltage.



(a)

(b) (c)

Figure 2.14: PS-10 smart power station; (a) functional block diagram (b) a snapshot of the actual product (c) variable autotransformer with carbon brushes

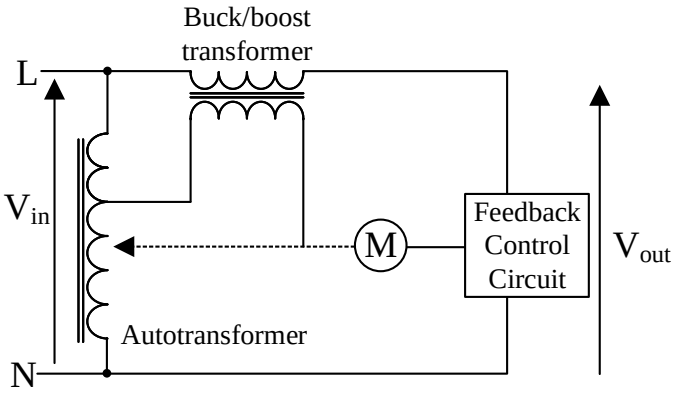


Figure 2.15: Basic servo based voltage regulator with a buck-boost transformer

An alternative method to orient the transformer windings to have a relative motion between each other is proposed in reference [13] as illustrated in Figure. 2.16(b) and (c). This technique employs an autotransformer with a stationary (primary) and a moving coil (secondary), which is actuated by a servo motor. These magnetic induction voltage regulators were popular in early days to control the voltage of electrical networks which has been then replaced by tap changing transformers. Nowadays, the usage has been limited to electrical laboratories and workshops using arc welding machines. Major drawback of this device is high open circuit current due to the air gap and lower efficiency in comparison to tap changing transformers [35].

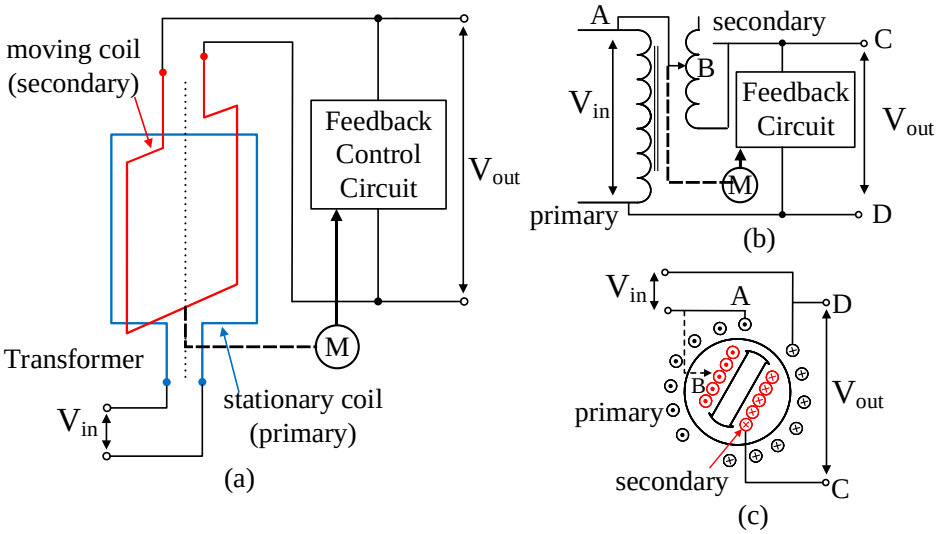


Figure 2.16: Servo induction voltage regulator (a) simplified diagram (b) single phase winding diagram (c) cross sectional view

In summary, these electromechanical voltage regulators are very old yet still in use due to their reliability, accuracy and low cost. But the mechanical structure comprising a motor, a servo mechanism and the gear wheels to drive the rotation not only makes the system bulky and heavy but it is slow to respond and may not be fast enough for electronic loads. In addition, the mechanical drive components such as brushes, contactors or relays require regular maintenance or replacement [11, 12].

2.2.2 Ferro-resonant regulators / Constant voltage transformers (CVT)

Ferro-resonant regulators have been invented in 1938 by Joseph Sola and since then apart from minor improvements, technology had been fundamentally unchanged. The regulator is based on the ferro-resonance principal; a transformer operates in magnetic saturation region. A basic diagram of a ferro-resonant regulator is shown in Figure 2.18(a) [14, 15, 76]. As shown in the Figure 2.17(b) when the transformer core is in magnetic saturation, in order to make a very small change in magnetic flux in the core need a relatively large winding current. Winding current and the magnetic flux are proportional to input and output voltage of the transformer. Therefore when the core is in saturation, a large change of input voltage is needed to make a very small change in the output voltage [14, 76, 77].

Assuming a transformer core with well-defined saturation characteristics as per Figure 2.17(b), and if the input voltage is sufficiently large so that transformer core drives into saturation from $-\phi_s$ to $+\phi_s$ within a half cycle. From the Faraday's law, the induced secondary voltage will be,

$$e_t = -N(d\phi/dt)$$

where,
N - number of turns in the secondary winding,
ϕ - total flux in the core,
t - time,
If the core saturates at the end of the half cycle within a certain time (τ),

$$\int_0^{\tau} e_t dt = -N \int_{-\phi_s}^{+\phi_s} d\phi$$

the half-cyclic average-secondary-voltage ($V_{av,out}$) induced in the coil is given by [15],

$$V_{av,out} = -4NB_sAf$$

where,
B_s - saturation flux density of the core,

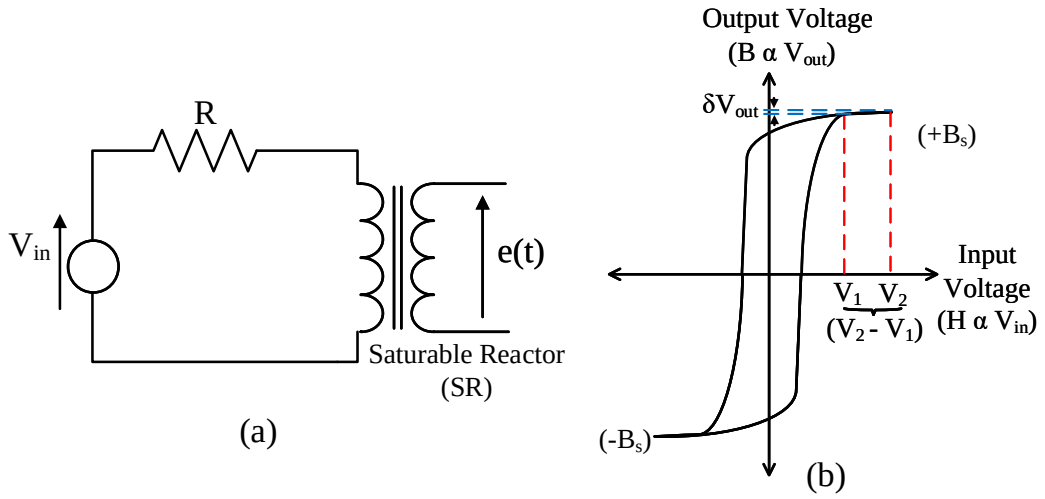


Figure 2.17: Saturable transformer operation (a) circuit diagram (b) B-H characteristics of the saturable transformer

A - cross-sectional area of the core,

f - source frequency

As long as the core is in saturation and the source frequency is fixed, the output voltage will be a constant value regardless of the input line voltage changes. Also when the core is driven into saturation, the output voltage follows the number of turn counts of the secondary winding.

As illustrated in Figure 2.18, a resistor is replaced with an inductor (L_1) to eliminate resistive power loss and a capacitor (C_1) is connected in parallel to saturable reactor (SR) for more effective and efficient regulation. Saturable reactor is a special form of inductor with a magnetic core that can be deliberately saturate from a direct current. They are commonly used for saturating transformers in constant voltage transformers.

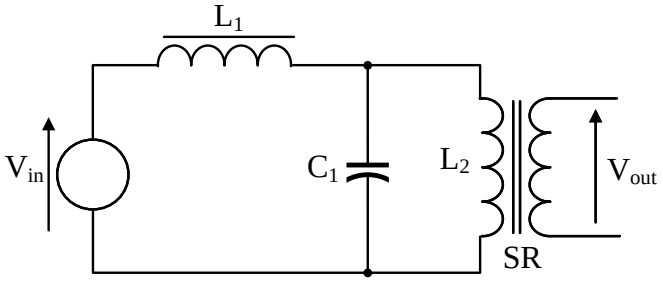


Figure 2.18: Basic ferro resonant regulator

The capacitor is tuned with the inductor near the input source frequency. When the SR saturates at time τ, before the end of the half-cucle, the capacitor (C_1) discharges and recharges in the opposite direction through saturated inductance (L_2) at a frequency

$$f = \frac{1}{2\pi}\frac{1}{\sqrt{L_2 C_1}}$$

When the current through SR goes to zero and reverses, the core comes out of saturation. Since the capacitor has an initial charge on it, a high voltage across the capacitor is kept until the core again saturates. Thus, regulation is maintained at a constant voltage.

Other advantages of this parallel capacitor are such that along with the inductor it makes a low-pass filter between input and the output to achieve an ideal output waveform for rectification and filtering and it can withstand any input voltage spikes.

This simple construction ensures reliable operation, and due to tuned LC circuit which provides low-pass filtering, the output is insensitive to input voltage spikes. Although this concept makes a good voltage regulation, operating in the saturation region has a substantial disadvantage of very poor electrical efficiency of the transformer [33, 76, 77]. In addition, the output voltage is frequency sensitive and since the core being the regulating element, the output voltage is affected by the load current changes due to voltage drop across the secondary winding-resistance [15].

2.2.3 Transformer tap changers

A low-cost solution for AC regulation relies on electronic transformer tap-changers. As shown in Figure 2.19, this regulator monitors the output by a feedback loop and automatically switches taps in the

secondary winding to change the turns ratio, hence maintain constant RMS voltage output. The tap changing mechanism works as follows.

The transformer secondary side contains several taps (multiple locations in the winding having different number of turn counts). A feedback controller driven motorized drive system (i.e. a servo mechanism) controls the motion of brushes or contactors/relays along the taps on the secondary winding until the output voltage falls within the desired range [17, 35, 36]. Thus at threshold voltage points, when the transformer taps are switched, uncontrolled "tap dancing" can occur if the input voltage fluctuates frequently [17, 35]. This could lead arching across taps, hence transients can appear at the output.

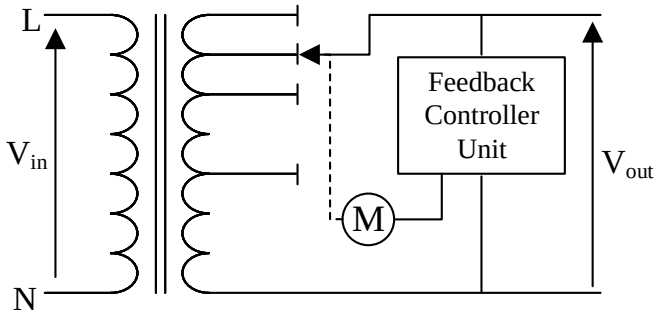


Figure 2.19: Basic transformer tap changer regulator

By implementing the buck- boost arrangement, the tap changing transformer regulator has been improved as illustrated in Figure 2.20. Buck-boost transformer is connected at the input-output load path, thus the output voltage level is maintained by injecting a suitable voltage in-series with the line, whereas the regulation transformer with multiple taps provide the required voltage to the primary of the buck-boost transformer. This method eliminates the load being disconnected by tap switching, hence transients due to switching effect will not be present at the output. But the additional transformer makes the device heavy and costly compared to the basic version and due to limited number of taps in the regulation transformer, the regulated output would be a desired voltage range rather than a constant value.

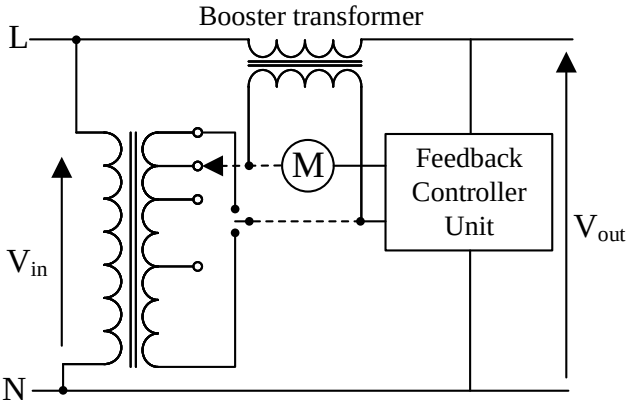


Figure 2.20: Tap changing regulator based on buck-boost transformer

Other than using a bulky mechanical arrangement for tap switching, electronic tap switching scheme can be implemented using solid state devices such as thyristors and triacs [34, 36].

2.2.4 Solid state regulators

The fourth category of RMS AC voltage regulators is the solid state regulators that use switching devices such as thyristors (SCR), triacs or insulated gate bipolar transistors (IGBT). There are two basic types of solid state regulators available in the market such as tyristor-based designs and high-frequency switching based inverters.

Thyristor-based voltage regulators

Figure 2.21 shows a simple construction of a thyristor-based voltage regulator which is used for many industrial application such as lighting control, speed control of induction motors and temperature control of heating elements (thyristors can be replaced by triacs) [20, 37, 78]. The conduction of the thyristor is controlled during each half cycle of an input AC voltage to maintain a constant RMS output voltage. Thyristor firing angle is determined by a feedback control unit measuring the difference between the input and the output. However, this simple phase control technique only can be used for step-down voltage regulation and as illustrated in Figure 2.21, thyristor triggering adds significant harmonics to the output which cause a considerable level of distortion in the output sine wave. The total distortion is proportional to the thyristor phase angle which is determined by the difference of input and output voltage, thus for larger deviation in the input line voltage, more distorted the output waveform [20].

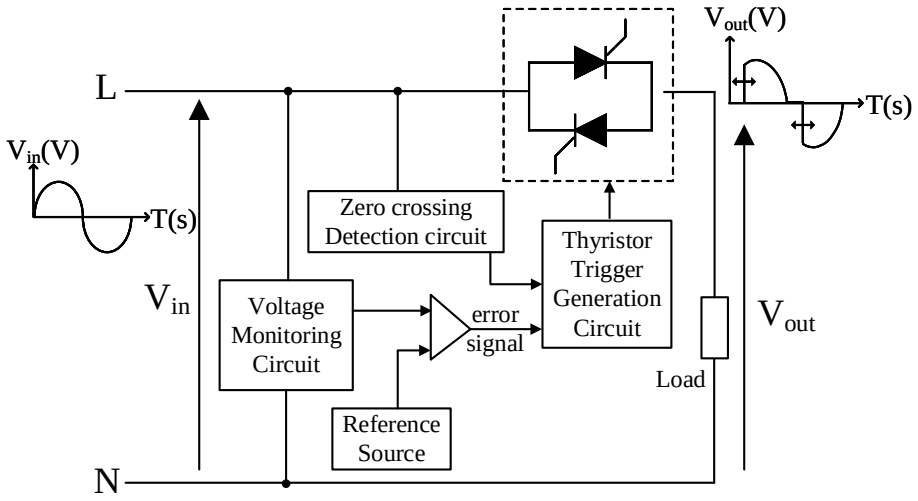


Figure 2.21: Basic thyristor-based AC voltage regulator

The output waveform distortion can be minimized by introducing an auto-transformer with multiple secondary taps as illustrated in Figure 2.22(a) [20,37]. During each half cycle, One of the lower and upper thyristors are fired alternatively, thus produce a less-distorted output sinusoidal waveform. Figure 2.22(b) illustrates a basic thyristor drive circuit based on a diode and a zener diode for each thyristor. This diode and the zener circuit is powered by a separate transformer winding called a trigger winding. This type of voltage regulator has fast response and reliability than its mechanical counterpart at a cost of high price. On the other hand, the thyristors can easily be damaged by high currents such as inrush, overload and short-circuit currents.

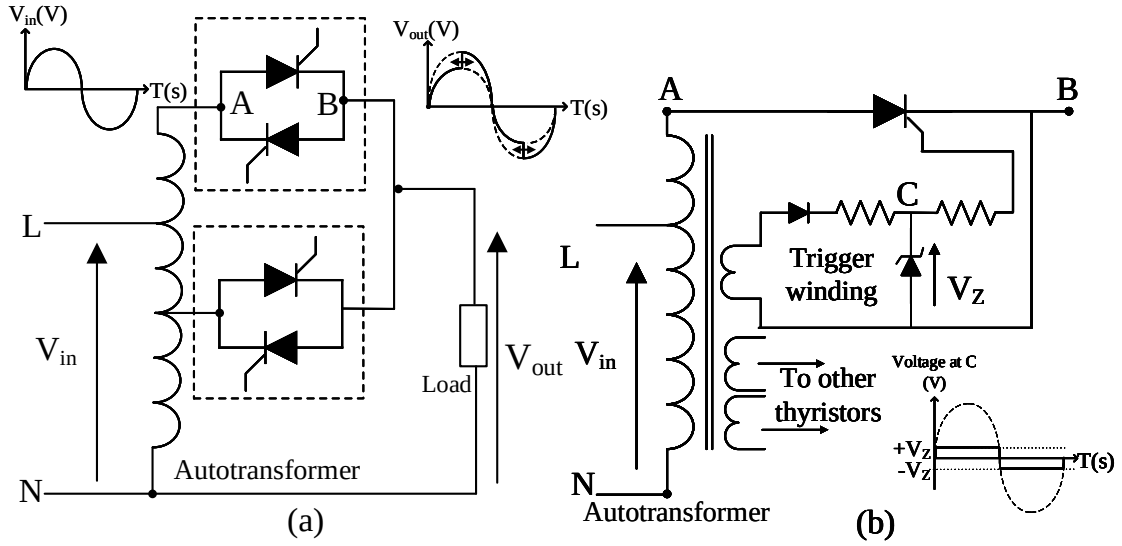


Figure 2.22: Autotransformer based thyristor regulator (a) schematic diagram (b) basic thyristor drive circuit derived from an additional winding

High-frequency switched RMS AC voltage regulators

High frequency AC-AC voltage regulators are very popular in the market due to the compact size, fast dynamic response and better efficiency. But there are well-known issues inherited with PWM based solid state regulators such as the RFI/EMI related issues and typically high harmonic content in the output waveform [23, 39]. In order to eliminate such issues, majority of solid state regulators come up with various types of snubber circuits and AC filters which adds an additional cost of manufacturing, higher component count and complexity of the circuit [18, 22, 24, 27]. Depending on the load requirements, the filter circuits can be simple or complex which will be reflecting from its market price. Therefore, a solid state regulator with less THD, suitable for an application in the presence of sensitive loads could be very expensive [22, 27]. Following paragraphs briefly discuss some of the existing solid state regulators available in the market.

Figure 2.23(a) illustrates a conventional step-down AC-AC voltage regulator based on two pairs of IGBTs, one pair connected in series to the load (S1a and S1b) and the other in parallel with the load (S2a and S2b) [16, 19, 22, 27]. The series-connected switches (S1) regulate the voltage output with respect to a PWM scheme and the parallel ones (S2) provide the freewheeling current path when S1 switches are turned-off. If S1 and S2 are both turned on at the same time, a short circuit can occur. Therefore a dead-time must be considered in between turning on and off of S1 and S2 power switches. However, switching losses produced in the power switches and the commutation problem of switching elements are major limitation of this technique where the latter can create voltage spikes specially for inductive loads. As illustrated in Figure 2.23(b), RC snubber circuits are used to solve the voltage spikes problem, but this leads to increase the total losses and reduce the efficiency of the device [16, 22, 27].

Improved PWM algorithms can be used to reduce the harmonic content of the output waveform generated by the switch-mode voltage regulators [16, 18, 22, 25–27, 38]. In some applications, the control scheme of the power switches (PWM based gate signal) is determined by detecting the polarity of the load current using voltage/current sensors. Such technique is described in [79] for implementing a voltage regulator for a voltage sag correction and is illustrated in Figure 2.24. During each half cycle, S1 and

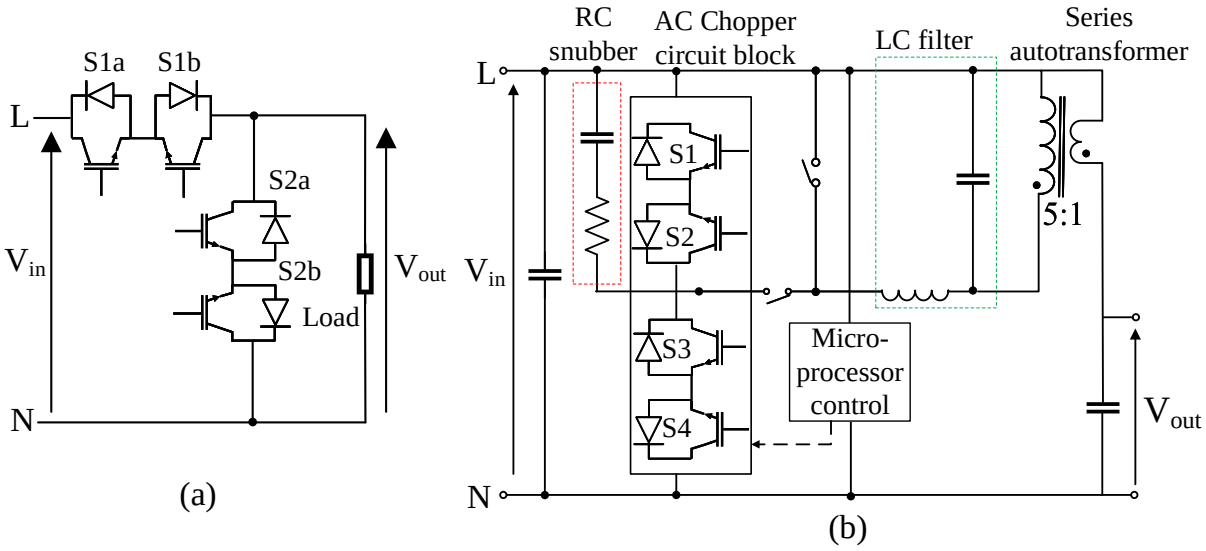


Figure 2.23: Conventional AC-AC regulator (a) basic circuit diagram (b) regulator with RC snubbers and LC filters

S2 switches operate alternatively. During positive (or negative) half cycle when S1 ON and S2 OFF (or S2 ON S1 OFF), current passes through the inductor L_2 while storing the energy, and when S2 is ON, the stored energy in the inductor is transferred to S2 and vice versa. A control circuit maintains a constant output by changing the duty cycle of the PWM signal to switch the bidirectional switches, based on the difference between the input and output voltage. But using voltage/current sensors will not only add extra cost for manufacturing but the control algorithm may malfunction due to unexpected noise or harmonics manifest on the mains supply.

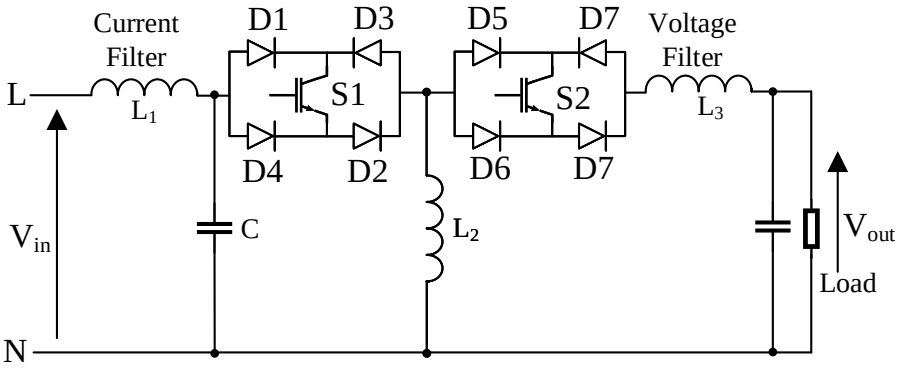


Figure 2.24: Regenerative snubbers to increase the regulator efficiency

The conventional PWM regulator as shown in Figs. 2.23, 2.24 have the common limitation of step-down type output regulation. Figure 2.25 illustrates an alternative technique to implement a step-up and down AC voltage regulation using a PWM chopper circuit and a tap changing transformer [16, 19, 25]. Tap selection and PWM signal generation is done by microprocessor based digital control circuit [16, 19, 38]

Most of the RMS AC voltage regulators described so far have common disadvantage of bulkiness due to the use of line-frequency transformers/ autotransformers with or without the motor-drive system. Based on a double conversion electronic voltage regulator, with a AC-to-AC electronic transformer can make RMS AC voltage regulators down-sized and more energy efficient. Figure 2.26 illustrates a basic

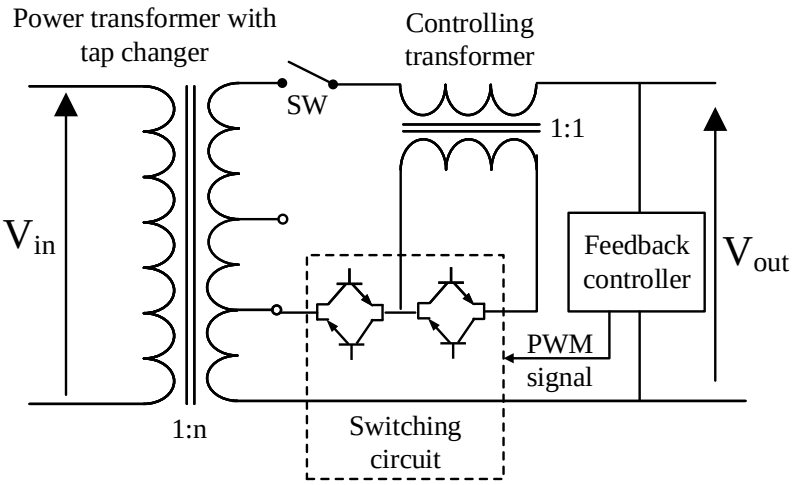


Figure 2.25: PWM AC chopper with tap changing transformer

block diagram of dual conversion voltage regulator including AC-to-DC and DC-to-AC conversions using high-frequency switches [35,36,80]. In this type of regulator, the voltage regulation is obtained by two methods; such as (i) regulating the DC output from the rectifier or (ii) supply a constant DC into the inverter stage and adjust the voltage during the inverter operation by adapting PWM technique during the DC-AC conversion using switching elements. However, the disadvantages include limited operation range (no buck regulation), double conversion technology where the conversion efficiency is normally not very high and potential problems for reactive loads.

The block diagram of AC-AC electronic voltage regulator shown in Figure 2.27(a), is capable of boosting the input voltage with a reduced size compared to similar capacity AC voltage regulators described above. As depicted in Figure 2.27(b), the AC reference generator produce an AC reference voltage, in-phase with input voltage. Two rectifier stages produce the rectified version of the reference voltage and the sample voltage taken from the output. These signals then fed to the comparator which generates the error signal representing the difference between the the AC reference and the output sample, thus, produces a PWM signal to control the electronic transformer [28, 80].

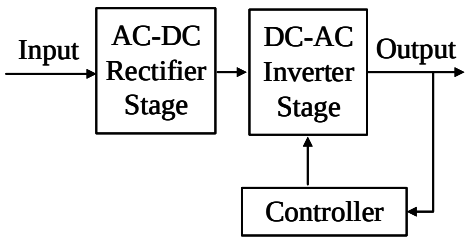


Figure 2.26: Dual conversion AC voltage regulator

Given the above summary on commercial RMS voltage regulators, none of them are well-positioned for worst-case power quality situations seen in most of the developing countries due to infrastructure limitations [29, 30]. In most of the cases, the urban areas of such countries are highly populated with residential and industrial sites where the loading condition of the electricity distribution lines get highly

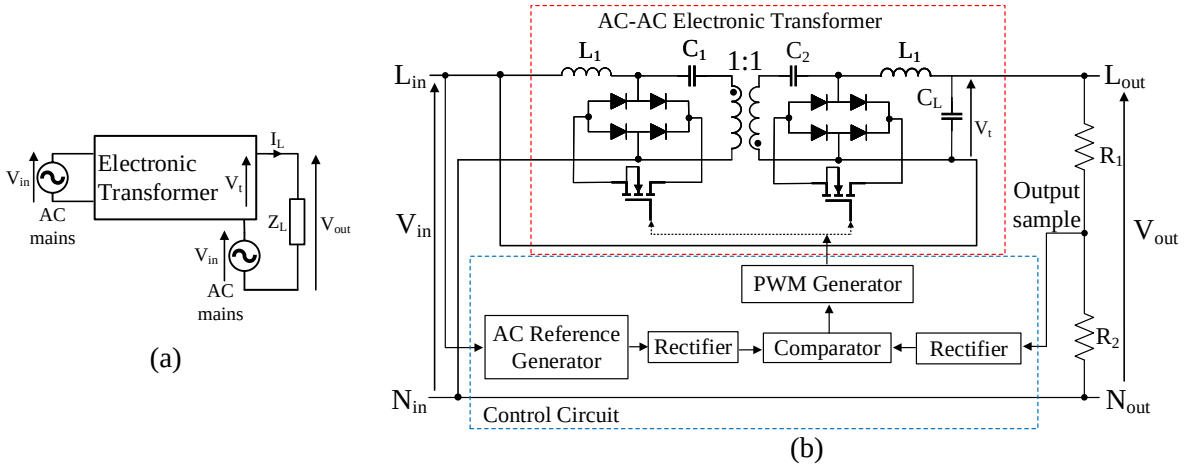


Figure 2.27: Dual conversion electronic AC voltage regulator; (a) simplified block diagram [35, 36] (b) electronic transformer based AC voltage regulator [80]

variable during peak consumption hours such as in the evening, and off-peak hours during the early morning. Therefore, during these periods, the line voltage broadly fluctuates around $\pm 15\%$ of the nominal value which does not comply with regulation standards of voltage fluctuations such as BS 7671, ANSI or IEC compliance. For such worst-case conditions, servo-driven, ferro-resonant or basic tap changing transformer type regulators are commonly used due to their lower cost, despite their common weaknesses such as bulkiness, slow response time and regular maintenance. On the other hand, solid-state regulators possess more advantages compared to the above types such as compact size and rapid response. Still, the limited operation range is a major drawback for adapting such systems in countries that require both boost and buck regulation. Also the cost of dual-mode regulators of solid-state type is beyond the budget; thus, are not very common.

Given this situation, a demand arose for a low-cost regulator that can operate in a wide input voltage range with high efficiency and better response time. Linear AC regulation technique was initially developed to overcome the typical issue of a flattened sine wave in a ferro-resonant regulator and the slow response time of servo-driven variacs. This design eliminates the complex issue of RFI/EMI problem typical to high-frequency PWM based designs as discussed in literature [18, 26]. However, the major drawback of the basic linear regulator is declining efficiency when the input line voltage reaches the nominal voltage and increases beyond that. The original work presented in this thesis covers two potential solutions to overcome this reduced efficiency at higher input voltages. Implementation details of these proposed solutions are discussed broadly in Chapters 4 and 5.

Series power transistor-array based linear AC regulator technique

The series power transistor-array based linear AC regulator is the newest member of AC voltage regulator family which is developed in the late 1980s' to address the significant drawbacks of the conventional regulators [41, 81, 82]. Although implementation details of the linear AC technique span through next chapters, a brief introduction given here explains the uniqueness of this technique in comparison to traditional designs.

Figure 2.28 illustrates the fundamental concept underpinning the linear AC technique based on a simple two-winding, a line-frequency transformer which provides a seamless buck and boost voltage at

the secondary winding, which is in series with the input supply and the output load. Variable impedance, Z_{series} that connected in series to the transformer primary winding, varies the effective impedance in relation to input voltage variations.

The overall operation of the power stage is based on the control of Z_{series} over a wide range of resistances from near zero to near infinity similar to linear DC regulators where the series power transistor acts as a variable resistor taking care of the input to output voltage difference. Traditional feedback control is implemented to monitor the output AC voltage and it continually keeps adjusting the impedance of Z_{series}.

The linear AC regulator technique discussed here is fundamentally different than the conventional methods due to the following properties:

1. A simple line-frequency step-down transformer with two windings is used
2. A series-connected power transistor array works in linear mode which does not require high frequency switching, thus eliminating RFI/EMI issues
3. The transistor array connected to a transformer primary winding is electronically controlled to vary its effective impedance from near zero to a very high value, thus eliminates the need to physically change the winding configuration between boost to buck modes [42].

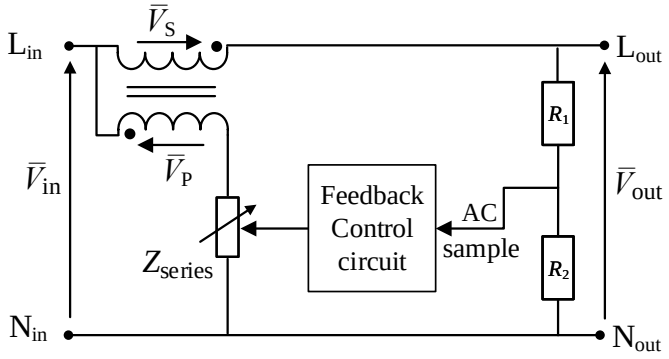


Figure 2.28: Fundamental block diagram of linear RMS AC regulator

The primary objective of this research is to develop a unique technique for upgrading the performance of an existing commercial product of an Australian company that employs a servo-driven technique which weighs more than 10 kg with a response time of $1.5-2$ s [30]. The linear Ac regulator presented here is comparatively light weight (approximately 3 kg) with a maximum response time of 125 ms, and an average efficiency of 95%. Preliminary prototype developed to demonstrate the validity of the new technique was targeted to achieve performance specifications comparable with other commercially available techniques [11,14,16,17,25,36]. Combining the efficiency and the speed of response, the targets were comparable with ferro-resonant and variac-driven systems respectively as well as less harmonics and no RFI/EMI issues like in switch mode regulators.

Chapter 3

Transistor Array Based Linear AC Voltage Regulator- Concept to Implementation

3.1 Fundamental Concepts of the Linear AC Regulator

Patented linear RMS AC regulator, following the simple concept of the linear DC regulator, was developed in the late 1980s to achieve a harmonic-free regulated output with waveform fidelity [81, 82]. Figure 3.1 compares the fundamental ideas underpinning DC and AC linear regulation [41, 42]. Figure 3.1(a) depicts a simple DC linear regulator in which a series transistor, Q, is used to buffer the voltage difference between the unregulated input voltage (V_{in}) and the regulated output voltage (V_{out}), using a control circuit block which changes the on-resistance of Q by changing its base current (i_{B}) [83–85]. One major disadvantage of this traditional technique is that its reduced efficiency due to power dissipation across the series pass device. Switching regulator is a good replacement to linear regulators, although noise and related issues which are inherent to switching techniques is a major disadvantage which cannot completely remove linear regulators in its many application including communication devices and sophisticated electronics.

In the linear AC technique illustrated in Figure 3.1(b), we replace this series transistor, Q with a secondary winding of a two-winding buck-boost transformer and makes use of the secondary winding to generate the boost (or buck) voltage correction when the AC mains voltage drops below (or rises above) the nominal value, and buffers the voltage difference between the input and the output. In order to achieve this, the primary winding of the transformer is connected to an electronically-variable series AC-impedance fed by a DC feedback loop, similar to the case of a linear DC voltage regulator.

The series transistor array-based linear AC voltage regulator is comprised of three important elements.

- Series variable impedance
- Buck-boost transformer
- Feedback control circuit

This chapter highlights the implementation details of the variable impedance, the action of the buck-boost transformer with regards to series impedance variation, and the feedback control circuit that controls the operation of the series variable impedance.

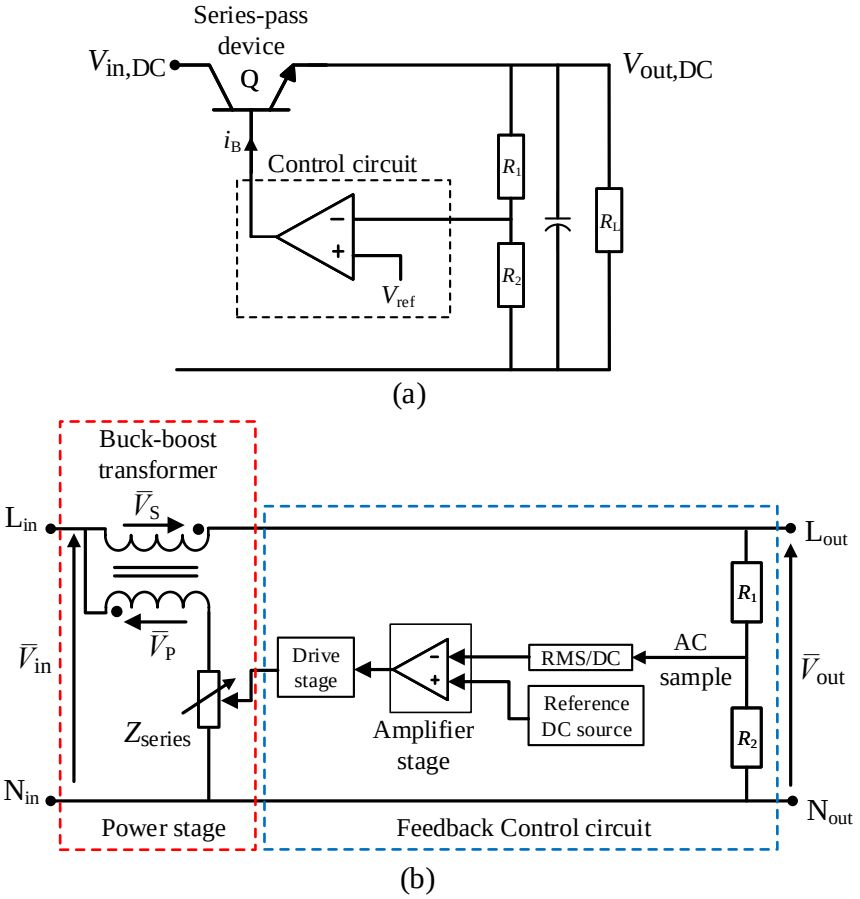


Figure 3.1: Linear AC regulator design (a) block diagram of the linear DC regulator; (b) block diagram of the linear AC regulator

In designing the prototype we have selected the boost mode operation to work up to around 180 V and the buck mode operation to be limited to about 260 V considering the real world practical situations of over-loaded distribution lines over a 24-hour period.

3.2 Implementation Aspects of the Electronically Variable Series AC Impedance

Based on the previous work [29, 42, 81, 82], the implementation of the electronically variable AC-impedance (Z_{series}) as in Figure 3.1(b) is discussed now. Developing the simple concept of a variable AC impedance (Z_{series}) as in Figure 3.1(b), comes with several significant challenges:

(a) Z_{series} should be electronically variable

(b) Z_{series} should be an AC impedance which could vary from zero ohms to an infinite value

(c) Z_{series} will be able to withstand several hundred volts (based on 230 V, 50 Hz nominal AC input)

(d) Necessity to keep the feedback loop electronically isolated from the power stage, for safety and reliability

Figure 3.2 illustrates the series AC-impedance based on a power transistor array where the AC-impedance can be electronically varied to any value between near-zero ohms to near-infinite value. Since

the power transistors cannot handle AC signals, a diode bridge is used to eliminate the voltage reversal across the transistor array.

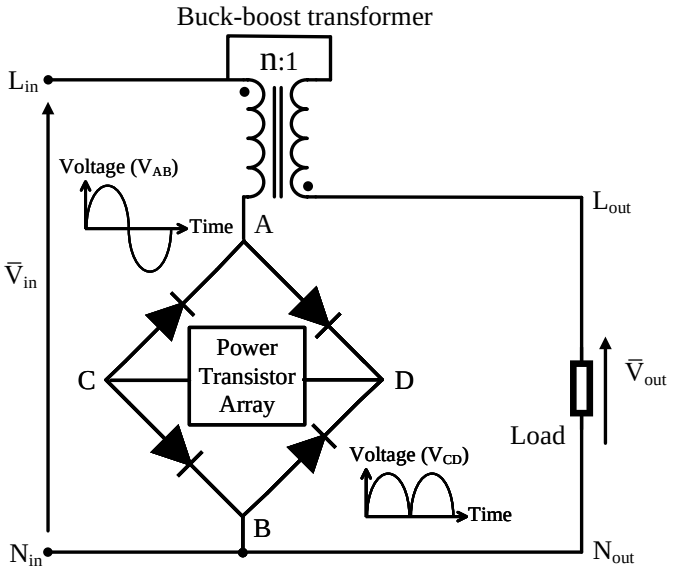


Figure 3.2: Implementation of the electronically variable series-impedance based on a power transistor array

To achieve variable resistance using a power transistor, we can place two resistors as in Figure 3.3(a) where R_{BC} is adjusted to change the base current, (i_B) while R_{BE} is adjusted to divert i_B when necessary. Two extreme cases are shown in Figure 3.3(b) and (c), where R_{CE} could be close to zero ohms (by short circuit R_{BC}) and infinitely large (by short circuit R_{BE}). Case in Figure 3.3(b) is equivalent to the case of a forward biased diode, and the case in Figure 3.3(c) is equivalent to reversed biased diode effect of the collector-base junction.

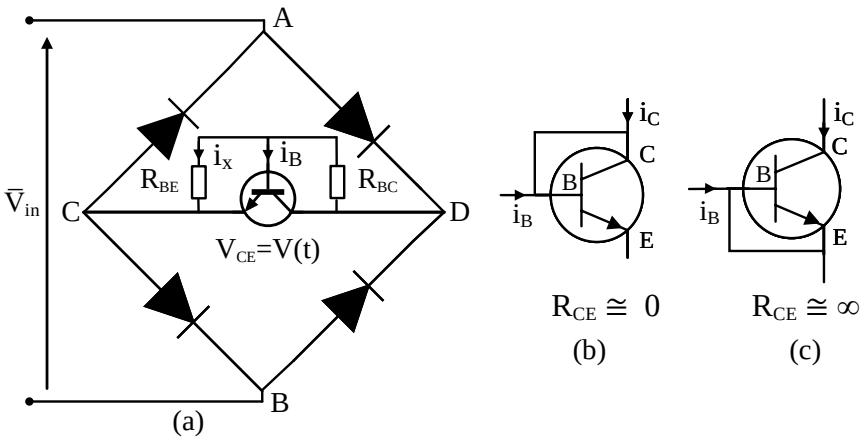


Figure 3.3: Electronically-variable AC-impedance; (a) single transistor implementation (b) transistor when fully saturated and cut-off

Figure 3.4 illustrates the achievement of electrical isolation between power stage and the control circuit using opto isolator circuits. Darlington pairs are used to enhance the current capability and to maintain adequate gain for each transistor [43, 86].

According to Figure 3.4, the effective instantaneous collector-emitter voltage of the transistor ($V_{CE}(t)$) can be written as follows,

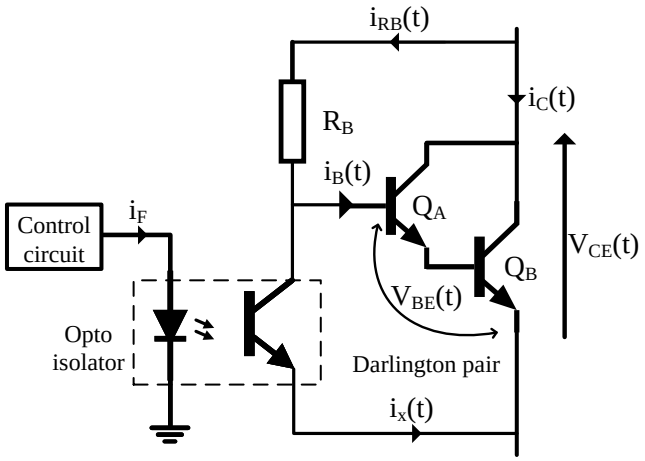


Figure 3.4: Optoisolator driven Darlington pair

$$V_{\mathrm{CE}}(t) = V_{\mathrm{BE}}(t) + R_{\mathrm{B}}[i_{\mathrm{B}}(t) + i\mathrm{x}(t)] \tag{3.1}$$

And the instantaneous non-linear resistance between the transistor collector and emitter junction, which is averaged out in a full AC cycle is given by,

$$R_{\mathrm{CE}}(t) = \frac{V_{\mathrm{CE}}(t)}{i_{\mathrm{C}}(t)} \tag{3.2}$$

where,

$V_{\mathrm{BE}}(t)$ - instantaneous base-emmiter voltage,

$i_{\mathrm{B}}(t)$ - instantaneous base current,

$i_{\mathrm{x}}(t)$ - diverted portion of the instantaneous base current

R_{B} - external resistance (base resistance) across the collector and base

$i_{\mathrm{c}}(t)$ - instantaneous collector current

Assuming the transistor has a constant current gain of h_{FE} and maintaining it in its linear operation region,

$$i_{\mathrm{C}}(t) = h_{\mathrm{FE}} i_{\mathrm{B}}(t) \tag{3.3}$$

Using Eqs.((3.1)), (3.2) and ((3.3)), the total instantaneous resistance of the transistor collector-emitter junction can be written as,

$$R_{\mathrm{CE}}(t) = \frac{V_{\mathrm{BE}}(t)}{h_{\mathrm{FE}} i_{\mathrm{B}}(t)} + \frac{R_{\mathrm{B}}}{h_{\mathrm{FE}}}\left(1 + \frac{i_{\mathrm{x}}(t)}{i_{\mathrm{B}}(t)}\right) \tag{3.4}$$

When the linear regulator operates in a range of RMS input voltages from 180 V to 250 V, the effective RMS voltage across the array could be a value range from 0 to $338\sqrt{2}$ V. This voltage is much larger than the transistor base-emitter voltage, thus, V_{BE} in Eq. (3.4) can be neglected, thus the simplified relationship is given by,

$$R_{\mathrm{CE}}(t) = \frac{R_{\mathrm{B}}}{h_{\mathrm{FE}}}\left(1 + \frac{i_{\mathrm{x}}(t)}{i_{\mathrm{B}}(t)}\right) \tag{3.5}$$

3.2.1 Multiple Element Power Transistor Array

As discussed in Section 3.2, when the regulator is driven at a full input voltage range of 180 V to 250 V, a resultant voltage of $338\sqrt{2} = 480$ V is applied across the transistor array when the input voltage reaches 250 V (for transformer turns ratio (n) of $180/50$). Figure 3.5 depicts how a high voltage across the bridge points of the transistor array can be equally distributed among several series connected transistors by suitably adjusting R_{B1} to R_{B4} values, while the effective transistor voltages and power dissipation are kept approximately equal [41].

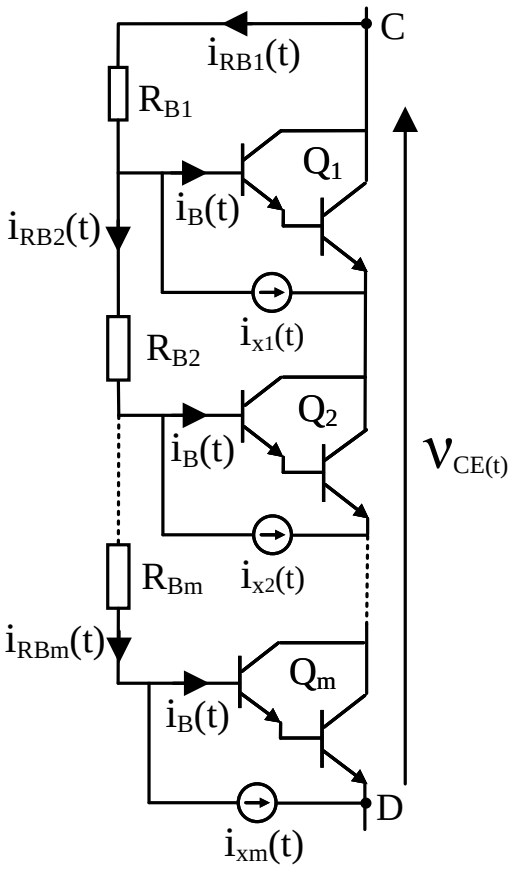


Figure 3.5: Configuration of the series transistor array

When the array has a uniform voltage distribution across all transistors, the instantaneous voltage across the m^{th} transistor of m element array (v_{CEm}) approximates to $\frac{v_{\text{CE}}(t)}{t}$.

In order to dissipate equal power across each element of the transistor array, the base currents and collector currents of each transistor should approximately be equal. Therefore;

$$i_{\text{B1}}(t) = i_{\text{B2}}(t) = i_{\text{B3}}(t) = \text{.....} = i_{\text{Bm}}(t) = i_{\text{B}}(t)$$
$$i_{\text{C1}}(t) = i_{\text{C2}}(t) = i_{\text{C3}}(t) = \text{.....} = i_{\text{Cm}}(t) = i_{\text{C}}(t)$$

Assuming large and identical transistor current-gain, β for all transistors, the collector currents can be written in terms of β and base currents as follows;

$i_{\text{C1}}(t) = h_{\text{FE}} i_{\text{B1}}(t)$; $\quad i_{\text{C2}}(t) = h_{\text{FE}} i_{\text{B2}}(t)$; $\quad i_{\text{C3}}(t) = h_{\text{FE}} i_{\text{B3}}(t)$; ..... $i_{\text{Cm}}(t) = h_{\text{FE}} i_{\text{Bm}}(t) = h_{\text{FE}} i_{\text{B}}(t)$

According to Figure (3.5),

R_{B1} - R_{Bm} - base resistors connected between the collector and the base of each transistor
$i_{RB1}(t)$ - $i_{RBm}(t)$ - instantaneous current flowing through the base resistors between each transistor

Then;

$$\begin{aligned} i_{RBm}(t) &= i_B(t) + i_x(t) \\ i_{RB(m\text{-}1)}(t) &= 2[i_B(t) + i_x(t)] \\ i_{RB(m\text{-}2)}(t) &= 3[i_B(t) + i_x(t)] \\ &\vdots \\ i_{RB3}(t) &= (m-2)[i_B(t) + i_x(t)] \\ i_{RB2}(t) &= (m-1)[i_B(t) + i_x(t)] \\ i_{RB1}(t) &= m[i_B(t) + i_x(t)] \end{aligned} \tag{3.6}$$

Now the instantaneous voltage across the array with respect to voltage drop across all the array elements is given by,

$$v_{CE}(t) = i_{RB1}(t)R_{B1} + i_{RB2}(t)R_{B2} + i_{RB3}(t)R_{B3} + ... + i_{RBm}(t)R_{Bm} + v_{BE}(t) \tag{3.7}$$

By using Eqs. ((3.6)) and ((3.7)) it yields,

$$v_{CE}(t) - v_{BE}(t) = R_{B1}[i_B(t) + i_x]m + R_{B2}[i_B(t) + i_x(t)](m-1) + R_{B3}[i_B(t) + i_x(t)](m-2) + ... + R_{Bm}[i_B(t) + i_x(t)] \tag{3.8}$$

If the base resistors from R_{B1} to R_{Bm} holds a relationship as follows

$$\begin{aligned} R_{B1} &= \frac{R_B}{m} \\ R_{B2} &= \frac{R_B}{m-1} \\ R_{B3} &= \frac{R_B}{m-2} \\ &\vdots \\ R_{Bm} &= R_B \end{aligned} \tag{3.9}$$

then the Eq. ((3.8)) can be written as

$$v_{CE}(t) - v_{BE}(t) = mR_B[i_B(t) + i_x(t)] \tag{3.10}$$

and simplified as

$$v_{CE}(t) - v_{BE}(t) = mi_B(t)R_B\left(1 + \frac{i_x(t)}{i_B(t)}\right) \tag{3.11}$$

Eq. ((3.11)) divide by i_C yields

$$\frac{v_{CE}(t)}{i_C(t)} - \frac{v_{BE}(t)}{i_C(t)} = \frac{mi_B(t)R_B}{i_C(t)}\left(1 + \frac{i_x(t)}{i_B(t)}\right) \tag{3.12}$$

By substituting $i_C(t)$ and $V_{CE}(t)$ from Eqs. ((3.1)) – ((3.3)), into Eq. ((3.12)), we obtain

$$R_{CE}(t) = \frac{mR_B}{h_{FE}}\left(1 + \frac{i_x(t)}{i_B(t)}\right) + \frac{v_{BE}(t)}{h_{FE}i_B(t)} \tag{3.13}$$

which can be further simplified as below ($V_{BE}(t)$ considered negligible compared to $V_{CE}(t)$ when the array is conducting),

$$R_{CE}(t) \approx m\frac{R_B}{h_{FE}}\left(1 + \frac{i_x(t)}{i_B(t)}\right) \tag{3.14}$$

3.2.2 Base Current Diversion Ratio (BCDR)

Based on Eq. (3.5), the effective instantaneous collector-emitter resistance can be controlled by varying either R_B or $i_x(t)$. The optotransistor between base and emitter controls $i_x(t)$ thus setting the $i_x(t)/i_B(t)$, the base-current diversion ratio (BCDR). The low base-emitter voltage (v_{BE}) of the transistor array permits an easy control of BCDR as shown in Figure 3.4. This optoisolator arrangement not only drives the transistor-array but also provides necessary electrical isolation between the high power handling transistors and the low-power control unit, as shown in Figure 3.6.

A high BCDR is required to obtain a maximum effective instantaneous array resistance ($R_{CE,max}(t)$). The high BCDR, nearly the total base current is diverted and transistors are driven into cut-off region. In practical scenario a minor transistor leakage effect is expected. However by neglecting the leakage effect, according to Eq. (3.9), $R_{CE,max}$ is given by,

$$R_{CE,max}(t) = R_B + \frac{R_B}{2} + \frac{R_B}{3} + \frac{R_B}{4} + \ .... \ + \frac{R_B}{m} \tag{3.15}$$

When the transistor array drives into saturation, that establishes a low BCDR by approximating $i_x(t) = 0$, the effective instantaneous resistance of the transistor array becomes minimum ($R_{CE,min}(t)$). As per Eq. (3.14),

$$R_{CE,min}(t) = \frac{mR_B}{h_{FE}} \tag{3.16}$$

Thus the effective resistance of the transistor array can be controlled in the range of $R_{CE,min}(t)$ to $R_{CE,max}(t)$ by varying the diode current (I_F) of the optoisolator unit which is controlled by the feedback control circuit. Implementation details of the feedback control circuit is discussed in detail in the Section 3.4.

Figure 3.6 illustrates an implementation of a full four-element transistor-array, which had been used for the first prototype of the linear AC regulator built in late 1980s' [41, 42, 81].

In the four-element case, assuming that transistors do not have any leakage effect, the effective resistance of the array is ranged as below and this can be controlled by varying the current through optoisolator diode.

$$R_{CE,min}(t) = \frac{4R_B}{h_{FE}}$$

$$R_{CE,max}(t) = 2.1R_B$$

3.2.3 Darlington Pair Implementation

In order to enhance the current capability and to maintain an adequate gain for each transistor, a Darlington pair arrangement is used in the transistor array, as illustrated in Figure 3.4. In this application, a lower and a high power rated n-p-n bipolar junction transistors are used, following the structure illustrated in Figure 3.7. In a Darlington arrangement, the current amplification achieved by the input transistor is further amplified by the output transistor resulting in a high current gain, as explained below.

As indicated in Figure 3.7, the emitter terminal of input-transistor (Q_1) energises the base terminal of the output-transistor. Given that h_{FE1}, h_{FE2} are the current gains of input and output transistors respectively, following relationships hold true,

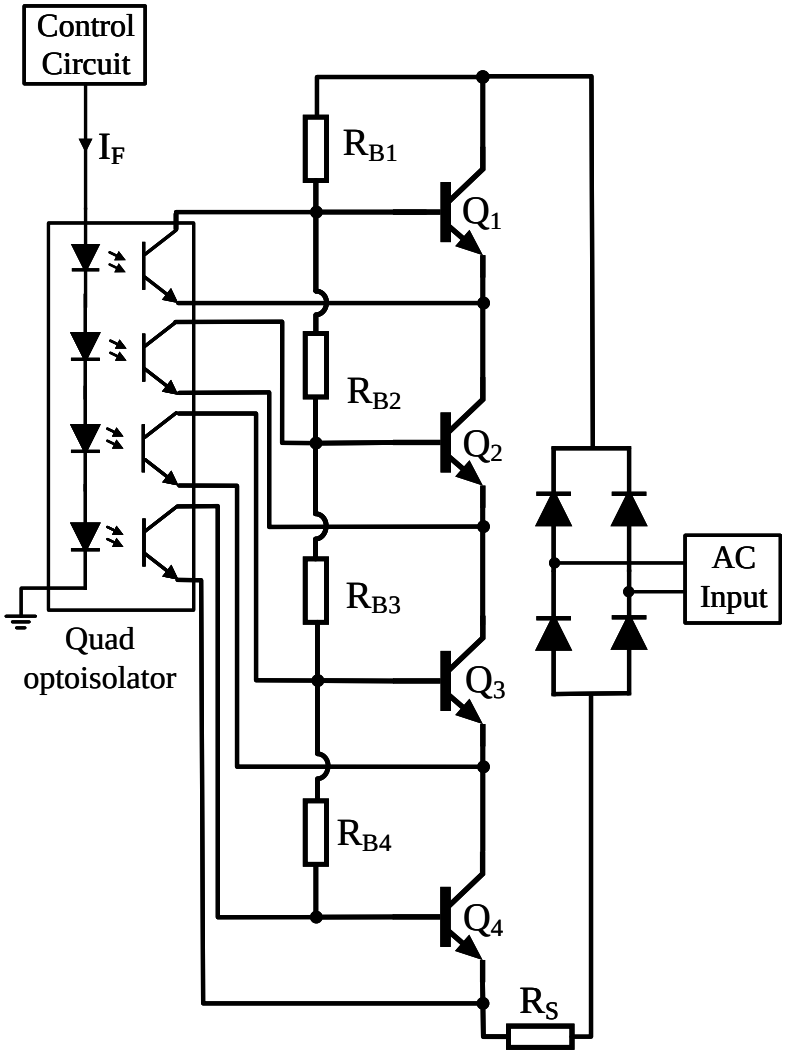


Figure 3.6: Four-element power transistor array

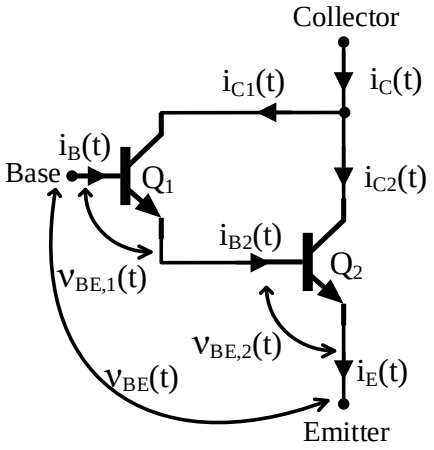


Figure 3.7: Structure of a Darlington pair

$$i_C(t) = i_{C1}(t) + i_{C2}(t) \tag{3.17}$$

$$i_C(t) = h_{FE1} i_B(t) + h_{FE2} i_{B2}(t) \tag{3.18}$$

Since the emitter current of Q_1 equals to the base current of Q_2,

$$i_{B2}(t) = i_{C1}(t) + i_B(t) \tag{3.19}$$

$$= h_{FE1} i_B(t) + i_B(t) \tag{3.20}$$

$$= i_B(t)(h_{FE1} + 1) \tag{3.21}$$

Substituting Eq.(3.21) into Eq.(3.18) yields,

$$i_C(t) = i_B(t)(h_{FE1} + h_{FE1}h_{FE2} + h_{FE2}) h_{FE,Darlington} = h_{FE1} + h_{FE1}h_{FE2} + h_{FE2} \tag{3.22}$$

If h_{FE1}, h_{FE2} are high enough, above relation can be approximated with,

$$h_{FE,Darlington} \approx h_{FE1} h_{FE2} \tag{3.23}$$

Thus the overall current gain of the Darlington pair is approximately equaled to the product of individual gains of the two transistors [87–89]. Since there are two junctions between the base and the emitter of the Darlington pair, the equivalent base-emitter voltage is the sum of individual base-emitter voltages of the two transistors as shown in the following equation.

$$V_{BE,Darlington}(t) = V_{BE,1}(t) + V_{BE,2}(t) \tag{3.24}$$

In the current prototype, a low-power rated input-transistor is used to bias a high-power rated output-transistor in order to drive it in linear operation region using a minimal base current, which is controlled by an optoisolator driver unit as explained in the section below.

When selecting the transistors for the Darlington pair, the following factors were considered.

- transistors for linear/active operation
- maximum effective instantaneous voltage across the array (0 V to $338\sqrt{2}$ V)
- maximum RMS current through the array (i.e. $\bar{I}_L = 5$ A, $n = 180/50 \Rightarrow \bar{I}_{array} = \bar{I}_L/n = 1.4$ A)
- maximum RMS power dissipation ($P_{max} = \overline{V}_{array,max} * \bar{I}_{array} = 480 * 1.4 = 670$ W)
- unit price
- DC current gain (h_{FE})
- transistor packaging type (i.e., TO-220 package to dissipate a relatively large amount of heat, easy mounting, and space-saving)

By considering the above parameters, Darlington pair transistors were selected. FJL6920 power transistor was selected as the high power output transistor, while BU931T was used as the low power input transistor.

High Power-Rated Output Transistor: FJL6920

This high power n-p-n transistor provides essential features required to implement the Darlington pair for the linear AC regulator application. It comes with TO-264 packaging for easy mounting and space saving. It has high collector-emitter voltage (V_{CEO}) 800 V specifically selected for the purpose of reducing the number of elements in the array. Figure 3.8 illustrates the typical h_{FE} vs I_C graph for constant V_{CE}, extracted from the manufacturers datasheet of Fairchild semiconductor.

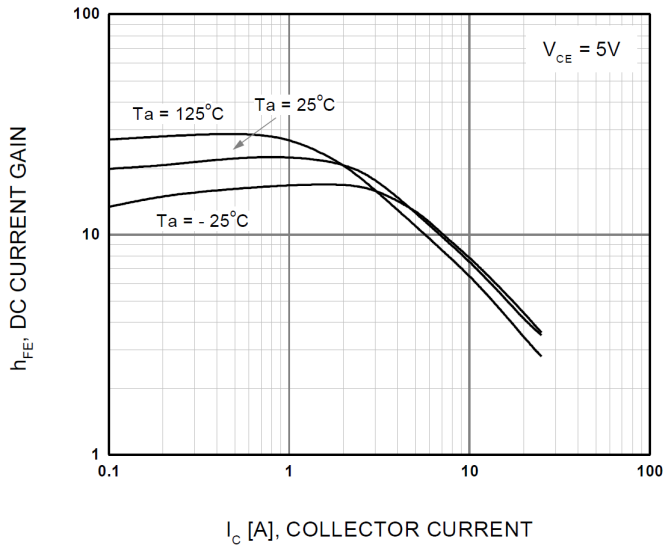


Figure 3.8: H_{FE} Vs i_C curve of FJL6920 power transistor; extracted from Fairchild Semiconductors datasheet

Table 3.1: Absolute Maximum Ratings of FJL6920 Power Transistor: at 25°C unless otherwise noted. (Fairchild Semiconductor)

Symbol	Parameter	Rating	Units
V_{CBO}	Collector-Base Voltage	1700	V
V_{CEO}	Collector-Emitter Voltage	800	V
V_{EBO}	Emitter-Base Voltage	6	V
I_C	Collector Current (DC)	20	A
I_{CP}*	Collector Current (Pulse)	30	A
P_C	Collector Dissipation	200	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	$-55 \sim 150$	°C

*Pulse Test: PW $= 300\ \mu s, Duty\ Cycle = 2\%\ Pulsed$

Low Power-Rated Input Transistor: BU406

BU406 is selected as the input transistor of the Darlington pair to drive the high-power transistor. It has the following characteristics that serve the purpose.

Figure 3.9 indicates the approximate current gain of the transistor for a load current of 1 A $-$ 5 A. In the application of variable impedance, the collector current takes a rectified sinusoid shape ranging from 0 to 1 A. This peak value is corresponding to a maximum load current of 5 A.

Table 3.2: Absolute Maximum Ratings of BU406 Transistor (On Semiconductor)

Symbol	Parameter	Rating	Units
V_{CEO}	Collector-Emitter Voltage	200	V
V_{CBO}	Collector-Base Voltage	400	V
V_{EBO}	Emitter-Base Voltage	6	V
I_C	Collector Current - Continuous - Peak Repetitive	7 10	A
I_{CM}	Collector Current - Peak (10 ms)	15	A
I_B	Base Current	4	A
P_D	Total Device Dissipation @$T_C = 25°C$ Derate above 25°C	60 0.48	W $W/°C$
T_J, T_{STG}	Operating and Storage Junction Temperature	-65 to 150	°C

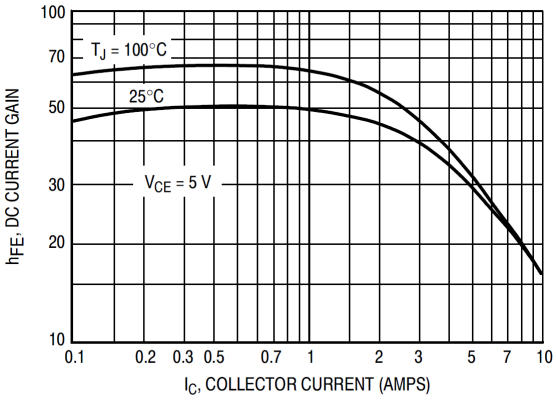


Figure 3.9: DC current gain Vs collector current; adapted from BU406 ON Semiconductor datasheet

3.2.4 Optoisolator Driver Unit

Optoisolators are useful in applications where an analog or a digital signal needs to be transferred between circuit modules of different power levels or presence of noise components [90]. Upon application in linear AC regulator, it provides main two advantages to its digital circuit.

- Driving high power rated transistor array by diverting a portion of the base current of power transistors in order to drive them in the linear region as required by the regulation process (see section 3.2.2) [85].
- It provides the essential electrical isolation between the high voltage power stage and the low voltage control circuit as illustrated in Figure 3.5.

As indicated in the discussion in Section 3.2, the requirement of a optoisolator is to drive a power transistor array that handles high current, high voltages RMS quantities by a very small driver signal coming from a low power handling digital control circuit. In such application, an optoisolator is configured as per Figure 3.10. In this diagram, the voltage of base-emitter (v_{BE}) applies on the optotransistor [85]. The value of Resistor (R) depends on the supply voltages ($+V_{CC}$ to $-V_{CC}$), and the maximum rating of the base current of Q.

When no current flows in the LED, the phototransistor is off, allowing the I_R current to flow into the base of Q, turning it "ON". This is the situation where optotransistor is in cut-off mode and Q in saturation. When the optotransistor is turned "ON" which provides a short-circuit path to flow I_R without flowing through the base of Q, thus turning "OFF" Q [85, 90].

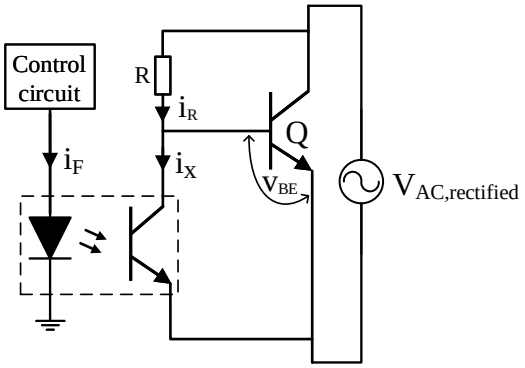


Figure 3.10: Optoisolator configuration used in linear AC technique

Thus the optoisolator operation between cut-off to saturation enables the control of BCDR of the Darlington-pair indicated in Section 3.2.2. For high BCDR, where maximum array resistance, $R_{\mathrm{CE,max}}$ is required, the Darlington-pair drives into cut-off region by entering the optotransistor into saturation, where $i_{\mathrm{x}} = i_{\mathrm{x,max}}$. On the other hand, a low BCDR is delivered by pumping the full portion of the base current into the array by driving the optotransistor into cut-off region ($i_{\mathrm{x}} = 0; i_{\mathrm{B}} = i_{\mathrm{B,max}}$). Intermediate BCDR is achieved when the optotransistor operates in the linear mode. Figure 3.11 illustrates the effect on collector-emitter voltage in relation to the collector current of the optotransistor, that is extracted from manufacturers datasheet of Toshiba TLP504A [91]. Optotransistor collector-emitter voltage is applied directly across the base-emitter junction of the Darling pair as shown in Figure 3.4, which is responsible for biasing the transistor array. The optotransistor collector current is set by the optodiode current, which is controlled by the output-sensing feedback control circuit as indicated by Figure 3.10.

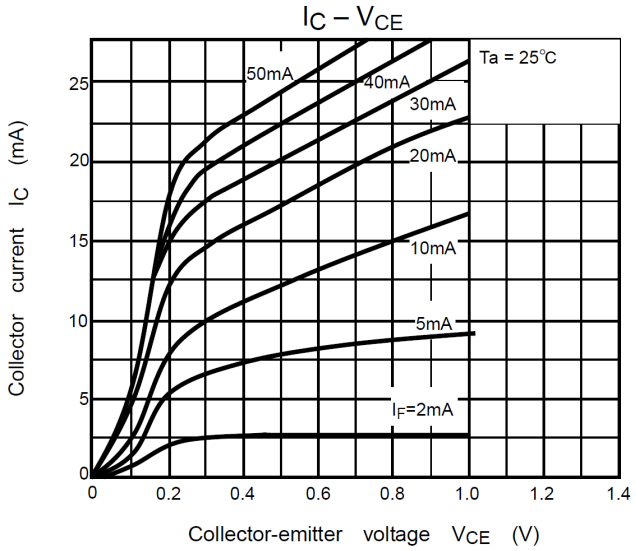


Figure 3.11: Collector current vs collector-emitter voltage adapted from Toshiba TLP504A Datasheet

Each element of the array needs a separate optoisolator to drive its base-emitter junction. Therefore TLP504-A quad optoisolator is used to drive a four-element transistor array. The following table provides essential electrical characteristics of the IC.

Table 3.3: Absolute Maximum Ratings of TLP504A Quad Optoisolator (Toshiba)

Characteristics	**Symbol**	**Rating**	**Unit**
LED			
Forward Current	I_F	60	mA
Reverse Voltage	V_R	5	V
Detector			
Collector-Emitter Voltage	V_{CEO}	55	V
Emitter-Collector Voltage	V_{ECO}	7	V
Collector Current	I_C	50	mA
Collector Power Dissipation (1 circuit)	P_C	150	mW
Operating Temperature Range	T_{opt}	$-55 \sim 100$	°C
Total Package Power Dissipation	R_T	250	mW
Total Package Power Dissipation Derating	$\Delta P_T/°C$	-2.5	mW/°C
Isolation Voltage	BV_s	2500 (AC, 1 min.)	V_{rms}

3.2.5 Rectifying Stage

Due to the design architecture of bipolar junction transistors (BJTs), the power transistor-array cannot handle voltage reversals or negative voltages. In order to provide a DC environment amidst the AC domain, a bridge rectifier is used. It is connected in between the transformer and the transistor array to convert the AC signal coming out from the transformer into a fully rectified DC signal that feeds the BJT array. Figure 3.3 depicts the bridge rectifier arrangement used in the power stage.

When selecting a suitable bridge rectifier IC, the operating voltage and the current rating need to be considered. The maximum ratings are specified by the maximum effective voltage across the transistor-array and the transformer primary current at the highest worst-case scenario of the input voltage. Considering the design specifications, the following bridge rectifier IC was selected to implement the rectifying stage.

Table 3.4: Absolute Maximum Ratings of GBJ1508 (On Semiconductor)

Symbol	**Parameter**	**Rating**	**Units**
V_{RRM}	Maximum Repetitive Reverse Voltage	600	V
V_{RMS}	Maximum RMS Bridge Input Voltage	420	V
V_R	DC reverse Voltage (Rated V_R)	600	V
$I_{F(AV)}$	Average Rectified Forward Current at @$T_C = 55°C$	25	A
I_{FSM}	Non-Repetitive Peak Forward Surge Current	300	A
T_{STG}	Storage Temperature Range	-55 to $+150$	°C
T_J	Operating Junction Temperature	-55 to $+150$	°C

3.3 Transistor Operation Under Rectified Voltage Supply

Throughout the preceding section as implied by the Eq.(3.3), the current gain, h_{FE}, considered a constant in the forward-active operation of a transistor. It is important to note here that the Darlington pair used in this particular application operates under a rectified waveform where the instantaneous voltage and current varies in a half sinusoid as indicated in Figure 3.2. During very low instantaneous voltages of the applied voltage where $V_{CE} < V_{BE}$, the current gain (h_{FE}) highly varies; thus, cannot be considered a constant.

The compound base-emitter voltage of a Silicon based Darlington pair ranges between $1.2-1.4$ V; therefore the non-linear effect of the highly-variant current gain is visible under very low voltages such as $V_{CE} < V_{BE}$. In comparison to the operation voltage range of the transistor array which is peaking at $340\sqrt{2}$, this non-linearity effect only becomes significant during the cross-over points of the sinusoidal waveform, which allows a near-ideal sine wave at the output. Because the effect was so insignificant, the non-linearity of the current gain did not affect to the basic calculations that was used to implement the AC operable variable impedance in Section 3.2. However, a concise discussion on the effect of the current gain during low input voltages is presented under this section.

In a typical n-p-n transistor, base-emitter and the base-collector junctions behave as two diode junctions when the transistor establishes a forward operation by forward-biasing the emitter-base junction (V_{BE}) and reverse-biasing the base-collector junction (V_{BC}), as illustrated in Figure 3.12. For a typical Silicon transistor, the base-emitter junction has a forward-biased voltage of $0.6-0.7$ V and exhibit a similar voltage current characteristics (i-v characteristics) of a diode as illustrated in Figure 3.13; this graph is extracted from the manufacturers datasheet of FJL6920 power transistor of Fairchild semiconductor.

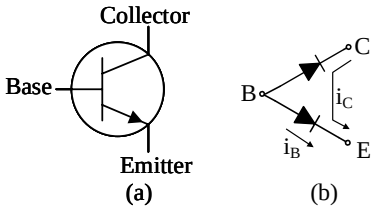


Figure 3.12: N-P-N trasistor (a) symbol (b) ohmmeter's view of transistor terminals

Transistor forward-biased operation is governed by the base-emitter voltage (V_{BE}), that determines the transistor collector current which is approximately proportional to the base current where the proportionality constant is defined as the current gain, h_{FE}. Following is the Ebers-Moll equations that determines I_C as a function of V_{BE} [92–94],

$$i_C = I_s \left[e^{V_{BE}/V_T} - 1 \right] \tag{3.25}$$

where,

I_s - saturation current or scale current defined by the device manufacturer

V_T, thermal voltage = kT/q = 25.3 mV at room temperature (68°F/20°C), k is Boltzmann's constant (1.38×10^{-23} joules/°K), q is the electric charge (1.60×10^{-19})

h_{FE}, current gain = i_C/i_B

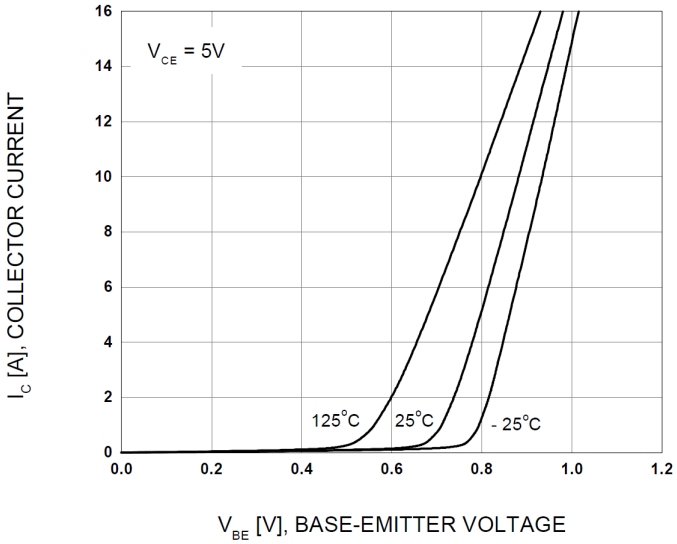


Figure 3.13: The i-v characteristics of the FJL6920 power transistor; extracted from Fairchild Semiconductors datasheet

In the active region, $I_s \ll I_C$, and in comparison with the exponential, -1 term in Eq. (3.25) can be neglected [92, 93]. Using this relationship, the base current can be determined in relation to the current gain such as,

$$i_B = \frac{I_s}{h_{\mathrm{FE}}} e^{V_{\mathrm{BE}}/V_{\mathrm{T}}} \tag{3.26}$$

Using Eq. (3.26), the term i_{B} in Eq. (3.4) can be substituted as,

$$R_{\mathrm{CE}} = \frac{V_{\mathrm{BE}}}{I_s e^{V_{\mathrm{BE}}/V_{\mathrm{T}}}} + R_{\mathrm{B}} \left(1 + h_{\mathrm{FE}} \frac{i_{\mathrm{x}}}{I_s e^{V_{\mathrm{BE}}/V_{\mathrm{T}}}}\right) \tag{3.27}$$

The value of current gain, h_{FE}, is typically ranging from $20-1000$ that depends on the transistor type, I_{C}, V_{CE} and temperature [93]. According to Eqs. (3.25) and (3.26), the collector and base currents exponentially relates to base-emitter voltage (V_{BE}) which suggests a non-linear relationship as illustrated in Figure 3.13. Normally, the manufacturer's datasheet provides the characteristic curves specified to that particular transistor, that relates the current gain to the other transistor parameters such as the collector current and collector-emitter voltage which are very useful in designing electronic circuits. Figure 3.8 illustrates the typical h_{FE} vs I_{C} graph for constant V_{CE} of FJL6920 transistor.

As indicated in Section 3.2, the BJT array works in the presence of a full-wave rectified waveform ranging its effective instantaneous voltage from $0-340\sqrt{2}\ \mathrm{V_{RMS}}$, as illustrated in Figure 3.2. Figure 3.14 illustrates the voltage and current waveforms indicating their peak and RMS values considering the regulator operation at 2 A load current and 260 V input voltage that maintains 230 V nominal voltage. The instantaneous voltage goes below the compound forward-biased voltage drop (V_{BE}) of the Darlington-pair (approximately $1.2-1.4$ V), twice during each half cycle, which is indicated in the shaded region in Figure 3.14. The voltages indicated in this region locate at the knee point of the transistor i-v characteristic curve shown in Figure 3.13, which give rise to non-linear distortions at very low supply voltages less than V_{BE}.

The effect of diode non-linearities can be seen in the output waveforms as cross-over distortions of the output sinusoid as illustrated in Figure 3.15. These output voltage waveforms were captured using Tektronix 2024, isolated channel oscilloscope at different voltage levels.

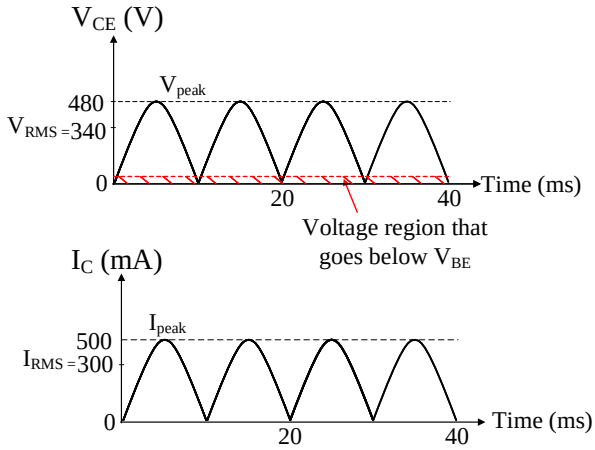
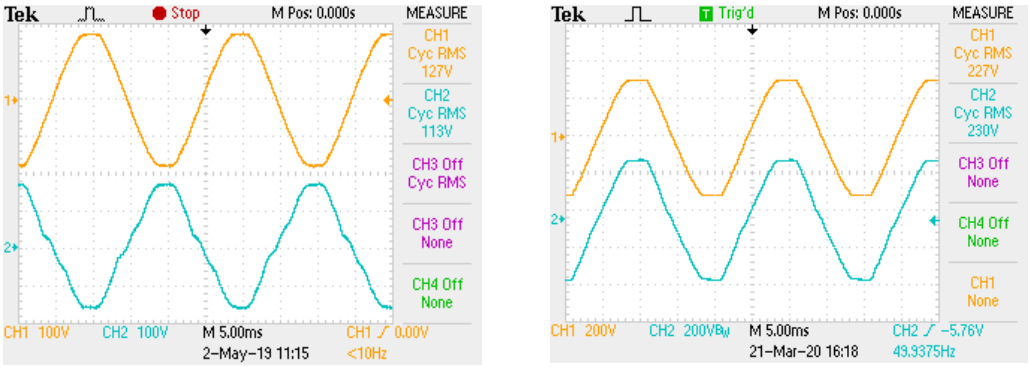


Figure 3.14: Rectified waveforms across the Darlington-pair



(a) (b)

Figure 3.15: Waveform distortion at different output voltages (a) at 115 V (b) at 230 V; the yellow and blue traces indicate input and output respectively

The Darlington pair characteristics under the low voltages and currents was observed using a test setup using bench power supplies as illustrated in Figure 3.16. The Darlington pair was supplied by a $0-30$ V variable power supply and a variable voltage is supplied at the compound base-emitter junction using an optoisolator. In this setup, the maximum collector current conducts into the Darlington pair is approximately equals to the peak value it receives in the actual AC operation. A series of tests were carried out at different voltages across collector-emitter terminals. Figure 3.17 illustrates the obtained results.

During low collector current, the Darlington pair drives into cut-off region whereas when the collector current increases, the compound transistor enters into saturation. In between these two extremes, during the active region, the Darlington operation exhibits approximately constant current gain.

The main purpose of the above experiment is to observe the behaviour of the Darlington pair, during the application of a variable collector current which emulates its actual operation under AC. By analysing the results, it can be concluded that the Darlington transistors can be operated in all three modes. One

important observation is that in the output waveform shows in Figure 3.15, the waveform distortion is only visible close to the cross over points whereas, the shape of the voltage peaks has not been distorted; which implies that only the non-linearity during the low collector current has an impact on the output waveform distortion. This concludes that the Darlington pair does not goes into saturation upon the application of a rectified sinusoidal current waveform but it traverses the cut-off region. More precise data is required to validate these results.

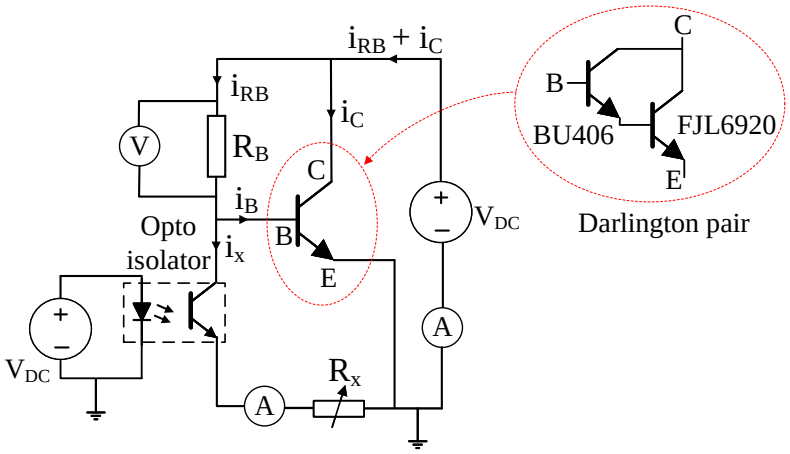


Figure 3.16: Experiment setup used to determine h_{FE} vs I_C under DC

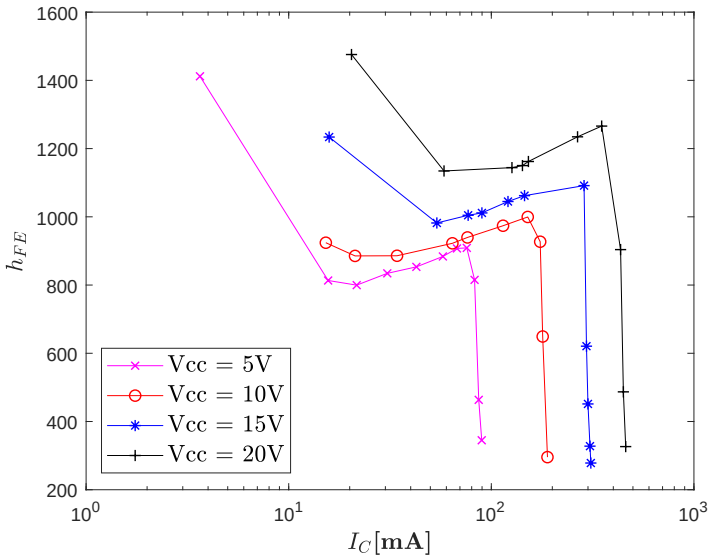


Figure 3.17: Experimental curves for current gain vs collector current

In an attempt to analyse the Darlington pair behaviour in its actual operation, where the instantaneous rectified voltage changes from 0 to $340\sqrt{2}$ V_{RMS}, the above experiment needs to be re-modelled by supplying a high DC voltage equals to the worst-case peak voltage that appears across the collector-emitter terminals, during its AC operation. But the experiment was restricted by unavailability of high voltage capable power supplies.

Alternatively, dynamic characteristics of the Darlington pair was tested by supplying a rectified voltage using a variable transformer (variac) and a diode bridge. The experimental set up and the resultant

phasor plots are given in Appendix B. The phasor plot illustrated in Figure B.2 that is generated from the rectified collector-emitter voltage (in x-axis) and collector current (in y-axis), determines the dynamic collector-emitter resistance (R_{CE}) during the operation.

The average collector-emitter resistance (R_{CE}) during the low voltage supply is very small compared to the average R_{CE} over the entire half cycle of the rectified waveform. Therefore, its non-linearity can be neglected compared to its linear behaviour over a entire half cycle. Based on this conclusion, the derivation of the transistor parameters discussed in Section 3.2 can be treated as valid approximations in a designers point of view.

A detailed discussion of non-linear effects is beyond the scope of this thesis and postgraduate research work is in progress.

3.4 Implementation Aspects of the Control Circuit

Section 3.2 discusses the essentials of the series impedance control. This section focus on the details of the control circuit implementation.

The control circuit works according to the feedback from the regulator output. Based on this feedback signal, the control circuit can manipulate the power transistor array to vary its effective impedance from near zero to near infinity. Not only the control signal but also it possesses the necessary galvanic isolation between the high power handling components such as the transformer and the power transistor array and the low power electronic components in the control circuit (see Appendix A). Figure 3.18 builds up the overall mechanism of the control circuit and the functionality of the key elements in each block and is described now.

Figure 3.18 shows an implementation of a 230 V, 50 Hz linear AC regulator. This block diagram illustrates the key operations for RMS output voltage control:

(a) AC sampling circuit extracts a sample from the regulator output with electrical isolation

(b) RMS/DC converter IC converts the output AC sample into a DC signal

(c) op-amp based amplifier circuit compares the DC signal of the RMS/DC output with a signal from a DC reference source and generates the feedback signal

(d) opto-isolator circuit drives the power transistor array according to the feedback signal to buffer the voltage difference between the output and the input

(e) electrical isolation between the high power transistors and the low power control circuit is achieved using a multi-stage optoisolator.

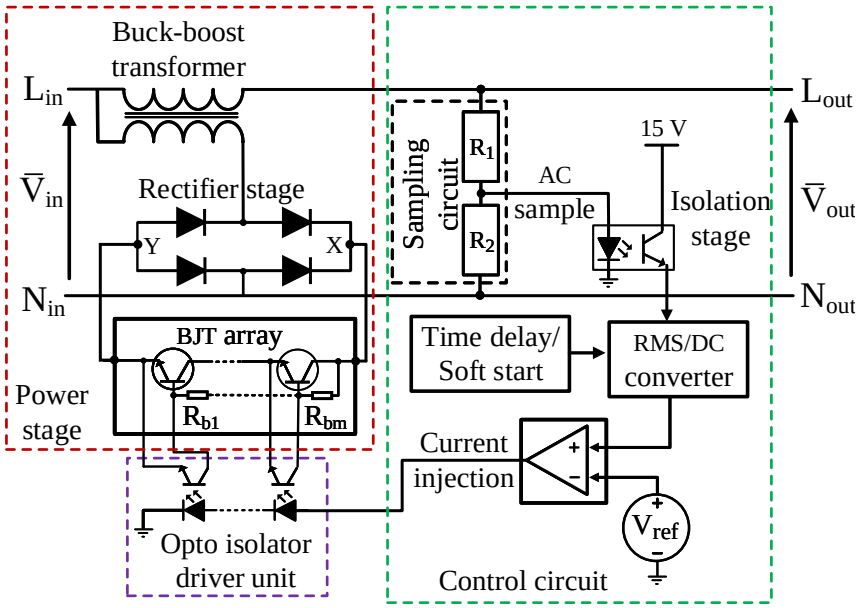


Figure 3.18: Detailed block diagram of linear RMS AC regulator

3.4.1 Sampling Circuit with Electrical Isolation

The control circuit includes an output sensing block that extracts an AC sample and converts the signal into an equivalent DC output by a true RMS to DC converter block. This equivalent DC signal is amplified by an op-amp based amplifier circuit and compared with a DC reference source to produce an error signal that feeds the optoisolator driver unit [41–43].

A sample from the device output is achieved by a potential divider network including R_1, R_2 and VR_1, variable potentiometer as illustrated in Figure 3.19(a) [41, 42]. This extracted signal is then fed to a transistor, Q, where its collector is series-connected to a photodiode of an optoisolator (see [95] for datasheet parameters). So the amplified signal from Q is transferred via the optoisolator into the other circuit blocks of the control unit. The optoisolator stage plays an important role in the digital control circuit by providing necessary galvanic isolation between the high power AC blocks and low voltage control circuit blocks. The DC power supply/voltage regulator block generates a 8.2 V DC source from the AC output power line to provide the required source voltage to power the input sample stage using $D_1 - D_3$ normal and Zener diodes which is illustrated in Figure 3.19(b) [41, 42, 83]. The D_1, LED (light-emitting diode) is used as a visual indicator of the circuit board being powered.

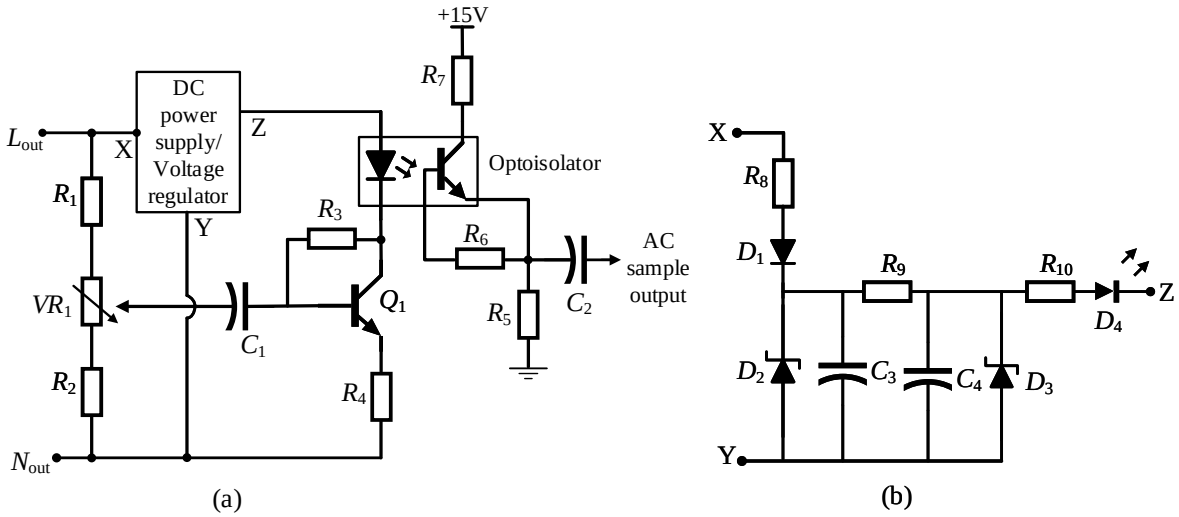


Figure 3.19: AC sampling circuit (a) Output AC sampling circuit (b) DC power supply/ Voltage regulator circuit

The extracted AC sample is fed into a RMS/DC converter unit. The details of the RMS to DC conversion is explained below.

3.4.2 RMS/DC Conversion

In practical sense, the definition for RMS (root mean square) value of a particular AC signal is that, the amount of equivalent DC value, required to produce the same amount of heat in a resistive element, when it is supplied with that particular AC signal. A graphical representation to define RMS voltage of a pure sinusoidal waveforn is illustrated in Figure 3.20.

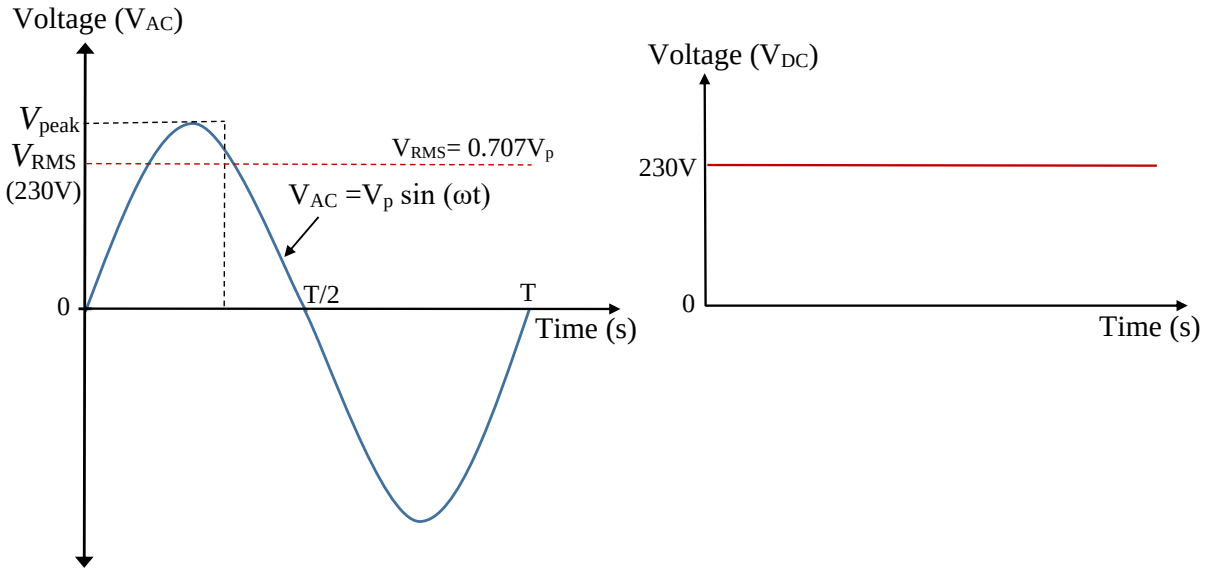


Figure 3.20: RMS/DC converter (a) RMS value of a pure sine wave (b) equivalent DC value

According to Figure 3.20 (a) if the function of the sinusoidal waveform is $Vpsin(\omega t)$, the equivalent RMS value can be written as

$$V_{\text{RMS}} = \sqrt{\frac{1}{T}\int_0^T (V_{\text{p}} \sin \omega t)^2}$$
$$= \frac{V_{\text{p}}}{\sqrt{2}} = 0.707 V_{\text{p}}$$

There are basic two computational methods to calculate an RMS value of a AC voltage [96]: direct or explicit computation and indirect or implicit computation.

Direct/Explicit Computation

Direct RMS computation of a AC signal performs a series of mathematical functions, such as squaring, averaging, and taking the square root using analog multipliers, filters, and operational amplifiers, respectively. High accuracy and excellent bandwidth can be achieved for the final result with a little error of $\pm 0.1\%$. However, this method has a limited dynamic range due to the squaring function, which has to deal with signals of high amplitude, that is impossible to compute. Therefore, the maximum achievable dynamic range for input signals is approximately $10:1$ [96]. Figure 3.21(a) illustrates a block diagram to explain the explicit computation of RMS values extracted from analog devices application note [96].

Indirect/Implicit Computation used by AD536A IC

When implementing the RMS/DC conversion in the control circuit, AD536A RMS/DC converter IC (D-14 package) was selected [96, 97]. This particular IC uses the implicit computation method to achieve a better dynamic range and less price. The implicit computation scheme uses output feedback to perform the squaring function without having to deal with signals of significant amplitude, as shown in Figure 3.21(b). The computation technique is now described.

According to the illustration, the input signal is first processed by a precision rectifier to obtain an absolute value, which drives an op-amp and produces a rectified current output. It is then squared and

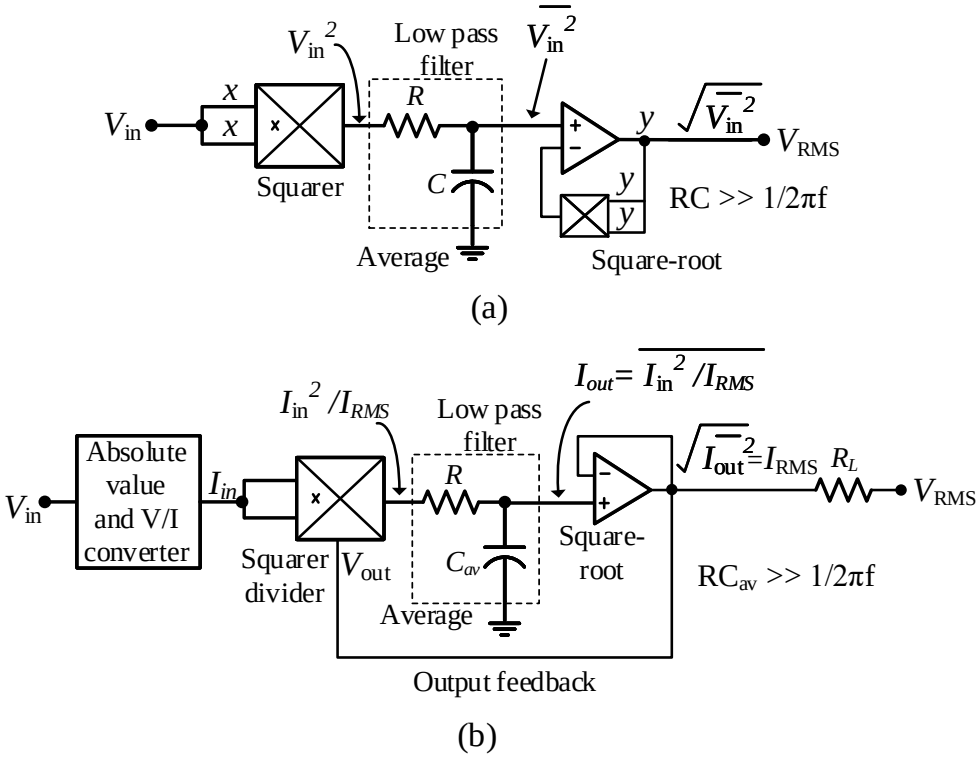


Figure 3.21: Block diagrams of RMS computation (a) direct/explicit method (b) indirect/implicit method

divided at the same time, by utilizing the output feedback. In this method, the multiplier output varies linearly (instead of squaring) with the input RMS signal, which increases the dynamic range of the circuit. The output of the squarer divider stage is then averaged by a low pass filter, including an internal resistor (R_L) and an externally connected filter capacitor (C_{av}). The product of R_L and C_{av} sets the averaging time constant, which should be higher than the longest period of the input signal, for effectively averaging the output current (I_{out}) [96,97]. Figure 3.22 indicates a graph that can be used to select an appropriate value for this capacitor.

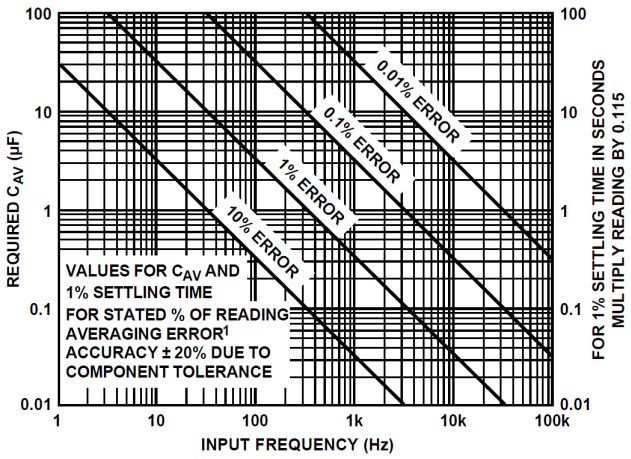


Figure 3.22: Settling time of AD536A

The averaged current is fed into a current mirror circuit block, which provides two outputs (i) the feedback current for the input squarer divider stage and (ii) the output current. Output current is set as twice the feedback current to develop the desired output voltage using an internal resistor (R_{L}) where the IC users have the option of choosing the current output or voltage output (by grounding R_{L}) [96]. The circuit diagram of the RMS/DC converter stage is illustrated in Figure 3.23.

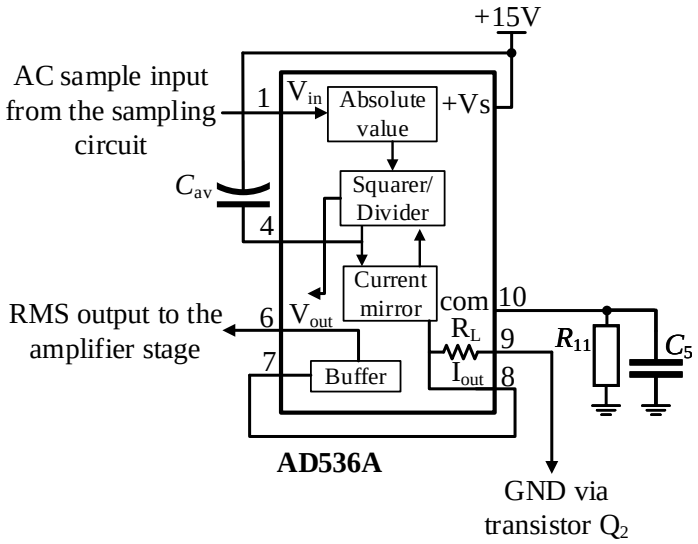


Figure 3.23: AD536A RMS-to-DC circuit configuration

The AD536A RMS-to-DC converter configured for a single supply rail of 15 V and the averaging time constant ($t_{\mathrm{av}} = R_{\mathrm{L}}C_{\mathrm{av}}$) is set to 25 ms (1.25 cycles) for a 50 Hz input by using a 1 μF averaging capacitor. Also, the internal resistor R_L is grounded to achieve an RMS voltage output, which gives an output of 1 V_{DC} per volt RMS input [97].

3.4.3 Time Delay/ Soft Start Circuit

As shown in Figure, the internal resistor R_L is connected to a transistor, Q_2, to prevent any overshooting of the AC output voltage during the start-up. The purpose of this application is described below.

The transistor, Q_2, is connected to a monostable stage that drives Q_2 off for two seconds during the start-up until any possible transients stages are passed. This enables a high DC voltage at the output of the RMS-to-converter, which prevents developing unnecessary voltages at the device output during the start-up.

The monostable multivibrator that was used in this circuit design is dual precision CD14538, that can be triggered either from leading- or trailing-edge of an input pulse, and produces a precise output pulse [98]. Based on the datasheet instructions, the output pulse width, duration and accuracy are determined by the external timing components, R_{x} and C_{x}; output pulse width, t = $R_{\mathrm{x}}C_{\mathrm{x}}$ s. The circuit diagram of time delay/soft start using two monostable stages of CD14538 IC is illustrated in Figure 3.24 [42, 98].

According to the above circuit diagram, the transistor, Q_2 is enabled from the output $\overline{Q_{\mathrm{B}}}$ (in 2^{nd} monostable stage) of a pulse width, $t_1 = 62$ k ohm $\times$ 33 μF ≈ 2 s. In addition, the 1^{st} monostable stage output a pulse of $t_2 = 82$ k ohm $\times$ 1 μF ≈ 0.082 s, to allow a momentary loss of input AC supply approximately 80 ms, before T_1 time delay comes into play.

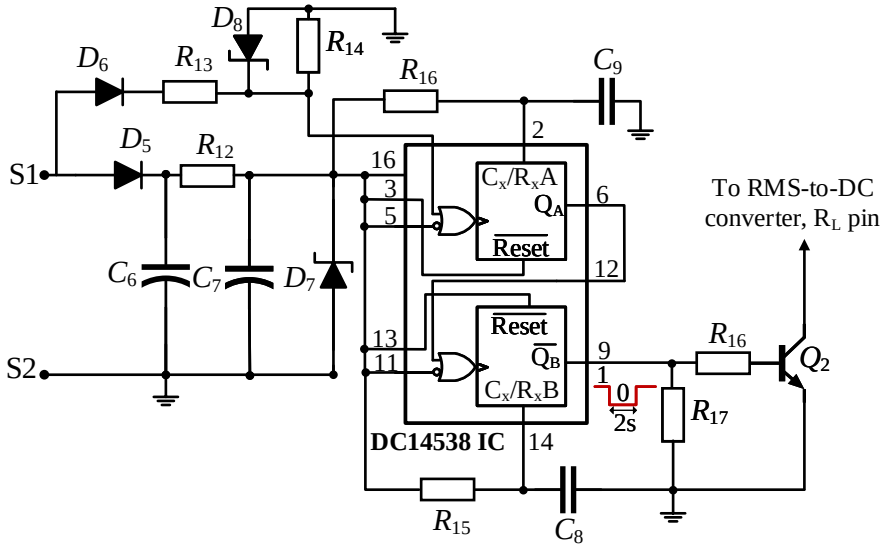


Figure 3.24: Circuit Diagram of time delay/soft start block

3.4.4 Op-Amp Based Amplifier Stage

The DC output of the RMS/DC stage is fed to a amplifier circuit which compares the output sample with a DC reference source (MC1403 Bandgap reference IC) which is a fraction of the desired RMS output voltage. Then it generates an error signal corresponding to the difference between the unrated RMS AC sample and the reference value that drives the quad optoisolator stage for impedance control as discussed in Section 3.2.

The amplifier circuit is illustrated in Figure 3.25. In this circuit application, the op-amp design is based on the assumption that it operates in its ideal conditions. The ideal op-amp characteristics are as follows [92, 99],

- infinite input impedance
- zero output impedancem,
- zero common-mode gain
- infinite open-loop gain
- infinite bandwidth

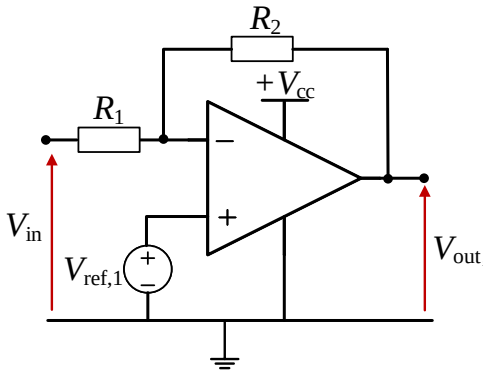


Figure 3.25: Circuit diagram of a differential amplifier

Assuming ideal properties, the relationships of the op-amp circuit in Figure 3.25(a) can be written,

$$V_{\text{in}} - v^{-} = IR_1 \tag{3.28}$$

$$v^{+} - V_{\text{out}} = IR_2 \tag{3.29}$$

for infinite input impedance,

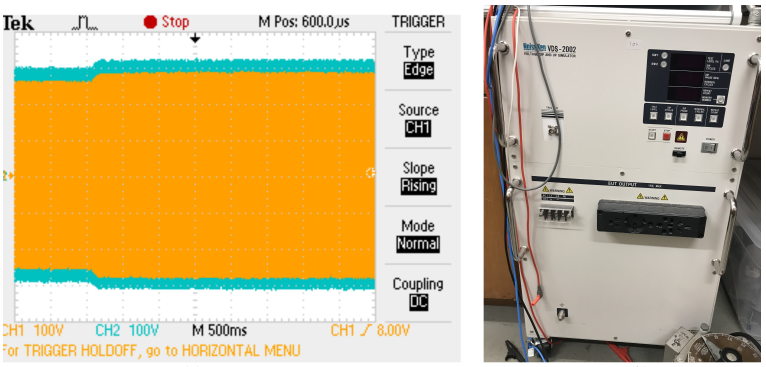
$$v^{+} = v^{-} = V_{\text{ref}}$$

$$\frac{V_{\text{in}} - V_{\text{ref}}}{R_1} = \frac{V_{\text{ref}} - V_{\text{out}}}{R_2} \tag{3.30}$$

$$V_{\text{out}} = \left(1 + \frac{R_2}{R_1}\right) V_{\text{ref}} - V_{\text{in}} \frac{R_2}{R_1} \tag{3.31}$$

The output current of the op-amp stage is adjusted as per the above relationships to control the optoisolator stage that can be driven from cut-off to saturation, in order to vary the transistor array impedance as required. References [100, 101] provides datasheet parameters of the optoisolator and the band gap reference ICs.

The time response of the control circuit discussed in this chapter is illustrated in Figure 3.26 (a) captured using a TPS 2024 isolated channel oscilloscope for a voltage dip of 200 V. According to the osillogram, the response time is approximately 150 ms.



(a) (b)

Figure 3.26: Response time of the control circuit (a) Response time (b) Noiseken dip and swell simulator

In this project, voltage dips and swells are generated using a Voltage Dip and Swell Simulator of type VDS-2002 (Noisken Laboratory Co. Ltd, Sagamihara, Japan), as illustrated in Figure 3.26 (b). The device perform voltage dip, swell, interruptions and variation tests in a manner which is complaint with the IEC standard of IEC 61000-4-11 (2020), setup by International Electromechanical Commission (IEC). IEC 61000-4-11 (2020) stands for testing and measurement techniques-voltage dips,short interruptions and voltage variation immunity tests for equipment with input current up to 16 A per phase [102].

In summary, this chapter discussed the implementation details of two significant elements of the linear voltage regulator, such as the variable impedance and the feedback control circuit. It is also discussed in brief, the diode non-linearities present in the transistor array and how it affects to the output waveform characteristics. The next chapter details the operation of the buck-boost transformer during boost and buck operation based on the behaviour of the variable impedance that is controlled by the feedback circuit.

Chapter 4

A Summary of Transformer Fundamentals and Reduced Efficiency Issue of the Linear AC Regulator

As indicated in Chapter 3, the linear AC regulator technique is based on a line frequency transformer at the centre of the power stage with its primary winding voltage varied by an AC operable variable impedance. Given this case, this chapter provides a summary of essential transformer theory and a discussion on how the efficiency is reduced at higher input AC voltages. Appendix C provides the fundamental theory of the transformer magnetics and the basic equations related to the magnetic properties of the transformer.

4.1 Summary of Transformer Theory Applied to a 50 Hz Transformer

An illustration in Figure 4.1 represents the construction of an ideal transformer containing a ferromagnetic core and two independent windings of N_p and N_s turns. When a sinusoidal voltage ($v_{\mathrm{p}} = V_{\mathrm{p,peak}} sin(2\pi f)$) of frequency, f, is applied across one winding, a sinusoidal current (i_{e}) flows through the winding. According to the Faraday's law, as explained above, the time-varying current causes a sinusoidal flux ($\Phi = \Phi_{\mathrm{peak}} sin(2\pi f)$) generation in the transformer core that induces a time-varying EMF, e_{p}, across that winding. Lenz's law states that this induced EMF (e_{p}) opposes v_{p}, thereby limits i_{e} [105–107]. Due to the flux, Φ being linked with the secondary winding, an EMF is induced in the secondary winding (e_{s}) as illustrated in Figure 4.1. For an ideal transformer operation,

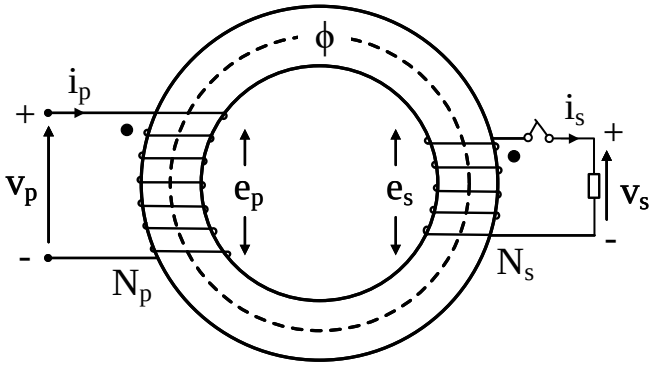


Figure 4.1: Physical geometry of a standard two-winding transformer

$$v_{\mathrm{p}} = -e_{\mathrm{p}} = -N_{\mathrm{p}}\frac{d\Phi}{dt} \tag{4.1}$$

$$v_{\mathrm{s}} = -e_{\mathrm{s}} = -N_{\mathrm{s}}\frac{d\Phi}{dt} \tag{4.2}$$

By eliminating the core flux, Φ yields,

$$\frac{e_{\mathrm{p}}}{N_{\mathrm{p}}} = \frac{e_{\mathrm{s}}}{N_{\mathrm{s}}} \tag{4.3}$$

When the switch of the secondary side is closed, a load current flows through the secondary winding, i_{s} as indicated in Figure 4.1. Transformer turns ratio (n), is defined as the ratio of the primary number of turns to the secondary number of turns, as indicated below,

$$\frac{e_{\mathrm{p}}}{e_{\mathrm{s}}} = \frac{N_{\mathrm{p}}}{N_{\mathrm{s}}} = n \tag{4.4}$$

For a maximum flux density of $B_{\max}$ and the core cross-sectional area is A, the RMS voltage ($\overline{E}_{\mathrm{p}} = e_{\mathrm{p,peak}}/\sqrt{2}$) induced in the primary winding can be derived from (4.1) and yields,

$$\overline{E}_{\mathrm{p}} = 4.44 B_{\max} N_{\mathrm{p}} A f \tag{4.5}$$

Please note that, the rest of the chapter discusses the RMS equivalent of the transformer parameters denoted by an over-bar symbol.

According to the magneto-motive force of the transformer in Figure 4.1 indicates [103],

$$MMF = N_{\mathrm{p}} i_{\mathrm{p}} + N_{\mathrm{s}} i_{\mathrm{s}} \tag{4.6}$$

Since $F = \Phi\Re$, (4.6) becomes,

$$\Phi\Re = N_{\mathrm{p}} i_{\mathrm{p}} + N_{\mathrm{s}} i_{\mathrm{s}} \tag{4.7}$$

In an ideal transformer, we assume the permeability of the core is infinite which implies that the magnetic reluctance of the core is zero and that there's no core losses and resistive power losses in the windings [103, 107]. Therefore, the relationship in (4.7) becomes, $N_{\mathrm{p}} i_{\mathrm{p}} + N_{\mathrm{s}} i_{\mathrm{s}} = 0$. This relationship was utilized by the multiple-winding transformer regulator, to realize the induced voltages of the additional transformer windings and the technique is discussed in detail in Chapter 6.

As the applied terminal voltage of the primary winding varies, the magnetic field in the core varies, leading a variable induced voltage at the secondary terminals. This concept is used by the linear AC regulator illustrated in Figure 4.2 and the relationship between the transformer parameters are discussed now.

Assuming an ideal condition of the transformer operation where there are no any power losses, the transformer input power ($\overline{V}_{\mathrm{p}}\bar{I}_{\mathrm{p}}$) is equals to the transformer output power ($\overline{V}_{\mathrm{s}}\bar{I}_{\mathrm{s}}$), thus,

$$\overline{V}_{\mathrm{p}}\bar{I}_{\mathrm{p}} = \overline{V}_{\mathrm{s}}\bar{I}_{\mathrm{s}} \tag{4.8}$$

$$\frac{\overline{V}_{\mathrm{p}}}{\overline{V}_{\mathrm{s}}} = \frac{\bar{I}_{\mathrm{s}}}{\bar{I}_{\mathrm{p}}} = n \tag{4.9}$$

According to the circuit configuration shown in Figure 4.2, as the secondary winding conducts the load current, $\bar{I}_{\mathrm{L}}$, the current relationship given in Eq.4.9 can be written as

$$\bar{I}_{\mathrm{p}} = \frac{\bar{I}_{\mathrm{L}}}{n} \tag{4.10}$$

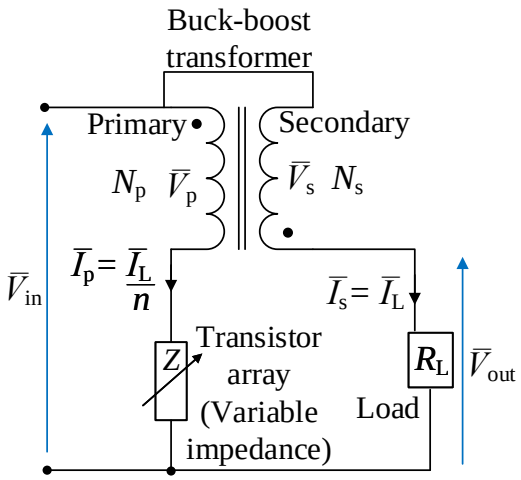


Figure 4.2: Basic circuit diagram of linear AC voltage regulator

Given that the transformer primary winding is connected in series to the transistor array as illustrated in Figure 4.2, the current, $\bar{I}_L/n$ conducts through the series arrangement of the transistor array and the primary winding. In addition, the effective input voltage, $\overline{V}_{in}$, is applied across the primary winding and the transistor array given that $\overline{V}_{in} = \overline{V}_p + \overline{V}_{array}$. By satisfying this relationship, the effective primary voltage can be manipulated in accordance with any variation done to the transistor-array voltage drop, V_{array}. This is the basic concept employed by the linear AC voltage regulator to achieve the required regulation at the output that is explained in detail in Section 4.2.

4.1.1 Transformer in Real Operation Condition

In a practical scenario, the transformer operation consists of losses categorized as core loss, copper loss and leakage effects in the flux path; therefore upon energizing the transformer primary winding when the secondary is loaded, the primary current establishes flux in the core while supplying core power losses (hysteresis and eddy current) and ohmic-resistive losses (copper losses) in the windings [103, 107]. For analytical purposes, these phenomena are represented in the transformer electrical circuit as equivalent circuit components that describe their behaviour in application of primary current when the transformer is loaded. Thus, components of a transformer equivalent circuit is described now.

The net magneto-motive force (mmf) of a transformer core can be related to the core reluctance, we can write

$$\Phi = \frac{N_1 i_1 + N_2 i_2}{\Re} \tag{4.11}$$

The core reluctance of an ideal transformer is zero whereas in a practical scenario, it is nonzero. Given that the induced EMF of a transformer winding is $e = N\frac{d\Phi}{dt}$, Eq. (4.11) can be rearranged as below,

$$e_1 = \frac{N_1^2}{\Re}\frac{d\left(i_1 + i_2\frac{N_2}{N_1}\right)}{dt} \tag{4.12}$$

Above equation introduces two terms such as the magnetizing inductance associated with the core reluctance and the magnetizing current referred to the primary side.

magnetizing inductance, $L_{\mathrm{m}} = N_1^2/\Re$;
magnetizing current, $i_{\mathrm{m}} = i_1 + i_2\frac{N_2}{N_1}$.

In loaded condition, the primary current has two components such as the exciting current component and the load component reflected in to the primary ($i_2^{'}$) as illustrated in Figure 4.3.

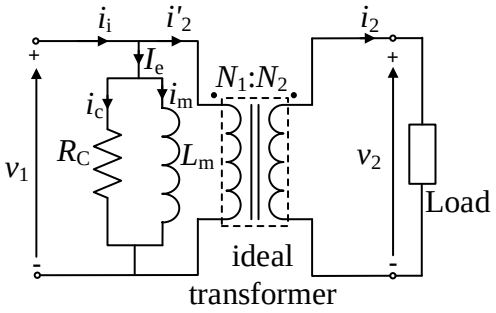


Figure 4.3: Electrical circuit of a real transformer

The exciting current splits into two parts; a true power component i_c, that supply the core loss and a reactive power component i_m that establish the core flux; which is known as the magnetizing current. Core loss is in phase with the applied voltage while the magnetizing current is in phase with the flux in the core which lags the applied voltage by θ° (power factor) [105, 107]. In an electrical circuit of a transformer, the flux in the core is represented by the magnetizing inductance L_{m} in a shunt branch connected across the applied voltage v_1, in parallel, as shown in Figure 4.3 while the core loss component is represented as a resistor R_{c}, parallel to the magnetizing inductance (L_{m}).

Core Loss

Core loss consisting of (a) hysteresis power loss and (b) eddy current loss in the magnetic core which is in phase with the applied voltage [103, 106].

(a) *Hysteresis loss* is caused by the magnetization and demagnetization of the magnetic material of a core as an alternating current flows in the forward and reversed directions as discussed above. It is the energy wasted in the form of heat due to hysteresis due to internal friction of the core that opposes the magnetic domains orientation reversal. The amount of hysteresis loss is given by the total area inside the hysteresis loop illustrated in Figure. C.3 (b) in Appendix C. The equation for hysteresis loss is given by [103],

$$P_h = k_h f V B_{\max}^{\beta} \tag{4.13}$$

where,
P_{h} is the hysteresis loss (W), k_h is the Steinmetz hysteresis coefficient based on the material (j/m^3), f is frequency of magnetic reversal (Hz), V is core volume (m^3), B is the maximum magnetic flux density (Wb/m^2) and β is the Steinmetz exponent based on the material ($\beta = 1.5-2$ for iron cores and $\beta = 2-3$ for ferrite cores) [103, 110].

(b) *Eddy-current loss* is formed due to induced internal voltages inside the core that give rise to circulating internal currents as illustrated in Figure 4.4. Since all ferromagnetic material are conductive, the time-varying flux within the core induces these internal voltages. The eddy-currents flow such

that the resulting magnetic field is opposing the applied field [103]. The eddy-current loss can be expressed as

$$P_e = k_e \frac{f^2 B_{\max}^2}{\rho} \tag{4.14}$$

where,

P_e is the eddy-current loss (W), k_e is the eddy-current loss coefficient , f is frequency of magnetic reversal (Hz), $B_{\max}$ is the maximum magnetic flux density (Wb/m^2), and ρ is the internal resistivity of the core material (Ωm) [103]. Insulated lamination of the core is a favourable method to minimize eddy-current losses.

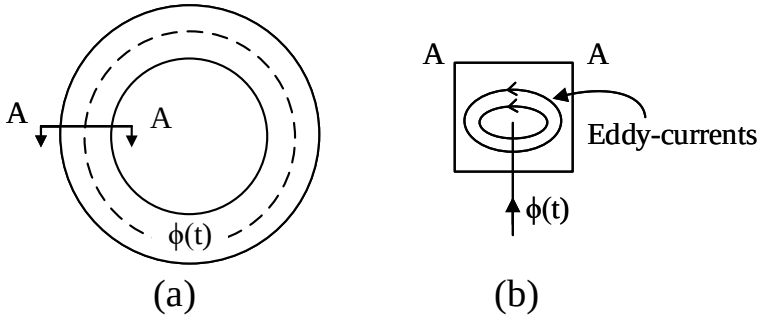


Figure 4.4: Eddy current loss (a) magnetic core (b) eddy-currents in section A-A

Leakage Inductance

In an ideal transformer, the total flux generates within the core links both windings that induce EMF related to the winding turns. In a real transformer, there is always a fraction of the total flux that links only one winding but not the other one. This is called leakage flux which usually leaks through the air as illustrated in Figure 4.5 [103, 104].

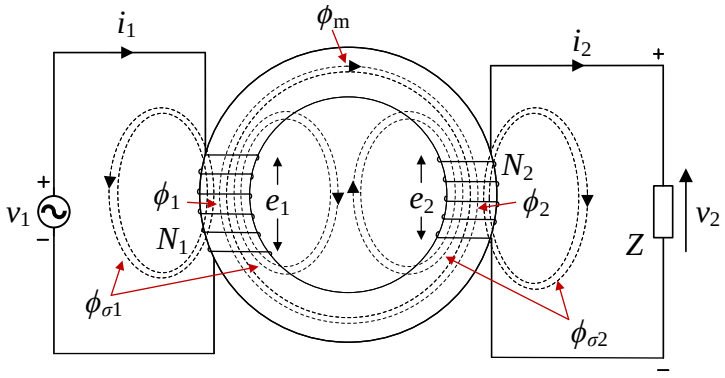


Figure 4.5: Leakage fields in a non-ideal transformer

The leakage flux leads to leakage inductances, $L_{\sigma p}$, $L_{\sigma s}$, of primary and secondary windings and represent as series inductors to the applied voltage in the transformer electrical circuit as illustrated in Figure 4.6 [103, 104]. If $\Phi_{\sigma p}, \Phi_{\sigma s}$ are the leakage flux in the two windings, we can write

$$L_{\sigma 1} = \frac{N_1 \Phi_{\sigma 1}}{i_1} \tag{4.15}$$

$$L_{\sigma 2} = \frac{N_2 \Phi_{\sigma 2}}{i_2} \tag{4.16}$$

Therefore in a practical transformer, the primary and secondary self inductances, L_1, L_2 can be written as an addition of leakage inductance and the magnetizing inductance placed in each side of the transformer [103, 107]. Thus,

$$L_1 = L_{\sigma 1} + L_{\mathrm{m1}} \qquad\qquad L_2 = L_{\sigma 2} + L_{\mathrm{m2}} \tag{4.17}$$

where,

L_{m1} - is the magnetizing inductance placed in the primary side

L_{m2} - is the magnetizing inductance placed in the secondary side.

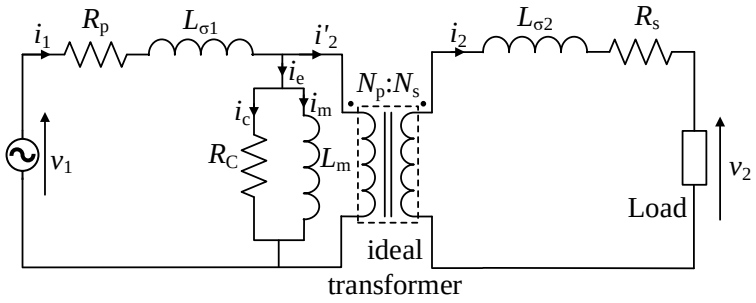


Figure 4.6: Transformer equivalent circuit

Recalling Eq. (C.14), we can write

$$L_{\mathrm{m1}} = M\frac{N_1}{N_2} \qquad\qquad L_{\mathrm{m1}} = M\frac{N_2}{N_1} \tag{4.18}$$

A term called coupling coefficient, k, can be defined to measure the degree of magnetic coupling between the transformer windings that is in the range of $-1 \leq k \leq 1$; k is given by [103],

$$k = \frac{M}{\sqrt{L_1 L_2}} \tag{4.19}$$

Copper-Loss

Transformer windings are conductors associate with an ohmic resistance which is given by

$$R = \frac{\rho l}{A} \tag{4.20}$$

where, ρ is the resistivity of coil material, l is the length of the wire and A is the cross sectional area of the wire.

Transformer windings are usually selected based on the rated current for the application which reflects from the wire gauge; thus, Eq. (4.20) suggests less resistance for higher cross sectional areas that enable high currents through the windings. Since the transformer windings are usually made out of copper, the associated ohmic power loss is known as copper loss which can be calculated as $P_{\mathrm{cu}} = I_{RMS}^2 R$, where the respective winding resistance, R, is represented in series with the applied voltage as shown in Figure 4.6 [103, 107]. The length of the coil is decided based on the core dimension and the required number of turns for the winding.

4.2 Application of a Standard Two-Winding Transformer in Buck- and Boost-Mode Regulation

The basis of the linear AC technique for regulating unrated input line voltage is to achieve a corrective voltage in a transformer secondary winding placed in the input/ output load path, thus, maintain a constant RMS output as discussed in Section 3.1. Linear AC voltage regulator was designed to regulate within a range of unrated input voltage, which is approximately $\pm 20\%$ of $\overline{V}_{\text{out}}$. Accordingly, the regulation criterion of the linear regulator can be categorized under two modes as below,

- Boost mode - when the input voltage is lower than the rated output voltage ($\overline{V}_{\text{in}} < \overline{V}_{\text{out}}$)
- Buck mode - when the input voltage is higher than the rated output voltage ($\overline{V}_{\text{in}} > \overline{V}_{\text{out}}$)

One significant advantage of the linear AC regulator technique is that it allows boost and buck control without any physical change of the transformer winding configuration. This chapter aims to discuss the behaviour of the buck-boost transformer, with respect to boost- and buck-mode operation.

4.2.1 Boost Mode Operation - ($\overline{V}_{\text{in}} < \overline{V}_{\text{out}}$)

Figure 4.7 shows an ideal transformer parameters with respect to boost- and buck-mode operation. The arrows indicate the voltage polarities of each winding. According to the action of the feedback loop, the transistor array is driven from saturation to cut-off to manipulate the winding voltages as described in Chapter 3.

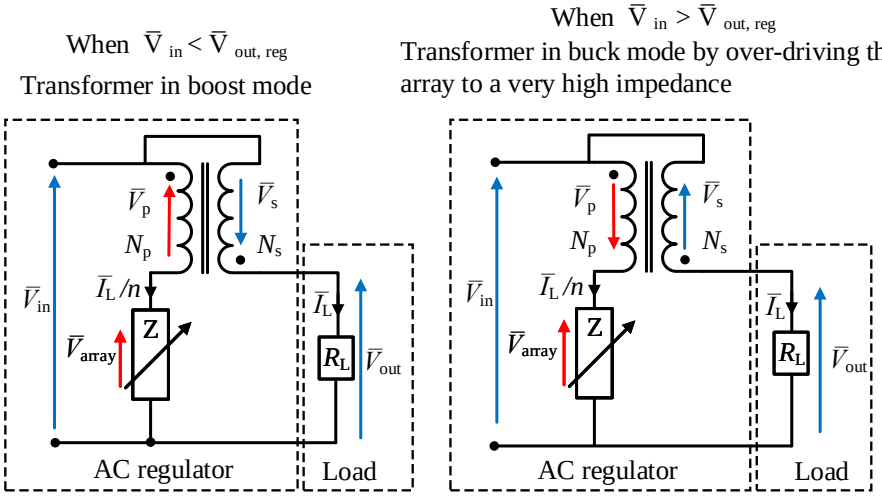


Figure 4.7: Transformer action in (a) boost mode and (b) buck mode

Since the transistor array connects in series to the transformer primary winding, the primary current acts on the transistor array that changes the primary winding voltage, determined by the difference between the input AC voltage $\overline{V}_{\text{in}}$, and the voltage across the array $\overline{V}_{\text{array}}$. Assuming ideal transformer behaviour, transformer action always ensures the relationship between the load current ($\overline{I}_{\text{L}}$) and the primary current ($\overline{I}_{\text{p}}$) as below,

$$\overline{I}_{\text{p}} = \frac{\overline{I}_{\text{L}}}{n} \tag{4.21}$$

where;
$\bar{I}_{\mathrm{L}}$ - load current (is equals to the current flowing through the secondary winding ($\bar{I}_{\mathrm{s}}$))

When the input voltage is below nominal ($\overline{V}_{\mathrm{in}} < \overline{V}_{\mathrm{out}}^{\mathrm{reg}}$) as illustrated in Fig. 4.7(a), the lower input voltage should boost up for regulation. This is done by simply adding an induced secondary voltage $\overline{V}_s$ to the input voltage. This vectorial addition of voltages makes a requirement that the induced secondary voltage should be additive and active in the direction shown in Fig. 4.7(a).

Thus the regulated output ($\overline{V}_{\mathrm{out}}$) in the boost mode operation can be written as

$$\overline{V}_{\mathrm{out}} = \overline{V}_{\mathrm{in}} + \overline{V}_{\mathrm{s}} \tag{4.22}$$

According to Fig. 4.7(a), the relationships of the input, output voltage with the array voltage is given by,

$$\overline{V}_{\mathrm{in}} = \overline{V}_{\mathrm{p}} + \overline{V}_{\mathrm{array}} \tag{4.23}$$

$$\overline{V}_{\mathrm{array}} = \bar{I}_{\mathrm{p}} R_{\mathrm{array}} \tag{4.24}$$

Depending on the control signal from the feedback loop, the transistor array voltage drop can be adjusted from near zero to a very high value. Therefore when the transistor array voltage (V_{array}) is set to desired magnitude by the feedback loop, the transformer primary voltage is automatically adjusted and then it induces the required magnitude of the secondary voltage for boost mode regulation.

The phaser diagram in Fig. 4.8 illustrates the regulation in boost mode. Here we assume the load current ($\bar{I}_{\mathrm{L}}$) is lagging the input voltage ($\overline{V}_{\mathrm{in}}$) by angle ϕ. If the array impedance is purely resistive and the transformer is ideal, based on the relationship in (4.27), the regulator can maintain a constant $\overline{V}_{\mathrm{out}}$ within the arc TT' of the circle with radius $|\overline{V}_{\mathrm{out}}|$. For a given transformer turns ratio, n, the boundaries of the regulation region are the two tangential points, T and T' of the worst case load phase angles of $\pm\phi_{\max}$.

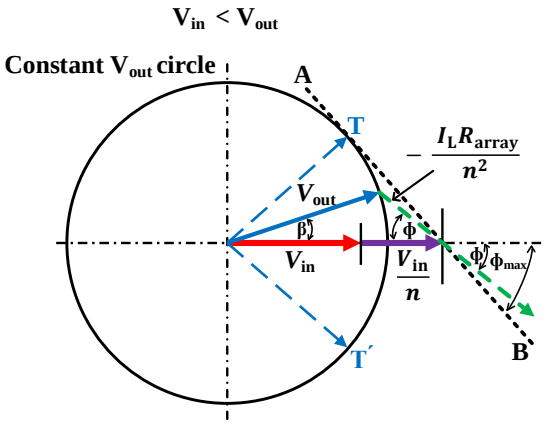


Figure 4.8: Phasor diagram for boost-mode regulation

From Eqs. (4.21) and (4.24) (4.23) becomes,

$$\overline{V}_{\mathrm{p}} = \overline{V}_{\mathrm{in}} - \frac{\bar{I}_{\mathrm{L}}}{n} R_{\mathrm{array}} \tag{4.25}$$

Since $\overline{V}_{\mathrm{s}} = \overline{V}_{\mathrm{p}}/n$, (4.22) can be rearranged as below,

$$\overline{V}_{\mathrm{out}} = \overline{V}_{\mathrm{in}} + \overline{V}_{\mathrm{p}}/n \tag{4.26}$$

By substituting $\overline{V}_{\rm p}$ in (4.26) into (4.25) yields,

$$\overline{V}_{\rm out} = \overline{V}_{\rm in}(1+\frac{1}{n}) - \frac{\overline{I}_{\rm L}}{n^2}R_{\rm array} \tag{4.27}$$

Note that the derivation of (4.27) is a general case when the regulator has a purely resistive load. For a given $\overline{V}_{\rm out}$ and a predetermined n (turns ratio) a constant output voltage is maintained by varying $R_{\rm array}$ appropriately according to different input voltages ($\overline{V}_{\rm in}$).

The condition for maximum efficiency at the minimum input voltage is given by (4.27) where the array is driven into saturation so that the array impedance approaches zero, whereas the power dissipation across the array is ideally zero.

If the transformer turns ratio is configured to achieve an optimum efficiency at the minimum worst-case input voltage, (4.27) simplifies as below ($\overline{V}_{\rm in} = \overline{V}_{\rm in}^{\rm min}$ and $R_{\rm array} \to 0$).

$$\overline{V}_{\rm in}^{\rm min} = \frac{n}{(1+n)}\overline{V}_{\rm out} \tag{4.28}$$

If $\overline{I}_{\rm out} = \overline{I}_{\rm L}$, and $\overline{I}_{\rm in} = \overline{I}_{\rm L} + \overline{I}_{\rm p}$ the overall efficiency (η) of the regulator can be written as,

$$\eta = \frac{n\overline{V}_{\rm out}}{(n+1)\overline{V}_{\rm in}} \tag{4.29}$$

Thus, for a constant output voltage, (4.29) shows the dependency of the optimum regulator efficiency on transformer turns ratio (n) at any input voltage.

The transistor array loss at the minimum input voltage can be calculated using (4.28) and (4.37) as below,

$$\frac{P_{\rm array}^{\rm min}}{P_{\rm out}} = \frac{\overline{V}_{\rm in}^{\rm min}(1+n) - n\overline{V}_{\rm out}}{n\overline{V}_{\rm out}}$$

$$P_{\rm array}^{\rm min} = \frac{n\overline{V}_{\rm out} - n\overline{V}_{\rm out}}{n\overline{V}_{\rm out}}P_{\rm load}$$

$$P_{\rm array}^{\rm min} = 0$$

Above results suggest the following practically useful tips,

1. For a given transformer configuration for maximum efficiency at a particular input voltage and satisfies $(1+n)\overline{V}_{\rm in} = n\overline{V}_{\rm out}$, the power dissipation in the array is minimum;
2. The above statement suggests that by increasing the number of taps in the transformer, we can obtain maximum efficiency under a wide range of input voltages.

4.2.2 Buck Mode Operation - ($\overline{V}_{\rm in} > \overline{V}_{\rm out}$)

In buck operation, the secondary winding should induce an opposing voltage to the input voltage, to regulate the output. Thus the induced secondary voltage should be applied in the reversed direction as indicated by the arrows in Figure 4.7(b). According to the diagram, the relationships of the input and output voltages related to the buck mode operation are given below.

$$\overline{V}_{\rm out} = \overline{V}_{\rm in} - \overline{V}_{\rm s} \tag{4.30}$$

Since the feedback loop is able to drive the transistor array from saturation to cut-off mode where the effective impedance,($Z_{\rm array}$), varies from zero to a very high value, when the input voltage goes beyond

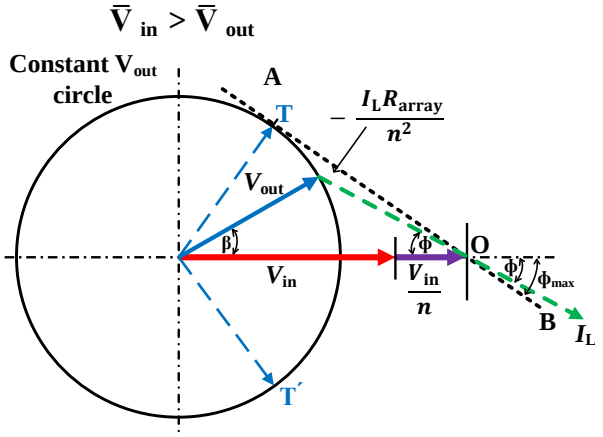


Figure 4.9: Phaser diagram for buck-mode regulation

the nominal value, the feedback loop keep on increasing the transistor array impedance in response to rising input voltage, in order to maintain the regulation at the output. Thus, during buck-mode, the array is driven into a high impedance; pushing the array voltage into a very high value. The relationship between the array and the input voltage in relation to the transformer primary voltage during buck-mode operation is given by,

$$\overline{V}_{\text{in}} = \overline{V}_{\text{array}} - \overline{V}_{\text{p}} \tag{4.31}$$

According to (4.31), a high voltage across the array forcefully reverses the phase of the primary winding voltage ($\overline{V}_{\text{p}}$); thus a phase reversal of the induced secondary voltage. This subtractive secondary voltage allows buck operation without the need to physically change the winding direction. Phaser diagram for the buck regulation is illustrated in Figure 4.9.

When the input voltage keeps on rising towards the highest worst-case scenario, a constant output voltage is maintained by increasing the array voltage from 0 V to a very high value. Lets assume the regulator is designed for an input voltage ranging from 180 V to 260 V and the transformer turns ratio, n, has been realized to cater the lower-worst case scenario, thus $n = 180/50 = 3.6$. If the input voltage has increased up to 260 V, and the output regulation is required at 230 V, we need a buck correction of 20 V (Eq.4.30). From the transformer voltage relationship given in Eq. 4.4, the primary voltage at this situation should be $30 \times 180/50 = 108$ V. In order to achieve 108 volts across the primary winding, the transistor array need to be driven up to $230 + 108 = 338$ V as per Eq. 4.31.

Assuming a load current of 5 A, the transistor array impedance (Z_{series}) can be calculated as $V_{\text{CE}}/\bar{I}_{\text{L/n}} = 338/(5 \times 50/180) = 243.36\ \Omega$. This results in a resistive type power dissipation across the transistor array of approximately $\bar{I}^2_{\text{L/n}} R_t extCE = (5 \times 50/180)^2 243.36 = 470$ W. The power dissipation across the transistor array in any given situation can be realized as below.

Since $\overline{V}_{\text{s}} = \overline{V}_{\text{p}}/n$, (4.31) can be rearranged as,

$$\overline{V}_{\text{array}} = \overline{V}_{\text{in}} + \frac{\overline{V}_{\text{s}}}{n} \tag{4.32}$$

The power delivered by the load can be presented as P_{load},

$$P_{\text{load}} = \overline{V}_{\text{out}} \bar{I}_{\text{L}} \tag{4.33}$$

The power dissipation across the array can be written as,

$$P_{\text{array}} = \overline{V}_{\text{array}} \bar{I}_{\text{p}} \tag{4.34}$$

Substituting (4.32) into (4.34) by replacing $\bar{I}_{\mathrm{p}}$ as per (4.21) yields,

$$P_{\mathrm{array}} = \left(\overline{V}_{\mathrm{in}} + \frac{\overline{V}_{\mathrm{s}}}{n}\right)\frac{\bar{I}_{\mathrm{L}}}{n} \tag{4.35}$$

The division of (4.33) by (4.35) obtains,

$$\frac{P_{\mathrm{array}}}{P_{\mathrm{load}}} = \frac{\overline{V}_{\mathrm{in}} + \frac{\overline{V}_{\mathrm{s}}}{n}}{n\overline{V}_{\mathrm{out}}} \tag{4.36}$$

Simplifying (4.36) by substituting $\overline{V}_{\mathrm{s}}$ from (4.30) brings us,

$$\frac{P_{\mathrm{array}}}{P_{\mathrm{out}}} = \frac{\overline{V}_{\mathrm{in}}(1+n) - n\overline{V}_{\mathrm{out}}}{n\overline{V}_{\mathrm{out}}} \tag{4.37}$$

Assuming a constant output voltage and current, and a fixed transformer turns ratio, the above equation implies that as the input voltage increases, array losses become more significant.

According to the technique described above, the linear regulator is able to regulate under both boost- and buck-modes with a limitation of significant heat dissipation during buck-operation. This issue can be considered as the major drawback of the technique in an attempt to implement it into a commercial product. It also limits the range of the buck-mode operation than the boost-operation due to the fact that it dissipates high amount of energy at higher input voltages, thus, diminish the overall efficiency of the device. Section 4.3 discusses these issues in detail while Section 4.4 introduces two potential solutions that can be adapted to overcome these issues and how it can be extended in to a viable commercial implementation.

Table 4.1 provides the essential theoretical relationships that describe the regulation process of the AC regulator under four distinct operational conditions of input voltage level. From Condition 1 to 4, the desired secondary voltage is obtained by increasing the impedance of the transistor array by driving the transistors from saturation to cut-off.

Table 4.1: Theoretical Relationships of the Transformer Parameters Related to Buck- and Boost-Mode Operation

Voltage levels	**Relationships of original linear AC regulator**	**Comments**
Condition 1 $\overline{V}_{\mathrm{in}} = \overline{V}_{\mathrm{in}}^{\mathrm{min}}$	$\overline{V}_{\mathrm{in}}^{\mathrm{min}} = n\overline{V}_{\mathrm{out}}/(1+n)$ $Z_{\mathrm{array}} = 0\,,\, \overline{V}_{\mathrm{array}} = 0$	Transistor-array saturates
Condition 2 $\overline{V}_{\mathrm{in}} < \overline{V}_{\mathrm{out}}^{\mathrm{nom}}$ (Boost mode)	$\overline{V}_{\mathrm{out}} = \overline{V}_{\mathrm{in}} + \overline{V}_{\mathrm{s}}$ $\overline{V}_{\mathrm{array}} = \bar{I}_{\mathrm{L}}/n \cdot Z_{\mathrm{array}}$ $Z_{\mathrm{array}} > 0$	Transformer secondary acts as a booster
Condition 3 $\overline{V}_{\mathrm{in}} = \overline{V}_{\mathrm{out}}^{\mathrm{nom}}$	$\overline{V}_{\mathrm{array}} = \overline{V}_{\mathrm{in}}^{\mathrm{nom}}$	Transistor-array drives into high impedance No boost/no buck
Condition 4 $\overline{V}_{\mathrm{in}} > \overline{V}_{\mathrm{out}} >= \overline{V}_{\mathrm{in}}^{\mathrm{max}}$ (Buck mode)	$\overline{V}_{\mathrm{out}} = \overline{V}_{\mathrm{in}} - \overline{V}_{\mathrm{s}}$ $\overline{V}_{\mathrm{array}} = \bar{I}_{\mathrm{L}}/n \cdot Z_{\mathrm{array}}$ $Z_{\mathrm{array}} >> 0$	Z_{array} is kept high by the feedback loop by driving the transistor-array into cut-off region

4.3 Drawbacks of the Basic Linear AC Voltage Regulator

The first version of a linear AC voltage regulator was developed in the 1980s, underpinning the concept described in Section 3.1. This regulator was able to operate over a wide range of input voltages from 160 V to 250 V allowing a regulation at 230 VAC. The turns ratio of the transformer used was set to 160/70 to ensure maximum efficiency at the worst case input voltage of 160 V by driving the transistor array into saturation.

Fig. 4.10 shows the efficiency data extracted from this first linear-regulator prototype of 5 A load current capacity as discussed in [42]. As indicated by the graphs, this prototype is able to operate bi-directionally (boost- and buck-mode regulation) over a wide range of input voltages from 160 V to 250 V allowing a regulation at 230 VAC [42]. As shown in the graphs, the efficiency is reduced at higher input voltages due to increasing array losses when driven into high impedance as discussed below.

In a situation where the input voltage reaches a nominal voltage level of 230 V, the correction voltage given by the secondary should be zero. To facilitate this, the control unit adjusts the quantity, $R_{\text{array}}\bar{I}_{\text{L}}/(n^2) = 230 \times 70/160$ (for a resistive load), from which the voltage at the primary side ideally becomes zero. One disadvantage of this particular situation is that, when the input line voltage is 230 V (so does not need regulation), the above prototype still dissipates power in the array; thus, efficiency is diminished as indicated in Figure 4.10. In the case of higher input voltages beyond nominal, regulation is maintained by increasing the effective instantaneous array voltage; thus, array power dissipation becomes more significant and results in a low-efficiency profile. Besides, to compensate for the excessive heat dissipation from the array, a heat sink of high volume needed to be fixed to the power transistors, which added an extra cost for implementation.

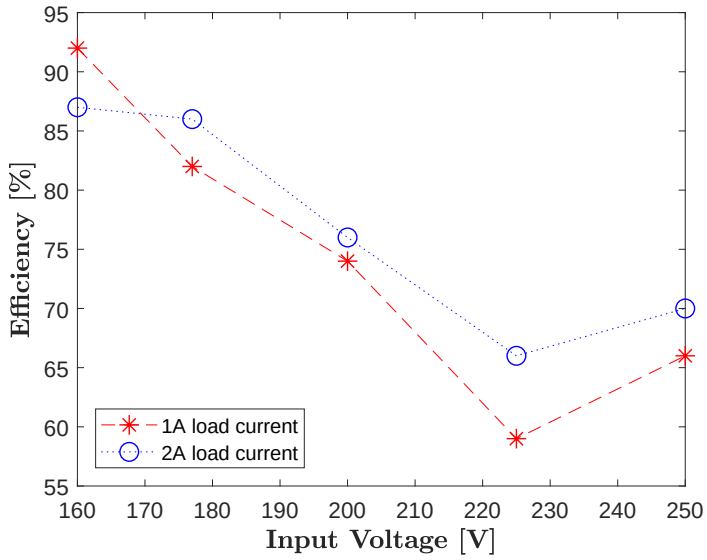


Figure 4.10: Efficiency of the basic linear regulator for 1 kVA prototype adapted from [42]

In summary, the basic linear AC regulator is a suitable replacement for commonly used saturating ferro-resonant regulators and slow responding servo-driven variacs. However, in a commercially useful prototype, its low efficiency at higher input voltages needs to be addressed. This motivates alternative design strategies aimed at efficiency enhancement for higher input voltages.

Figure 4.11 illustrates an alternative configuration to eliminate the extra losses in the transistor array when the input voltage exceeds the nominal line voltage. As shown in the diagram, the two terminals of the secondary winding has been switched, contrary to the configuration demonstrated in Fig. 4.7(a) and (b); therefore the polarity of the induced secondary voltage is applied to the opposite direction, in a subtractive manner, with compared to the polarity indicated in Figure 4.7(a). This winding arrangement allows the transformer to produce the required bucking voltage to regulate in buck mode without driving the array into high impedance. Figure 4.7(b) illustrates the respective phasor diagram, which indicates the operation in buck mode, assuming an ideal transformer and a resistive array impedance.

This technique can be realized by using a set of AC switches to change the configuration between forward and reversed secondary-winding arrangement during boost and buck modes respectively. The major drawback of this implementation is that, assuming an input voltage range of 180 V to 250 V for a 230 V nominal output, the secondary winding should be capable of inducing $0-50$ V during boost-mode and $20-0$ V during buck-mode operation, which means 3 times larger winding than the original implementation to cater both of these situations. Although it seems a good option, this technique needed further improvement before going into commercial implementation. However, this principle has been improved into viable solutions for efficiency enhancement to the original linear technique and presented in detail in Chapters 5 and 6.

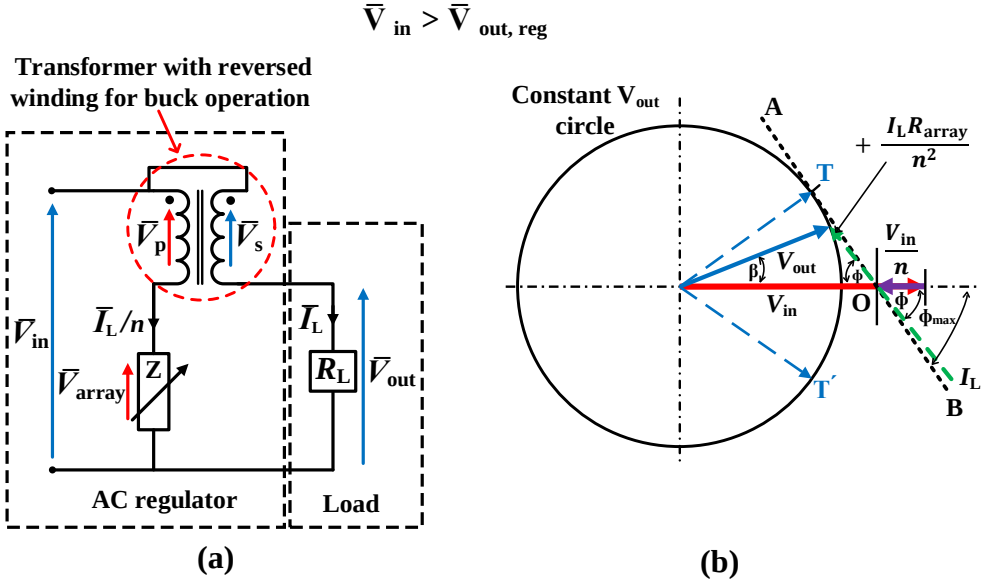


Figure 4.11: An alternative option for a transformer configuration with a reversed winding for buck operation and its phaser diagram

4.4 Suggested Two Techniques for Efficiency Enhancement of the Original Linear AC Voltage Regulator

The original technique discussed in Section 4.2 have the advantage of one single transformer configuration without any tap changes or configuration changes. However, when the input voltage rises above the nominal, larger heat sinks are required, which increases the cost of the commercial product.

By utilizing the concept discussed in Figure 4.11, two potential solutions are proposed to eliminate the reduced efficiency at higher input line voltages such as,

- multi-transformer regulator
- multi-winding transformer regulator

4.4.1 Multi-Transformer Regulator

To achieve voltage-bucking capability with the transistor array operating at lower voltage for good efficiency, we could use two transformers which comes into operation alternatively. This is the case of combining the configurations in Figure 4.7(a) and (b).

Figure 4.12 shows a possible solution that employs two series-connected low-power transformers in which the primary windings are connected in series with two transistor arrays controlled by a feedback circuit. During the change-over from boost to buck, the active regulation shifts from one transformer to the other, with the transformer windings being configured to induce voltages of opposite polarities to allow for boost or buck action. This eliminates the requirement for driving the transistor array into very high impedance, hence minimizing the significant power losses during buck regulation. This new technique employs a mechanism to by-pass the regulating circuit when the input voltage falls within a $\pm 2\%$ tolerance level ($V_{\text{in}} = 225 - 235$ V) of nominal voltage. This will prevent array dissipating power unnecessarily at the input voltage range falls within the accepted level of nominal voltage, avoiding the drop in device efficiency shown in Figure 4.10. Due to the lower cost, availability and easy mass-scale

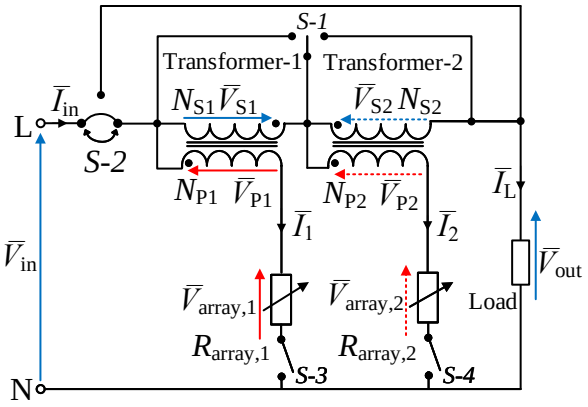


Figure 4.12: Proposed dual-transformer regulator

manufacturing of standard low-power transformers, the dual-transformer approach is the more economical approach for achieving a good overall efficiency. However, in a commercial product, requiring two separate transformers is not optimal due to practical issues such as transformer-beating. Hence the commercial partner of this project required the research team to consider a single-transformer solution for efficiency improvements.

4.4.2 Multi-Winding Transformer Regulator

In order to eliminate the constraints of the dual-transformer approach while achieving an efficiency enhancement, a novel approach using a single transformer was introduced. This technique employs a step-down transformer with two distinct primary windings which are able to induce voltages of opposite

polarities in the secondary for boost and buck regulation, as indicated in Figure 4.13. To manipulate the two primary windings independently, separate transistor arrays are connected in series with each winding. When the input line voltage falls within $\pm 2\%$ of the nominal voltage ($225 - 235$ V), the regulating circuit

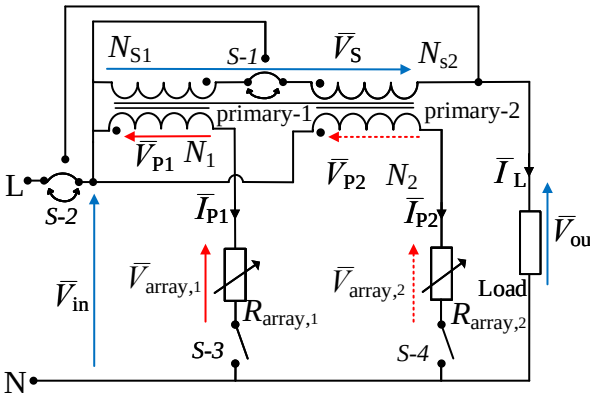


Figure 4.13: Proposed multi-winding transformer regulator

is by-passed as discussed above to allow maximum efficiency at the nominal voltage.

As indicated by the commercial partner of the project, multi-winding approach is more acceptable to single phase commercial products, thus, it has been further improved by incorporating a feedback control circuit to achieve automatic regulation in boost and buck-modes. The more details of these two potential solutions are discussed in detail in Chapters 5 and 6.

Chapter 5

Implementation of a Series Multiple-Transformer Regulator

5.1 An Overview of the Series Multiple-Transformer Approach

The original linear AC voltage regulator discussed in Chapter 4 has the advantage of one single transformer configuration without any tap changes or configuration changes for regulation in boost and buck modes in a wider operational voltages from 160 V – 250 V. However, when the input line voltage rises above the nominal (buck mode operation), power dissipation of the transistor array becomes more prevalent and leading to diminished regulator efficiency as well as creating a need of larger heat sinks that increases the cost of a commercial implementation [41, 42, 81].

When developing the linear AC regulator into a commercially useful prototype, the reducing efficiency during higher voltages should be eliminated and the base technique needs to be modified to achieve competitive efficiency levels compared to traditional RMS voltage regulators. Thus, a new prototype development comes with the following challenges:

1. Enhance the device efficiency during higher input voltages (buck mode operation)
2. Prevent the array from being driven into high impedance during buck regulation
3. Ensure the solution is cost effective for commercial implementation

When addressing above challenges, two unique techniques were proposed and tested, such as (i) multi-transformer and (ii) multi-winding transformer. This chapter discusses the multi-transformer based solution.

To achieve voltage-bucking capability with the transistor array operating at lower voltage for good efficiency, we could use two transformers which comes into operation alternatively [108, 109]. It is important to highlight here that the AC voltage fluctuations in a domestic situation is generally a slow variation, mostly dependent on the loading effects on the relevant local transformer, feeding the household distribution circuit. Therefore, in a dual-transformer operation, the required configuration change-overs are very infrequent.

Figure 5.1 shows the circuit configuration employing two series-connected low-power transformers in which the primary windings are connected in series with two transistor arrays controlled by a feedback circuit. In this design, the secondary windings of two transformers are connected in series to the input/output load path. This configuration allows induced secondary voltage to act as the corrective voltage which could either be additive or subtractive to the input line voltage in order to maintain a constant output voltage. During the change-over from boost to buck, the active regulation shifts from one

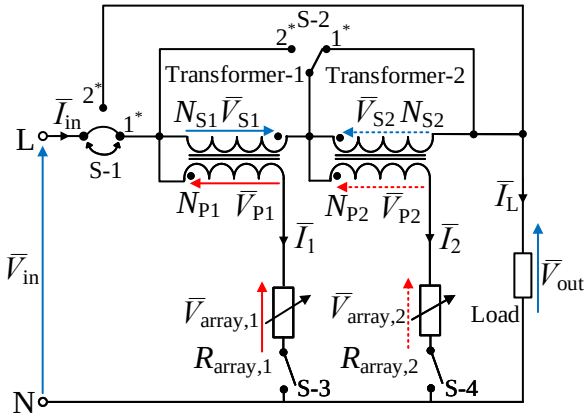


Figure 5.1: Schematic diagram of the series dual-transformer regulator; *Please note that the two positions of switches S1 and S2 are indicated by 1 and 2.

transformer to the other, with the transformer windings being configured to induce voltages of opposite polarities to allow boost or buck action.

As indicated by the dots, Transformer-2 is connected in reversed-direction to Transformer-1 which enables subtractive voltage to be induced in the Secondary-2 that comes into action during the buck mode [108,109]. This eliminates the requirement for driving the transistor array into very high impedance, hence minimizing the significant power losses during buck regulation [108, 109]. Operation of the two distinct transformers corresponding to boost and buck modes will be described in detail in a later section.

5.1.1 Operation Principle of the Dual-Transformer Regulator

In order to obtain a general relationship for the above transformer configuration, lets first assume that both transformers are simultaneously operating as illustrated in Figure 5.2.

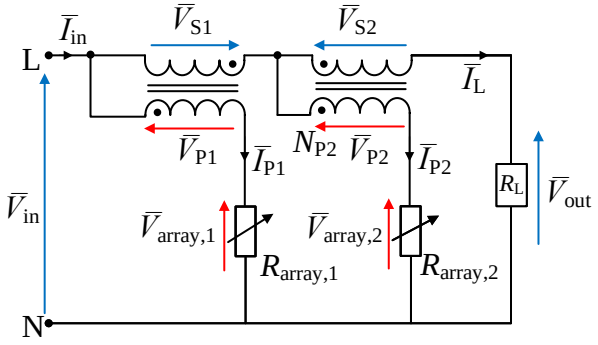


Figure 5.2: Dual-transformer series operation

If the induced secondary voltages are $\overline{V}_{s1}$ and $\overline{V}_{s2}$, the regulated output is given by,

$$\overline{V}_{out} = \overline{V}_{in} + \overline{V}_{s1} \pm \overline{V}_{s2} \tag{5.1}$$

The ($\pm$) sign denotes the voltage polarity induced in the windings of Transformer-2. Other basic relationships between the transformer parameters and the array voltages are as follows,

$$\overline{V}_{in} = \overline{V}_{p1} + \overline{V}_{array,1} \tag{5.2}$$

$$\overline{V}_{\text{in}} + \overline{V}_{\text{s1}} - \overline{V}_{\text{p2}} = \overline{V}_{\text{array,2}} \tag{5.3}$$

Assuming ideal transformer properties, the primary and secondary voltages are related to the number of turns of the two windings (N_p, N_s respectively) as follows,

$$\frac{\overline{V}_{\text{p}}}{\overline{V}_{\text{s}}} = \frac{N_p}{N_s} = n \tag{5.4}$$

Now lets consider the situation where the Transformer-2 is reversely connected to produce a voltage of negative polarity which is subtractive to the input voltage. Under this situation Eq. (5.1) and Eq. (5.3) can be rearranged using Eq. (5.4) as below,

$$\overline{V}_{\text{out}} = \overline{V}_{\text{in}} + \frac{\overline{V}_{\text{p1}}}{n_1} - \frac{\overline{V}_{\text{p2}}}{n_2} \tag{5.5}$$

$$\overline{V}_{\text{in}} + \frac{\overline{V}_{\text{p1}}}{n_1} - \overline{V}_{\text{p2}} = \overline{V}_{\text{array,2}} \tag{5.6}$$

Eqs. (5.2) and (5.6) can be substituted into (5.5) and yields,

$$\overline{V}_{\text{out}} = \overline{V}_{\text{in}} + \frac{1}{n_1}(\overline{V}_{\text{in}} - \overline{V}_{\text{array,1}}) - \frac{1}{n_2}(\overline{V}_{\text{in}} + \overline{V}_{\text{s1}} - \overline{V}_{\text{array,2}})$$

$$\overline{V}_{\text{out}} = \overline{V}_{\text{in}}\left(1 + \frac{1}{n_1} - \frac{1}{n_2}\right) - \frac{\overline{V}_{\text{array,1}}}{n_1} - \frac{\overline{V}_{\text{s1}}}{n_2} + \frac{\overline{V}_{\text{array,2}}}{n_2}$$

$$\overline{V}_{\text{out}} = \overline{V}_{\text{in}}\left(1 + \frac{1}{n_1} - \frac{1}{n_2}\right) - \frac{\overline{V}_{\text{array,1}}}{n_1} - \frac{\overline{V}_{\text{p1}}}{n_1 n_2} + \frac{\overline{V}_{\text{array,2}}}{n_2}$$

$$\overline{V}_{\text{out}} = \overline{V}_{\text{in}}\left(1 + \frac{1}{n_1} - \frac{1}{n_2}\right) - \frac{\overline{V}_{\text{array,1}}}{n_1} - \frac{1}{n_1 n_2}\left(\overline{V}_{\text{in}} - \overline{V}_{\text{array,1}}\right) + \frac{\overline{V}_{\text{array,2}}}{n_2}$$

$$\overline{V}_{\text{out}} = \overline{V}_{\text{in}}\left(1 + \frac{1}{n_1} - \frac{1}{n_2} - \frac{1}{n_1 n_2}\right) - \overline{V}_{\text{array,1}}\left(\frac{1}{n_1} - \frac{1}{n_1 n_2}\right) + \frac{\overline{V}_{\text{array,2}}}{n_2} \tag{5.7}$$

As indicated in Chapter 4 for ideal transformer properties transformer action ensures $\bar{I}_{\text{p}} = \bar{I}_{\text{L}}/n$. Accordingly, two primary winding currents are,

$$\bar{I}_1 = \bar{I}_{\text{L}}/n_1$$
$$\bar{I}_2 = \bar{I}_{\text{L}}/n2$$

Since $\overline{V}_{\text{array}} = \bar{I}_{\text{p}} \times R_{\text{array}}$ Eq. (5.7) simplifies as below,

$$\overline{V}_{\text{out}} = \overline{V}_{\text{in}}\left(1 + \frac{1}{n_1} - \frac{1}{n_2} - \frac{1}{n_1 n_2}\right) - \frac{\bar{I}_{\text{L}}}{n_1}\overline{R}_{\text{array,1}}\left(\frac{1}{n_1} - \frac{1}{n_1 n_2}\right) + \frac{\bar{I}_{\text{L}}}{n_2^2}\overline{R}_{\text{array,2}}$$

Assuming an ideal transformer with no flux leakage or winding resistances, the output of the dual-transformer based approach is given by,

$$\overline{V}_{\text{out}} = \overline{V}_{\text{in}}\left(1 + \frac{1}{n_1}\right)\left(1 - \frac{1}{n_2}\right) - \frac{\bar{I}_{\text{L}}}{n_1^2}R_{\text{array,1}}\left(1 - \frac{1}{n_2}\right) + \frac{\bar{I}_{\text{L}}}{n_2^2}R_{\text{array,2}} \tag{5.8}$$

According to Kirchoffs' current law the current relationship of Figure 5.1 can be written

$$I_{\text{in}} = \bar{I}_{\text{L}} + \bar{I}_1 + \bar{I}_2 \tag{5.9}$$

$$= \bar{I}_{\text{L}} + \bar{I}_{\text{L}}/n_1 + \bar{I}_{\text{L}}/n_2 \tag{5.10}$$

$$= \bar{I}_{\text{L}}\left(1 + \frac{1}{n_1} + \frac{1}{n_2}\right) \tag{5.11}$$

In terms of input/output voltages and the turns ratios, the regulator efficiency can be simplified as below, By using the above expression, the regulator efficiency can be written

$$\eta = \frac{\overline{V}_{\text{out}}\bar{I}_L}{\overline{V}_{\text{in}}\bar{I}_{\text{in}}} \tag{5.12}$$

$$= \frac{\overline{V}_{\text{out}}\bar{I}_L}{\overline{V}_{\text{in}}\bar{I}_{\text{L}}\,(1+1/n_1+1/n_2)} \tag{5.13}$$

$$\eta = \frac{n_1 n_2 \overline{V}_{\text{out}}}{(n_1 n_2 + n_1 + n_2)\overline{V}_{\text{in}}} \tag{5.14}$$

Boost- and Buck-Mode Operation

When two transistors arrays are simultaneously operating, the power dissipation across both arrays will be accountable for determining the overall efficiency of the regulator. In order to yield optimum efficiency for a wide range of input voltages, two transformers are energized alternatively. The distinct operation of the two transformers in boost- and buck mode can be elaborated by Figures 5.3 – 5.5 as follows.

According to the Figure 5.1, the transformer selection is done by using a set of AC switches. Table 5.1 presents the state of the switches S1 to S4 with respect to the mode of operation. This table is used as a reference when describing the regulator operation in boost- and buck-mode, in the following section.

Table 5.1: Truth Table of Switch Operation

Voltage levels		**Switch operation**			
		S1	**S2**	**S3**	**S4**
Condition 1	$\overline{V}_{\text{in}} = \overline{V}_{\text{in}}^{\text{min}}$	1	1	ON	OFF
Condition 2	$\overline{V}_{\text{in}} < \overline{V}_{\text{in}}^{\text{nom}}$	1	1	ON	OFF
Condition 3	$\overline{V}_{\text{in}} = \overline{V}_{\text{in}}^{\text{nom}}$	2	1	OFF	OFF
Condition 4	$\overline{V}_{\text{in}} > \overline{V}_{\text{out}} \geq \overline{V}_{\text{in}}^{\text{max}}$	1	2	OFF	ON

Boost–mode Operation

As illustrated in Figure 5.3, when the input voltage is below the nominal value, Transformer-1 operates and induces the required correction voltage in its secondary winding. According to the dot convention indicated in the Figure 5.3, the correction voltage is additive to the input voltage. Please refer Condition 1 and 2 of Table 5.1, for the switch operation. The relationships of the transformer parameters following the above configuration is given below.

$$\overline{V}_{\text{out}} = \overline{V}_{\text{in}} + \overline{V}_{\text{s1}} \tag{5.15}$$

$$\overline{V}_{\text{in}} = \overline{V}_{\text{p1}} + \overline{V}_{\text{array,1}} \tag{5.16}$$

Given that Transformer-2 is bypassed and can be omitted from the equations, Eq. (5.8) can be simplified into

$$\overline{V}_{\text{out}} = \overline{V}_{\text{in}}\left(1+\frac{1}{n_1}\right) - \frac{\bar{I}_{\text{L}}}{n_1^2}R_{\text{array,1}} \tag{5.17}$$

Whereas the overall efficiency of the regulator is given by Eq. (5.14) as follows,

$$\eta = \frac{n_1 \overline{V}_{\text{out}}}{(n_1+1)\overline{V}_{\text{in}}} \tag{5.18}$$

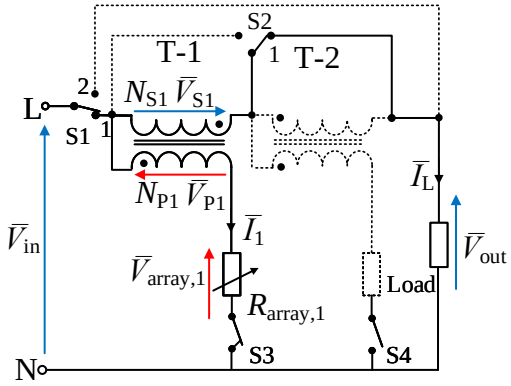


Figure 5.3: Operation of Transformer-1 at boost mode

Above equations Eq. (5.17) and Eq. (5.18) indicates a similar operation to the technique described in Chapter 2 based on a standard single transformer of two windings.

Buck–mode Operation

In the current prototype, the buck-mode is governed by Transformer-2 while Transformer-1 is bypassed as illustrated in Figure 5.4. The switch operation related to the transformer selection is given under Condition-4 of Table 5.1. According to the transformer winding configuration indicated by the dot convention, a subtractive voltage is induced in the Secondary-2 to maintain a constant output voltage. The relationships between the winding voltages and input, output, array voltages are as follows,

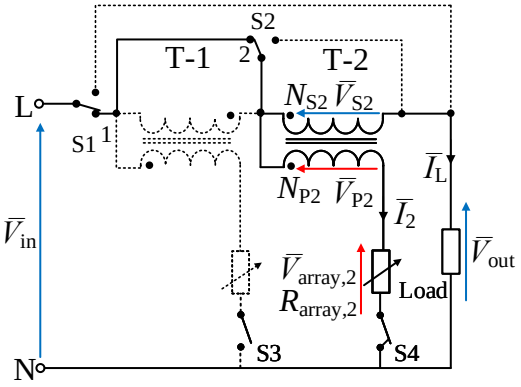


Figure 5.4: Operation of transformer-2 at buck mode

$$\overline{V}_{out} = \overline{V}_{in} - \overline{V}_{s2} \tag{5.19}$$

$$\overline{V}_{in} = \overline{V}_{p2} + \overline{V}_{array,2} \tag{5.20}$$

Similar to boost operation, indicated that Transformer-1 is bypassed ($n_1 \approx \infty$), Eq. (5.8) and Eq. (5.14) become,

$$\overline{V}_{out} = \overline{V}_{in}\left(1 - \frac{1}{n_2}\right) + \frac{\overline{I}_L}{n_2^2} R_{array,2} \tag{5.21}$$

$$\eta = \frac{n_2 \overline{V}_{out}}{(n_2+1)\overline{V}_{in}} \tag{5.22}$$

Regulator Under Nominal Condition

As discussed in Section 4.3, one significant drawback of the basic linear AC regulator was reduced

efficiency when the input line voltage falls within a ±2% tolerance level of nominal voltage due to unnecessary regulation even though it is not required. Therefore, As Table 5.1 indicates under Condition-3, Figure 5.5 illustrates how the regulating circuit has been bypassed to avoid dropping the device efficiency during voltage variations within acceptable levels.

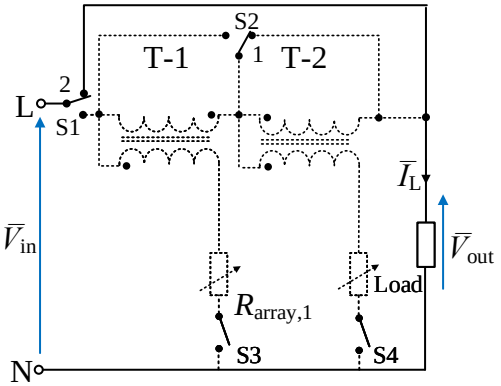


Figure 5.5: Regulator under nominal condition

Although the transistor-arrays remain idle, a small leakage current flows through the Darlington pair that lead to unnecessary power dissipation. This is prevented by mechanically disconnecting the arrays from the loop by switching OFF S-3 and S-4.

Table 5.2 presents the transformer utilization with respect to the mode of operation. Appendix D indicates the relationships of the transformer parameters of the regulator designs presented in this thesis, in relation to the different levels of input voltage.

Table 5.2: Theoretical Relationship of the Transformer Parameters of Dual-Transformer Regulator

Voltage levels	**Relationships of series dual-transformer regulator**		**Comments**
	Transformer-1	**Transformer-2**	
Condition 1 $\overline{V}_{in} = \overline{V}_{in}^{min}$	$\overline{V}_{out} = \overline{V}_{in} + \overline{V}_{s1}$ $Z_{array,1} = 0$ $\overline{V}_{array,1} = 0$	Secondary-2 bypassed	Array-1 saturates
Condition 2 $\overline{V}_{in} < \overline{V}_{nom}$ (Boost mode)	$\overline{V}_{out} = \overline{V}_{in} + \overline{V}_{s1}$ $\overline{V}_{p1} = n_1\,\overline{V}_{s1}$ $\overline{V}_{array,1} = \overline{V}_{in} - \overline{V}_{p1}$ $Z_{array,1} > 0$	Secondary-2 bypassed	$Z_{array,1}$ keeps increasing
Condition 3 $\overline{V}_{in} = \overline{V}_{in}^{nom}$	Secondary windings are bypassed		No boost/no buck
Condition 4 $\overline{V}_{in} > \overline{V}_{out} \geq \overline{V}_{in}^{max}$ (Buck mode)	Secondary-1 bypassed	$\overline{V}_{out} = \overline{V}_{in} - \overline{V}_{s2}$ $\overline{V}_{array,2} = \overline{V}_{in} + \overline{V}_{p2}$ $Z_{array,2} \geq 0$	$Z_{array,2}$ keeps increasing
$\overline{V}_{in} = \overline{V}_{in}^{max}$		$Z_{array,2} = 0$	Array-2 saturates

5.1.2 Calculation of Real Transformer Parameters

When developing the transformer equivalent circuit model for the dual-transformer regulator, illustrated in Figure 5.6, the transformer parameters were tested by performing the short- and open-circuit tests on the line-frequency (50 Hz) toroidal transformer rated at 240 VA referenced to the primary side. The procedure of these two tests are given in Appendix E [103–105, 107, 110].

The measurements taken from these two tests are given in Table 5.3.

Table 5.3: Transformer test data to calculate real transformer parameters

Parameter	**Test Data**	
	Transformer-1 (n=6.7)	**Transformer-2** (n=24)
Short-circuit test		
V_{sc}	16.8 V	11.4 V
I_{sc}	0.97 mA	1.07 A
P_{sc}	16 W	12 W
Open-circuit test		
V_{oc}	199.3 V	237.3
I_{oc}	22 mA	22.8 mA
P_{oc}	3.2 W	3.4 W

Using above data, a sample calculation for Transformer-1 is shown below.

Short-circuit test data are used to calculate the equivalent copper loss ($R_{eq} = R_1 + n_1^2 R_2$) and the equivalent leakage inductance ($L_{eq} = L_\sigma 1 + n_1^2 L_\sigma 2$). Using Eq. (E.1), total impedance,($Z_{eq} = R_{eq} + jX_{eq}$) can be written as

$$Z_{sc} = Z_{eq} = \frac{V_{sc}}{I_{sc}} = \frac{16.8}{0.97} = 17.32\ \Omega \tag{5.23}$$

The copper loss is calculated by Eq. (E.2);

$$R_{eq} = \frac{P_{sc}}{I_{sc}^2} = \frac{16}{0.97^2} = 17.00\ \Omega \tag{5.24}$$

Then the equivalent leakage reactance is given by Eq. (E.4)

$$X_{eq}\sqrt{(Z_{eq}^2 - R_{eq}^2)} = \sqrt{(17.32^2 - 17^2)} = 3.31\ \Omega \tag{5.25}$$

The reactance can be converted in to inductance by dividing from $2\Pi f$, where f is the frequency of the supplied voltage in Hz.

$$L_{eq} = \frac{3.31}{2 \times \Pi \times 50} = 10.5\ mH \tag{5.26}$$

The excitation branch that includes the core loss and the magnetizing inductance is calculated using the open-circuit test data by solving Eqs. (E.7) to (E.9).

The core impedance is given by

$$\begin{aligned} \frac{1}{Z_{oc}} &= \frac{I_{oc}}{V_{oc}} \\ &= \frac{0.02}{199.3} \end{aligned} \tag{5.27}$$

Thus;

$$Z_{oc} = 9965\ \Omega$$

The core-loss resistance is:

$$R_{\mathrm{c}} = \frac{V_{\mathrm{oc}}^2}{P_{\mathrm{oc}}} = \frac{199.3^2}{3.2} = 12412.6\ \Omega \tag{5.28}$$

The magnetizing reactance can be deduced from

$$X_{\mathrm{m}} = \frac{1}{\sqrt{\frac{1}{Z_{\mathrm{oc}}^2} - \frac{1}{R_{\mathrm{c}}^2}}} = \frac{1}{\sqrt{\frac{1}{9965^2} - \frac{1}{12412.6^2}}} = 16.715\ \mathrm{k}\Omega \tag{5.29}$$

Finally, the magnetizing inductance is given by

$$L_{\mathrm{m}} = \frac{16715}{2 \times \Pi \times 50} = 53.2\ \mathrm{H} \tag{5.30}$$

The coupling coefficient of the two transformers can be calculated substituting the transformer parameters computed above. A sample calculation is presented here for the benefit of the reader.

The self-inductance of the primary winding can be calculated by substituting values into Eq. (4.17),

$$L_1 = L_{\sigma 1} + L_{\mathrm{m1}} = 10.5\ \mathrm{mH} + 53.2\ \mathrm{H} = 53.21\ \mathrm{H} \tag{5.31}$$

The mutual inductance, M is given by Eq. (C.14)

$$M = L_{\mathrm{m1}}/n_1 = 53.2\ \mathrm{H}/6.7 = 7.94\ \mathrm{H} \tag{5.32}$$

The secondary self-inductance can be calculated as,

$$\begin{aligned} L_2 = L_{\sigma 2} + L_{\mathrm{m2}} &= 10.5/n_1 + M/n_1 \\ &= 10.5 \times 10^{-3}/6.7 + 7.94/6.7 \\ &= 1.57 \times 10^{-3} + 1.190 \\ L_2 &= 1.2\ \mathrm{H} \end{aligned} \tag{5.33}$$

Thus, the coupling coefficient of Transformer-1, k_1 is

$$\begin{aligned} k_1 &= \frac{M}{\sqrt{L_1 \times L_2}} \\ &= \frac{7.94}{\sqrt{53.21 \times 1.20}} \\ &= 0.99 \end{aligned} \tag{5.34}$$

Following similar computational method coupling coefficient of the Transformer-2 can be calculated and the results are summarized in the Table 5.4.

Transformer Efficiency

With the losses associated with the transformers as computed above, a real transformer possesses less than 100% full-load efficiency. A transformer efficiency at 1A load current is calculated as follows,

$$\begin{aligned} \text{Efficiency at full load }, \eta &= \frac{\text{Output power}}{\text{Input power}} \times 100\% \\ \text{Output power} &= \text{Input power} - \text{Losses} \end{aligned} \tag{5.35}$$

$$\begin{aligned} \text{Losses} &= \text{Core loss} + \text{Copper loss} \\ &= V_p I_e sin\theta + I_1^2 R_{\text{eq}} \\ &= 199.3 \times 21.2 \times 10^{-3} \times sin(42)^\circ + 1/6.7 \times 17.32 \\ &= 2.79 + 0.38 = 3.17 \text{ W} \end{aligned} \tag{5.36}$$

The power factor, $cos\theta$ can be calculated using Eq. (5.40) or measured. When performing these transformer tests, the power factor was measured from the Fluke power analyser and it is 0.73 for Transformer-1 and 0.71 for Transformer-2.

The Transformer-1 efficiency is given by Eq. (5.35)

$$\eta = \left(1 - \frac{\text{Losses}}{V_{\text{in}} I_{\text{in}} cos\theta}\right) = 1 - \frac{3.17}{200 * 1.2 * 0.73} \qquad = 98.1\% \tag{5.37}$$

Following above steps, Transformer-2 efficiency can be computed and it is approximately 97.5%. See Appendix H for the calculation.

5.2 Series Dual-Transformer Equivalent Circuit Analysis

The real transformer parameter deduced above can be used to model the dual-transformer regulator as illustrated in Figure 5.6.

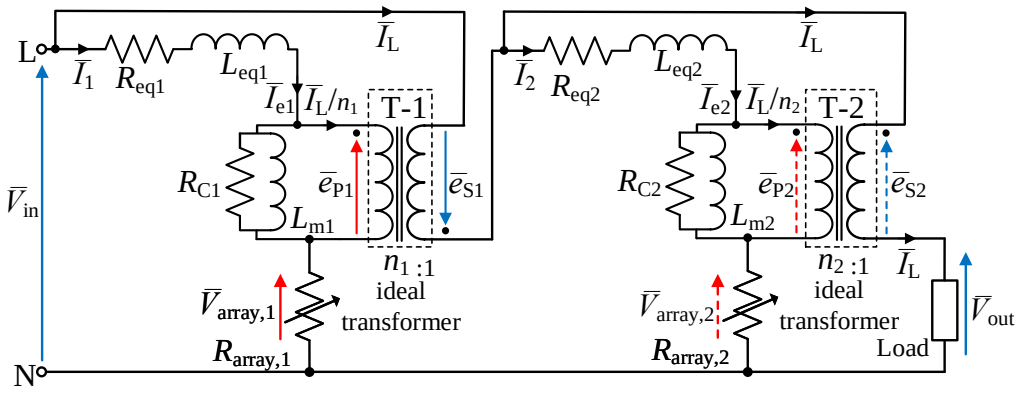


Figure 5.6: Equivalent circuit diagram of the dual-transformer regulator

Table 5.4: Real Transformer parameters

	Calculated values	
Transformer parameters	**Transformer-1** (n=6.7)	**Transformer-2** (n=24)
Primary referred magnetizing inductance, L_M	53.2 H	53.5 H
Primary referred core-loss, R_C	12.4 kΩ	16.6 kΩ
Equivalent leakage inductance, L_{eq}	10.5 mH	6 mH
Primary resistance, r_{p}	4 Ω	5.3 Ω
Secondary resistance, r_{s}	0.3 Ω	0.13 Ω
Excitation current, $\bar{I}_e$	21.2 mA	22 mA
Self-inductance of primary, L_1	53.21 H	53.51 H
Self-inductance of secondary, L_2	1.2 H	92.9 mH
Mutual inductance, M	7.9 H	2.23 H
Coupling coefficient, k	0.99	0.98

Following Figure 5.6, the basic relationships that govern the dual-transformer regulator including real transformer parameters can be written as follows,

$$\overline{V}_{\text{in}} = \overline{e}_{\text{p1}} + \overline{I}_1(Z_{\text{array,1}} - Z_{\text{eq1}}) \tag{5.38}$$

$$\overline{V}_{\text{in}} = \overline{e}_{\text{p2}} + \overline{I}_2(Z_{\text{array,2}} - Z_{\text{eq2}}) - \overline{e}_{\text{s1}} \tag{5.39}$$

where,

$Z_{\text{eq1}} = R_{\text{eq1}} + jX_{\text{eq1}}$; $\quad Z_{\text{eq2}} = R_{\text{eq2}} + jX_{\text{eq2}}$

$X_{\text{eq1}} = 2\pi f L_{\text{eq1}}$; $\quad X_{\text{eq2}} = 2\pi f L_{\text{eq2}}$

Assuming constant magnetizing impedance on loaded conditions, the induced primary voltage ($\overline{e}_{\text{p1}}$) is given by,

$$|\overline{e}_{\text{p1}}| = \overline{I}_{\text{e}}\sqrt{\left(\frac{R_{\text{c1}}^2 X_{\text{m1}}}{R_{\text{c1}}^2 + X_{\text{m1}}^2}\right)^2 + \left(\frac{R_{\text{c1}} X_{\text{m1}}^2}{R_{\text{c1}}^2 + X_{\text{m1}}^2}\right)^2}$$

$$\angle e_{\text{p1}} = \theta = \cos^{-1}\left(\frac{X_{\text{m1}}}{R_{\text{c1}}}\right) \tag{5.40}$$

The regulator output voltage is given by,

$$\overline{V}_{\text{out}} = \overline{V}_{\text{in}} + \overline{e}_{\text{s1}} - \overline{e}_{\text{s2}} \tag{5.41}$$

Due to ideal transformer action $e_{\text{s}} = e_{\text{p}}/n$, thus, Eq. (5.41) can be rearranged into

$$\overline{V}_{\text{out}} = \overline{V}_{\text{in}} + \frac{\overline{e}_{\text{p1}}}{n_1} - \frac{\overline{e}_{\text{p2}}}{n_2} \tag{5.42}$$

Primary winding voltages, e_{p1} and e_{p2} is given by Eqs. (5.38) and (5.39), and these expressions can be substituted into Eq. (5.42) and yields regulator output voltage, $\overline{V}_{\text{out}}$;

$$\begin{aligned}
\overline{V}_{\text{out}} &= \overline{V}_{\text{in}} + \frac{\overline{V}_{\text{in}} - \overline{I}_1 R_{\text{array,1}} + \overline{I}_1 Z_{\text{eq1}}}{n_1} - \frac{\overline{V}_{\text{in}} - \overline{I}_2 R_{\text{array,2}} + \overline{I}_2 Z_{\text{eq2}} + \overline{e}_{\text{s1}}}{n_2} \\
&= \overline{V}_{\text{in}}\left(1 + \frac{1}{n_1} - \frac{1}{n_2}\right) + \frac{\overline{I}_1}{n_1}\left(Z_{\text{eq1}} - R_{\text{array,1}}\right) + \frac{\overline{I}_2}{n_2}\left(Z_{\text{eq2}} - R_{\text{array,2}}\right) - \frac{\overline{e}_{\text{p1}}}{n_1 n_2} \\
&= \overline{V}_{\text{in}}\left(1 + \frac{1}{n_1} - \frac{1}{n_2}\right) + \frac{\overline{I}_1}{n_1}\left(Z_{\text{eq1}} - R_{\text{array,1}}\right) + \frac{\overline{I}_2}{n_2}\left(Z_{\text{eq2}} - R_{\text{array,2}}\right) - \frac{1}{n_1 n_2}\left(\overline{V}_{\text{in}} - \overline{I}_1 R_{\text{array,1}} + \overline{I}_1 Z_{\text{eq1}}\right) \\
&= \overline{V}_{\text{in}}\left(1 + \frac{1}{n_1} - \frac{1}{n_2} - \frac{1}{n_1 n_2}\right) + \frac{\overline{I}_1 Z_{\text{eq1}}}{n_1}\left(1 - \frac{1}{n_2}\right) - \frac{\overline{I}_1 R_{\text{array,1}}}{n_1}\left(1 - \frac{1}{n_2}\right) + \frac{\overline{I}_2}{n_2}\left(Z_{\text{eq2}} - R_{\text{array,2}}\right) \\
\overline{V}_{\text{out}} &= \overline{V}_{\text{in}}\left(1 + \frac{1}{n_1} - \frac{1}{n_2} - \frac{1}{n_1 n_2}\right) + \frac{\overline{I}_1}{n_1}\left(1 - \frac{1}{n_2}\right)\left(Z_{\text{eq1}} - R_{\text{array,1}}\right) + \frac{\overline{I}_2}{n_2}\left(Z_{\text{eq2}} - R_{\text{array,2}}\right)
\end{aligned} \tag{5.43}$$

For a real transformer, the net magneto-motive force is non-zero, thus, $N_p\bar{I}_p - N_s\bar{I}_s = \Phi\Re$ that can be applied to two transformers in Figure 5.6 and simplifies as below.

$$\begin{aligned}
N_1\bar{I}_1 - N_2\bar{I}_2 &= \Phi\Re \\
\bar{I}_1 - \frac{N_2}{N_1}\bar{I}_2 &= \frac{\Phi\Re}{N_1} \\
\bar{I}_1 &= \frac{\Phi\Re}{N_1} + \frac{\bar{I}_L}{n_1}
\end{aligned} \tag{5.44}$$

Since $L_{m1} = N_1^2/\Re$, for Transformer-1 given that N_1 is 293 and L_{m1} is 53.2 H, the core reluctance is given by

$$\Re_1 = \frac{N_1^2}{L_{m1}} = \frac{293^2}{53.2} = 1613.7 \text{ H}^{-1}$$

Using Eq. (4.5), the total flux for rated voltage (200 V) can be calculated.

$$\begin{aligned}\Phi_1 &= \frac{V_{RMS}}{4.44 \times N_1 \times f} = \frac{200}{4.44 \times 293 \times 50} \\ &= 3.06 \times 10^{-}3 \text{ Wb}\end{aligned}$$

Thus, Eq. (5.44) gives Transformer-1 primary current, $\bar{I}_1$

$$\begin{aligned}\bar{I}_1 &= \frac{3.06 \times 10^{-}3 \text{ Wb} \times 1613.7 \text{ H}^{-1}}{293} + \frac{1 \text{ A}}{6.67} \\ &= 0.167 \text{ A}\end{aligned}$$

Following similar steps, Transformer-2 parameters can be computed and the results are given below,
magnetizing inductance, $L_{m2} = 54.1$ H,
transformer primary number of turns $N_3 = 360$,
core reluctance, $\Re_2 = 2395.6 \text{ H}^{-1}$,
total maximum flux at rated voltage (240 V), $\Phi_2 = 3.00 \times 10^{-}3$ Wb,
primary current $\bar{I}_2 = 0.061$ A.

The real transformer parameters calculated above are used to compute the device efficiency during the boost- and buck-mode operation which is discussed in detail in the following sections.

5.2.1 Determination of the Transformer Core Parameters

During the implementation of the dual-transformer regulator, the initial target of the research team was to achieve 1 kW output capacity. To cater this power rating, a toroidal transformer rated at 240 VA, 50 Hz was used in this implementation which can handle maximum of 4 A load current. Compared to the other conventional voltage regulator techniques that utilize a similar transformer rating as the output power rating of the device, the linear technique introduces a significant advantage by reducing the transformer size and its ratings to half of the output rating of the device. During the first prototype implementation of the dual-transformer regulator, aiming at the conceptual implementation and verification of the technique, the device ratings were reduced to 0.5 kW of output capacity.

The toroidal transformers that were used in the current dual-transformer prototype, shown in Figure 5.7 has identical cores with a cross sectional area of 2.49×10^{-3} m^2. According to the total flux calculated for two transformers above, the B-fields at which the cores are operates at are calculated below.

For Transformer-1;

$$B = \Phi_1/A = 3.06 \times 10^{-}3 \text{ Wb}/2.49 \times 10^{-3} \text{ m}^2 \qquad = 1.22 \text{ T} \tag{5.45}$$

For Transformer-2;

$$B = \Phi_2/A = 3.00 \times 10^{-}3 \text{ Wb}/2.49 \times 10^{-3} \text{ m}^2 \qquad = 1.20 \text{ T} \tag{5.46}$$

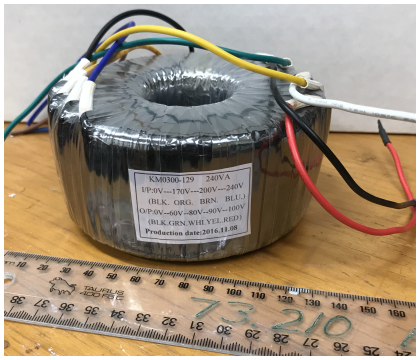


Figure 5.7: Transformer used for this implementation

By considering the maximum B-field values calculated above using the measured transformer parameters, it can be predicted that the transformer has a form of a powdered core. But due to the lack of information, the specific core type cannot be given here.

According to the current specification of the prototype for a maximum load current of 4 A, the optimum winding gauges for the two transformers are given in Table 5.5.

Table 5.5: Transformer Winding Details

Transformer winding	**Rated current (A)**	**Gauge number (awg)**
Transformer-1 (n=6.7)		
Primary	0.6	39
Secondary	4	35
Transformer-2 (n=24)		
Primary	0.16	39
Secondary	4	35

5.3 Simulation and Experimental Results of the Dual-Transformer Regulator

Series dual-transformer is an efficient technique to overcome the low efficiency issue of the basic linear AC regulator due to the role played by the second transformer that governs the buck-mode operation. Figure 5.8 illustrates a comparison of efficiency achieved by the two configurations.

For the dual-transformer design, the transformer turns ratios were selected as $200/30 = 6.67$ and $240/10 = 24$ to suit lower and higher worst-case scenarios. And in the single-transformer design the turns-ratio was $200/30 = 6.67$, which cater the lower worst-case scenario only. It is important to indicate here that the highest possible efficiencies in these cases are limited by the transformer mainly. As shown in Figure5.8, the single-transformer case shows a declining efficiency curve. This is because, when the input voltage is rising, the regulation is maintained by increasing the array-impedance that results in rising effective array-voltage. This leads to ohmic power dissipation in the array which improves with the input voltage and results in degraded overall device efficiency.

On the other hand, the dual-transformer design shows an efficiency improvement at higher input voltages due to the bucking action of the second transformer which eliminate the array being driven into high impedance. The regulator maintains the regulation by shifting the operation of one transformer to

the other when the input voltage transits from boost to buck mode. The switching between transformers is required only when the input voltage drops below the nominal or increases beyond nominal by more than $\pm 2\%$.

The efficiency graph of dual-transformer regulator shows a significant jump in efficiency when the input line voltage reaches the nominal voltage range as both transformers are bypassed such that the input line voltage is directly fed to the load. This strategy is used to eliminate unnecessary energy dissipation across the array at such situations when the regulation is not required. In addition, an improved efficiency is seen at 230 V since Transformer-2 takes over the buck-regulation while short-circuiting the Transformer-1; whereas the Transformer-2 turns ratio was configured to have an optimum efficiency at 240 V. The switching patterns of transformers are described in Table 5.2.

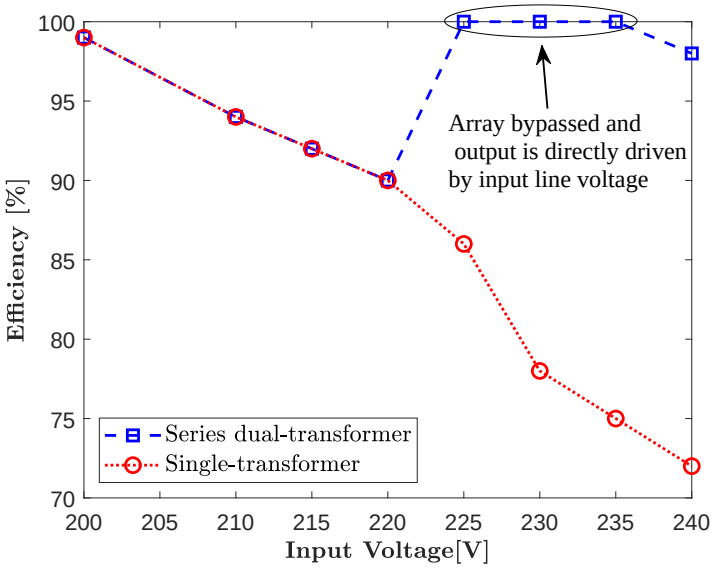


Figure 5.8: Efficiency comparison between the dual-transformer and the original version for 1 A load current

Figure 5.9 shows the efficiencies versus input voltage for the dual-transformer regulator, comparing the measured efficiency versus the two calculated cases. In the graph showing highest performance, the transformer is treated as ideal. In the next case, where the transformer is treated as non-ideal, the efficiency was calculated based on transformer parameters shown in Table 5.4. Theoretical calculations are based on MATLAB R2017b software and the real and ideal case equivalent circuits were simulated and results were validated using LTSpice software. The MATLAB code for theoretical efficiency calculation using the calculated and measured real transformer parameters is given in Appendix G.

Measured efficiency curve indicates slightly lower values, due to measurement errors, secondary losses such as the PCB track losses and other connections.

Figure 5.10 illustrates the LTspice model of the regulator during the boost mode operation where Transformer-1 is responsible for regulating. It indicates the real transformer parameters used in both LTspice and MATLAB simulations. The LTspice model indicates only the transformer operation at 50 Hz line frequency and 230 V nominal voltage. The model of the variable impedance has not included in the above simulation as it is out of the scope of this study. More details of the transistor array model and simulation results are given in [111].

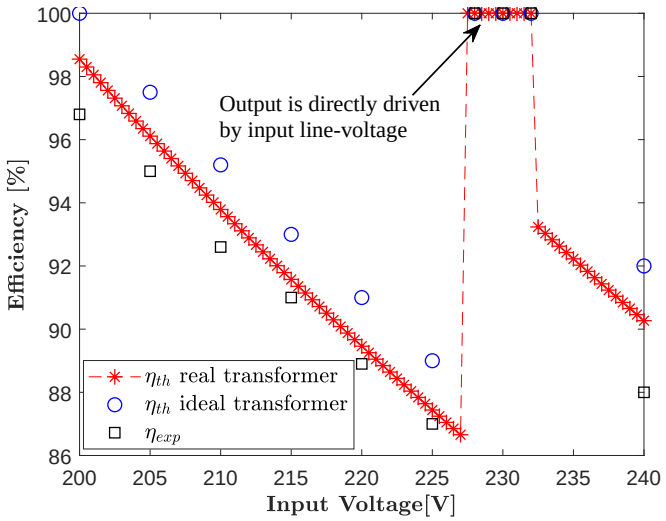


Figure 5.9: Efficiency of dual-transformer regulator for 230 V nominal voltage; experimental and calculated results

Figure 5.11 illustrates the dual-transformer regulator efficiency curves under different load currents such as 0.5 A, 1.0 A and 1.5 A that regulates at 230 V nominal voltage. As shown in the graphs,

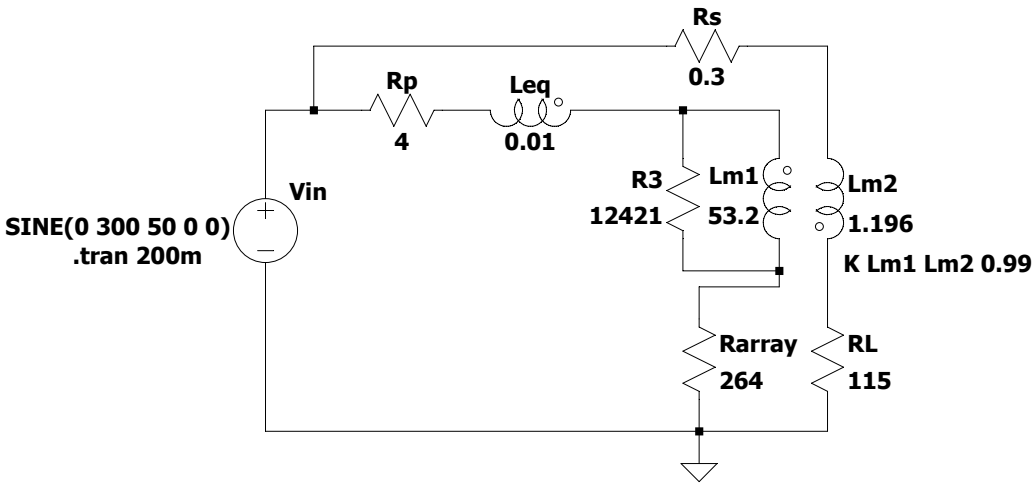


Figure 5.10: LTspice simulation for boost regulation using Transformer-1

A set of oscillograms based on measurements using a Tektronix 2000 series oscilloscope is shown in Figure 5.12 (a) and (b). Each oscillogram displays voltage, current waveforms of input and output of single-transformer and dual-transformer configurations at $V_{\text{out}} = 230$ V and $I_{\text{L}} = 1.2$ A.

In the single transformer design, a distorted output waveform is observed. This is because when the input voltage rises above nominal, the array is driven into very high impedance that makes the cross-over distortion and related non-linear effects of the transistors/diodes become more significant. Figures. 5.13 and 5.14 indicates the harmonic spectrum of the output voltage waveforms of the two designs. The distortion of the output waveform is improved with increasing load current.

Please note that, in all the waveforms indicated in Figure 5.13, the input side also has a flattened top distortion. This is the typical waveform received by the university, due to the fact that a large amount of switch mode power supplies are energized simultaneously. The flattened-top waveform is the effect of a non-linear current drawn by these switching type loads as discussed in subsection 2.1.1.

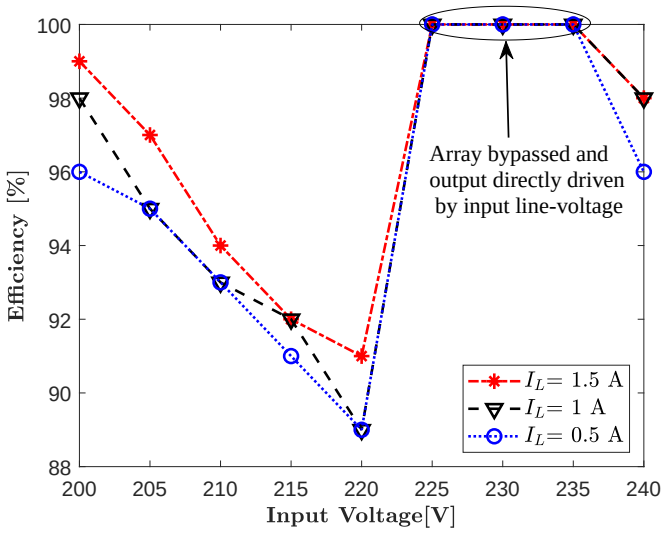
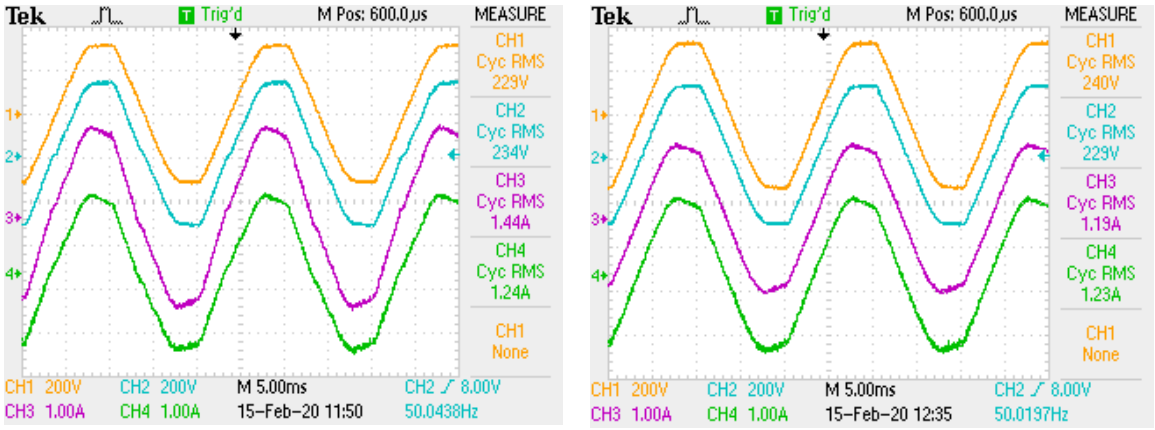


Figure 5.11: Efficiency curves under different load current



(a) Single-transformer regulator (b) Dual-transformer regulator

Figure 5.12: Waveforms of two prototypes; yellow and purple- input parameters; blue and green-output parameters

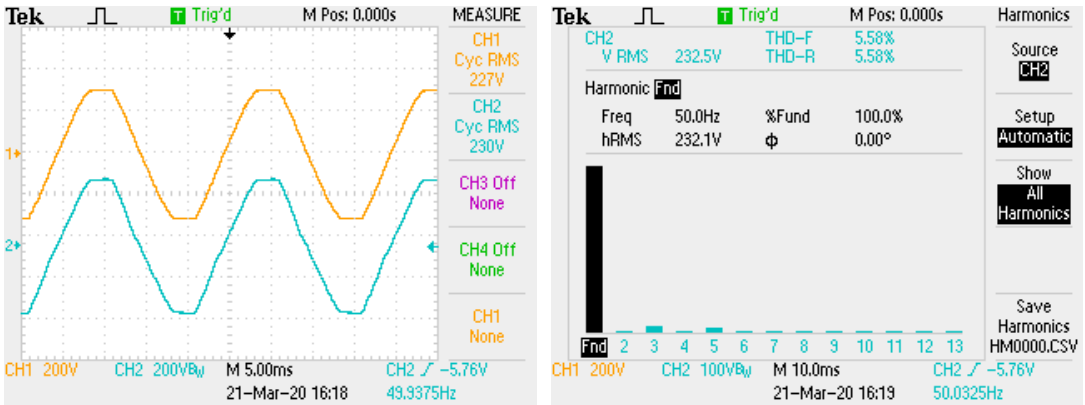


Figure 5.13: Basic single transformer regulator

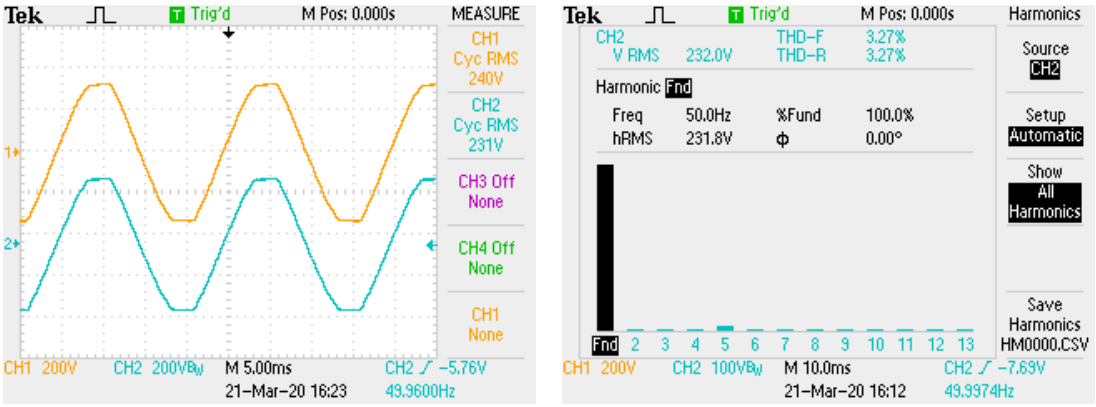


Figure 5.14: Dual-transformer regulator

Due to the availability of high power capable transistors, the four element transistor-array discussed in Chapter 3 now has been upgraded to a single Darlington pair implementation for low current applications of low power loads. Therefore, the current prototype is now using a power stage including a single Darlington pair. But when the load current is increased, the power stage needs to be upgraded as appropriately. The manufacturing cost of the power stage is a significant portion of the total manufacturing cost of the product. Therefore, the ability to change the number of elements of the transistor array is a useful property to reduce the additional component cost during product development with different output capacity. The circuit diagram of the single element Darlington pair is illustrated in Appendix **??**.

In conclusion, the dual-transformer approach is considerably more economical and efficient system compared to the original single transformer method considering the power loss of the transistor array and the overall efficiency of the regulator. But in commercial implementations, as indicated by the commercial partner of the project, requiring two transformers represents an additional cost to the final product, which includes the price for two cores and assembly cost. In addition, placing the transformers in close proximity may result in secondary problems such as “transformer beating” due to the mutual induction between two transformers when energized. Therefore a requirement emerged for a viable solution using a single transformer to enhance regulator efficiency.

Chapter 6

Implementation of a Multiple-Winding Transformer Regulator

6.1 Introduction to Multiple-Winding Transformer Regulator

Basic linear RMS AC voltage regulator, presented in Chapters 3 and 4 was developed to address most of the well-known issues of the conventional RMS regulators, however, the technique inherent a major draw back of reducing efficiency at higher input voltages. Chapter 5 described a potential solution to increase the efficiency of the regulator up to 90% range, where originally it was reducing to 70% when the input voltage increases beyond the nominal value. Despite the efficiency improvement capability, the multi-transformer technique had some limitations in the commercial implementation standpoint, pointed out by the commercial partner of the project. Thus, in this chapter a novel approach using a single transformer is proposed.

Multi-winding transformer regulator presented in this chapter is capable of enhancing the efficiency upto 90% range providing an easy, low cost manufacturability. As illustrated in Figure 6.1, this prototype employs a step-down transformer with two distinct primary windings which are able to induce voltages of opposite polarities in the secondary for boost and buck regulation. To manipulate the two primary windings independently, separate transistor arrays are connected in series with each winding. A feedback circuit drives the two transistor arrays in response to the output voltage of the regulator as indicated in the block diagram. Distinctive transformer windings are energized alternatively in boost- and buck-mode by energizing a set of AC switches (S1 to S4) according to the input line variation sensed by an input sensing circuit, driven by a PIC microcontroller. A detailed block diagram illustrated in Figure 6.2 and discussion on this prototype implementation and experimental results followed by simulations is given below.

Please note that, throughout this chapter, transistor array refers to the single Darlington pair based implementation which is illustrated in Appendix F. But due to the convenience of understanding and to maintain compatibility of identification of key components used by the prototypes, 'transistor array' word phrase will be used in the rest of the chapter.

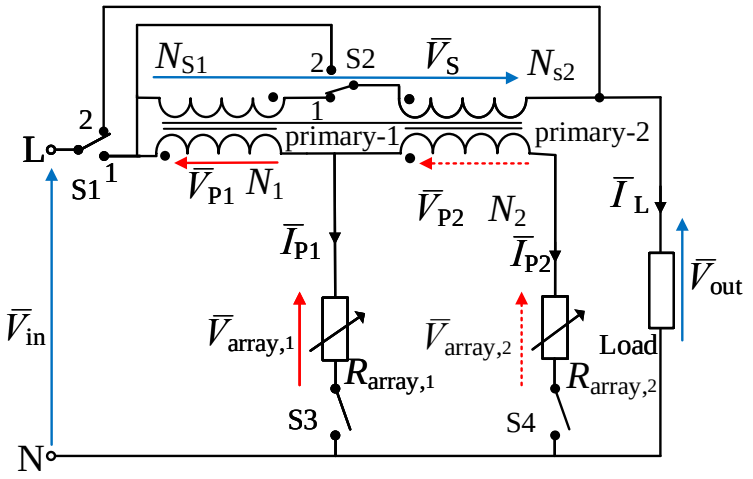


Figure 6.1: Schematic diagram of the multi-winding transformer regulator

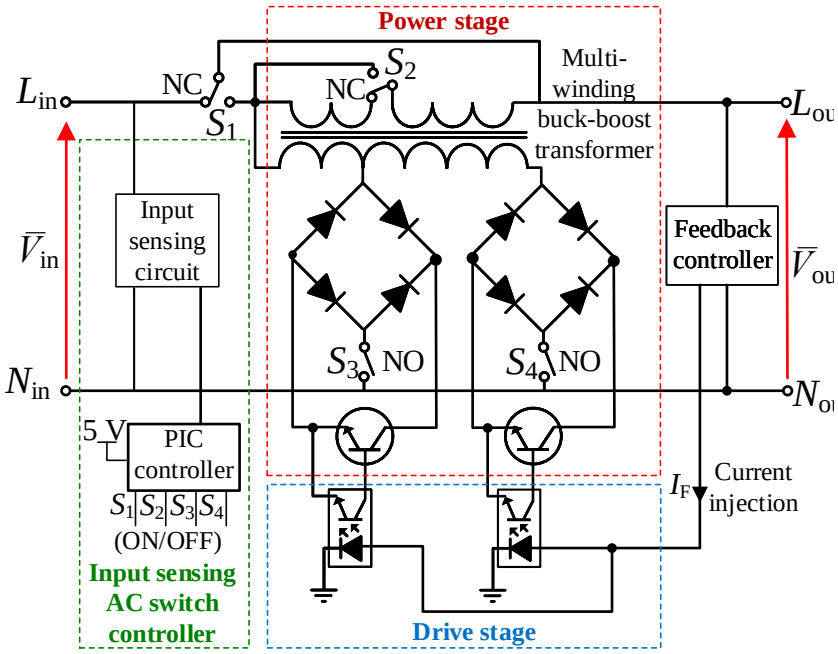


Figure 6.2: Schematic diagram of the multi-winding transformer regulator

6.1.1 Fundamentals of multi-winding transformer

As explained in Appendix C, when an electrical conductor carrying a current, i, a magnetic field of intensity H is induced around the conductor. When this current carrying conductor is wound around a magnetic medium forming N number of turns, it produces flux in the magnetic core whose magnitude is determined by the reluctance of the core. A term called 'Magneto-motive force (MMF)' is determined to present the driving force in the magnetic circuit that creates flux in the core as a result of current conducting through the conductor (coil). The Ampere's law states the sum of the magneto-motive force

(MMF) around a closed magnetic loop having a length of the circumference l is zero [103]. Thus,

$$\sum MMF_{\text{loop}} = 0 \tag{6.1}$$

The drop of MMF (MMF_{drop}) for an element in the magnetic circuit is equals to Hl A. turns. Since MMF can also be written in terms of total flux and reluctance of the core as $MMF = \Phi\Re$, for a current i passes through a coil having N number of turns, the following relationship hold true.

$$\Phi\Re = Ni \tag{6.2}$$

Lets now consider a toroidal transformer as shown in Figure 6.3, that consists of three coils whose number of turns of primary-1, primary-2 and the secondary are N_1, N_2 and N_3 respectively, and the currents flowing through these coils are i_1, i_2 and i_3. According to Eq.6.2, the total MMF of the three winding toroidal transformer can be written as,

$$N_1\bar{i}_1 + N_2\bar{i}_2 + N_3\bar{i}_3 = \Phi\Re \tag{6.3}$$

In a loss-less transformer, the core reluctance is ideally zero ($\Re = 0$) and the winding resistances are neglected; thus, is called an ideal transformer. Assuming ideal transformer characteristics for the three winding transformer stated above, the MMF of the core is equals to zero, which simplifies the above relationship as follows,

$$N_1\bar{i}_1 + N_2\bar{i}_2 + N_3\bar{i}_3 = 0 \tag{6.4}$$

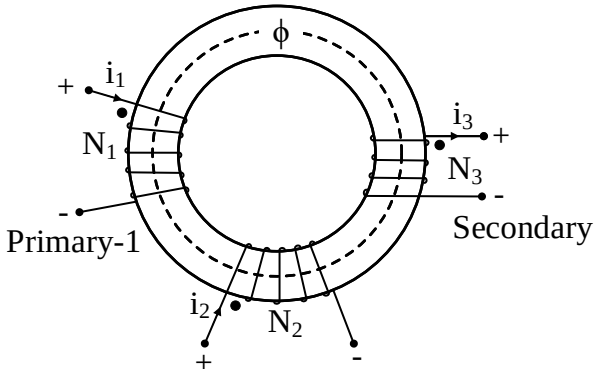


Figure 6.3: Transformer with multiple windings

As per the basic transformer theory for an ideal transformer, $\frac{N_1}{N_3} = n_1$ and $\frac{N_2}{N_3} = n_2$; here n_1 and n_2 are transformer turns ratios of Primary-1 and Primary-2 windings with respect to secondary winding. Note that for the transformer secondary winding, $i_3 = i_s = i_L$.

By dividing the above equation by N_3 gives

$$n_1 i_1 + n_2 i_2 + i_L = 0 \tag{6.5}$$

6.1.2 Multi-winding transformer operation

As in Figure 6.2, a tapped transformer of unique configuration that replaces the operation of dual transformers is used while maintaining the efficiency improvements of the linear regulator. Two primary windings with different winding turns (N_1, N_2) are connected in series with two transistor arrays 6.2. In addition, two secondary windings (Secondary-1 and Secondary-2) of opposite polarity are connected

in series in the input/output load path designed to operate in boost and buck mode respectively. The secondary winding connections were implemented using make/break contacts as shown in Figure 6.2. This arrangement allows to alter the winding connectivity to the primary and the load for a case of 230 V_{ac}, 50 Hz regulated output requirement.

This new technique makes use of two independent primary windings that couples with a secondary winding that has the capability of changing its effective turn counts. In order to implement this circuit diagram as indicated in Figure 6.2, a customized transformer having two primary windings is needed. It is important to point out that, when the current prototype was developed, a readily available tapped-transformer was used by customizing its windings as suitably for the research purpose. The winding arrangement and its operation discussed below is depends on the transformer winding configuration and can be altered if necessary.

As per Figure 6.2, when both winding sets are energized simultaneously, the relationships between the input, output voltages ($\overline{V}_{\text{in}}, \overline{V}_{\text{out}}$), the secondary voltage ($\overline{V}_{\text{s}}$), and the primary-1, primary-2 voltages ($\overline{V}_{\text{p1}}$, $\overline{V}_{\text{p2}}$) are given by,

$$\overline{V}_{\text{out}} = \overline{V}_{\text{in}} \pm \overline{V}_{\text{s}} \tag{6.6}$$

$$\overline{V}_{\text{in}} = \overline{V}_{\text{p1}} + \overline{V}_{\text{array,1}} \tag{6.7}$$

$$\overline{V}_{\text{in}} = \overline{V}_{\text{p2}} + \overline{V}_{\text{array,2}} \tag{6.8}$$

The ($\pm$) sign denotes the voltage polarity induced in the secondary winding; when the induced secondary voltage is additive to the input voltage, V_{s} considered positive and if the voltage is subtractive, V_{s} considered negative. Therefore, boost and buck operation can be implemented respectively.

Transformer action ensures the voltage ratio between primary to secondary winding is equals to the ratio between its number of turn counts [106, 107];

$$\frac{V_p}{V_s} = \frac{N_p}{N_s} = n \tag{6.9}$$

According to this concept, we can write the induced secondary voltage relation to Primary-1 and Primary-2 winding voltages as below,

$$\overline{V}_{\text{s}} = \frac{\overline{V}_{\text{p1}}}{n_1} = \frac{\overline{V}_{\text{p2}}}{n_2} \tag{6.10}$$

Voltages across the transistor-arrays ($\overline{V}_{\text{array,1}}, \overline{V}_{\text{array,2}}$) in terms of current ($\bar{I}_1, \bar{I}_2$) and array-resistance ($R_{\text{array,1}}, R_{\text{array,2}}$) can be written

$$\overline{V}_{\text{array,1}} = \bar{I}_1 R_{\text{array,1}} \tag{6.11}$$

$$\overline{V}_{\text{array,2}} = \bar{I}_2 R_{\text{array,2}} \tag{6.12}$$

Boost–mode Operation

When the regulator operates in boost mode in the input voltage range of $\overline{V}_{\text{in}} \leq \overline{V}_{\text{out}}^{\text{reg}}$, Secondary-1 and Secondary-2 windings are series connected by the switch S-2 as shown in Figure 6.4 which is coupled with Primary-1 winding that induces a corrective voltage, additive to the input voltage to maintain a constant output voltage. In this situation, the turns ratio is set to $n_1 = 180/50 = 3.6$ to achieve an optimum efficiency during the lower worst case input voltage of 180 V, that maintains an output voltage of 230 V.

It is important to point out here that he total correction required in the boost regulation is higher than the correction required in the buck-mode. In order to have higher correction voltage in boost-mode, secondary-1 needs more turns than secondary-2, which implies $N_{S1} > N_{S2}$.

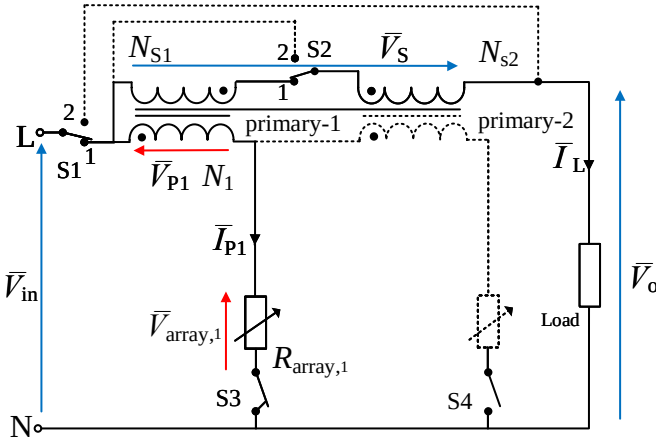


Figure 6.4: Multi-winding transformer in boost-mode operation

Given this situation, the above equation can be further simplified to describe the transformer operation during the boost-mode.

$$\overline{V}_{out} = \overline{V}_{in} + \overline{V}_s \tag{6.13}$$

$$\overline{V}_{in} = \overline{V}_{p1} + \overline{V}_{array,1} \tag{6.14}$$

Table 5.1 presents the state of the switches S1 to S4 with respect to the mode of operation. This table is used as a reference when describing the regulator operation in boost- and buck-mode.

Table 6.1: Truth Table of Switch Operation

Voltage levels		**Switch operation**			
		S1	**S2**	**S3**	**S4**
Condition 1	$\overline{V}_{in} = \overline{V}_{in}^{min}$	1	1	ON	OFF
Condition 2	$\overline{V}_{in} < \overline{V}_{in}^{nom}$	1	1	ON	OFF
Condition 3	$\overline{V}_{in} = \overline{V}_{in}^{nom}$	2	1	OFF	OFF
Condition 4	$\overline{V}_{in} > \overline{V}_{out} \geq \overline{V}_{in}^{max}$	1	2	OFF	ON

Regulator Under Nominal Condition

When the input voltage varies within a tolerance level of $\pm 2\%$ of the nominal voltage, the regulator circuit is bypassed to avoid unnecessary array losses when they are being conducting. The situation is illustrated in Figure 6.5 with the transformer is bypassed by tuning ON switch S1. This S1 switch is a single pole double throw (SPDT) type switch which comes into position-2 when the relay coil is energized.

Buck–mode Operation

As explained above, Secondary-2 winding layout is configured in the opposite polarity to the Secondary-1 winding. Therefore the induced subtractive voltage will ensure buck action ($\overline{V}_{in} > \overline{V}_{out}^{reg}$), as illustrated

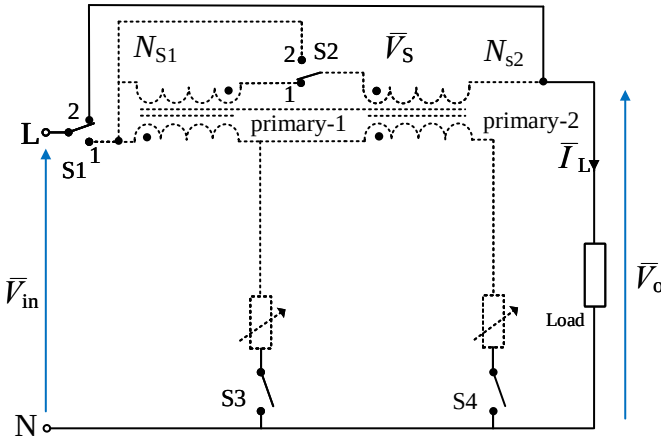


Figure 6.5: Multi-winding transformer regulator under nominal condition

in Figure 6.6. Given that buck-mode required lower correction voltage (maximum of 30 V), the transformer turns ratio is now increased compared to boost-mode. Thus, Primary-2 operates with Secondary-2 with the turns-ratio of $n = 260/30 = 8.7$ to maintain buck mode regulation.

Relationships of the transformer parameters during buck operation are as follows,

$$\overline{V}_{\text{out}} = \overline{V}_{\text{in}} - \overline{V}_{\text{s2}} \tag{6.15}$$

$$\overline{V}_{\text{in}} = \overline{V}_{\text{p2}} + \overline{V}_{\text{array,2}} \tag{6.16}$$

In Figure 6.2, switches S1 and S2 are used to alter the secondary windings' turn counts to change the useful turns ratio as required by the boost- and buck-mode operation which are illustrated in Figures 6.4 and 6.6. When the input line voltage falls within $\pm 2\%$ of the nominal voltage ($225 - 235$ V), the regulating circuit is bypassed by switch S1 (see Figure 6.5), thus giving maximum efficiency. See Appendix D, Table D.1 that summarizes the winding selection using the switches.

Substituting Eqs. (6.11) and (6.12) into Eqs. (6.7) and (6.8) yield

$$\overline{V}_{\text{in}} = \overline{V}_{\text{p1}} + \overline{I}_1 R_{\text{array,1}} \tag{6.17}$$

$$\overline{V}_{\text{in}} = \overline{V}_{\text{p2}} + \overline{I}_2 R_{\text{array,2}} \tag{6.18}$$

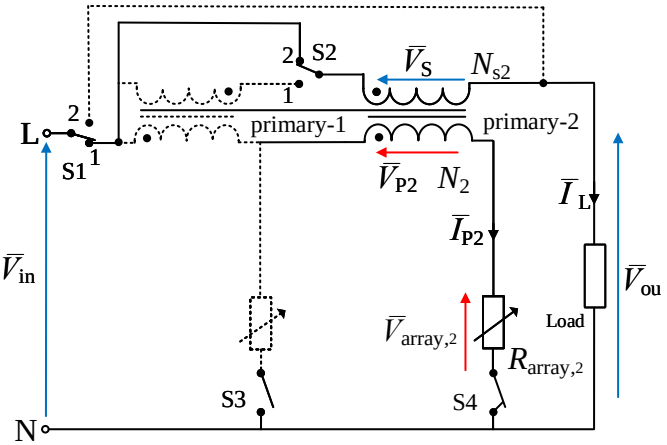


Figure 6.6: Multi-winding transformer in buck-mode operation

Using the above expressions Eq. (6.10) can be elaborated,

$$\overline{V}_{\mathrm{s}} = \frac{\overline{V}_{\mathrm{in}} - \bar{I}_1 R_{\mathrm{array},1}}{n_1} = \frac{\overline{V}_{\mathrm{in}} - \bar{I}_2 R_{\mathrm{array},2}}{n_2} \tag{6.19}$$

Thus, $\bar{I}_1$ and $\bar{I}_2$ can be written

$$\bar{I}_1 = \frac{\overline{V}_{\mathrm{in}} - \overline{V}_{\mathrm{s}} n_1}{R_{\mathrm{array},1}} \tag{6.20}$$

$$\bar{I}_2 = \frac{\overline{V}_{\mathrm{in}} - \overline{V}_{\mathrm{s}} n_2}{R_{\mathrm{array},2}} \tag{6.21}$$

Since $\bar{I}_L = n_1\bar{I}_1 + n_2\bar{I}_2$, $\bar{I}_1$ and $\bar{I}_2$ can be replaced by Eqs. (6.20) and (6.21) and simplified as below.

$$\bar{I}_{\mathrm{L}} = n_1\left(\frac{\overline{V}_{\mathrm{in}} - \overline{V}_{\mathrm{s}} n_1}{R_{\mathrm{array},1}}\right) + n_2\left(\frac{\overline{V}_{\mathrm{in}} - \overline{V}_{\mathrm{s}} n_2}{R_{\mathrm{array},2}}\right) \tag{6.22}$$

$$\bar{I}_{\mathrm{L}} = \overline{V}_{\mathrm{in}}\left(\frac{n_1}{R_{\mathrm{array},1}} + \frac{n_2}{R_{\mathrm{array},2}}\right) - \overline{V}_{\mathrm{s}}\left(\frac{n_1^2}{R_{\mathrm{array},1}} + \frac{n_2^2}{R_{\mathrm{array},2}}\right) \tag{6.23}$$

From Eq. (6.6), V_s can be replaced by $V_{\mathrm{out}} - V_{\mathrm{in}}$ which yield

$$\bar{I}_{\mathrm{L}} = \overline{V}_{\mathrm{in}}\left(\frac{n_1}{R_{\mathrm{array},1}} + \frac{n_2}{R_{\mathrm{array},2}}\right) - \left(\overline{V}_{\mathrm{out}} - \overline{V}_{\mathrm{in}}\right)\left(\frac{n_1^2}{R_{\mathrm{array},1}} + \frac{n_2^2}{R_{\mathrm{array},2}}\right) \tag{6.24}$$

Thus, for any general load connected at the regulator output, the regulated output voltage is given by,

$$\overline{V}_{\mathrm{out}} = \overline{V}_{\mathrm{in}}\left(1 + \frac{A}{B}\right) - \frac{\bar{I}_{\mathrm{L}}}{B} \tag{6.25}$$

where, $A = \frac{n_1}{R_{\mathrm{array},1}} + \frac{n_2}{R_{\mathrm{array},2}}$ $B = \frac{{n_1}^2}{R_{\mathrm{array},1}} + \frac{{n_2}^2}{R_{\mathrm{array},2}}$

Corresponding to boost- and buck-mode operation where only one transformer winding set is energized, the above equation synthesizes a relationship between the input, output and array voltages in terms of turns ratio and array resistance as described below.

During boost-mode when Primary-1 winding induces a corrective voltage in the secondary winding, while Primary-2 is not conducting due to the array-2 being cut-off, thus, array-resistance becomes a very large value close to infinity ($R_{\mathrm{array},2} \approx \infty$). Therefore, $A = n_1/R_{\mathrm{array},1}$ and $B = n_1^2/R_{\mathrm{array},1}$,
Then Eq. (6.25) becomes,

$$\begin{aligned}
\overline{V}_{\mathrm{out}} &= \overline{V}_{\mathrm{in}}\left(1 + \frac{n_1/R_{\mathrm{array},1}}{n_1^2/R_{\mathrm{array},1}}\right) - \frac{\bar{I}_{\mathrm{L}}}{n_1^2/R_{\mathrm{array},1}} \\
\overline{V}_{\mathrm{out}} &= \overline{V}_{\mathrm{in}}\left(1 + \frac{1}{n_1}\right) - \frac{\bar{I}_{\mathrm{L}}}{n_1^2} R_{\mathrm{array},1}
\end{aligned} \tag{6.26}$$

A similar relationship is obtained in buck-mode operation with array-2 resistance, $R_{\mathrm{array},2}$ and Primary-2 to secondary turns ratio n_2 as below,

$$\overline{V}_{\mathrm{out}} = \overline{V}_{\mathrm{in}}\left(1 + \frac{1}{n_2}\right) - \frac{\bar{I}_{\mathrm{L}}}{n_2^2} R_{\mathrm{array},2} \tag{6.27}$$

Equation (6.27) suggest a single transformer operation indicated by Eq. (4.27).

By simplifying Eq. (6.20) by substituting Eq. (6.6) yield Primary-1 winding current

$$\bar{I}_1 = \frac{\overline{V}_{\text{in}}}{R_{\text{array,1}}} - \frac{\left(\overline{V}_{\text{out}} - \overline{V}_{\text{in}}\right) n_1}{R_{\text{array,1}}} \tag{6.28}$$

$$\bar{I}_1 = \overline{V}_{\text{in}} \left(\frac{1+n_1}{R_{\text{array,1}}}\right) - \frac{n_1}{R_{\text{array,1}}} \overline{V}_{\text{out}} \tag{6.29}$$

Similarly, using Eqs. (6.21) and (6.6), I_2 can be computed

$$\bar{I}_2 = \overline{V}_{\text{in}} \left(\frac{1+n_2}{R_{\text{array,2}}}\right) - \frac{n_2}{R_{\text{array,2}}} \overline{V}_{\text{out}} \tag{6.30}$$

Substituting Eq. (6.5) into (6.10) gives

$$\frac{\overline{V}_{\text{p1}}}{\overline{V}_s} \bar{I}_1 + \frac{\overline{V}_{\text{p2}}}{\overline{V}_s} \bar{I}_2 = \bar{I}_L \tag{6.31}$$

$$\overline{V}_{\text{p1}} \bar{I}_1 + \overline{V}_{\text{p2}} \bar{I}_2 = \overline{V}_{\text{s}} \bar{I}_L \tag{6.32}$$

Transformer winding voltages, $\overline{V}_{\text{p1}}$, $\overline{V}_{\text{p2}}$ and $\overline{V}_{\text{s}}$ can be written in terms of input, output and array voltages given by Eq. (6.7), Eq. (6.8) and Eq. (6.6) that yields

$$\left(\overline{V}_{\text{in}} - \overline{V}_{\text{array,1}}\right) \bar{I}_1 + \left(\overline{V}_{\text{in}} - \overline{V}_{\text{array,1}}\right) \bar{I}_2 = \left(\overline{V}_{\text{out}} - \overline{V}_{\text{in}}\right) \bar{I}_L \tag{6.33}$$

Rearranging Eq. (6.33), we can write

$$\overline{V}_{\text{in}} \left(\bar{I}_1 + \bar{I}_2 + \bar{I}_L\right) - \overline{V}_{\text{array,1}} \bar{I}_1 - \overline{V}_{\text{array,2}} \bar{I}_2 = \overline{V}_{\text{out}} \bar{I}_L \tag{6.34}$$

According to Figure 6.2, $\bar{I}_{\text{in}} = \bar{I}_1 + \bar{I}_2 + \bar{I}_L$; therefore, Eq. (6.34) simplifies into

$$\overline{V}_{\text{in}} \bar{I}_{\text{in}} - \overline{V}_{\text{array,1}} \bar{I}_1 - \overline{V}_{\text{array,2}} \bar{I}_2 = \overline{V}_{\text{out}} \bar{I}_L \tag{6.35}$$

where
$\overline{V}_{\text{in}} \bar{I}_{\text{in}}$ gives input power, P_{in}
$\overline{V}_{\text{array,1}} \bar{I}_1$ - array-1 power loss, $P_{\text{array,1}}$
$\overline{V}_{\text{array,2}} \bar{I}_2$ - array-2 power loss, $P_{\text{array,2}}$ and
$\overline{V}_{\text{out}} \bar{I}_{\text{L}}$ - output power, P_{out}

When Eq. (6.35) is divided by $\overline{V}_{\text{in}} \bar{I}_{\text{in}}$, the regulator efficiency can be achieved,

$$\eta = 1 - \frac{P_{\text{array,1}}}{P_{\text{in}}} - \frac{P_{\text{array,2}}}{P_{\text{in}}} \tag{6.36}$$

Above equation suggests minimizing array losses will optimize regulator efficiency.

Section 6.1.2 describes the transformer operation during the boost- and buck-mode regulation under different input voltage levels by shifting the operation of transformer windings. Table 6.2 presents a summary of the section which summarizes the winding operation and the relationships between transformer parameters under four different input voltage levels from Condition-1 to 4.

Table 6.2: Theoretical Relationship of the Transformer Parameters of Multi-Winding Regulator

Voltage levels	**Relationships of series dual-transformer regulator**		**Comments**
	Primary-1	**Primary-2**	
Condition 1 $\overline{V}_{\text{in}} = \overline{V}_{\text{in}}^{\text{min}}$	$\overline{V}_{\text{out}} = \overline{V}_{\text{in}} + \overline{V}_{\text{s}}$ $R_{\text{array,1}} = 0$ $\overline{V}_{\text{array,1}} = 0$	Secondary-2 bypassed	Array-1 saturates
Condition 2 $\overline{V}_{\text{in}} < \overline{V}_{\text{nom}}$ (Boost mode)	$\overline{V}_{\text{out}} = \overline{V}_{\text{in}} + \overline{V}_{\text{s}}$ $\overline{V}_{\text{p1}} = n_1 \overline{V}_{\text{s}}$ $\overline{V}_{\text{array,1}} = \overline{V}_{\text{in}} - \overline{V}_{\text{p1}}$ $R_{\text{array,1}} > 0$	Secondary-2 bypassed	$R_{\text{array,1}}$ keeps increasing
Condition 3 $\overline{V}_{\text{in}} = \overline{V}_{\text{in}}^{\text{nom}}$	Secondary windings are bypassed, Input line voltage directly connected with the load		No boost/no buck
Condition 4 $\overline{V}_{\text{in}} > \overline{V}_{\text{out}} \geq \overline{V}_{\text{in}}^{\text{max}}$ (Buck mode)	Secondary-1 bypassed	$\overline{V}_{\text{out}} = \overline{V}_{\text{in}} - \overline{V}_{\text{s}}$ $\overline{V}_{\text{array,2}} = \overline{V}_{\text{in}} + \overline{V}_{\text{p2}}$ $R_{\text{array,2}} \geq 0$	$R_{\text{array,2}}$ keeps increasing
$\overline{V}_{\text{in}} = \overline{V}_{\text{in}}^{\text{max}}$		$R_{\text{array,2}} = 0$	Array-2 saturates

6.1.3 Realization of the Transformer Winding Turns Ratios

In the linear AC regulator, a transistor array is being used as a variable impedance that adjusts its effective resistance when the input voltage varies. However, the array produce a resistive power loss of I^2R type during conduction, which keeps on increasing with the input voltage rise. This array power loss directly impact on the efficiency, hence multiple windings are set in the regulating transformer to enhance the efficiency by reducing array power loss.

Selection of transformer turns-ratios and number of windings are critical in overall efficiency calculation. We make this selection based on the following factors:

- input voltage range
- required efficiency level
- manufacturing cost of the product

Following paragraphs describe the impact of above factors.

The strategy used to minimize array losses for better device performance is to split the transformer operation among many windings that comes into play under different input voltages. Since $\overline{V}_{\text{in}}^{\text{min}} = \frac{n}{(1+n)}\overline{V}_{\text{out}}$, given by Eq. (4.27), for optimum efficiency at the worst case input voltage is achieved by setting the turns ratio to cater the corresponding input voltage. For an example, a regulator providing a nominal output of 230 V gives maximum efficiency at 160 V and 240 V if its winding turns ratios are set to $160/70$ and $240/10$. If the required input voltage range is wider, we can add another set of transformer windings to increase the overall device efficiency.

Figure 6.7 illustrates the effect of number of transformer windings and their turns ratios on the device efficiency. The regulator input voltage range is 160 V - 260 V, and the three options present here employ different winding arrangements as described below.

Option 1 - transformer having one pair of windings

Option 2 - transformer having two winding pairs of turns ratios 160/70 and 260/30
Option 3 - transformer having three winding pairs of turns ratios 160/40, 200/30 and 260/30 Based

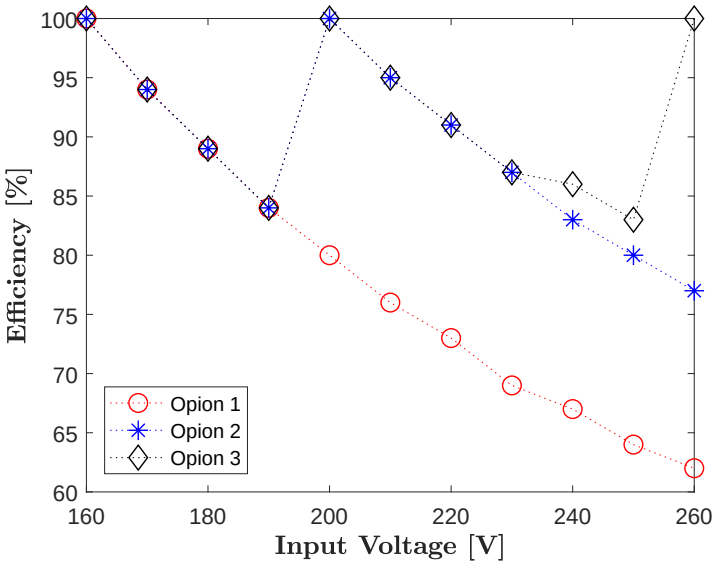


Figure 6.7: Estimated efficiencies of multi-winding designs

on the efficiency curves shown in Figure. 6.7, the option employing more transformer windings exhibit higher overall efficiency compared to the option that utilize only one pair of windings. On the other hand, adding customized windings in a transformer formulates an additional cost than buying standard two-winding transformers.

The prototype employing the multi-winding transformer utilized the winding turns ratios as follows. Calculations are based on the case of maximum efficiency at the worst case input voltages.

- For $\overline{V}_{\text{in}}^{\text{min}}$ in boost-mode (Fig. 6.2(b)): $n_1 = N_1/(N_{s1}+N_{s2})$
- For $\overline{V}_{\text{in}}^{\text{max}}$ in buck-mode (Fig. 6.2(d)): $n_2 = N_2/N_{s2}$

6.2 Switching Transformer Windings

As discussed in Section. 6.1.2, the transformer windings operates alternatively in the boost- and buck-modes, in order to maintain the regulation. This section describes the mechanism that was used to energize the two windings alternatively in response to the input line voltage changes.

Figure. 6.8 illustrates a microprocessor based control circuit that controls a set of AC switches based on the voltage level of the power line that feeds the regulator. According to the illustration, the circuit extracts an equivalent DC value related to the AC signal in the supply line. This value is read by an analog pin of the microprocessor which is used to output a digital signal based on the magnitude of the AC signal.

In this circuit, an Arduino UNO program kit was used to process the analog signal from the sampling circuit and output a digital control signal to the switches S1 to S4. Arduino UNO program board includes the Atmel ATMEGA328P microprocessor with 10-bit ADC pins which provides sufficient accuracy for reading the input AC sample signal [112]. The microprocessor code is attached in Appendix I.

When implementing the current prototype of multi-winding regulator shown in Figure. 6.2, a set of basic relay type AC switches were used. A single pole double throw (SPDT) type relays were used for

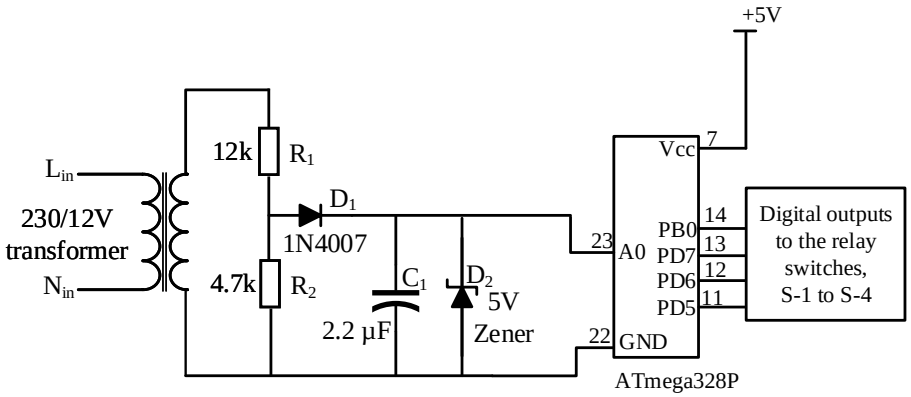


Figure 6.8: Input sensing circuit

S1 and S2, while single pole single throw (SPST) for S-3 and S-4. The wiring diagrams are shown in Figure 6.9.

Figure 6.9(a) indicates the positioning of these relay switches in the current multi-winding prototype. Figure 6.9(b) and (c) illustrates the relay winding diagram, driven by an NPN transistor and a flyback diode, connected parallel to the relay coil.

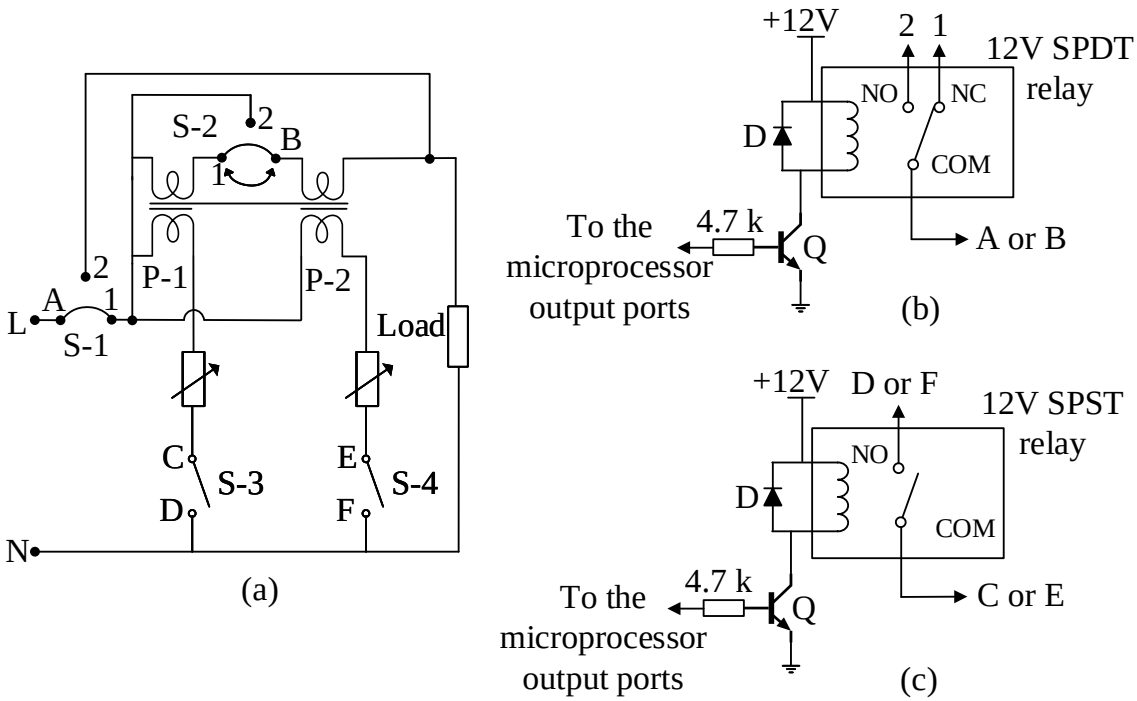


Figure 6.9: Wiring arrangement of the switches (a) Block diagram of the multi-winding arrangement (B) SPDT relay (C) SPST relay

It is important to mention here that this switching arrangement was a basic circuit that was built for the purpose of demonstrating the working principle of the proposed multi-winding technique. The relay based switching arrangement can introduce transients to the circuit which could display at the output waveform.

6.3 Transformer Equivalent Circuit Model

The Section 6.1.2 presented a discussion on the multi-winding transformer regulator assuming a loss-less transformer which operates in ideal condition. In reality transformers are lossy devices which will reduce the transformer efficiency considerably, thus may exhibit poor performance. This section presents an equivalent circuit model of the multi-winding transformer regulator, considering real transformer parameters. The calculated transformer parameters are used to estimate the efficiency of the regulator and the results are presented in comparison to experimental efficiency of the design.

6.3.1 Computation of Real Transformer Parameters

As discussed in Chapter 5, traditional transformer tests such as open- and short-circuit tests were carried out to compute real transformer parameters of the transformers which have been used in developing the proposed prototypes. For more details of the open- and short circuit tests, please refer Appendix E. The measurements of obtained from the two tests are listed in Table 6.4 which will be used in the calculations given later in the section.

As illustrated in Figure 6.2, the core of the new regulator design is based on a transformer winding configuration change, by introducing a third winding to a traditional two-winding buck-boost transformer. This new transformer configuration employs two independent primary windings and a secondary winding which couples with both primaries. Figure 6.10 illustrates an equivalent transformer model including the three windings and their related losses. In this diagram, all transformer parameters such as magnetizing inductance (L_{m1}, L_{m2}) core loss (R_{C1}, R_{C2}), copper loss (R_{eq1}, R_{eq2}) and leakage inductance (L_{eq1}, L_{eq2} are included.

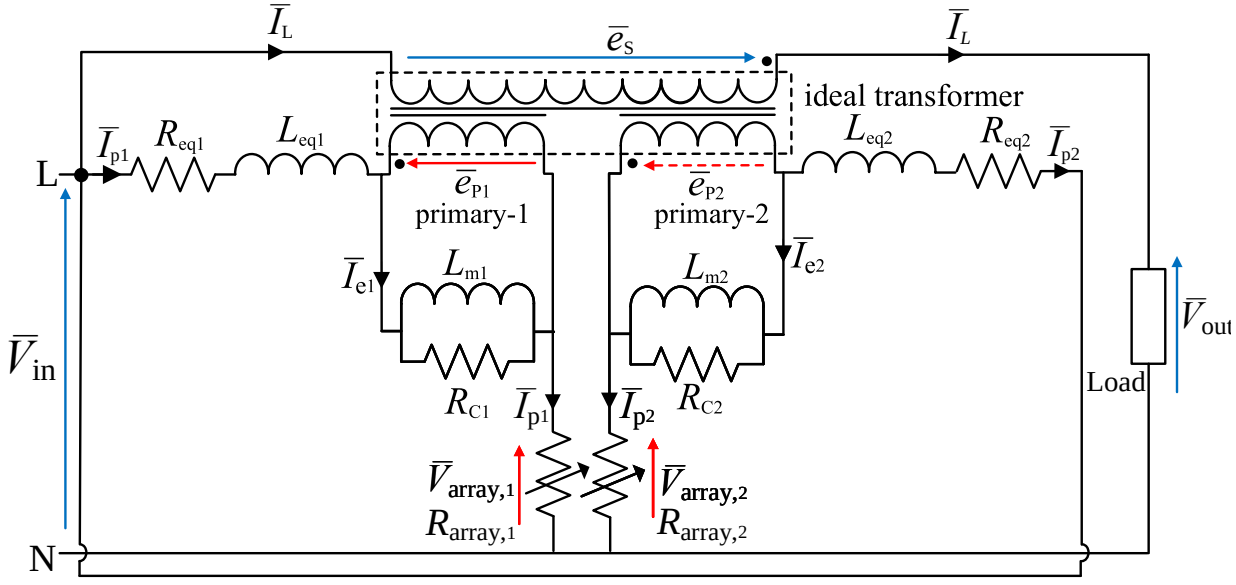


Figure 6.10: Equivalent circuit of the multi-winding transformer regulator

When implementing the multi-winding transformer regulator, we have used an identical transformer which we have used in developing the dual-transformer regulator discussed in Chapter 5 with suitable winding modification as shown in Figure 6.11. We have used the original configuration of the transformer

Table 6.3: Transformer test data to calculate real transformer parameters

Parameter	**Test Data**	
	Primary-1 (n=6.7)	**Primary-2** (n=24)
Short-ciruit test		
V_{sc}	16.8 V	22.9 V
I_{sc}	0.98 mA	0.24 mA
P_{sc}	16.1 W	5.5 W
Open-ciruit test		
V_{oc}	199.5 V	228.5
I_{oc}	21.2 mA	20 mA
P_{oc}	3.3 W	3.7 W

for the Primary-1/ Secondary-1 winding couple which is dedicated for boost-operation whereas a new Primary-2 winding was made to satisfies the optimum efficiency during the buck-operation.

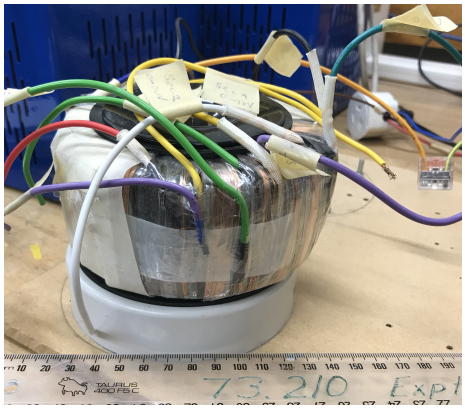


Figure 6.11: Image of the multi-winding transformer

Transformer test data presented in Table 6.3 is used to compute the transformer parameters using the equations given in Appendix E. A sample calculation for Primary-2/ Secondary-2 winding pair is presented under this section.

Calculation of series circuit elements such as copper losses and leakage inductances of the windings can be done using the measurements of the short-circuit test and parallel circuit components of the transformer namely magnetizing inductance and the core loss are computed using open-circuit test measurements.

Substituting values to Eq. (E.1), the equivalent components of the primary and the secondary losses defined by $Z_{eq} = R_{eq} + L_{eq}$ are given as,

$$Z_{eq} = \frac{V_{sc}}{I_{sc}} = \frac{22.9}{0.24} = 95\ \Omega \tag{6.37}$$

Then using Eq. (E.2), the copper loss can be calculated as

$$R_{eq} = \frac{P_{sc}}{I_{sc}^2} = \frac{5.5}{0.24^2} = 95\ \Omega \tag{6.38}$$

The reason for obtaining a high winding resistance is because this new primary winding has been wound in the laboratory using a very thin copper wire guage of AWG 38 which adds a significant resistance to the winding. This high guage copper wire was the only solution to have an additional winding with the

remaining window size of the toroidal transformer used in this prototype at a cost of lower rated current through the winding upto 2 A [113].

The equivalent leakage reactance is given by Eq. (E.4)

$$X_{\text{eq}}\sqrt{(Z_{\text{eq}}^2 - R_{\text{eq}}^2)} = \sqrt{(95.42^2 - 95.4^2)} = 3.81\ \Omega \tag{6.39}$$

Thus the equivalent leakage inductance is

$$L_{\text{eq}} = \frac{3.8}{2 \times \Pi \times 50} = 12.12\ mH \tag{6.40}$$

Components of the excitation branch is computed using the open-circuit test data as follows. The core-loss (R_C) is given by Eq. (E.8),

$$R_{\text{c}} = \frac{V_{\text{oc}}^2}{P_{\text{oc}}} == \frac{228.5^2}{3.7} = 14111\ \Omega \tag{6.41}$$

The core reactance is

$$\frac{1}{Z_{\text{oc}}} = \frac{V_{\text{oc}}}{I_{\text{oc}}} = \frac{228.5.3}{0.02} = 11425\ \Omega \tag{6.42}$$

Finally the magnetizing reactance is given by Eq. (E.9),

$$X_{\text{m}} = \frac{1}{\sqrt{\frac{1}{Z_{\text{oc}}^2} - \frac{1}{R_{\text{c}}^2}}} = \frac{1}{\sqrt{\frac{1}{11425^2} - \frac{1}{14111.4^2}}} = 19\ \text{k}\Omega \tag{6.43}$$

Finally, the magnetizing inductance is

$$L_{\text{m}} = \frac{19466}{2 \times \Pi \times 50} = 61.9\ \text{H} \tag{6.44}$$

A similar approach is used to calculate the parameters of the transformer when Primary-1/ Secondary-1 is in action and the results are listed in Table 6.4.

Using results obtained above, we can derive core parameters of the transformer used in the prototype and estimate the practical transformer efficiency. A step-by-step computation is given below.

If L_1, L_2 are the self-inductances of the primary and secondary windings respectively, Eq. (4.18) gives

$$\begin{aligned} L_1 = L_{\sigma 1} + L_{\text{m1}} &= 10\ \text{mH} + 61.9\ \text{H} \\ &= 61.9\ \text{H} \end{aligned} \tag{6.45}$$

The mutual inductance, M is given by Eq. (C.14)

$$M = L_{\text{m2}}/n_2 = 61.9\ \text{H}/24 = 2.58\ \text{H} \tag{6.46}$$

$$\begin{aligned} L_2 = L_{\sigma 2} + L_{\text{m2}} &= 12/n_2 + M/n_2 \\ &= 12/24 + 2580/24 \\ &= 0.5 + 107.5 = 108\ \text{mH} \end{aligned} \tag{6.47}$$

Thus, coupling coefficient of Primary-2, k_2 is

$$\begin{aligned} k_2 &= \frac{M}{\sqrt{L_1 \times L_2}} \\ &= \frac{2.58}{\sqrt{61.91 \times 0.1}} \\ &= 0.78 \end{aligned} \tag{6.48}$$

Table 6.4: Real Transformer parameters corresponding to two pairs of transformer windings

	Calculated values	
Transformer parameters	**Primary-1** (n=6.7)	**Primary-2** (n=24)
Primary referred magnetizing inductance, L_M	53.2 H	61.9 H
Primary referred core-loss, R_C	12.4 kΩ	14.1 kΩ
Equivalent leakage inductance, L_{eq}	10 mH	12 mH
Primary resistance, r_{p}	4 Ω	35 Ω
Secondary resistance, r_{s}	0.3 Ω	0.2 Ω
Excitation current, $\bar{I}_e$	21.2 mA	24 mA
Self-inductance of primary, L_1	53.2 H	61.91 H
Self-inductance of secondary, L_2	1.19 H	108 mH
Mutual inductance, M	8 H	2.58 H
Coupling coefficient, k	0.99	0.78

Above steps can be repeated to calculate coupling coefficient of Primary-1 when it is operating in boost-mode. The results are tabulated in Table 6.4.

During the buck mode operation, winding configuration of the transformer is such that the Primary-2 couples with Secondary-2 where, N_2 is 352 and L_{m2} is 61.9 H. Using the relationship $L_m = N^2/\Re$ in Eq. (C.13), the core reluctance is given by

$$\Re_2 = \frac{N_2^2}{L_{\text{m2}}} = \frac{352^2}{61.9} = 2002 \text{ H}^{-1}$$

Using Eq. (4.5), the total flux for rated voltage is given by,

$$\begin{aligned}\Phi_2 &= \frac{V_{\text{RMS}}}{4.44 \times N_2 \times f} = \frac{240}{4.44 \times 352 \times 50} \\ &= 3.07 \times 10^{-}3 \text{ Wb}\end{aligned}$$

Thus, Eq. (5.44) gives Primary-2 current, $\bar{I}_2$

$$\begin{aligned}\bar{I}_2 &= \frac{3.07 \times 10^{-}3 \text{ Wb} \times 2001 \text{ H}^{-1}}{352} + \frac{1 \text{ A}}{24} \\ &= 0.059 \text{ A}\end{aligned}$$

Calculation shown in Appendix H gives the transformer parameters for Primary-1/ Secondary-1 configuration as below,
core reluctance, $\Re_1 = 1613.7 \text{ H}^{-1}$,
total flux for rated voltage, 200 V $= 3.06 \times 10^{-}3$ Wb
Primary-1 current, $\bar{I}_1 = 0.16$ A,

Please note that, when developing the current prototype of the multi-winding transformer regulator, we have used an identical transformer which was used to develop the dual-transformer regulator and altered its existing windings to obtain the Primary-2/ Secondary-2 winding configuration to satisfy the requirement of the optimum turns ratio during buck-operation. But we have used the same set of windings to achieve the boost-operation as we have done in dual-transformer configuration. Therefore, the transformer parameters given above are similar to the Transformer-1 parameters in Chapter 5.

The toroidal transformer used in this prototype has a core cross sectional area of 2.49×10^{-3} m^2. During the operation of the Primary-1/Secondary-1 configuration, the maximum B-fields at rated voltage can be calculated as below.

Operation of Primary-1/ Secondary-1;

$$B = \Phi_1/A = 3.06 \times 10^{-}3 \text{ Wb}/2.49 \times 10^{-3} \text{ m}^2 \qquad = 1.22 \text{ T} \tag{6.49}$$

Similarly, the maximum B-field during the operation of Primary-2/ Secondary-2 is given by,
Operation of Primary-2/ Secondary-2;

$$B = \Phi_2/A = 3.07 \times 10^{-}3 \text{ Wb}/2.49 \times 10^{-3} \text{ m}^2 \qquad = 1.23 \text{ T} \tag{6.50}$$

Both of the secondary windings are designed to conduct the maximum load current of 4 A, thus, the wire gauge was designed with awg 35. Primary-1 winding is designed to conduct a maximum of 2 A, and the wire gauge is awg 39. Since the Primary-2 winding was limited by the available window size of the existing transformer, we had to go for the thinnest wire of 0.0799mm diameter of gauge awg 40.

6.3.2 Equivalent Circuit Analysis

As indicated in the equivalent circuit model of the multi-winding transformer regulator shown in Figure 6.10 , the relationship between transformer parameters and the input/output voltages can be achieved as follows.

$$\overline{V}_{\text{out}} = \overline{V}_{\text{in}} \pm \overline{e}_{\text{s}} \tag{6.51}$$

$$\overline{V}_{\text{in}} = \overline{e}_{\text{p1}} + \bar{I}_1(Z_{\text{array,1}} - Z_{\text{eq1}}) \tag{6.52}$$

$$\overline{V}_{\text{in}} = \overline{e}_{\text{p2}} + \bar{I}_2(Z_{\text{array,2}} - Z_{\text{eq2}}) \tag{6.53}$$

Primary winding voltages $\overline{e}_{\text{p1}}$ and $\overline{e}_{\text{p2}}$ follows the general form given by Eq. (5.40).
where,
$Z_{\text{eq1}} = R_{\text{eq1}} + jX_{\text{eq1}}; \qquad Z_{\text{eq2}} = R_{\text{eq2}} + jX_{\text{eq2}}$

$X_{\text{eq1}} = 2\pi f L_{\text{eq1}}; \qquad X_{\text{eq2}} = 2\pi f L_{\text{eq2}}$

Using the relationship obtained in Eq. (6.10), the induced secondary voltage can be presented as

$$\overline{e}_{\text{s}} = \frac{\overline{e}_{\text{p1}}}{n_1} = \frac{\overline{e}_{\text{p2}}}{n_2} \tag{6.54}$$

which substitutes the primary voltages of Eqs. (6.52) and (6.53) yields

$$\begin{aligned} \overline{V}_{\text{in}} &= n_1\overline{e}_{\text{s}} + \bar{I}_1(Z_{\text{array,1}} - Z_{\text{eq1}}) \\ \overline{V}_{\text{in}} &= n_2\overline{e}_2 + \bar{I}_2(Z_{\text{array,2}} - Z_{\text{eq2}}) \end{aligned} \tag{6.55}$$

rearranging Eq. (6.55)

$$\begin{aligned} \bar{I}_1 &= \frac{\overline{V}_{\text{in}} - n_1\overline{e}_{\text{s}}}{(R_{\text{array,1}} - Z_{\text{eq1}})} \\ \bar{I}_2 &= \frac{\overline{V}_{\text{in}} - n_2\overline{e}_{\text{s}}}{(R_{\text{array,2}} - Z_{\text{eq2}})} \end{aligned} \tag{6.56}$$

when these primary currents are substituted in Eq. (6.3),

$$\begin{aligned}\Phi\Re &= n_1\left(\frac{\overline{V}_{\text{in}}-\overline{e}_{\text{s}}n_1}{R_{\text{array},1}-Z_{\text{eq1}}}\right)+n_2\left(\frac{\overline{V}_{\text{in}}-\overline{e}_{\text{s}}n_2}{R_{\text{array},2}-Z_{\text{eq2}}}\right)-\bar{I}_{\text{L}}\\ &= \overline{V}_{\text{in}}\left(\frac{n_1}{(R_{\text{array},1}-Z_{\text{eq1}})}+\frac{n_2}{(R_{\text{array},2}-Z_{\text{eq2}})}\right)-\overline{e}_{\text{s}}\left(\frac{n_1^2}{(R_{\text{array},1}-Z_{\text{eq1}})}+\frac{n_2^2}{(R_{\text{array},2}-Z_{\text{eq2}})}\right)-\bar{I}_{\text{L}}\end{aligned} \tag{6.57}$$

defining $C=\frac{n_1}{(R_{\text{array},1}-Z_{\text{eq1}})}+\frac{n_2}{(R_{\text{array},2}-Z_{\text{eq2}})}$ and $B=\frac{{n_1}^2}{(R_{\text{array},1}-Z_{\text{eq1}})}+\frac{{n_2}^2}{(R_{\text{array},2}-Z_{\text{eq2}})}$,
Equation (6.57) can be simplified as follows,

$$\Phi\Re = \overline{V}_{\text{in}}(C)-\overline{e}_s(D)-\bar{I}_{\text{L}} \tag{6.58}$$

since $\overline{e}_s$ is $\overline{V}_{\text{out}}-\overline{V}_{\text{in}}$, above equation can be rearranged into,

$$\begin{aligned}\Phi\Re &= \overline{V}_{\text{in}}C-(\overline{V}_{\text{out}}-\overline{V}_{\text{in}})D-\bar{I}_{\text{L}}\\ &= \overline{V}_{\text{in}}(C+D)-D\overline{V}_{\text{out}}-\bar{I}_{\text{L}}\end{aligned} \tag{6.59}$$

which yields a relationship between input and output voltages in terms of load current and transformer turns ratios similar to Eq. (6.25) with the real transformer parameters as below,

$$\overline{V}_{\text{out}} = \overline{V}_{\text{in}}\left(\frac{C}{D}+1\right)-D\overline{V}_{\text{out}}-\frac{\bar{I}_{\text{L}}}{D}-\frac{\Phi\Re}{D} \tag{6.60}$$

Transformer Efficiency

Using the equations derived in Chapter 5, transformer efficiency at full load can be calculated. These figures are important to visualize the transformation efficiency during the operation in boost- and buck-mode where the transformer winding configurations are changed.

The efficiency of the transformer during the operation of Primary-2/Secondary-2, at a load current of 1 A is calculated when the power factor ($cos\theta$) is measured to be 0.82.

$$\text{Efficiency at full load }, \eta = 1-\frac{\text{losses}}{\text{Input power}}\times 100\% \tag{6.61}$$

$$\begin{aligned}\text{Losses} &= \text{Core loss}+\text{Copper loss}\\ &= V_pI_e sin\theta + I_2^2R_{\text{eq}}\\ &= 230\times(24\times10^{-3})\times sin(35)^\circ+\frac{1}{24}\times 95\\ &= 3.16+0.16\\ &= 3.32\text{ W}\end{aligned} \tag{6.62}$$

The transformer efficiency during the operation of Primary-2/ Secondary-2 is given by Eq. (5.35),

$$\begin{aligned}\eta &= \left(1-\frac{\text{Losses}}{V_{\text{in}}I_{\text{in}}cos\theta}\right)\\ &= 1-\frac{3.32}{230*0.95*0.82}\\ &= 98.2\%\end{aligned} \tag{6.63}$$

Similarly the transformer efficiency during Primary-1/Secondary-1 operation was computed to be 98.0%. See Appendix H for calculation steps.

When customizing the transformer windings, Primary-2 winding was made by using a very thin wire of awg 38 gauge. This new winding adds a significant series resistance to the transformer equivalent circuit as you can see in the last column of Table 6.4, which is ten times larger than a normal winding. However, the conducting current through this winding is very low, which does not highlight in the copper loss component in Eq. (6.62).

6.4 Experimental and Simulation Results of the Multi-Winding Transformer Regulator

This section discusses experimental results of this two-winding transformer regulator that was developed to reach the efficiency targets comparable to commercial RMS voltage regulators.

This new technique makes use of two independent primary windings that couples with a secondary winding that has the capability of changing its effective turn counts. In this prototype, a standard tapped-transformer was used by customizing its windings to suit the purpose. Accordingly, the transformer turns ratios are set at $200/30 = 6.7$ and $240/10 = 24$ to suit lower and higher worst-case scenarios.

These two transformer windings, Primary-1 and Primary-2 of turns ratios 6.7 and 24 become active during boost- and buck-mode respectively. Therefore, similar to the dual-transformer operation, Primary-2 winding regulates in the buck-mode and maintain the regulator efficiency in the range of $90's\%$. In comparison to basic single-transformer design, this new configuration is able to enhance the efficiency when the input voltage increases beyond the nominal. Figure. 6.12 illustrates an efficiency comparison of the multi-winding and single-transformer configurations ar 1 A load current and 230 V nominal voltage. The single-transformer regulator maintains regulation by increasing the array impedance, which leads to resistive power loss across the transistors. On the other hand, the multi-winding regulator maintains the regulation by shifting the operation between winding pairs which are dedicated for operation under two modes; which eliminates the array driven into high impedance, hence enhance the efficiency.

The switching between windings is required only when the input voltage drops below the nominal or increases beyond nominal by more than $\pm 2\%$. Within these two limits such as $230 + 2\% = 235$V and $230 - 2\% = 225$V, the regulating circuit including the transformer is bypassed by a set of AC switches, thus, the input line voltage is directly conducts to the load. This method eliminates unnecessary regulation of the input voltage where it is not necessary. This option was not implemented in the original single-transformer technique, thus, a reduced efficiency around the nominal voltage can be seen in the efficiency curve of Figure. 6.12.

According to the transformer equivalent model presented in Figure 6.10, a MATLAB simulation was carried out find the theoretical efficiencies of the regulator under different input voltage levels. In this case, the losses of the multi-winding transformer was taken into account. In contrast, assuming this transformer as a loss-less device that exhibit ideal performance, regulator efficiency was calculated. These calculated efficiencies were compared with the experimental results of the regulator prototype and is indicated in Figure 6.13

Results achieved as expected. The measured efficiency curve indicates slightly lower values than the theoretical values which indicates the measurement errors, losses of the PCB tracks and other connecting

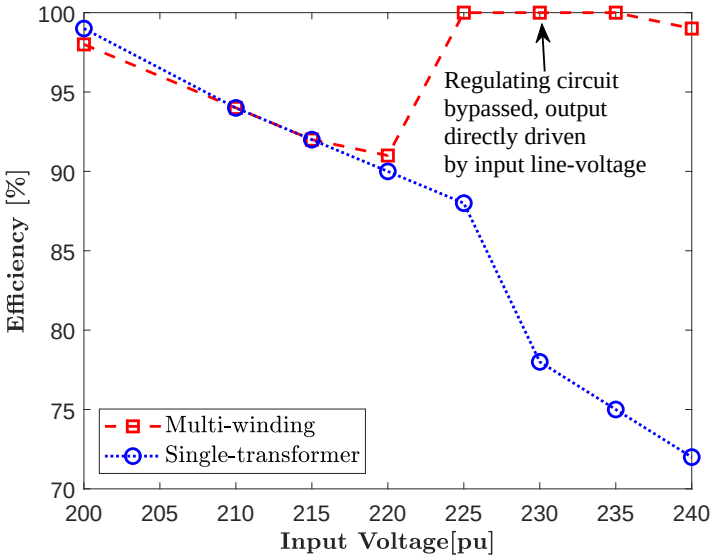


Figure 6.12: Efficiency comparison; multi-winding vs single-transformer designs

wires and secondary losses of other circuit components. Figure 6.14 illustrates the LTspice model of the

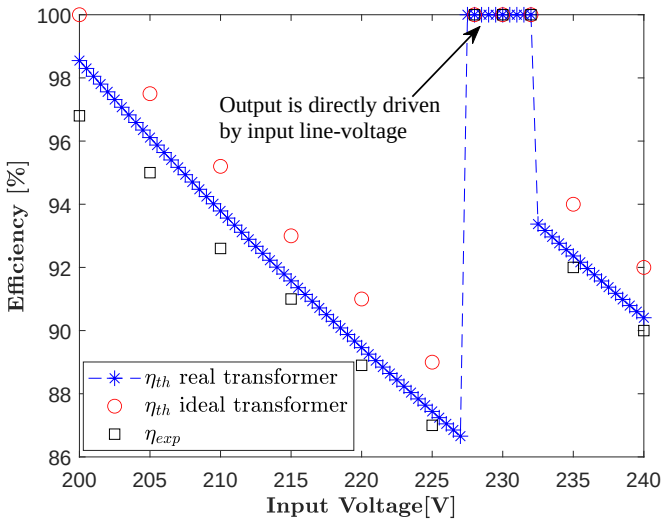


Figure 6.13: Regulator efficiency based on experimental and calculated results

regulator during the buck-mode operation where Primary-2 is responsible for regulating. The figure indicates the real transformer parameters used in both LTspice and MATLAB simulations. Figure 6.15 illustrates the multi-winding regulator efficiency under different load currents. When reconfiguring the tapped-transformer which was already available in the laboratory, the third winding was made using a very thin copper wire of guage AWG 38 that limits the current rating of the prototype. More over, this new winding adds a significant ohmic resistance compared to the other transformer windings.

The line regulation curve for different load currents is presented in Figure 6.16. The region pointed out by the red double-arrow is achieved due to the regulating circuit being bypassed at $\pm 2\%$ of the input line voltage.

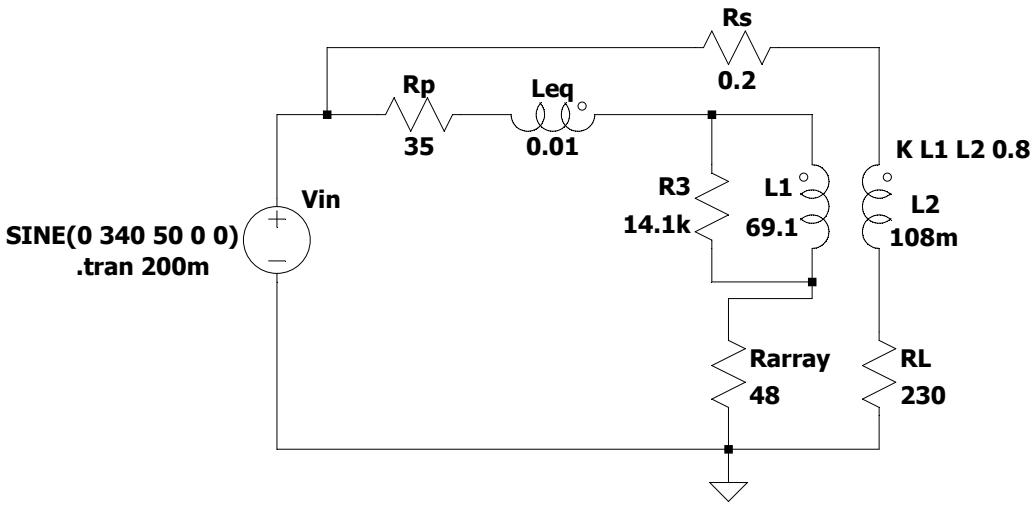


Figure 6.14: LTspice simulation for buck regulation

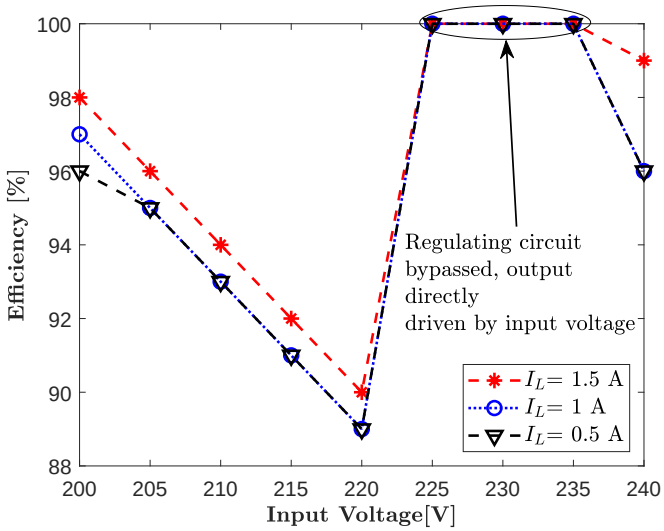


Figure 6.15: Regulator efficiency for different load current

Figure 6.17 displays the input and output waveforms of the multi-winding regulator against waveforms of the basic single transformer design. These were are captured using Tektronix 2000 series oscilloscope. The traces display voltage and current at $V_{\text{out}} = 230$ V and $I_{\text{L}} = 1.5$ A.

Figures. 6.18 and 6.19 indicate the harmonic spectrum of the output voltage waveforms of the two regulator designs. An output waveform distortion is visible in the single-transformer regulator in comparison to the waveform of the multi-winding transformer due to the significant cross-over distortion of the non-linear components used in the design. The significant amount of cross-over distortion adds to the output by the transistor array which improves with increasing load current and array voltage.

Figures 6.20 to 6.22 shows the images of the current prototype.

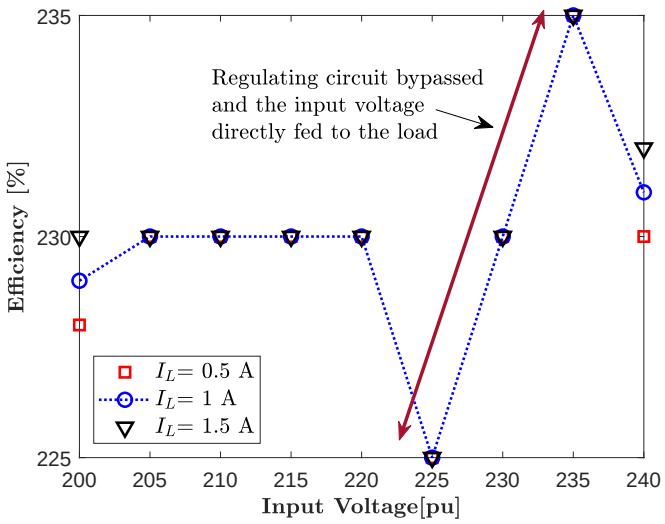
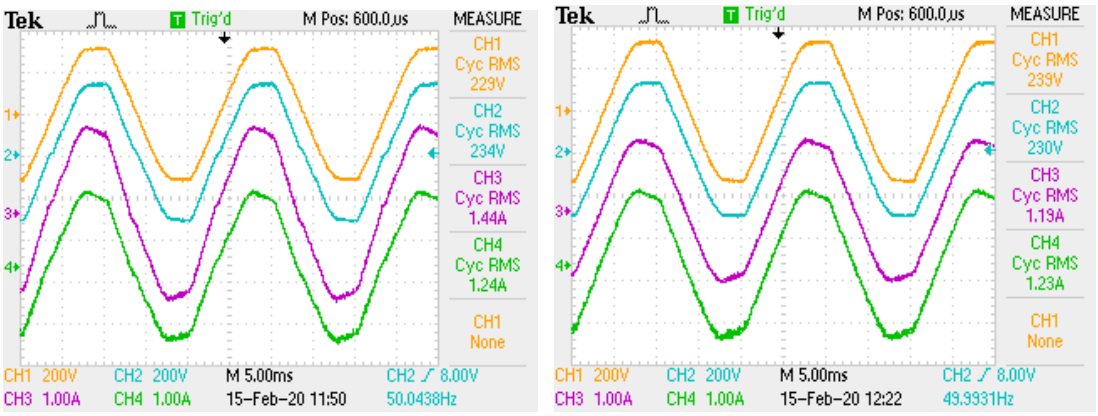


Figure 6.16: Line regulation for different load current



(a) Single-transformer regulator (b) Multi-winding transformer regulator

Figure 6.17: Waveforms of two prototypes; yellow and purple- input parameters; blue and green-output parameters

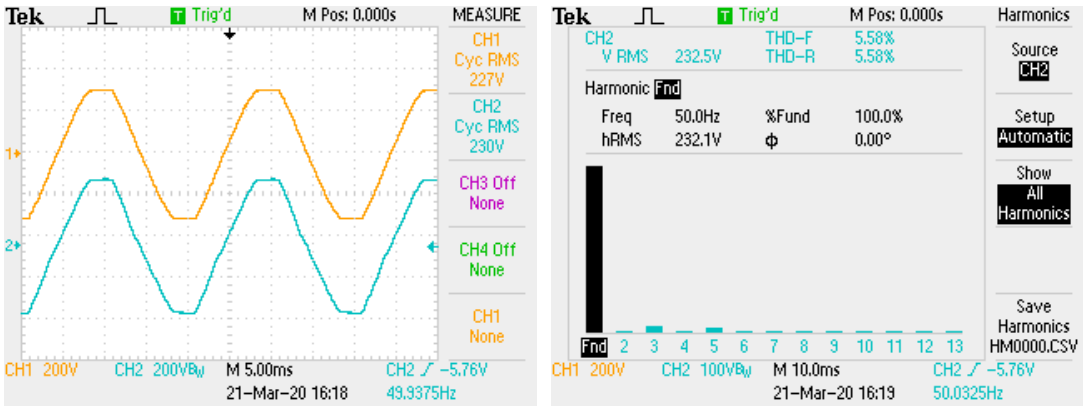


Figure 6.18: Basic single transformer regulator

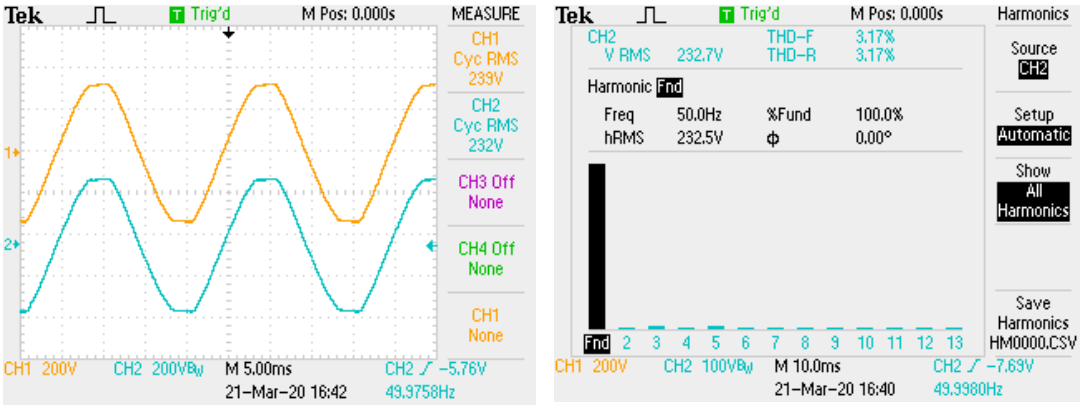


Figure 6.19: Muiti-winding transformer regulator

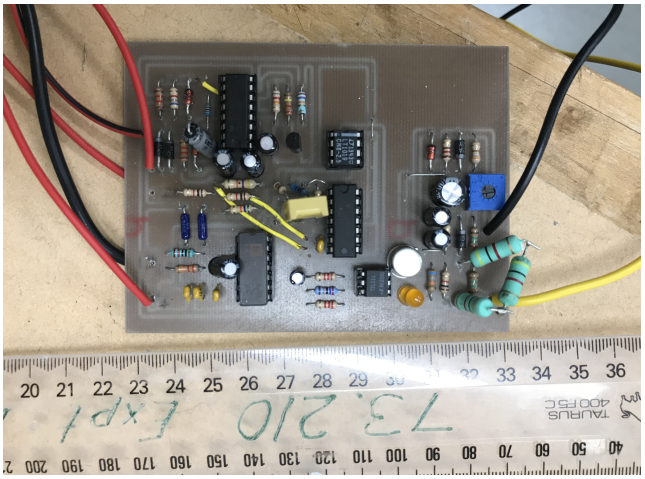


Figure 6.20: Implementation of the control circuit

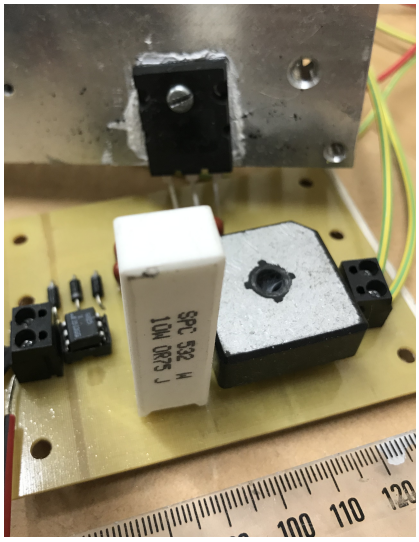


Figure 6.21: Implementation of the single Darlington-pair based AC impedance

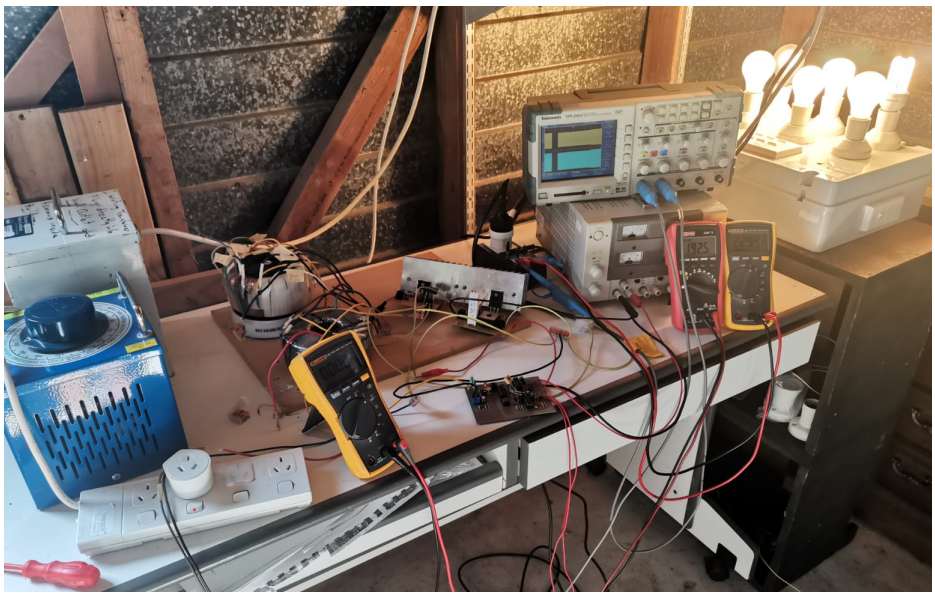


Figure 6.22: Test setup

Chapter 7

Conclusions and Future Work

7.1 Conclusion

Linear RMS AC voltage regulator is a relatively new technique for correcting incoming RMS voltage variations in the power line at the customer premises. The original linear AC technique was developed in $1980's$ to address the significant drawbacks of the well-known RMS AC voltage regulators such as servo-driven variacs, ferro resonant regulators and high-frequency switching based electronic regulators. It is a stand-alone single phase device that is capable of regulating long- and short-duration RMS voltage variations in the power line.

Although, the original linear technique functions well in regulating RMS fluctuations, it has a major drawback of reduced-efficiency when the input line voltage increases beyond the nominal value. The purpose of this thesis is to present potential solutions to overcome this reduced-efficiency issue.

Two potential solutions are presented in the thesis to enhance the efficiency of the linear AC regulator of approximately $15-20\%$ than the original technique. Two techniques are based on (i) multi-transformer and (ii) multi-winding transformer designs. Implementation details of the two prototypes and experimental results are presented followed by a mathematical validation of the results.

Both implementations perform well in regulating RMS variations which has equal or better efficiency compared to traditional RMS AC regulators. Once the commercial consideration related to low frequency transformer are taken into account, the multi-winding transformer technique was more attractive, in the single phase AC regulators in the range of 300 VA $-$ 5 kVA output capacity.

Based on the final results of the prototype developed from the multi-winding transformer technique, the following conclusions can be made.

- Performance efficiency of 90%
- Ability to deliver fast response of approximately 150 ms
- Operation in a wider input voltage ranging from $160-260$ V without any configuration change
- Can be extended in to high power application

7.2 Future Work

Multi-winding transformer regulator maintains regulation by changing transformer windings during the boost- and buck-modes. The current prototype uses a relay based winding change-over circuit which introduces contactor arcing effects when energizing high power loads. It is important to indicate here that this basic relay based circuit was implemented to confirm the winding change-over mechanism of the multi-winding technique at a primary level. In a commercial implementation, it is highly recommended to introduce a soft switching mechanism that does not modify the output waveform during the winding change-over. Since the secondary winding is located in between the input and the output load path, the change-over between secondary windings are very critical, as the connection between the load and the input supply discontinue for a short duration, determined by the operation delay of the switching element. Since the regulator handles AC, a zero-crossing detection circuit can be introduced prior to the switching circuit, where the winding change-over can be implemented during a zero crossing of the supply voltage.

The overall efficiency of the regulator is optimised by the efficiency of the transformer used in the design. Considering the size and the performance, a toroidal core transformer is used when developing the prototype. Different options for transformer cores can be tested to obtain an optimum transformer efficiency, where, the ultimate regulator efficiency will be improved.

A detailed analysis to quantify the diode non-linearities introduced by the transistor array is recommended for future work. As discussed in Chapter 3, the diode non-linearities during low voltage operation of the transistor-array is responsible for cross-over distortion of the output waveform as shown in Figures 6.18 and 6.19. This effect can be improved by harmonic components transmitted in the input line voltage.

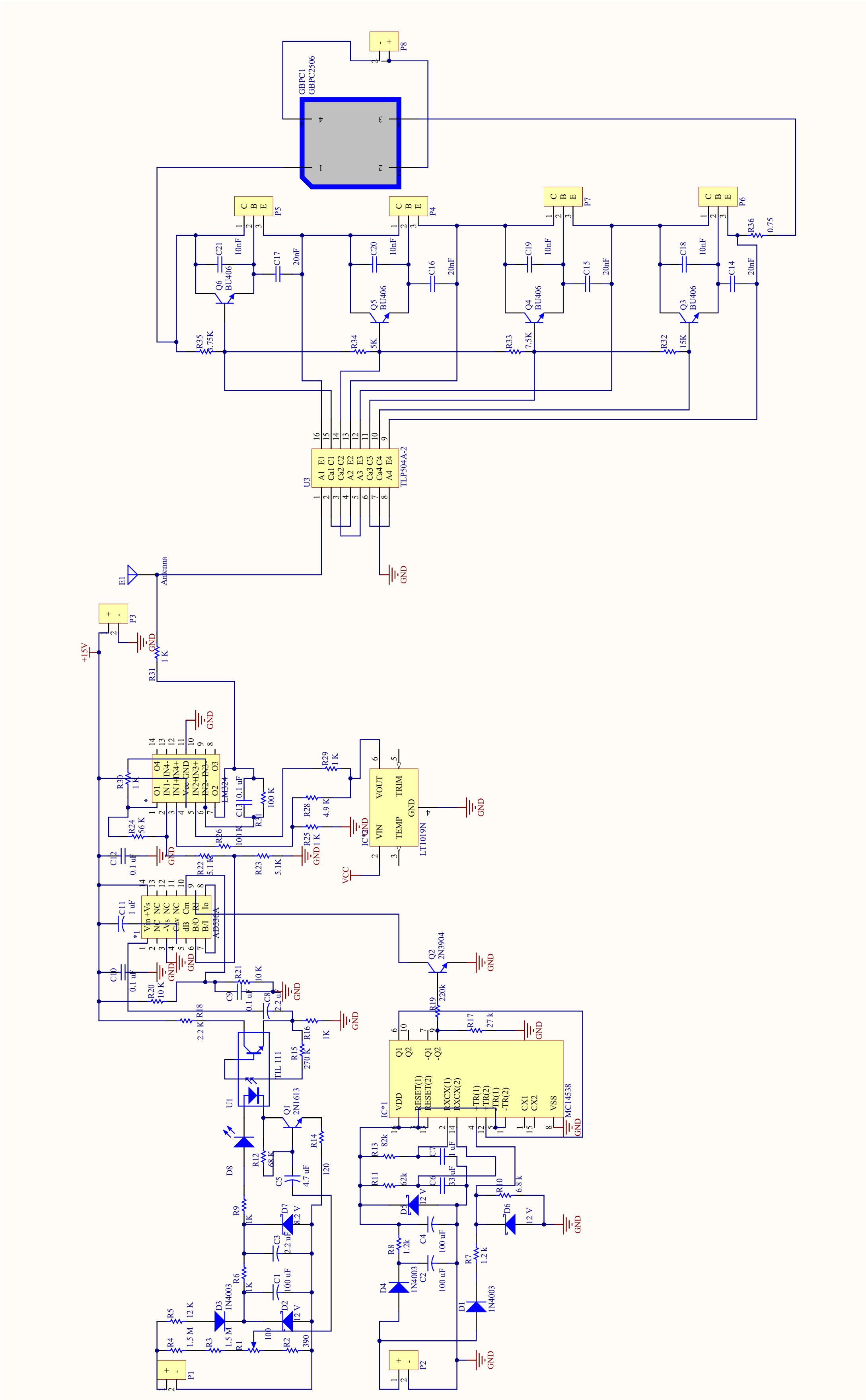
A concise description is included in Chapter 3 to identify the dynamic characteristics of the current gain which determines the dynamic resistance across the collector-emitter terminals of the Darlington pair. The transistor behaviour in the presence of a rectified supply is complex and need precise data to quantify the relationship. However, the analysis of the waveform distortion is beyond the scope of this thesis and future work is encouraged.

Appendix A

Schematic Diagram of the Control Circuit

The PCB diagram of the electronic circuit is designed using the Altium Designer Software. Following PCB contains the digital control circuit including the AC sampling circuit, RMD/DC converter unit, Op-Amp based amplifier circuit and the power transistor-array with opto-isolator based isolator stage to provide galvanic isolation between the low power control circuit and high power handling power transistor-array.

When assembling the final product, the control circuit and the power-transistor board are designed as two separate PCBs where the power-transistor board has been mounted on a heat sink to avoid thermal damage to sensitive electronics.


GBPC1
GBPC2506
P8
P5
P4
P7
P6
C21 10nF
C20 10nF
C19 10nF
C18 10nF
C17 20nF
C16 20nF
C15 20nF
C14 20nF
Q6 BU406
Q5 BU406
Q4 BU406
Q3 BU406
R35 3.75K
R34 5K
R33 7.5K
R32 15K
R36 0.75
U3
TLP504A-2
E1
Antenna
P3
+15V
R31 1 K
LM324
AD536A
LT1019N
MC14538
TIL 111
U1
Q1 2N1613
Q2 2N3904
D1 1N4003
D3 1N4003
D4 1N4003
P1
P2
GND
VCC

Appendix B

Dynamic Behaviour of the Darlington Pair

Figure B.1 illustrates a test setup used to observe the dynamic behaviour of the Darlington pair in the presence of a rectified voltage. Phasor plot in XY plane is observed using Tektronix TPS 2024 isolated channel oscilloscope, as shown in Figure B.2. In this plot, the x-axis represents voltage across the collector-emitter terminals (V_{CE}) and y-axis, the collector current (I_C). The curve represents the dynamic resistance of the Darlington pair at the particular voltage and current illustrated in Figure B.3.

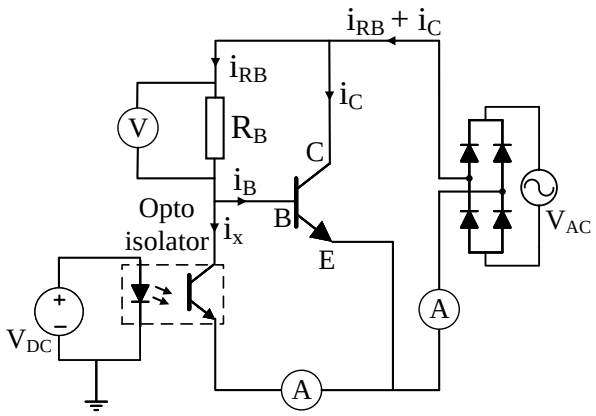


Figure B.1: Test setup for testing under rectified AC

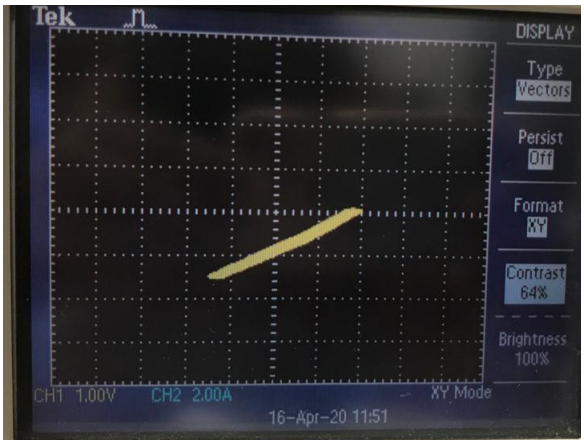


Figure B.2: Phasor plot of I_C vs V_{CE}

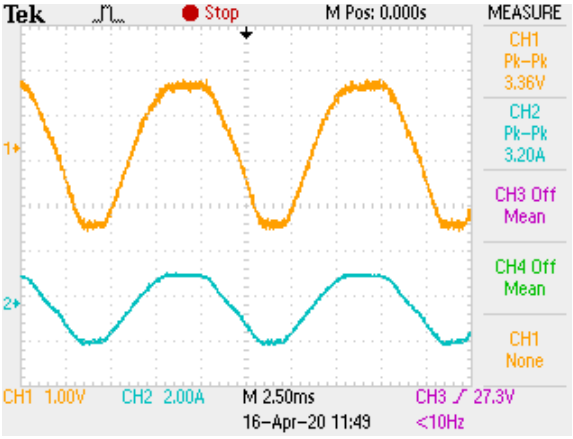


Figure B.3: Waveforms of voltage and current; yellow and blue traces represent voltage and current respectively

Appendix C

Magnetic Properties of a Transformer and Derivation of Basic Equations

In early 19th century, many experimental and theoretical developments of electromagnetic were accomplished by several scientists around the world such as Charles-Augustin de Coulomb, Andre-Marie Ampere, Michael Faraday, Emil Lenz and Franz Ernst Neumann. These experimental results and the theories were summed up by James Clerk Maxwell by writing them down as a set of equations namely the Maxwell equation. Specific parts of these Maxwell equations such as the Ampere's law, Faraday's law, Gauss's law and the Lenz's law are the basis of magnetic circuit analysis and will describe a summary of these equations related to the transformer operation as needed.

Transformers are passive electrical devices that use electromagnetic induction to transfer electrical energy between magnetic circuits. The simplest form of a transformer contains pair of windings usually wound round a core made of ferromagnetic material. The functionality of the transformer windings is based on the Ampere's law followed by the Faraday's law of electromagnetic induction. This section is dedicated to present a brief summary of the transformer operation and derive essential transformer relationships that have been used throughout this research.

C.1 Magnetic Properties of a Transformer

As illustrated in Figure C.1 when an electrical conductor carries a current, a magnetic field is induced around the conductor, which is characterized by its magnetic field intensity, H, the direction of which is explained by the rule of thumb as indicted in the illustration. According to Ampere's law, the magnetic field intensity, H, is defined: the integral of H, around a closed path is equal to the total current passing through the interior of the path [103]. If the currents flow in a coil with N turns, then

$$\oint_l Hdl = \int_S JdS = Ni \tag{C.1}$$

where,

H	- field intensity vector (A/m)
dl	- vector length element pointing int he direction of the path l (m)
J	- electrical current density vector (A/m^2)
dS	- vector area having direction normal to the surface (m^2)
l	- length of the circumference of the contour (m)
S	- surface of the contour (m^2)
i	- coil current (A)

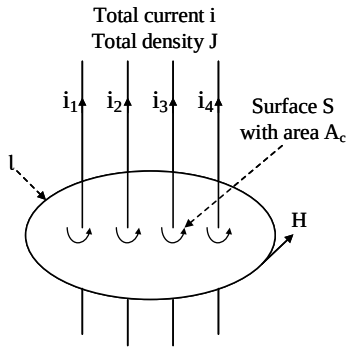


Figure C.1: Illustration of Ampere's law

N - number of the turns

In Eq. (C.1), the term $\oint_l Hdl$ and Ni are equivalent to magneto-motive force, MMF ($A.turns$), which is the driving force in the magnetic circuits that creates flux in the circuit, analogous to EMF in electrical circuits. Thus, the magneto-motive force of a magnetic circuit can be expressed as,

$$MMF = \oint_l Hdl = Ni = \sum_{n=1}^{n} i = i_1 + i_2 + i_3 \tag{C.2}$$

The magnetic field intensity H results to a magnetic flux density B also known as magnetic induction, which is defined as the total magnetic flux through a unit area taken perpendicular to the direction of the magnetic flux [105],

$$B = \mu H \tag{C.3}$$

where, μ is a specific characteristic of the magnetic material and can be written in terms of relative permeability of free space ($\mu_0 = 4\pi \times 10^{-7}$ Hm) and relative permeability of a magnetic material such as $\mu = \mu_0\mu_\mathrm{r}$. The permeability of ferromagnetic material is in the range of hundreds of thousands and are very useful in making magnetic components used in power electronics such as transformer or inductor cores.

As illustrated in Figure C.1, the total magnetic flux passing through the surface S is given by

$$\Phi = \int_S B.dS \tag{C.4}$$

Assuming a uniform flux (B) that is perpendicular to the surface area A_c, Eq. (C.4) simplifies into,

$$\Phi = BA_\mathrm{c} \tag{C.5}$$

Substituting $H = B/\mu$ and $B = \Phi/A_\mathrm{c}$, into Eq. (C.2),

$$MMF = Hl = \Phi\frac{l}{\mu A_\mathrm{c}} \tag{C.6}$$

By using the analogy made between electrical and magnetic circuits, a term called reluctance is introduced which is characterized by the properties of the magnetic material of the core and its physical dimensions and is given by

$$\Re = \frac{l}{\mu A_\mathrm{c}} \tag{C.7}$$

Since the units of MMF is *A.turns* (from Eq. (C.2)), and total flux (Φ) is measured in webers (Wb), the units of reluctance is given by $A.turns/Wb$. In Eq. (C.6), the magneto-motive force, F can be written in terms of reluctance ($\Re$) and total flux (Φ),

$$F = Hl = \Phi\Re \tag{C.8}$$

In Eq. (C.8), the total magnetic flux is analogous to current in electrical circuits, the reluctance $\Re$ is to resistance and the magneto-motive force is to voltage or potential difference.

C.2 Magnetization Process of a Transformer

Ferromagnetic materials exhibit strong magnetism in the same direction of the field when a magnetic field is applied to it. Notably, iron, cobalt, nickel and alloys containing these elements (i.e., alnico contains all three elements) are categorized as ferromagnetic materials for exhibiting strong magnetic field strengths in the presence of an external magnetic field [103, 104]. When we consider a structure of a metal, it contains free electrons that possess an electric charge, own magnetic moment (spin), and orbital moment, caused by its rotation around its own nucleus. The combination of spin and orbital moment establishes magnetic characteristics of the atoms. In many elements, the electrons are arranged in such a way that the net atomic moment is almost zero [105].

In metals, the atomic moments are inter-coupled by inter-atomic forces, and they are arranged in parallel with crystal lattice sites where the moments of individual atoms tend to be summed up and is known as the ferromagnetic effect [104]. These aligned regions within the metal lattice structure are called domains, and they act like tiny magnets called atomic magnets, which is illustrated in Figure C.2. When an external magnetic field is applied to this material, these magnetic domains align to the direction of the applied magnetic field that increases in field strength, and the material is said to be magnetized. Upon removing the external field, the material becomes demagnetized. When the applied external field is kept on increasing, it will result in more domains get aligned, thus, increasing the magnetization and ultimately becomes saturated when all the domains are aligned with the field. Once the ferromagnetic material is saturated, the removal of the external field does not necessarily reorient the domains to its original orientation, causing a residual magnetism left in the material. This is discussed in detail in the following section.

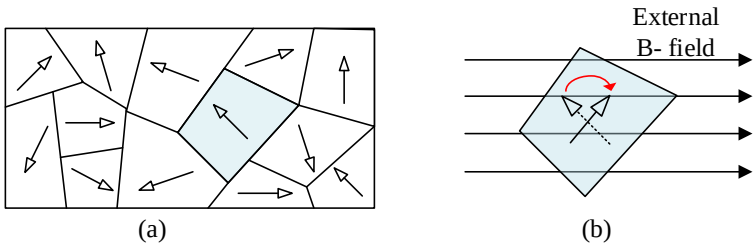


Figure C.2: Magnetic domains (a) neutral material (b) domain reorientation

C.2.1 Hysteresis Loop

As shown in Figure. C.3 (a), a coil is wound around a ferromagnetic core. In the beginning, let us assume the net magnetic flux density, B, magnetic field intensity, H, and the time-varying, excitation-current in the coil is zero [103].

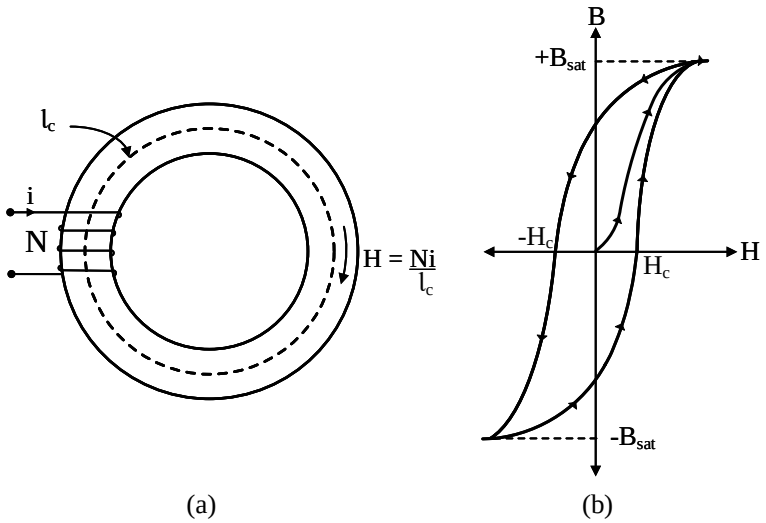


Figure C.3: (a)Test circuit (b) hysteresis loop

When the current, i is gradually increased, at first, the applied field intensity, H and the flux density, B is slowly increased corresponding to the reversible orientation of domain walls, as illustrated in Figure. C.3 (b). After that, the B-field is gradually increased with increasing H, resulting in a much steeper curve [103]. This significant increase of B is due to Barkhausen jumps of domain walls, which happens after a certain level of applied field intensity. After the Barkhausen jump, the domain walls are almost aligned with the external field; further, an increase in field intensity leads to core saturation beyond the point of maximum B, B_{sat} [103].

As the field intensity is decreased, some of the domain walls start to reorient into the first direction, thus, reduces the resultant B-field. Since some domain walls remain unchanged in its orientation, thus, the B-field does not return along the same path as illustrated in the magnetization curve, which results in a hysteresis loop. When H reaches zero, a residual flux density or remanence, B_{r}, remains in the core, that requires a negative or reversed field, H, to remove the residual flux. The negative value of H at which the flux density becomes zero is known as the coercive force of coercivity, H_{c} of the material [103].

According to Faraday's Law, a voltage is induced in a looped wire (a coil) in the presence of a time-varying magnetic flux [104]. If the coil contains N number of turns and assuming the total flux, Φ, links with all the loops, the induced EMF is given by

$$E_{\text{ind}} = -N\frac{d\Phi}{dt} \tag{C.9}$$

Heinrich Lenz defines the polarity of the induced EMF and it is denoted in the above equation by the negative sign [103]. When a current, i, flows through the above coil, it establish flux in the core which is known as self-inductance of the coil and can be written as,

$$L = \frac{N\phi}{i} \tag{C.10}$$

Since $B = \mu H$ and $H = Ni/l$, (C.10) can be rewritten as,

$$L = N\frac{BA}{i} = N\frac{\mu Ni}{li}A = \mu\frac{N^2A}{l} \tag{C.11}$$

Since, $\mu A/l = 1/\Re$, which is defined as the permeance of the magnetic circuit and termed as Λ, thus the above equation becomes,

$$L = N^2\Lambda \tag{C.12}$$

which can also given by

$$L = \frac{N^2}{\Re} \tag{C.13}$$

Permeance of a given core can be considered a constant, thus, the coil inductance is proportional to the turns squared ($L \propto N^2$) [103].

In a two winding transformer, when one coil is energized, it establish flux in the core which links to the coil itself and to the other coil too. This magnetic coupling between the windings of a transformer is known as mutual inductance, M [103]. The mutual inductance of the two windings in Figure 4.1 can be written as,

$$M = \frac{N_1\Phi_{12}}{I_2} = \frac{N_2\Phi_{21}}{I_1} \tag{C.14}$$

where,

Φ_{12} - the magnetic flux linking the primary winding as a result of the current in the secondary winding

Φ_{21} - the magnetic flux linking the secondary winding as a result of the current in the primary winding

Appendix D

Relationships of the Transformer Parameters Of Three Regulator Configurations

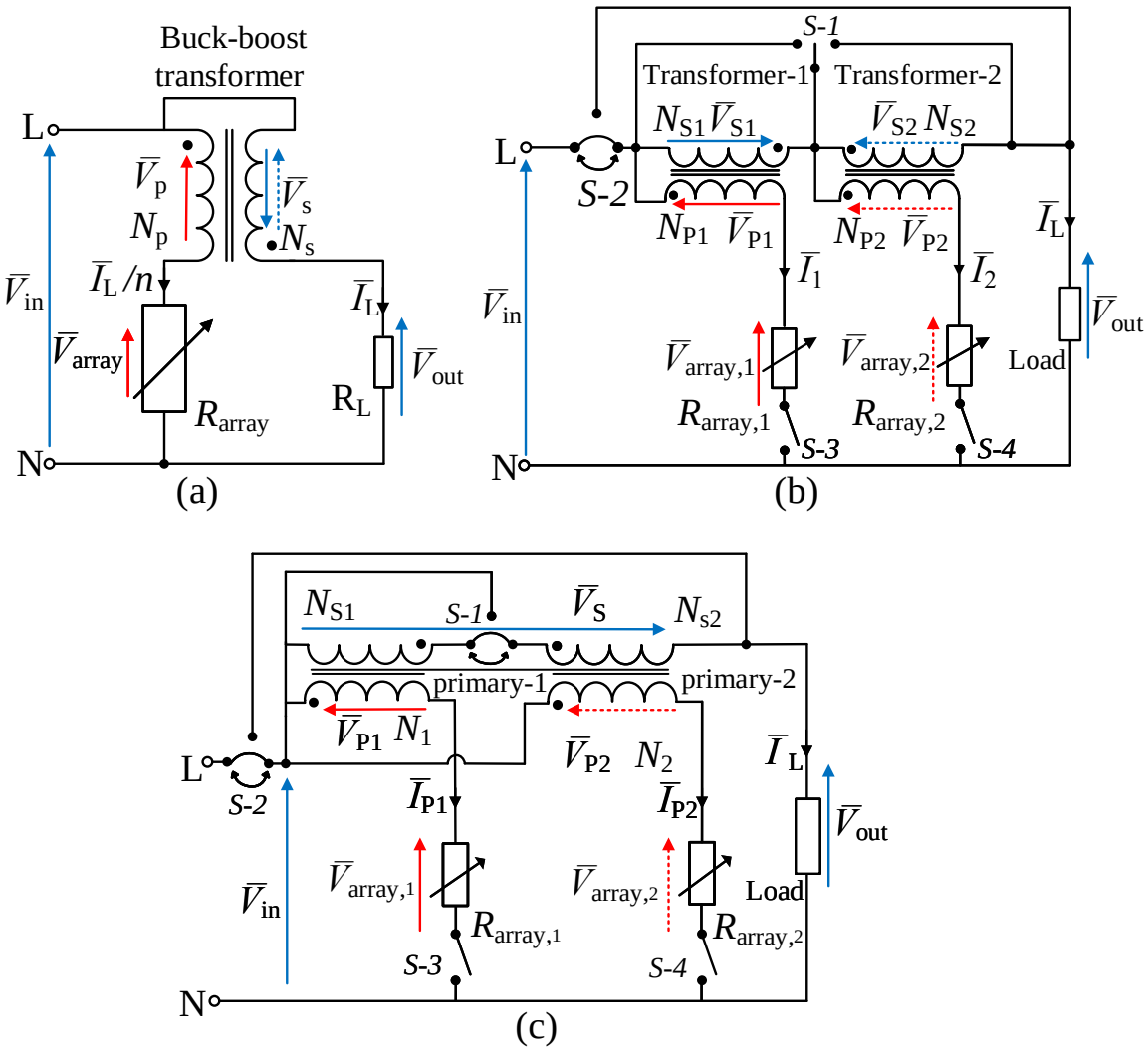


Figure D.1: Circuit diagrams; (a) single transformer two-winding (b) series dual-transformer (c) multi-winding transformer

Table D.1: Theoretical Relationship of the Transformer Parameters of Single-Transformer, Dual-Transformer and Multi-Winding Transformer Regulators

Mode of operation	**Relationships of single transformer configuration (Fig. 4)**	**Relationships of basic two-series transformer configuration (Fig. 5)**		**Relationships of multi-winding configuration (Fig. 6)**
		Transformer-1	**Transformer-2**	
Case 1 $\overline{V}_{in} = \overline{V}_{in}^{min}$ (Transistor-array saturates)	$\overline{V}_{out} = \overline{V}_{in} + \overline{V}_{in}/n_1$ $Z_{array} = 0$ $\overline{V}_{array} = 0$	$\overline{V}_{out} = \overline{V}_{in} + \overline{V}_{s1}$ $Z_{array,1} = 0$ $\overline{V}_{array,1} = 0$	Transformer secondary by-passed $\overline{V}_{array,2} = \overline{V}_{in}^{min}$	Primary-1 operates Secondary-1/Secondary-2 series operation $\overline{V}_{out} = \overline{V}_{in} + \overline{V}_{s}$ $Z_{array} = 0$ and $\overline{V}_{array} = 0$
Case 2 $\overline{V}_{in} < \overline{V}_{nom}$ $[\overline{V}_{nom} = \overline{V}_{out}^{reg}]$ (Boost Mode)	$\overline{V}_{out} = \overline{V}_{in} + \overline{V}_{s}$ $\overline{V}_{p} = n\,\overline{V}_{s}$ $\overline{V}_{array} = \bar{I}_L/n \cdot Z_{array}$ $= \overline{V}_{in} - \overline{V}_{p}$ $Z_{array} > 0$ Transformer sec. acts as a booster	$\overline{V}_{\mathbf{out}} = \overline{V}_{\mathbf{in}} + \overline{V}_{\mathbf{s1}} - \overline{V}_{\mathbf{s2}}$ $\overline{V}_{array,1} = \bar{I}_L/n_1 \cdot Z_{array,1}$ $= \overline{V}_{in} - \overline{V}_{p1}$ $Z_{array,1} > 0$ Transformer sec. acts as a booster	$\overline{V}_{array,2} = \bar{I}_L/n_2 \cdot Z_{array,2}$ $= \overline{V}_{in} + \overline{V}_{s1} + \overline{V}_{p2}$ $Z_{array,2} > 0$ Transformer sec. in buck mode	Primary-1 operates Secondary-1/Secondary-2 series operation $\overline{V}_{out} = \overline{V}_{in} + \overline{V}_{s}$ $\overline{V}_{s} = \overline{V}_{s1} \pm \overline{V}_{s2}$ $0 \geq Z_{array,1}, Z_{array,2} > \infty$
Case 3 $\overline{V}_{in} = \overline{V}_{in}^{nom}$ (Transistor-array cut-off)	$\overline{V}_{out} = \overline{V}_{nom}$ $\overline{V}_{array} = \overline{V}_{in}^{nom}$ No boost / no buck	Transformer secondary by-passed $\overline{V}_{array} = \overline{V}_{in}^{nom}$ No boost / no buck		Secondary windings by-passed $\overline{V}_{array} = \overline{V}_{in}^{nom}$ No boost / no buck
Case 4 $\overline{V}_{in} > \overline{V}_{out} > \overline{V}_{in}^{max}$ (Buck Mode)	$\overline{V}_{p} = n\overline{V}_{s}$ $\overline{V}_{array} = \bar{I}_L/n \cdot Z_{array}$ $= \overline{V}_{in} + \overline{V}_{p}$ Z_{array} is kept high by the feedback loop	Transformer secondary by-passed $\overline{V}_{array,1} = \overline{V}_{in}$	$\overline{V}_{out} = \overline{V}_{in} - \overline{V}_{s2}$ $\overline{V}_{array,2} = \bar{I}_L/n_2 \cdot Z_{array,2}$ $Z_{array,2} \geq 0$ if $\overline{V}_{in} = \overline{V}_{in}^{max}$, $Z_{array,2} = 0$	Primary-2 operates Secondary-2 operates $Z_{array,2} \geq 0$

Appendix E

Transformer Tests

This appendix shows the steps of transformer open and short circuit tests and to calculate the transformer parameters based on the test results [104, 107].

E.1 Short Circuit Test

A short circuit is placed across the transformer secondary while supplying a voltage to the primary winding in the range of $3-15\%$ of rated voltage at rated frequency, which is sufficient to establish a rated current in the secondary winding. As per Figure E.1(a), a voltmeter, ammeter and a power analyser (or wattmeter) is inserted on the primary side while an ammeter across the secondary winding. Starting from zero, the primary voltage, V_{sc}, is increased until the rated current appears on the ammeter in the secondary side. The measurements are taken in the primary winding and refer the secondary quantities when needed. Following are the measurement taken during the short-circuit test;

- V_{sc} short-circuit primary voltage
- I_{sc} short-circuit primary (rated) current
- P_{sc} short-circuit power

During the short-circuit test, the excitation branch is ignored as a negligible current flows through it due to low input voltage. The series impedance of primary and secondary windings are significant in this test and the corresponding equivalent circuit is illustrated in Figure E.1(b). Using the recorded data, the following equations solve for the series equivalent impedance, Z_{eq} including the copper loss (R_{eq}) and the leakage reactance (X_{eq}).

$$Z_{sc} = Z_{eq} = \frac{V_{sc}}{I_{sc}} \tag{E.1}$$

The real part of Z_{eq} is the equivalent resistance representing copper loss of two windings. According to the above illustration, this equivalent resistance is the addition of the primary winding resistance and the secondary winding resistance reflected into the primary side. If the primary to secondary turns ratio is n:

$$R_{eq} = \frac{P_{sc}}{I_{sc}^2} \tag{E.2}$$

$$= (R_1 + n^2 R_2) \tag{E.3}$$

The imaginary part of Z_{eq} is the equivalent leakage reactance of the two windings.

$$X_{eq} = \sqrt{(Z_{eq}^2 - R_{eq}^2)} \tag{E.4}$$

$$= (X_{\sigma 1} + n^2 X_{\sigma 2}) \tag{E.5}$$

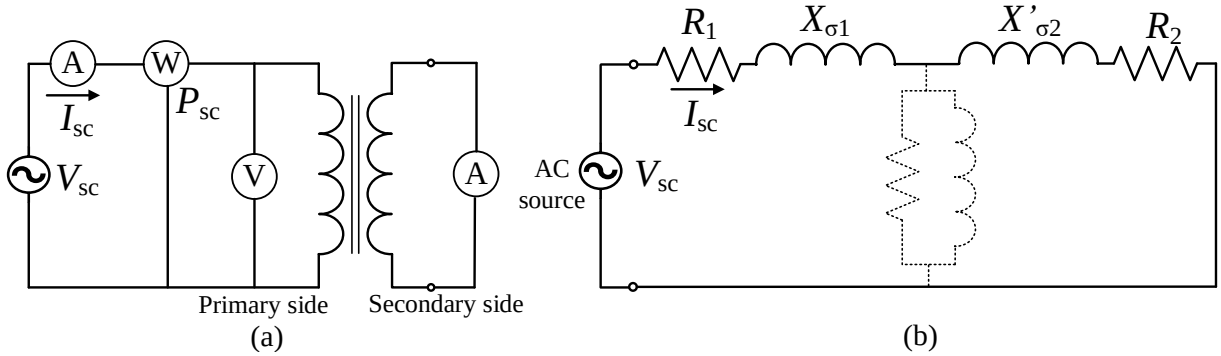


Figure E.1: Transformer short-circuit test

E.2 Open Circuit Test

The rated voltage at rated frequency is applied across the primary winding while the secondary winding open circuited during the open-circuit test. The excitation current flows through the primary winding which is in the order of tens of milliamperes, thus the voltage drop across the series impedance is very small and negligible compared to the significant shunt branch elements including the core loss (R_c) and the magnetizing reactance (X_m). As illustrated in the Figure E.2(a), the ammeter, voltmeter and a power analyser (or wattmeter) is placed in the primary winding and following measurements are taken in order to deduce the core parameters using the equations given below. Figure E.2(b) indicates the corresponding equivalent circuit.

- V_{oc} open-circuit primary (rated) voltage
- I_{oc} open-circuit primary current
- P_{oc} open-circuit power

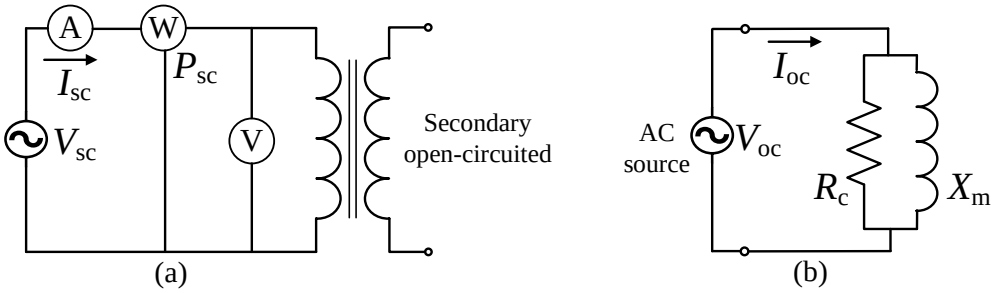


Figure E.2: Transformer open-circuit test

$$\frac{1}{Z_{oc}} = \frac{1}{R_c} + \frac{1}{jX_m} \tag{E.6}$$

$$\frac{1}{Z_{oc}} = \frac{I_{oc}}{V_{oc}} \tag{E.7}$$

The core-resistance is:

$$R_c = \frac{V_{oc}^2}{P_{oc}} \tag{E.8}$$

The magnetizing reactance is:

$$X_m = \frac{1}{\sqrt{\frac{1}{Z_{oc}^2} - \frac{1}{R_c^2}}} \tag{E.9}$$

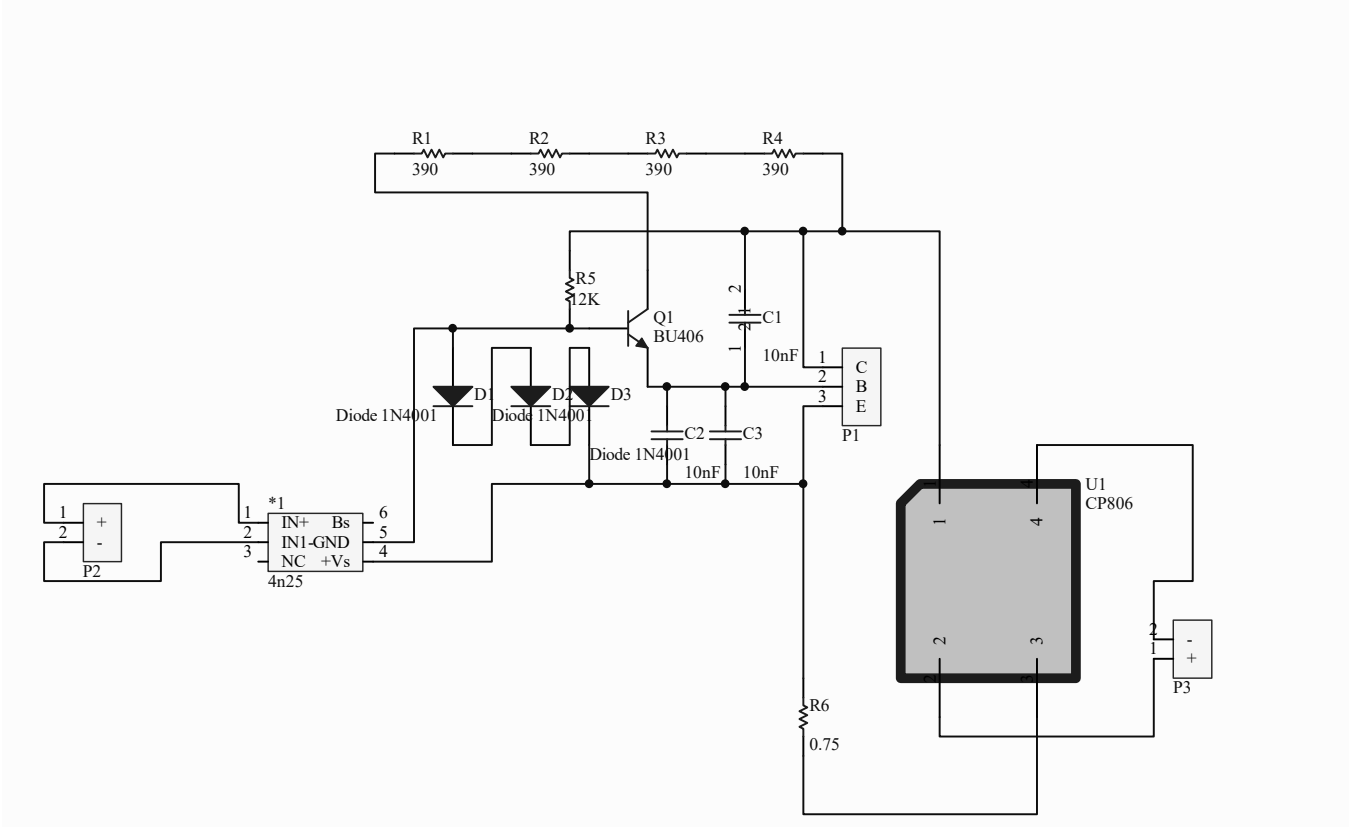
The open-and short-circuit tests may be performed on either side of the transformer, high voltage or low voltage side (primary or secondary) and will yield the same results. The choice is based on the available voltage source or the convenience of working at particular voltage and current levels and availability of reliable measuring equipment with suitable precision and accuracy. For an example, the open-circuit current or the excitation current measured in the primary or high voltage winding is very critical as it is usually in the order at tens of milliamperes.

During open-circuit test, if the low voltage side (or secondary) is fed with the rated voltage, the open terminals will be at higher voltage. And if the short-circuit test is performed in the low voltage side (or secondary) where the readings are taken in that winding, the high voltage side terminals (or primary terminals) should be short-circuited. The readings are now referenced to the low voltage side (or secondary side).

Appendix F

Single Darlington Pair Based Power Stage

The PCB diagram of the single Darlington pair based power stage is designed using the Altium Designer Software.



Appendix G

MATLAB codes

This appendix shows programming codes used to generate efficiency graphs related to the dual-transformer regulator. The program codes are written using MATLAB R2017b software. Similar syntax was used to generate graphs in Chapter 6 with updated values for the multi-windings of the transformer; thus, are not given here.

MATLAB code 1

```
% Efficiency comparison between basic single-transformer two-winding
% regulator and the series dual-transformer regulator

x=[0.85 0.9 0.95 1 1.05 1.1 1.15]; % Per-unit values of line voltage
y1=[99 94 90 100 99 94 93];         % Efficiency for series-Dual-transformer
y2=[99 94 90 86 83 80 78];            % Efficiency for two-winding

% plot the graphs
plot(x,y1,'s--', 'LineWidth',1.5,'Color', 'b', 'MarkerSize',8)
hold on           % hold previous plot
plot(x,y2,'o:','LineWidth',1.5, 'Color', 'r', 'MarkerSize',8)

% Set graph properties
ax = gca; set(ax,'FontSize',12);
xlabel('\bf Input Voltage[V]', 'fontsize', 13,'interpreter','latex');
ylabel('\bf Efficiency [\%]','fontsize', 13,'interpreter','latex');
h=legend({'Series dual-transformer','Single-transformer'},...
'FontSize',13,'Location', 'Southwest'), hold off
set(h, 'interpreter', 'latex')

% Create textarrow
annotation('textarrow',[0.558928571428571 0.523214285714286],...
[0.742857142857143 0.914285714285715],'LineWidth',1);

% Create textbox
annotation('textbox',...
```

```
[0.438499999999999 0.497619047619048 0.482928571428572 0.259523809523811],...
'String',{'Array bypassed and',' output is directly driven',...
'by input line voltage'},...
'LineStyle','none',...
'FontSize',13,...
'FontName','Times New Roman',...
'FitBoxToText','off');

% print the graph in PDF
print ('efficiency_curve_1A','-dpdf','-r300')
```

MATLAB code 2

```
% Dual-transformer regulator efficiency calculation
% using real transformer parameters
clear all;
% Declaring the constants used in the equations
ep = 200:0.5:240;       % Input voltage range in volts
IL= 1;                  % Load current 1A
Vo = 230;               % Nominal output voltage
Pout = Vo*IL;           % Power output
Re_1= 1613.7;           % Transformer-1 Reluctance
Re_2= 2395.6;           % Transformer-2 Reluctance
N_1= 293;               % Transformer-1 primary number of turns
N_2=360;                % Transformer-2 primary number of turns
n_1=200/30;             % Transformer-1 turns-ratio
n_2=240/10;             % Transformer-2 turns-ratio
f=50;                   %Line-frequency

% for loop to calculate regulator efficiency for boost- and buck-modes
for jj = 1:length(ep)
 if ep(jj) >= 200 && ep(jj) <= 227.4        % Calculate regulator efficiency
    P(jj)= ep(jj)/ (4.44*N_1*f);            % at boost mode.
    I(jj)= IL + ((P(jj)*Re_1)/N_1 + IL/n_1);
    Pin = ep(jj)*I(jj);
    eta(jj)=(Pout/Pin)*100;
 elseif ep(jj) >= 227.5 && ep(jj) <= 232.4  % Calculate regulator efficiency during
   I(jj)= IL;                               % the acceptable input voltage range.
   eta(jj)=(ep(jj)/ep(jj))*100;
 else ep(jj) >= 232.5                       % Calculate regulator efficiency
   P(jj)= ep(jj)/ (4.44*N_2*f);             % at buck mode.
```

```
   I(jj)= IL +  (P(jj)*Re_2)/N_2 + IL/n_2;
   Pin = ep(jj)*I(jj);
   eta(jj)=(Pout/Pin)*100;
 end
end
% end of for loop

% Plot the efficiency graphs
figure;
plot(ep,eta,'*--', 'Color', 'r', 'MarkerSize',8) % Theoretical efficiency
hold on                                  % with real transformer parameters
x1=[200 205 210 215 220 225 228 230 232 240];  % input voltage
y1=[100 97.5 95.2 93 91 89 100 100 100 92];    % Theoretical efficiency
                                                % for ideal transformer
y2=[96.8 95 92.6 91 88.9 87 100 100 100 88];   % Experimental values
plot(x1,y1,'o', 'Color', 'blue', 'MarkerSize',8) % Shows raw data points
hold on           % hold previous plot
plot(x1,y2,'s', 'Color', 'black', 'MarkerSize',8)% Shows raw data points
hold on

% Set graph properties
ax = gca; set(ax,'FontSize',12);
xlabel('\bf Input Voltage[V]', 'fontsize', 13,'interpreter','latex');
ylabel('\bf Efficiency [\%]','fontsize', 13,'interpreter','latex');
h=legend({'$\eta_{th}$ real transformer','$\eta_{th}$ ideal transformer',...
 '$\eta_{exp}$'}),
hold off;
set(h,...
'Position',[0.136309523809524 0.129365076853169 0.370326251835551
0.160476187410809],...
'Interpreter','latex','FontSize',13);

% Create textbox
annotation('textbox',...
[0.310714285714286 0.67857142857143 0.342857142857143 0.116666666666669],...
'String',{'Output is directly driven','by input line-voltage'},...
'LineStyle','none','FontSize',13,'FontName','Times New Roman',...
'FitBoxToText','off');

% Create textarrow
annotation('textarrow',[0.5875 0.680357142857143],...
[0.776190476190476 0.904761904761905],'LineWidth',1);
```

```
% print the graph in PDF
print ('efficiency_theory_vs_experimental','-dpdf','-r300')
```

MATLAB code 3

```
% Dual-Transformer regulator efficiency comparison for different load currents
x=[200 205 210 215 220 225 230 235 240];
y1=[99 97  94  92  91  100 100 100 98];    % 1.5 A load current
y2=[98 95  93  92  89  100 100 100 98];    % 1 A load current
y3=[96 95  93  91  89  100 100 100 96];     % 500mA load current


% plot the graphs
plot(x,y1,'o:','linewidth',1.5,'Color', 'r', 'MarkerSize',8)
hold on           % hold previous plot
plot(x,y2,'v--','linewidth',1.5,'Color', 'black', 'MarkerSize',8)

% Set graph properties
ax = gca; set(ax,'FontSize',12);
xlabel('\bf Input Voltage[V]', 'fontsize', 13,'interpreter','latex');
ylabel('\bf Efficiency [\%]','fontsize', 13,'interpreter','latex');
lgd=legend('1 A load current','500 mA load current','Location', 'Southwest');
set(lgd,'FontSize', 13, 'interpreter','latex');
hold off

% Create textbox
annotation('textbox',...
[0.631357142857141 0.164285714285716 0.245428571428573 0.259523809523813],...
'String',{'Output is directly','driven by input','line-voltage'},...
'LineStyle','none',...
'FontSize',13,...
'FontName','Times New Roman',...
'FitBoxToText','off');
```

```
% Create arrow
annotation('arrow',[0.746428571428571 0.716071428571429],...
[0.419047619047619 0.894977168949772],'LineWidth',1.5);

% print the graph in PDF
print ('dual_transformer_efficiency','-dpdf','-r300')
```

Appendix H

Real transformer Parameter Calculation

Calculation of the transformer parameters used by the dual-transformer technique

Using real transformer parameters in Table 5.3, calculation of real transformer parameters for Transformer-2 is shown below.

Estimation of the series components of the transformer equivalent model illustrated in Figure H.1 and H.2.

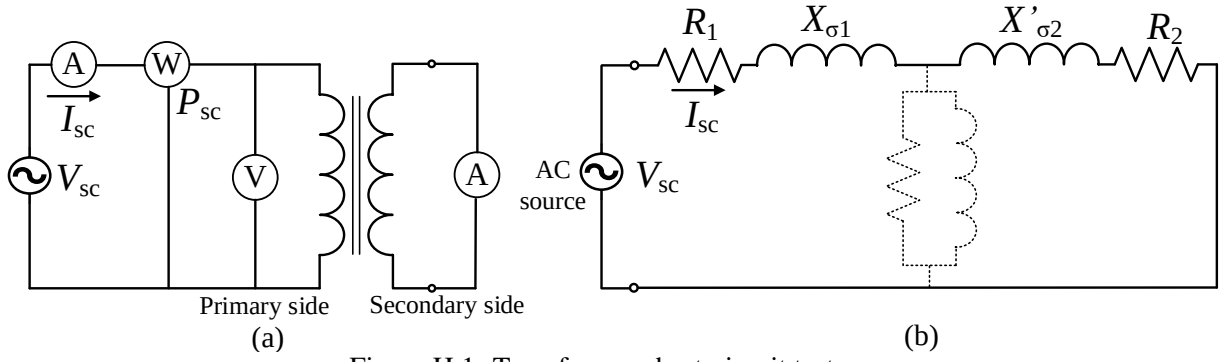


Figure H.1: Transformer short-circuit test

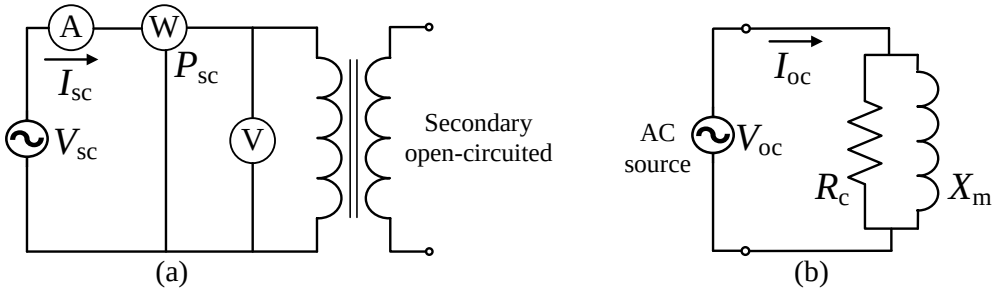


Figure H.2: Transformer open-circuit test

$$Z_{sc} = Z_{eq} = \frac{V_{sc}}{I_{sc}} = \frac{11.4}{1.07} = 10.65\ \Omega \tag{H.1}$$

The equivalent copper loss, R_{eq}

$$R_{eq} = \frac{P_{sc}}{I_{sc}^2} = \frac{12}{1.07^2} = 10.48\ \Omega \tag{H.2}$$

Equivalent leakage reactance X_{eq}

$$X_{\text{eq}}\sqrt{(Z_{\text{eq}}^2 - R_{\text{eq}}^2)} = \sqrt{(10.65^2 - 10.5^2)} = 1.89\ \Omega \tag{H.3}$$

Thus the leakage inductance at 50Hz frequencies given by

$$L_{\text{eq}} = \frac{1.89}{2 \times \Pi \times 50} = 6\ \text{mH} \tag{H.4}$$

Estimation of the excitation branch.

$$Z_{\text{oc}} = \frac{V_{\text{oc}}}{I_{\text{oc}}} = \frac{237.3}{0.02} = 11.8\ k\Omega \tag{H.5}$$

Transformer core-loss resistance,

$$R_{\text{c}} = \frac{V_{\text{oc}}^2}{P_{\text{oc}}} = \frac{237.3^2}{3.4} = 16.6\ k\Omega \tag{H.6}$$

$$\begin{aligned} X_{\text{m}} &= \frac{1}{\sqrt{\frac{1}{Z_{\text{oc}}^2} - \frac{1}{R_{\text{c}}^2}}} \\ &= \frac{1}{\sqrt{\frac{1}{11.8^2} - \frac{1}{16.6^2}}} \\ &= 16.8\ \text{k}\Omega \end{aligned} \tag{H.7}$$

Magnetizing inductance is given by

$$L_{\text{m}} = \frac{16.8}{2 \times \Pi \times 50} = 53.5\ \text{H} \tag{H.8}$$

Estimation of the coupling coefficient.
The self-inductance of the primary (L_1) and secondary (L_2)

$$L_1 = L_\sigma 1 + L_{\text{m1}} = 6 \times 10^{-3} + 53.5 = 53.51\ \text{H} \tag{H.9}$$

The mutual inductance, M is given by Eq. (C.14)

$$\begin{aligned} M &= \frac{L_{\text{m1}}}{n_1} \\ &= 53.5/3.5 = 2.276\ \text{H} \end{aligned} \tag{H.10}$$

The secondary self-inductance can be calculated as,

$$\begin{aligned} L_2 = L_\sigma 2 + L_{\text{m2}} &= 6/n_2 + M/n_2 \\ &= \frac{6x10^{-3}}{23.5} + \frac{2276}{23.5} \\ &= 93\text{mH} \end{aligned} \tag{H.11}$$

Coupling coefficient of Transformer-2, k_2

$$\begin{aligned} k_2 &= \frac{M}{\sqrt{L_1 \times L_2}} \\ &= \frac{2.23}{\sqrt{53.51 \times 0.09}} \\ &= 0.98 \end{aligned} \tag{H.12}$$

Estimation of the transformer efficiency,η

$$\begin{aligned} \text{Transformer Losses} &= \text{Core loss} + \text{copper loss} \\ &= V_p I_e sin\theta + I_1^2 R_{\text{eq}} \\ &= 238 \times 21.2 \times 10^{-3} \times sin(45) + 1/23.5 \times 10.48^2 \\ &= 3.56 + 0.45 \\ &= 4 \text{ W} \end{aligned} \tag{H.13}$$

$$Input\,power = V_{\text{in}} \times I_{\text{in}} \times PF \tag{H.14}$$

Transformer efficiency for 1 A load current, and 240 V input voltage,

$$\begin{aligned} \eta &= 1 - \frac{Losses}{PowerInput} \\ &= 1 - \frac{4}{240 \times 0.9 \times 0.71} \\ &= 97.5\% \end{aligned} \tag{H.15}$$

Calculation of parameters of the multi-winding transformer.

The following parameter estimation is based on the winding configuration during the boost-mode regulation where Primary-1/Secondary-1 is in operation.

Estimation of series transformer components,

$$Z_{\text{sc}} = Z_{\text{eq}} = \frac{V_{\text{sc}}}{I_{\text{sc}}} = \frac{16.8}{0.97} = 17.32\ \Omega \tag{H.16}$$

The copper loss;

$$R_{\text{eq}} = \frac{P_{\text{sc}}}{I_{\text{sc}}^2} = \frac{16}{0.97^2} = 17.00\ \Omega \tag{H.17}$$

$$X_{\text{eq}} \sqrt{(Z_{\text{eq}}^2 - R_{\text{eq}}^2)} = \sqrt{(17.32^2 - 17^2)} = 3.31\ \Omega \tag{H.18}$$

Equivalent leakage inductance;

$$L_{\text{eq}} = \frac{3.31}{2 \times \Pi \times 50} = 10.5\ mH \tag{H.19}$$

Estimation of excitation branch components.

The core impedance;

$$\begin{aligned}\frac{1}{Z_{\text{oc}}} &= \frac{I_{\text{oc}}}{V_{\text{oc}}} \\ &= \frac{0.02}{199.3}\end{aligned} \tag{H.20}$$

Thus;

$$Z_{\text{oc}} = 9965\ \Omega$$

The core-loss resistance;

$$R_{\text{c}} = \frac{V_{\text{oc}}^2}{P_{\text{oc}}} = \frac{199.3^2}{3.2} = 12412.6\ \Omega \tag{H.21}$$

The magnetizing reactance;

$$X_{\text{m}} = \frac{1}{\sqrt{\frac{1}{Z_{\text{oc}}^2} - \frac{1}{R_{\text{c}}^2}}} = \frac{1}{\sqrt{\frac{1}{9965^2} - \frac{1}{12412.6^2}}} = 16.715\ \text{k}\Omega \tag{H.22}$$

Magnetizing inductance;

$$L_{\text{m}} = \frac{16715}{2 \times \Pi \times 50} = 53.2\ \text{H} \tag{H.23}$$

The self-inductance of the primary winding;

$$L_1 = L_\sigma 1 + L_{\text{m1}} = 10.5\ \text{mH} + 53.2\ \text{H} = 53.21\ \text{H} \tag{H.24}$$

The mutual inductance;

$$M = L_{\text{m1}}/n_1 = 53.2\ \text{H}/6.7 = 7.94\ \text{H} \tag{H.25}$$

The secondary self-inductance;

$$\begin{aligned}L_2 = L_\sigma 2 + L_{\text{m2}} &= 10.5/n_1 + M/n_1 \\ &= 10.5 \times 10^{-3}/6.7 + 7.94/6.7 \\ &= 1.57 \times 10^{-3} + 1.190 \\ L_2 &= 1.2\ \text{H}\end{aligned} \tag{H.26}$$

Coupling coefficient of the transformer,

$$\begin{aligned}k_1 &= \frac{M}{\sqrt{L_1 \times L_2}} \\ &= \frac{7.94}{\sqrt{53.21 \times 1.20}} \\ &= 0.99\end{aligned} \tag{H.27}$$

Estimation of the transformer efficiency during boost-mode regulation.

$$\begin{aligned}\text{Efficiency at full load}\ , \eta &= \frac{\text{Output power}}{\text{Input power}} \times 100\% \\ \text{Output power} &= \text{Input power} - \text{Losses}\end{aligned} \tag{H.28}$$

$$\begin{aligned} \text{Losses} &= \text{Core loss}(V_p I_e sin\theta) + \text{Copper loss}(I_1^2 R_{\text{eq}}) \\ &= 199.3 \times 21.2 \times 10^{-3} \times sin(42)^\circ + 1/6.7 \times 17.32 \\ &= 2.79 + 0.38 = 3.17 \text{ W} \end{aligned} \tag{H.29}$$

If the power factor is 0.73, transformer efficiency;

$$\eta = \left(1 - \frac{\text{Losses}}{V_{\text{in}} I_{\text{in}} cos\theta}\right) = 1 - \frac{3.17}{200 * 1.2 * 0.73} \qquad = 98\% \tag{H.30}$$

Appendix I

Microprocessor Code

```
//initilise variables
int aPin=A0;
int s1Pin=11;
int s2Pin=12;
int s3Pin=13;
int s4Pin=14;
int readVal;
float V2;


void setup() {
// declare inputs and outputs
Serial.begin(9600);
pinMode(aPin,INPUT);  //set A0 as input
pinMode(s1Pin,OUTPUT); //set PD5 as output
pinMode(s2Pin,OUTPUT); //set PD6 as output
pinMode(s3Pin,OUTPUT); //set PD7 as output
pinMode(s4Pin,OUTPUT); //set PB0 as output
}

// main code
void loop() {
// put your main code here, to run repeatedly:
readVal=analogRead(aPin); //read analog values from pin A0
V2=(readVal*.2395); //converts analog value into input AC supply value

if (V2<2) {
digitalWrite(s1Pin, LOW);
digitalWrite(s2Pin, LOW);
digitalWrite(s3Pin,HIGH);
```

```
digitalWrite(s4Pin,LOW);

}
if (V2>=2 && V2<=3){
digitalWrite(s1Pin, HIGH);
digitalWrite(s2Pin,LOW);
digitalWrite(s3Pin,LOW);
digitalWrite(s4Pin,LOW);
}
if (V2>3) {
digitalWrite(s1Pin, LOW);
digitalWrite(s2Pin, HIGH);
digitalWrite(s3Pin,LOW);
digitalWrite(s4Pin,HIGH);

}

}
```

References

[1] A. Bendre, D. Divan, W. Kranz, and W. Brumsickle, "Equipment failures caused by power quality disturbances," in *Industry Applications Conference, 39th IAS Annual Meeting. Conference Record of the IEEE*, vol. 1, Seattle, WA, USA, 2004.

[2] "What is power quality?" Electric Power Research Institute, Technical Report, December 2004. [Online]. Available: https://www.epri.com/#/pages/product/000000000001017101/?lang=en-US

[3] C. Sankaran, *Power quality*. CRC press, 2001.

[4] "Tnranspower planning report 2020," July 2020, transower New Zealand Ltd.

[5] "Energy, electricity and nuclear power estimates for the period of up to 2050," 2020, international Atomic Energy Agency.

[6] P. Ferracci, "Caheier technique no. 199, power quality," Schneider Electric, Tech. Rep., October 2001. [Online]. Available: https://electrical-engineering-portal.com/download-center/books-and-guides/schneider-electric/power-quality

[7] "IEEE recommended practice for monitoring electric power quality (IEEE std 1159-2019)," IEEE Power and Energy Society, Standard.

[8] List of voltages and frequencies (Hz) arond the world.

[9] Mains electricity by country.

[10] R. P. Bingham, "Sags and swells," *Manager of Technology and Products Dranetz-BMI, New Durham Road Edison, NJ 08818-4019 USA*, 1998.

[11] Y. Y. Pyone, "Design of transformers for 60 kVA automatic voltage stabilizer," in *International Conference on Computer and Automation Engineering*, Bangkok, Thailand, March 2009), pp. 318–322.

[12] P. Eswaran and M. Nishanth, "Design of fuzzy logic controller for customized servo voltage stabilizer," in *2nd International Conference on Electronics and Communication Systems (ICECS)*, Coimbatore, Feb 2015), pp. 103–106.

[13] M. Louise, "Induction voltage regulator of the moving coil type," 1965, Oct. 19).

[14] M. G. Lind, W. Xiao, and W. G. Dunford, "Modeling of a constant voltage transformer," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 2, pp. 409–418, 2006.

[15] R. Kakalec, "A feedback-controlled ferroresonant voltage regulator," *IEEE Transactions on Magnetics*, vol. 6, no. 1, pp. 4–8, 1970.

[16] D. Jang and G. Choe, "Step-up/down ac voltage regulator using transformer with tap changer and PWM AC chopper," *IEEE Transactions on Industrial Electronics*, vol. 45, no. 6, pp. 905–911, 1998.

[17] M. E. Newmann and A.-C. Corporation, "Tap changing voltage regulator which eliminates preventive autotransformer," 1978, Dec. 19).

[18] C. Jiong, Z. Feng, C. Xia, Z. Lizhi, and W. Luyang, "Design of ac chopper voltage regulator based on PIC16F716 microcontroller," in *IEEE PES Innovative Smart Grid Technologies*, Tianjin, China, 2012, pp. 1–4.

[19] M. M. Hoque, "Design, implementation and performance study of programmable automatic voltage regulator," *Journal of Electrical Systems*, vol. 10, no. 4, 2014.

[20] R. Thompson, "AC voltage regulators," *Wireless World*, vol. 79, no. 1453, pp. 339–344, 1973.

[21] L. Gyugyi, "Dynamic compensation of AC transmission lines by solid-state synchronous voltage sources," *IEEE Transactions on Power Delivery*, vol. 9, no. 2, pp. 904–911, 1994.

[22] M. R. Hajimoradi, A. Yazdian, and H. Mokhtari, "Double stage switch mode AC voltage regulator," in *2nd Conference on Power Electronics Drive Systems and Technologies (PEDSTC), IEEE*, Tehran, Iran, 2011), pp. 187–192.

[23] J. Nan, T. Hou-Jun, L.-Y. Bai, X. Geng, and X.-L. Yang, "Analysis and control of two switches ac voltage regulator," vol. 9, no. 7, April 2010, pp. 208–217.

[24] C.-M. Wang, C.-H. Lin, C.-H. Su, and S.-Y. Chang, "A novel single-phase soft-switching ac chopper without auxiliary switches," *IEEE transactions on power electronics*, vol. 26, no. 7, pp. 2041–2048, 2010.

[25] S. M. Hietpas and M. Naden, "Automatic voltage regulator using an AC voltage-voltage converter," *IEEE Transactions on Industry Applications*, vol. 36, no. 1, pp. 33–38, 2000.

[26] M. Hajimoradi, E. Karimi, H. Mokhtari, and A. Yazdian, "Performance improvement of a double stage switch mode AC voltage regulator," in *3rd conference on Power Electronics and Drive Systems Technology (PEDSTC)*, Tehran, Iran, 2012, pp. 181–186.

[27] H.-J. Ryoo, J.-S. Kim, G.-H. Rim, J. Jeon, and D. Kim, "Series compensated step-down ac voltage regulator using ac chopper with transformer," in *Sixth International Conference on Electrical Machines and Systems, 2003. ICEMS 2003.*, vol. 1. IEEE, 2003, pp. 427–430.

[28] D. Chen and Y. Chen, "Step-up ac voltage regulators with high-frequency link," *IEEE transactions on power electronics*, vol. 28, no. 1, pp. 390–397, 2012.

[29] N. Kularatna and C. Jinadasa, "Analysis and design aspects of a series power semiconductor array with digital waveform control capability for single phase AC voltage regulators and other applications," *Circuits and Systems*, vol. 2, no. 3, p. 249, 2011.

[30] F. Vandy, "Design and implementation of an AC voltage regulator based on series power semiconductor array," 2014. [Online]. Available: https://researchcommons.waikato.ac.nz/handle/10289/9006

[31] Y. Suzuki and I. Sugawara, "AC voltage regulator," May 22 2001, US Patent 6,236,192.

[32] S. Venkatesh and K. Muthiah, "Power fluctuations–usage of servo voltage stabilizers in industries," *International Journal of Applied Engineering Research, Dindigul*, vol. 2, no. 1, 2011.

[33] "CVT-constant voltage transformer," http://www.circuitstoday.com/cvt-constant-voltage-transformer, accessed: 13 April 2017.

[34] M. Ali, N. Anwar, S. T. Zahra, A. Hayat, S. Zaffar, and S. Iqbal, "Triac based automatic voltage stabilizer," *University of Wah Journal of Science and Technology (UWJST)*, vol. 3, pp. 23–28, 2019.

[35] "The AVR guide : Tap changing voltage regulator operation," https://ustpower.com/comparing-automatic-voltage-regulation-technologies/, accessed: 11 January 2019.

[36] P. Nystrom, "A comparison of AC voltage regulation technologies," Tsi Power, Tech. Rep., June 2012. [Online]. Available: http://www.tsipower.com/technical-resources/white-papers

[37] V. C. George, William, "Root mean square voltage regulator," 17 1973, US Patent 3,746,970.

[38] T. Tomioka, "Voltage regulator and semiconductor device," Oct. 24 2017, uS Patent 9,798,341.

[39] J. Nan, T. Hou-Jun, L. Wei, and Y. Peng-Sheng, "Analysis and control of buck-boost chopper type ac voltage regulator," in *2009 IEEE 6th International Power Electronics and Motion Control Conference*. IEEE, 2009, pp. 1019–1023.

[40] J.-M. Flores-Arias, A. Moreno-Munoz, F. Domingo-Perez, V. Pallares-Lopez, and D. Gutierrez, "Voltage regulator system based on a pwm ac chopper converter," in *2011 IEEE International Symposium on Industrial Electronics*. IEEE, 2011, pp. 468–473.

[41] N. Kularatna, "Low cost fast ac regulator provides high waveform fidelity," *Power Conversion and Intelligent Motion [PCIM](USA)*, pp. 76–78, 1988.

[42] N. Kularatna, "Low cost, light weight AC regulator employing bipolar power transistors," in *Proceedings of the 21st International Power Quality Conference-PCIM/Power Quality*, vol. 90, 1990, pp. 67–76.

[43] N. Kularatna, "Techniques based on bipolar power transistor arrays for regulation of AC line voltage," in *Power Electronics and Applications, Fifth European Conference on*, Brighton, UK, 1993, pp. 96–100.

[44] E. F. Fuchs and M. S. Masoum, Mohammad, *Power Quality in Power systems and Electrical Machines*. Elsevier Academic Press, 2008.

[45] P. Jon Bickel, "An overview of transients in power systems," Schneider Electric, Tech. Rep., June 2019. [Online]. Available: https://www.se.com/ww/en/download/document/998-20579579_GMA/

[46] D. Dorr and B. Howe, "PQ standards for system compatibility," Electric Power Research Institute, Technical Report, December 2007. [Online]. Available: https://www.epri.com/#/pages/product/000000000001017108/?lang=en-US

[47] F. D. Martzloff, "A standard for the 90s: IEEE C62.41 surge ahead," National Institute of Standards and Technology, Tech. Rep., September 1991. [Online]. Available: https://www.nist.gov/publications/standard-90s-ieee-c6241-surges-ahead

[48] G.T.. Heydt, "Electric power quality: a tutorial introduction," *IEEE Computer Applications in Power*, vol. 11, no. 1, pp. 15–19, 1998.

[49] International standards and conformity assessment for all electrical, electronic and related technologies. [Online]. Available: https://www.iec.ch/search/?q=IEC%2061050-161

[50] H. Markiewicz and A. Klajn, "Voltage disturbances," Coppor Development Association and Wroclaw University of technology, Poland, Application Guide, July 2004. [Online]. Available: http://copperalliance.org.uk/uploads/2018/03/542-standard-en-50160-voltage-characteristics-in.pdf

[51] M. Wamundson, "Calculating voltage dips in power systems using probability distribution of dip durations and implementation of the moving fault node method," 2007. [Online]. Available: http://publications.lib.chalmers.se/records/fulltext/64474/64474.pdf

[52] "Voltage sags, swells, and interruptions characterized in dpq phase ii project," Electric Power Research Institute, Technical Report, December 2004. [Online]. Available: https://www.epri.com/#/pages/product/000000000001008505/?lang=en-US

[53] Power quality in electrical systems. [Online]. Available: http://www.powerqualityworld.com/2011/04/cbema-curve-power-quality-standard.html

[54] S. Rajagopalan, "Electric motors and power quality disturbances," Electric Power Research Institute, Technical Report, December 2011. [Online]. Available: https://www.epri.com/#/pages/product/000000000001024472/?lang=en-US

[55] K.M. Michaels, "Sensible approaches to diagnosing power quality problems," in *Industrial and Commercial Power Systems Technical Conference.* IEEE, 1996, pp. 109–115.

[56] D. Koval, R. Bocancea, K. Yao, and M. Hughes, "Canadian national power quality survey: Frequency and duration of voltage sags and surges at industrial sites," *IEEE Transactions on Industry Applications*, vol. 34, no. 5, pp. 904–910, 1998.

[57] P. Barker and B. Howe, "Power quality monitoring: Concepts, equipment and applications," Electric Power Research Institute, Technical Report, February 2009. [Online]. Available: https://www.epri.com/#/pages/product/000000000001018668/?lang=en-US

[58] "Motor protection against single-phasing," Cooper Industries, Inc, Tech. Rep., May 1993. [Online]. Available: http://www.cooperindustries.com

[59] W. M. Grady and R. J. Gilleskie, "Harmonics and how they relate to power factor," *Proceedings of EPRI Power Quality and Opportunities Conference (PQA93)*, November 1993.

[60] "Power factor correction and harmonic filtering in electrical plants," ABB SACE, Italy, Technical Application Papers (08), July 2008.

[61] V. J. Gosbell, S. Perera, and V. Smith, "Harmonc distortion in the electric supply system," Integral Energy Power Quality Center, University of Wollongong, NSW, Australia, Technical Note No.03, March 2000.

[62] W. M. Grady and S. Santoso, "Understanding power system harmonics," *IEEE Power Engineering Review*, vol. 21, no. 11, pp. 8–11, 2001.

[63] Definition of harmonics. [Online]. Available: http://www.electrical-installation.org/enwiki/Definition_of_harmonics

[64] T. M. Blooming and D. J. Carnovale, "Application of IEEE STD 519-1992 harmonic limits," in *Conference Record of 2006 Annual Pulp and Paper Industry Technical Conference*, Appleton, WI, USA, June 2006, pp. 1–9.

[65] "SPEEDFAX 2017 Product Catalog," Siemens Industry, Inc, pp. 15–19. [Online]. Available: https://w3.usa.siemens.com/powerdistribution/us/en/speedfax-product-catalog/Documents/2017/SF-17-Sect-T-ALL-web.pdf

[66] "PowerLogic PM5500 series User manual," Schneider Electric, pp. 137–139, 2018. [Online]. Available: https://www.productinfo.schneider-electric.com/pm5500/

[67] P. M. Balasubramaniam and G. Gurusamy, "Evaluation and implementation of a shunt active power filter under balanced source voltages," *Journal of Engineering Science and Technology Review*, vol. 5, pp. 35–41, 2012.

[68] L. Cividino, "Power factor, harmonic distortion; causes, effects and considerations," in *[Proceedings] Fourteenth International Telecommunications Energy Conference - INTELEC '92*, 1992, pp. 506–513.

[69] J. Zhu, D. Xie, F. Wang, and T. Cao, "Study on harmonics of switching power supply," *International Workshop on Information and Electronics Engineering (IWIEE), Procedia Engineering, ELSEVIER*, vol. 29, pp. 2098–2102, 2012.

[70] N. Kularatna, *Power Supply CookBook*, 2nd ed. Newnes, 2001.

[71] S. M. Machado and N. D. Silva, "Stability and harmonic rejection analysis of single-phase grid-connected inverter inteded for renewable energy systems considering distorted grid onditions," in *International COlloquium on EMC, Lightning and Power Quality COnsiderations for Renewable Energy Systems*, 2016.

[72] Total harmonic distortion effects on motors. [Online]. Available: https://www.plantengineering.com/articles/total-harmonic-distortion-effects-on-motors/

[73] D. Robinson, S. Perera, V. J. Gosbell, and V. Smith, "Voltage fluctuations in the electric supply system," Integral Energy Power Quality Center, University of Wollongong, NSW, Australia, Technical Note No.07, August 2003.

[74] N. Kularatna, "Worst case power quality environments and design of power electronics products: Experiences of a design team in a developing country," in *Proceedings of Power Systems World Conference (Power Quality)*, 2000, pp. 109–116.

[75] H. R. West, "Induction voltage regulator," Feb. 15 1944, uS Patent 2,341,968.

[76] H. R. Soal, "Costant potential transformer," Aug. 31 1938, uS Patent 2,143,745.

[77] H. Hart and R. Kakalec, "The derivation and application of design equations for ferroresonant voltage regulators and regulated rectifiers," *IEEE Transactions on Magnetics*, vol. 6, no. 3, pp. 668–668, 1970.

[78] P. Cesare, J. and J. Flanders, N., "AC voltage regulator," 18 1979, US Patent 4,168,476.

[79] P. Banerjee, M. Choudhury, and G. T. Rasul, "AC voltage regulation by switch mode buck-boost voltage controller," in *3rd Int. Confonf. ICECE, Bangladesh*, 2004, pp. 351–354.

[80] L. Yim-Shu, D. K. W. Cheng, and Y. C.Cheng, "Design of a novel ac regulator," *IEEE Transactions on Industrial Electronics*, vol. 38, no. 2, pp. 89–94, April 1991.

[81] N. Kularatna, "A linear technique for AC voltage regulation using an ordinary transformer and power semiconductors," 1990).

[82] N. A. D. V. Kularatna and M. D. C. S. K. Jinadasa, "Digital control for controlling and linearizing an AC impedance," 2015, Sep.15).

[83] N. Kularatna, *DC Power Supplies: Power Management and Surge Protection for Power Electronic Systems*. CRC Press, 2016.

[84] "Linear and switching voltage regulator fundamental part 1," Texas Instruments, 2011.

[85] N. Kularatna, *Modern component families and circuit block design*. Newnes, 2000.

[86] N. Kularatna and P. Cho, "A power sharing series power BJT array with isolated low voltage control for AC power control applications," in *32nd Annual Conference on IEEE Industrial Electronics (IECON)*. Paris, France, 2006, pp. 1715–1720.

[87] S. Darlington, "Semiconductor signal translating device," 1952).

[88] L. Trajkovic and A. Willson, "Replacing a transistor with a compound transistor," *IEEE transactions on circuits and systems*, vol. 35, no. 9, pp. 1139–1146, 1988.

[89] M. M. Green, "A method for identifying combinations of transistors that can be replaced with a single transistor when applying the nielsen-willson theorem," in *Proceedings of ISCAS'95-International Symposium on Circuits and Systems*, vol. 1. IEEE, 1995, pp. 105–108.

[90] Agilent Technologies, "Linear applications of optocouplers," Appl. note 951-2, 1999.

[91] "TLP504A, TLP504A-2," Toshiba, Data Sheet.

[92] D. A. Neamen, *Microelectronics circuit analysis and design*, 4th ed. Mc Graw Hill, 2010.

[93] P. Horowitz and W. "Hill, *The art of electronics*, 2nd ed. Cambridge University Press, 1996.

[94] J. Seymour, *Electronic Devices and Components*, 2nd ed. Longman Scientific and Technical, 1998.

[95] "Phototransistor optoisolator - TIL111," Fairchild Semiconductor, Data Sheet.

[96] C. Kitchin and L. Counts, "RMS to DC conversion application guide," 1986, analog Devices Inc.

[97] "True RMS-to-DC converter," Analog Devices Inc., Data Sheet.

[98] "CD14538B Types - CMOS dual precision monostable multivibrator," Texas Instruments, Data Sheet.

[99] A. S. Sedra and K. C. Smith, *Microelectronic circuits*, 5th ed. Oxford University press, 2004.

[100] "TL08xx JFET-input operational amplifiers," Texas Instruments, Data Sheet.

[101] "MC1403,b - low voltage reference," ON Semiconductor, Data Sheet.

[102] "A practical guide for EN 61000-4-11: Testing and measurement techniques," EMC Standards, Technical Report. [Online]. Available: https://www.emcstandards.co.uk/a-practical-guide-for-en-61000-4-11-testing-an

[103] V. C. Valchev and A. Van den Bossche, *Inductors and transformers for power electronics*. CRC press, 2005.

[104] H. W. Gingrich, *Electrical machinery, transformers, and control*. Prentice Hall, 1979.

[105] J. H. Harlow, *Electric Power Transformer Engineering, 3rd edition*. Taylor and Francis, 2012.

[106] *Transformers*. McGraw-Hill, 2005, Bharat Heavy Electricals Ltd.

[107] W. G. Hurley and W. H. Wolfle, *Transformers and Inductors for power electronics: Design and Applications*. John Wiley and Sons, Ltd, 2013.

[108] P. N. Wijesooriya, N. Kularatna, J. Fernando, and D. A. Steyn-Ross, "Two-transformer-series approach in developing a transistor based-AC voltage regulator for consumer-end applications," in *43rd Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Beijing, China, 2017, pp. 6437–6442.

[109] P. N. Wijesooriya, N. Kularatna, J. Fernando, and D. A. Steyn-Ross, "Fast acting linear ac voltage regulator for consumer applications: Implementation options," in *2018 IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES)*, Hamilton, New Zealand, 2018, pp. 277–282.

[110] C. W. T. McLyman, *Transformer and inductor design handbook*. CRC press, 2016.

[111] M. Jinadasa, "High power linear AC electronic load for testing UPS systems," 2007.

[112] "ATmega328P," Atmel Corporation, Data Sheet.

[113] Americal wire guage.