Bipolar Amplifier Bias Technique for Robust IM3 Null Tracking Independent of Internal Emitter Resistance

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***Abstract*— Bipolar amplifiers can be biased to give a deep null in third order non-linearity, with the potential for high IP3 amplifier stages. This requires maintaining a precise voltage drop across a small resistive emitter degeneration resistance, whose value is related to kT/q. To make such a scheme practical, the bias must not only take into account the change in kT/q with temperature, but must compensate for variations in the degeneration resistance. In this paper we present a bias technique for IM3 null tracking that can take account of temperature and resistance tolerances, and is also insensitive to the value of the internal emitter resistance. Simulations using a 27 GHz BiCMOS technology indicate that the bias of an amplifier can be maintained over temperature, representative element tolerances, and mismatch such that the IP3 performance is maintained within $\pm$9.5 dBV of the optimum null condition. The technique is applicable for a range of bipolar BiCMOS technologies and is attractive for amplifiers where high IP3 is required with moderate noise figure.**

I. Introduction

The third-order null at a particular bias condition is a fundamental property of a degenerated BJT amplifier structure [1] [2] [3]. In principle it is possible to achieve very high IIP3 figures by the use of modest resistive degeneration and setting the bias such that the voltage across this resistance is $kT/2q$ [4] [5]. Such a configuration is potentially very attractive in applications where linearity is paramount while some noise figure can be sacrificed, such as in the RF mixer input in a radio receiver. However, to realise the theoretical benefits it is necessary to set the bias conditions with regard to the ambient temperatures so that the ideal degeneration voltage is maintained regardless of the temperature. This implies not only having a bias proportional to absolute temperature (PTAT), but also taking into account the temperature coefficient of the degeneration resistor itself. Both of these factors may be compensated for by means of a conventional PTAT bias and a matched resistance [6] [7]. However, the idea breaks down when the intrinsic device resistances are considered, since these cannot be easily accommodated in a conventional PTAT bias circuit. Indeed, the sensitivity of the third order null to the intrinsic emitter resistance is large enough that it can be used as a sensitive method for extracting the resistance value for a particular device layout [8]. The objective of this work is to develop a method for setting a BJT amplifier bias such that it operates at the third order null point over a wide temperature range, despite variations in the external degeneration resistance. Fig. 1 shows an IM3 null, and consequently an IIP3 peak, for a generic common-emitter amplifier. The null can be approximately modelled by (1) derived in [1] [4]

$$I_C = \frac{kT}{2qR_{ee}} \tag{1}$$

where I_C is the DC collector current, kT/q is the thermal voltage and R_{ee} is the summation of internal and external emitter resistance. This resistance should also contain the parasitic base resistance R_b reflected through the beta of the transistor. Assuming R_b is small and the beta is large, it can be approximated to just the internal and external emitter resistances. From this equation we see that any error in the effective value of R_{ee} will cause the bias current to not be placed in the null. Hence, as (1) implies, we need to accurately extract the internal emitter resistance and use it with any external emitter resistance to bias a single transistor amplifier so as to maintain a voltage of $kT/2q$ across the total emitter resistance.

II. Translinear Extraction

A translinear stack circuit which allows cancellation of emitter resistances (sometimes broadly referred to as logarithmic-conformance error) [6] [7], will form the basis which allows the design of a PTAT current source which is insensitive to internal emitter resistances. A simplified version of this is shown in Fig. 2a. This circuit relies on the current amplifier at the top, attempting to force equal currents through each transistor branch. The governing equation for a stack such as this is given by

$$V_{R1a} = I_1 R_{1a} = \frac{kT}{q} ln(A) - xI_1 R_E \tag{2}$$

where R_E is the internal emitter resistance. This equation was simplified by taking scale factors x and A which are given by (3) and (4) below, where M_n is the emitter area size for a

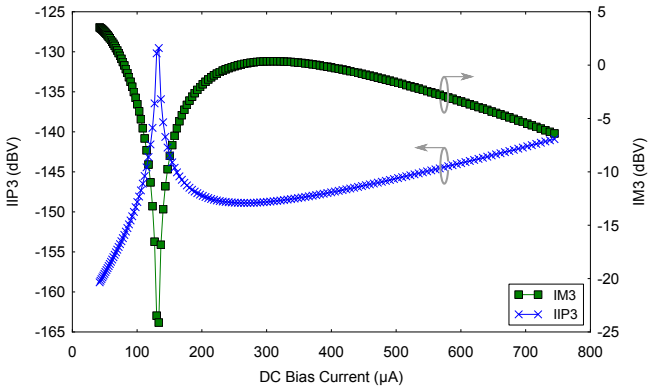

Fig. 1. Third order non-linearity null in a generic common-emitter amplifier using the 0.5 μm BiCMOS model and chosen nominal circuit values.

given transistor.

$$x = \frac{1}{M_4} + \frac{1}{M_5} + \frac{1}{M_6} - \frac{1}{M_1} - \frac{1}{M_2} - \frac{1}{M_3} \tag{3}$$

$$A = \frac{M_4 M_5 M_6}{M_1 M_2 M_3} \tag{4}$$

The first logarithmic term of (2) is an ideal PTAT component, but the last term xI_1R_E is the portion of V_{R1a} created by the devices' internal emitter resistance through the stack. It is possible to select conditions on scale factors x and A such that the contribution from the devices' internal emitter resistance is eliminated from V_{R1a}. This is done by observing the restrictions $\frac{1}{M_4} + \frac{1}{M_5} + \frac{1}{M_6} - \frac{1}{M_1} - \frac{1}{M_2} - \frac{1}{M_3} = 0$ and $M_4M_5M_6 > M_1M_2M_3$. We can express this condition as in (5) below, so that the value V_{R1a} only contains the PTAT component.

$$V_{R1a} = I_1 R_{1a} = \frac{kT}{q} ln(A) \tag{5}$$

It is thus possible to construct one complete translinear stack with the emitter resistance contribution completely removed (Fig. 2a) and a further similar stack where there is a contribution from a scaled portion of internal emitter resistance (Fig. 2b). The transistors in the first stack are dimensioned such that $x = 0$ and while those in the second are set such that $x > 0$, while both stacks use an equal scale factor for A. This creates two voltages, V_{R1a} in the first stack and V_{R1b} in the second stack, across the respective R_1 resistors which are temperature independent and contain known scaled portions of voltage contributed by internal emitter resistance. Because the two stacks must have different total parallel emitter areas to satisfy the required conditions, different equilibrium currents are set up in each stack. This prevents the extraction of the transistors internal emitter resistance by a simple subtraction of (2) and (5), but with more complex circuit design it is possible to extract the value of the devices as fabricated in each die.

III. Bias Current Equation

To produce the correct bias current we manipulate the two voltages V_{R1a} and V_{R1b}. To express the required bias current

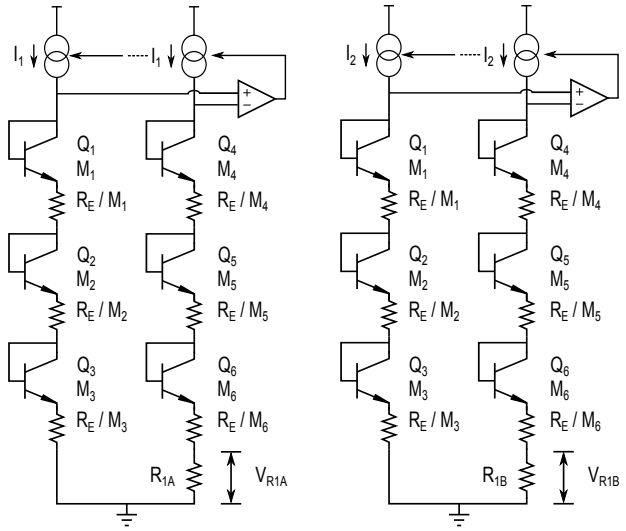

Fig. 2. Two translinear stack circuits, identical expect in BJT area ratios. Consequently a) uses I_1 to produce V_{R1A} and b) uses I_2 to produce V_{R1B}.

mathematically, we define V_3 from the subtraction of the two voltages created from (2) and (5) as below.

$$V_{R1a} = I_1 R_{1a} = \frac{kT}{q} ln(A) \tag{6}$$

$$V_{R1b} = I_2 R_{1b} = \frac{kT}{q} ln(A) - xI_2R_E \tag{7}$$

$$V_3 = V_{R1b} - V_{R1a} = xI_2R_E \tag{8}$$

I_2 is the equilibrium current in the second stack with a non-zero x value, so V_3 contains knowledge of R_E. Equation (1) implies that the target bias voltage will be $kT/2q$, and we seek a current that will drop this voltage across R_E added to another resistor, R_1. We will achieve this using a reference current from which a portion is adjusted to allow for the R_E contribution. I_1 is suitable for the reference as it contains no portion contributed by internal emitter resistance and is easily manipulated out of the first stack. From (6) we can obtain our desired reference bias current below in (9).

$$I_{Ref} = \frac{kT}{2qR_1} = \frac{I_1}{2ln(A)} \tag{9}$$

It is also possible to rearrange (8), as below, to obtain R_E on its own in terms of the known resistance R_1 (equal to R_{1a} and R_{1b}) and the equilibrium currents of the two stacks, or as part of the total degeneration resistance $R_E + R_1$.

$$\frac{R_1}{R_E + R_1} = \frac{xI_2}{xI_2 + I_1 - I_2} \tag{10}$$

This creates a divider ratio for the internal and external emitter resistances. Combining this with the scale current in (9) we obtain our final equation for the bias current.

$$I_{Bias} = \frac{I_1}{2ln(A)} \frac{xI_2}{xI_2 + I_1 - I_2} \tag{11}$$

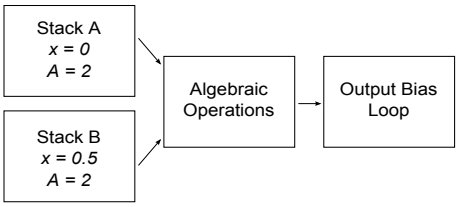

Fig. 3. Bias circuit blocks showing the four main stages of the circuit.

IV. Extraction Circuit Design

The complete system has been designed and simulated using parameters from a commercial 0.5 μm 27GHz BiCMOS process, typical for such RF applications, with a nominal 3.3V supply. Note that the system implementation is not specific to this technology, but the availability of NMOS and PMOS transistors is useful in the construction of the amplifiers and mirroring functions needed. The overall bias circuit consists of four main blocks as shown in Fig. 3. Firstly, the two translinear circuit stacks are used to extract two component voltages V_{R1a} and V_{R1b}, and the related current values I_1 and I_2. These currents are passed to a third block which performs the required algebraic operations on the two voltages to produce an output scaled bias current. Finally, a bias loop uses the output to set the operating current in the signal path amplifier of interest (Q1) so that the voltage across its total degeneration resistance is $kT/2q$ regardless of temperature and any variations in the values of R_E or R_1. Current scaling, multiplication, and division circuit operations are required to obtain the mathematical result in (11). Current scaling can be done relatively easily with current mirrors and a multiply/divide operation can be achieved with a conventional translinear multiplier circuit which forms the majority of the second block. A servo current mirror loop can be used to build the driver block as seen in Fig. 5. The scale factors are chosen to be $A = 2$ for both stacks, and $x = 0, x = 0.5$ for Stack A and B respectively. These stacks scale factors are accomplished with $M_{1-6} = 2, 2, 2, 1, 4, 4$ and $M_{1-6} = 4, 4, 8, 1, 16, 16$ for stacks A and B respectively. Numerical computations show that this combination is the smallest collective transistor array size which allows an $x = 0.5$ scale factor in Stack B. This factor is appealing as it allows the design of scaled current mirrors with minimal error.

A. Multiplier Divider Design

A translinear multiplier configuration is used, as presented by [9]. It is a conventional multiplier/divider circuit modified to produce smaller error between the output and input currents. This can be seen in Fig. 4 showing how its operation fits in well with the required operations of (11).

B. Amplifier Bias Loop Design

Following the multiplier operation, its output current is then scaled by the reference current and applied to the main signal amplifier using a servo current mirror. The simplified layout of this can be seen in Fig. 5. Each side of the current mirror must be balanced in order to get an accurate bias current in the amplifier, hence the degeneration resistance R_1 is used on each side of the mirror, adding to the devices internal resistance value RE on each side. R_{2A} isolates the signal path from the bias section, and R_{2B} equalizes the voltage drop due to base currents. In order to further minimise error contributed by loss of base current from the reference, a base current compensation MOS transistor is used on the input side.

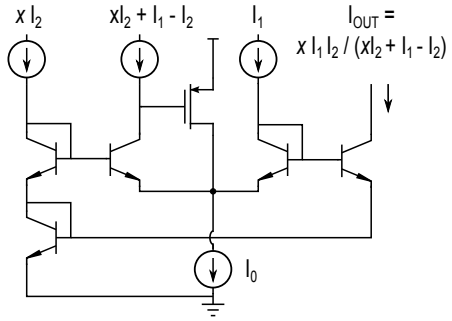

Fig. 4. Translinear multiplier used to perform algebraic operations required by the second circuit block.

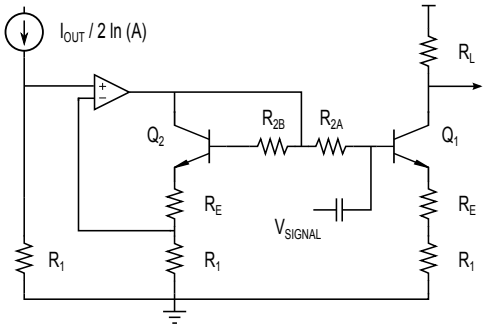

Fig. 5. Output bias loop used to set the bias current in the output transistor such that it operates at the third order null.

V. Error Analysis

Error sensitivity is a major consideration in this design for two reasons. Firstly, the IM3 null is sharply defined so a small change in the target emitter voltage can lead to a large change in the IIP3 magnitude and secondly it is a moderately large circuit in which there is the potential for errors to accumulate.

A. Multiplier Output Error

Process variation simulations were undertaken based on industry typical corner values for this type of 0.5 μm BiCMOS technology. Resistor absolute values were varied over $\pm 20\%$ and resistor matching simulations were made with $\pm 2\%$ variation. Spice simulations show how these variations affect the bias current and the target emitter degeneration voltage. Nominal circuit values are chosen as $R_1 = 60\Omega$, ambient temperature = 27°C, and supply voltage = 3.3V. From simulation we see the equilibrium current in Stack A (I_1) and Stack B (I_2) are 304.0 μA and 223.6 μA respectively. These currents are used with (11) to calculate an ideal multiplier output current of 127.5 μA, our target current for all multiplier output error

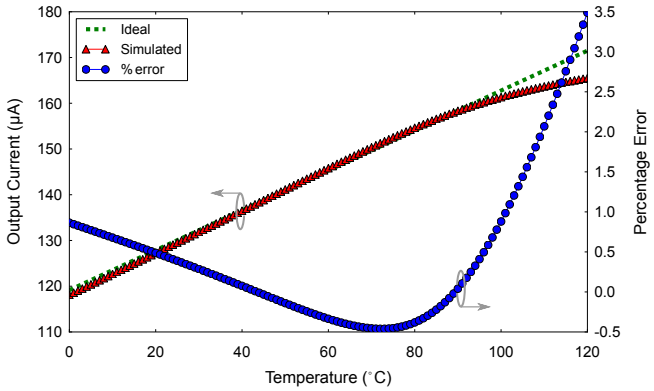

Fig. 6. Bias current variation vs. temperature variation compared with the ideal bias current, at the multiplier output.

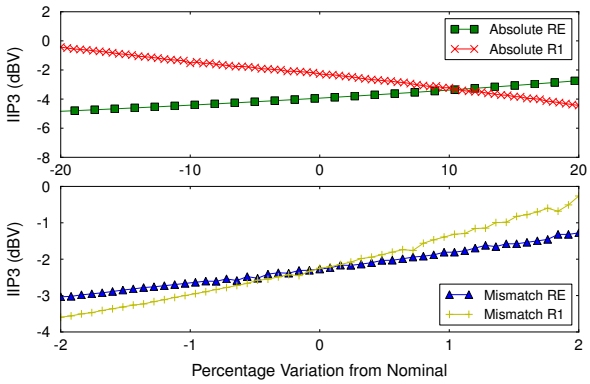

Fig. 7. Variation of absolute component values and mismatched component values vs. IIP3.

calculations. Fig. 6 shows the variations of temperature as well as the resulting percentage error compared to the ideal calculated bias current, and it suggests the circuit is relatively unaffected by temperature variation. The data reveals that in the temperature range of 0–100°C the expected variation in bias current is $\leq$0.8%. The error increases steadily at higher values than 100°C, eg. 3.5% at 120°C. Similar data for the supply voltage shows the worst case sensitivity is $\leq$3.1%, obtained by varying the supply by $\pm$20%.

B. Signal Amplifier Bias Current Error

Simulations were run for the variation in amplifier output bias current due to variations in R_1 and R_E for the expected absolute and mismatch process errors. The results are summarised in Table 1. This shows the worst case variation from the ideal amplifier bias current is $\leq$2% in all cases.

C. IM3 Nulling Error

The primary goal of this work is to obtain a method of guaranteeing the bias of an amplifier at the null in 3rd order non-linearity, over process, supply variations, and temperature (PVT) and so the sensitivity of the complete system to IM3 is a critical measure. Fig. 7 shows the absolute and mismatch variations of R_1 and R_E versus its effect on the IIP3 of the bias output current. From the nominal IIP3 value set by the nominal component values, these variations lead to a maximum IIP3 variation of $\pm$6.0 dBV, reflecting the bias current error of where the circuit sits in the IM3 null. Including temperature and supply variations of 20%, the maximum IIP3 variation increases to approximately $\pm$9.5 dBV.

VI. Conclusion

A bias circuit has been developed that sets a BJT amplifier in its natural IM3 null and can maintain this despite variations in temperature and in tolerances of the degeneration resistance. Furthermore, a technique has been developed using matched translinear stacks to extract the value of the transistors internal emitter resistance as fabricated on each die. This resistance extraction, combined with the PTAT currents generated, creates a reference bias that takes into account the total effective degeneration resistance to fix the operating point at the IM3 null. The error limits of the extracted bias current show insensitivity to variation from key circuit components and with further work this error may be reduced. Temperature and supply voltage variations around the nominal design values are shown to have minimal effect and the IM3 of a demonstrator amplifier is maintained close to its ideal null.

TABLE I

Error Limits in Bias Current due to Component Variation

Variation type	Component	Error Limits
Absolute values (20%)	R_1	-1.90%, -0.63%
	R_E	+0.42%, -1.95%
Mismatch values (2%)	R_1	<0.1%, -1.97%
	R_E	-0.42%, -1.50%

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