Energy-Efficient SMPS-Based Pulse Generator for Neurostimulators

Sinduja Seshadri, *Student Member, IEEE*, Jonathan Scott, *Senior Member, IEEE*

***Abstract*—There is a need in the neuromodulation industry for a very energy-efficient pulse generator. Little data is observed in literature to develop a power efficient pulse generator that can deliver the required stimulus. A typical stimulator has a boost stage, a low-dropout (LDO) stage and an analog circuit that delivers the stimulus in the form of a pulse to the patient. Such a system is found to be $\sim 40\%$ efficient. There are two new methods that can improve this efficiency rating significantly. (1) A modification to existing pulse generator by adding microprocessors to control the output voltages of boost and LDO in the circuit, as proposed by the manufacturer; (2) a Single-Ended Primary Inductance Converter (SEPIC) based design proposed by the authors, with the input connected to a battery and the output to electrodes. Comparing with existing design, the modification offered a consistent 75% efficiency for output voltages from 3.9V to 6.6V. SEPIC had an efficiency rating of 80% to 86% across the same voltage range.**

keywords: pulse generator, energy-efficient, biomedical, SEPIC

I. Introduction

A neurostimulator system consists of a centralised Implantable Pulse Generator (IPG), one or more leads and one or more electrodes (for stimulating and recording signals) [1]. The IPG generates and delivers the pulses to the electrodes inserted in the patient. Electrical charge in each pulse stimulates the neural tissue and provides the patient with relief. The charge produced is of the form of a pulse defined by its pulse-width, amplitude and occurs at varying specified frequencies. The typical internal circuitry of the IPG is shown in Fig. 1.

Boost converters are most prevalent in medical implants due to their high efficiency [3] to obtain a large intermediate voltage and analogue circuitry to administer the required stimulation. References [4, 5, 6, 2, 7] have focused their efforts on using boost converters or configurations that involve the boost converter to improve the Switched Mode Power Supply (SMPS) efficiency. In the same vein, switched-capacitor networks have also been used to step-up the input voltage and a current mirror array to deliver precise pulses to the patient [8].

Much of the endeavour is committed to obtaining a highly efficient SMPS to increase the input voltage to the LDO. Energy dissipation in the analog circuitry that delivers the pulses to the load is not investigated. The ratio of output energy (i.e. energy dissipated to the load) to input energy (i.e. the battery + SMPS) define the IPG efficiency.

There are two methods through which the IPG efficiency can be improved. The first design is applying a modification to Fig. 1 which is a proposal from the manufacturer of the medical implants. Controlling the voltages that the SMPS and LDO output allow for an efficient delivery of pulses to the load. The second design is replacing the boost converter, LDO and the current mirror from Fig. 1 with just a SEPIC, a design proposed by the authors. These two designs are shown in Figs. 2 and 3, respectively.

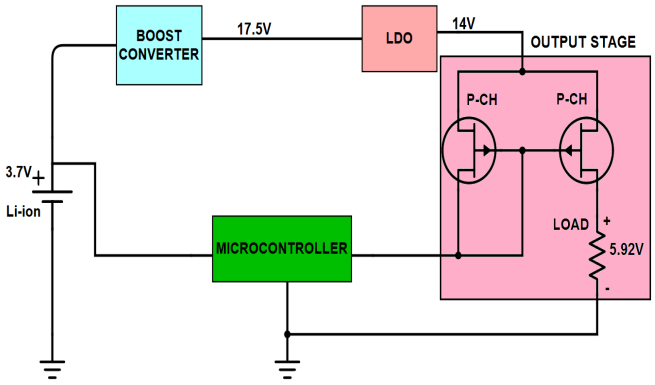

Fig. 1. The internal circuitry of an IPG in a neurostimulation system, modified from [2]. The battery is usually a 3.7V Li-ion cell which is stepped-up by the boost converter (17.5V) while the LDO regulator steps down the voltage (14V) to the required level. The current mirror array delivers the pulses (3V - 7V) to the electrodes, modelled as a resistive load ($\sim$1kΩ).

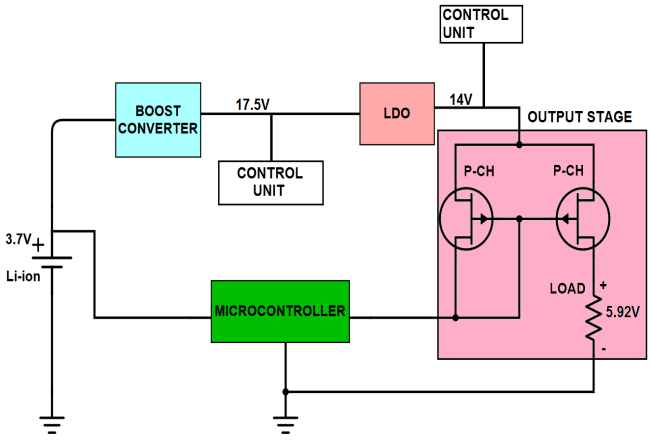

Fig. 2. Modification to existing topology in Fig. 1. The control unit blocks will regulate the voltages that the SMPS and LDO output.

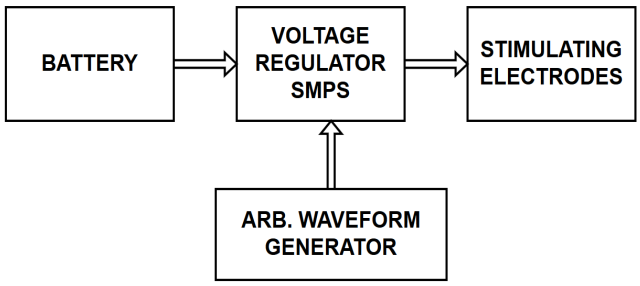

Fig. 3. Block diagram of a proposed IPG design. Replacing the boost converter, LDO and the current mirror stages with one SMPS, the SEPIC.

II. METHODOLOGY

A. Typical IPG Efficiency

The efficiency of the IPG in Fig. 1 is approximately 40 %. A numerical example of IPG efficiency calculation, with values typical to the neuromodulation industry will demonstrate this.

$$\begin{aligned} V_{in} = 3.7\,\mathrm{V},\ V_{intm} = 14\,\mathrm{V}, \\ t = 200\,\mu\mathrm{s},\ \beta = 0.8, \\ R_{load} = 750\,\Omega,\ V_{out} = 6\,\mathrm{V}, \end{aligned} \tag{1}$$

where V_{in} is the battery voltage, V_{intm} is the intermediate voltage level that a switching converter boosts it up to, t is the approximate duration of a pulse, β is the typical efficiency of a switching converter, R_{load} is the general characterisation of the electrode-tissue impedance and, V_{out} is a standard output voltage seen at the load. To calculate the efficiency, we need:

$$Q_{out} = \frac{V_{out}}{R_{load}} \cdot t, \tag{2a}$$

$$E_{in} = \frac{Q_{out} \cdot V_{intm}}{\beta}, \tag{2b}$$

$$E_{out} = Q_{out} \cdot V_{out}, \tag{2c}$$

$$\eta = \frac{E_{out}}{E_{in}} \cdot 100\,\%, \tag{2d}$$

where Q_{out} is the charge delivered to the load, E_{in} is the input energy with respect to the efficiency of the switching converter, E_{out} is the output energy received by the load and, η is the efficiency of the IPG. For the values in (1), the IPG efficiency is (3),

$$\begin{aligned} Q_{out} &\approx 1.6\,\mu\mathrm{C}, \\ E_{in} &\approx 55\,\mu\mathrm{J}, \\ E_{out} &\approx 20\,\mu\mathrm{J}, \\ \eta &\approx 36\,\%. \end{aligned} \tag{3}$$

The dominant sources of energy loss are twofold: the boost converter and the analog circuitry. A typical boost converter has a maximum realistic efficiency of 80%. The current mirror array is inefficient when considering the minimum allowed output voltage and the parasitic capacitances plus switching losses of the MOSFETs. Power is also dissipated due to the limitations of the LDO's internal circuitry. Furthermore, the fixed voltages from the boost converter and the LDO limits the performance of the current mirror. For efficient energy dissipation to the load, the output voltages from LDO and boost converter have to be of a specific amplitude.

B. Design for Modifying Existing IPG

Fig. 2 shows the internal circuitry of an implant with the capacity to adjust the output voltages of the boost converter and the LDO, as proposed by the manufacturer. The IPG typically senses the load impedance from previous pulses, as it does not change drastically from pulse to pulse. Therefore, it can calculate the anticipated output voltage and current ahead of delivering a pulse. Thus the overhead and the LDO output voltage can be scaled appropriately using the microprocessors (control units in Fig. 2). Controlling the SMPS and LDO output voltage allows the current mirror array to operate effectively.

The control units work effectively due to the limitations of the boost converter and overhead of the LDO. The voltage drop across the LDO is small but significant and exists because the boost converter cannot respond quickly. There is a capacitor between the boost converter and the LDO to sustain the input voltage to the LDO for the duration of a pulse. As a result, the LDO only gets down to its lowest possible dropout voltage at the end of a maximum-current, maximum-duration pulse.

The sources of loss for this method are similar to the losses highlighted for Fig. 1. However, the ability to control the output of the boost converter and LDO corrects for the energy loss in the current mirror array.

C. SEPIC based IPG

We propose a new design shown in Fig. 3 that does not incorporate cascading voltage regulator stages. Instead, we propose a SEPIC as the SMPS that delivers pulses required to stimulate the electrodes. A more detailed version of the block diagram of Fig. 3 is shown in Fig. 4. The SEPIC is built and tested using a bench power supply instead of a Li-ion battery, a function generator to switch the MOSFET at 1 MHz, and a Tektronix oscilloscope to measure the results. DC-DC converters like SEPIC have the problem of overshoot before settling to steady-state. This problem has been addressed and a solution has been proposed in paper [9].

The converter is developed using the dynamic model of SEPIC for effective analysis of ideal efficiency. The active switch (MOSFET) is replaced by a current source (4a) and the passive switch (diode) by a voltage source (4b) [10]. Current, $i(t)d(t)$ is the average current through the MOSFET and voltage $v(t)d(t)$ is the average voltage drop across the diode.

$$i(t)d(t) = (i_{L_1}(t) + i_{L_2}(t))d(t) \tag{4a}$$

$$v(t)d(t) = (v_o(t) + v_{C_1}(t))d(t) \tag{4b}$$

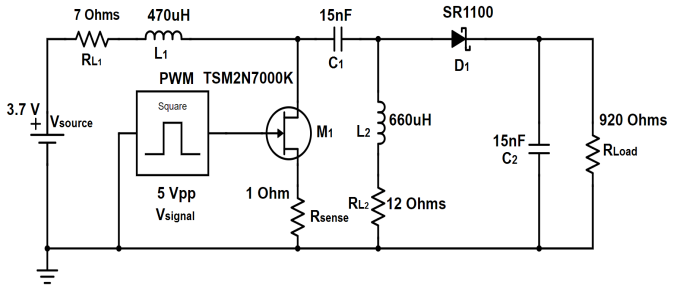

Fig. 4. SEPIC with the values of components calculated using (7)-(10). The model includes the parasitic resistances of the inductors along with the $1\,\Omega$ resistor to measure drain current. The electrode-tissue impedance is characterised as a resistive load of $920\,\Omega$. The source is typically a Li-ion battery and the PWM is an Agilent 33220A arbitrary waveform generator that drives the gate.

The dynamic model is described by the set of differential equations (5) modified from [10].

$$L_1 \frac{di_{L_1}(t)}{dt} = v_{in}(t) - (1 - d(t))(v_{C_1}(t) + v_o(t)) \tag{5a}$$

$$L_2 \frac{di_{L_2}(t)}{dt} = d(t)v_{C_1}(t) - (1 - d(t))v_o(t) \tag{5b}$$

$$C_1 \frac{dv_{C_1}(t)}{dt} = (1 - d(t))i_{L_1}(t) - d(t)i_{L_2}(t) \tag{5c}$$

$$C_2 \frac{dv_o(t)}{dt} = (1 - d(t))(i_{L_1}(t) + i_{L_2}(t)) - \frac{v_o(t)}{R} \tag{5d}$$

where L_1, L_2, C_1 and C_2 are the input and output inductors and capacitors, respectively. v_{in} and v_o are the input and output voltages, v_{C_1} is the voltage drop across C_1, R is the load, dt and $d(t)$ is with respect to the ON and OFF time of the MOSFET.

Component values are obtained through steady state analysis using (5) from [10] and [11]. Replacing dt and $d(t)$ in (5) with respect to duty cycle of the pulse driving the gate and switching frequency of the MOSFET, we can rewrite the set of differential equations as (6).

$$L_1 \frac{\Delta I_{L_1}}{DT} = V_{in} - (1 - D)T \cdot (V_{C_1} + V_o) \tag{6a}$$

$$L_2 \frac{\Delta I_{L_2}}{DT} = DT \cdot V_{C_1} - (1 - D)T \cdot V_o \tag{6b}$$

$$C_1 \frac{\Delta V_{C_1}}{DT} = (1 - D)T \cdot I_{L_1} - DT \cdot I_{L_2} \tag{6c}$$

$$C_2 \frac{\Delta V_o}{DT} = (1 - D)T \cdot (I_{L_1} + I_{L_2}) - \frac{V_o}{R}. \tag{6d}$$

We can perform circuit analysis based on MOSFET ON and OFF times and reduce (6) to obtain steady state equations. L_1 dominates and becomes active during ON time,

$$(1 - D)T \cdot (V_{C_1} + V_o) = 0$$

so,

$$L_1 = \frac{V_{in} \cdot DT}{\Delta I_{L_1}}. \tag{7}$$

L_2 becomes active during ON time of MOSFET as it gets charged by C_1 and discharges through the diode during OFF time, which means

$$DT \cdot V_{C_1} - (1 - D)T \cdot V_o = V_{in}$$

so,

$$L_2 = \frac{V_{in} \cdot DT}{\Delta I_{L_2}}. \tag{8}$$

C_1 discharges during ON time and charges during OFF time,

$$(1 - D)T \cdot I_{L_1} - DT \cdot I_{L_2} = I_o$$

where I_o is the output current so,

$$C_1 = \frac{I_o \cdot DT}{\Delta V_{C_1}}. \tag{9}$$

C_2 becomes active during ON time and charges during OFF time. Substituting the value for I_o,

$$I_{L_1}T - DT \cdot I_{L_1} + I_{L_2}T - DT \cdot I_{L_2} - (I_{L_1}T - DT \cdot I_{L_1} - DT \cdot I_{L_2}) = I_{L_2}T.$$

I_{L_2} is output charge over time so,

$$C_2 = \frac{V_o \cdot DT}{\Delta V_o \cdot R}. \tag{10}$$

ΔI_{L1} and ΔI_{L_2} are the changes in inductor currents and is set at $30\,\%$, which is typical in DC-DC converter design. ΔV_{C_1} and ΔV_o are the input and output ripple and is set at $5\,\%$, an accepted value in IPG design industry.

While the component values are calculated for ideal efficiency, sources of loss exist. These are the parasitic resistances of the inductors, the resistor that measures drain current, resistance of the diode, the resistance that lives in the gate drive and, finally the switching losses of the MOSFET and diode. Each loss consumes power from the battery affecting the power that reaches the $920\,\Omega$ load.

III. Results and Discussion

The results for the existing and modified designs, from Figs. 1 and 2 are simulated using SPICE and compared with simulated and measured results of SEPIC from Fig. 4. The values for efficiency is calculated using (2d), Fig. 5 shows the efficiency plot for the three designs.

The three patient conditions in Spinal Cord Stimulation (SCS) industry is used as an example to determine the efficacy of the existing, modified and SEPIC-based IPG designs: sitting, standing and supine. The typical required voltages to be delivered in each pulse for the patient to experience pain relief during sitting is $6.0\,\mathrm{V}$, standing is $6.6\,\mathrm{V}$ and, supine is $4.6\,\mathrm{V}$. The efficiency of the three designs for each of these patient conditions is shown in Fig. 5.

Fig. 5 shows that the measured results of SEPIC outperforms the existing design. The existing design is very energy inefficient as it ranges from $22\,\%$ to $38\,\%$. The modification to existing design offers a consistent $75\,\%$ efficiency across the voltage range. SEPIC is the most efficient of the three designs ranging from $80\,\%$ to $86\,\%$.

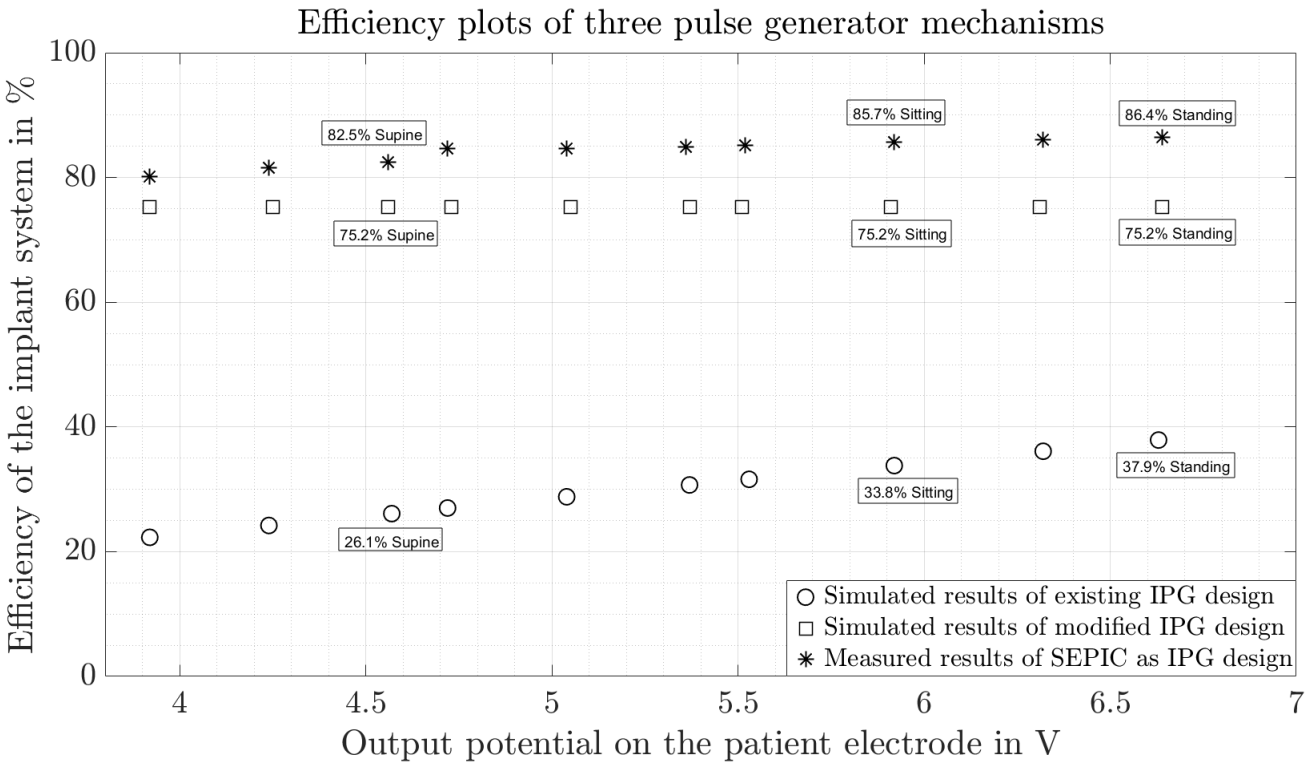

Fig. 5. Efficiency plots of three implant pulse generator systems with three sample patient conditions highlighted for comparison.

Fig. 6 shows the the simulated and measured results of SEPIC. The measured results of SEPIC given by the asterisk symbol in Figs. 5 and 6, and the repeated measurements given by the plus symbol in Fig. 6 used the same DUT but different measuring equipment, i.e. oscilloscope. Tektronix TPS 2014 observed SEPIC behaviour for the former set of measurements, and Tektronix MSO 4054 Mixed Signal Oscilloscope for the latter set of measurements. There is uncertainty in the two measured results. The error for each measured point is given in Table I using the simulated measurements as the reference. The standard error for the initial set of efficiency measurements is $84.2\,\% \pm 1\,\%$ and for the repeated efficiency measurements is $83.5\,\% \pm 1.2\,\%$.

The simulated results are obtained by creating a realistic SEPIC model on SPICE and are compared with the measured results by doing nodal measurements. The drain node voltages of the MOSFET (i.e. after the first inductor in Fig. 4), in measured and simulated vary by $260\,\mathrm{mV}$ and rise times vary by $1\,\mathrm{ns}$ on average. The diode node voltages (i.e. just before the diode in Fig. 4), in measured and simulated vary by $400\,\mathrm{mV}$ and rise times vary by $2.2\,\mathrm{ns}$ on average. The simulated results show higher efficiency than the measured results.

The discrepancy in the efficiency between simulated and measured results is attributed to the series AC resistance of the inductors. The reactance X_L, of inductors vary according to frequency, $X_L = 2\pi f L$, owing to skin effect and core losses. Measuring the $470\,\mu\mathrm{H}$ inductor's impedance and phase characteristics using Solartron 1260A Impedance/Gain-Phase Analyzer yielded a series AC resistance of $2.9\,\mathrm{k}\Omega$ at the switching frequency of $1\,\mathrm{MHz}$. SPICE cannot model the frequency-dependent series resistance. Therefore, the efficiency of the converter can be increased by $3\,\%$ if higher-quality inductors were used, but the choice was made to use small, SMD inductors consistent with use in an implant.

IV. Conclusion

There are two methods to improve IPG efficiency: (1) the proposal from the manufacturer is to modify the existing design by adding microprocessors to control SMPS and LDO outputs; (2) we propose a complete revamp of the IPG architecture and use SEPIC as a pulse generator. The modification to existing IPG system delivers pulses with consistently the same efficiency of $75\,\%$ for output voltages from $3.9\,\mathrm{V}$ to $6.6\,\mathrm{V}$. The SEPIC-based IPG design we proposed, provides better efficiency ranging from $80\,\%$ to $86\,\%$. However, it requires a complete change to the hardware for $10\,\%$ improvement in efficiency when compared to the modified IPG design. The modification to the IPG design, on the other hand, requires only a firmware change and rates high on efficiency. Nonetheless, the SEPIC offers opportunities for further research into optimising IPGs in neuromodulation systems.

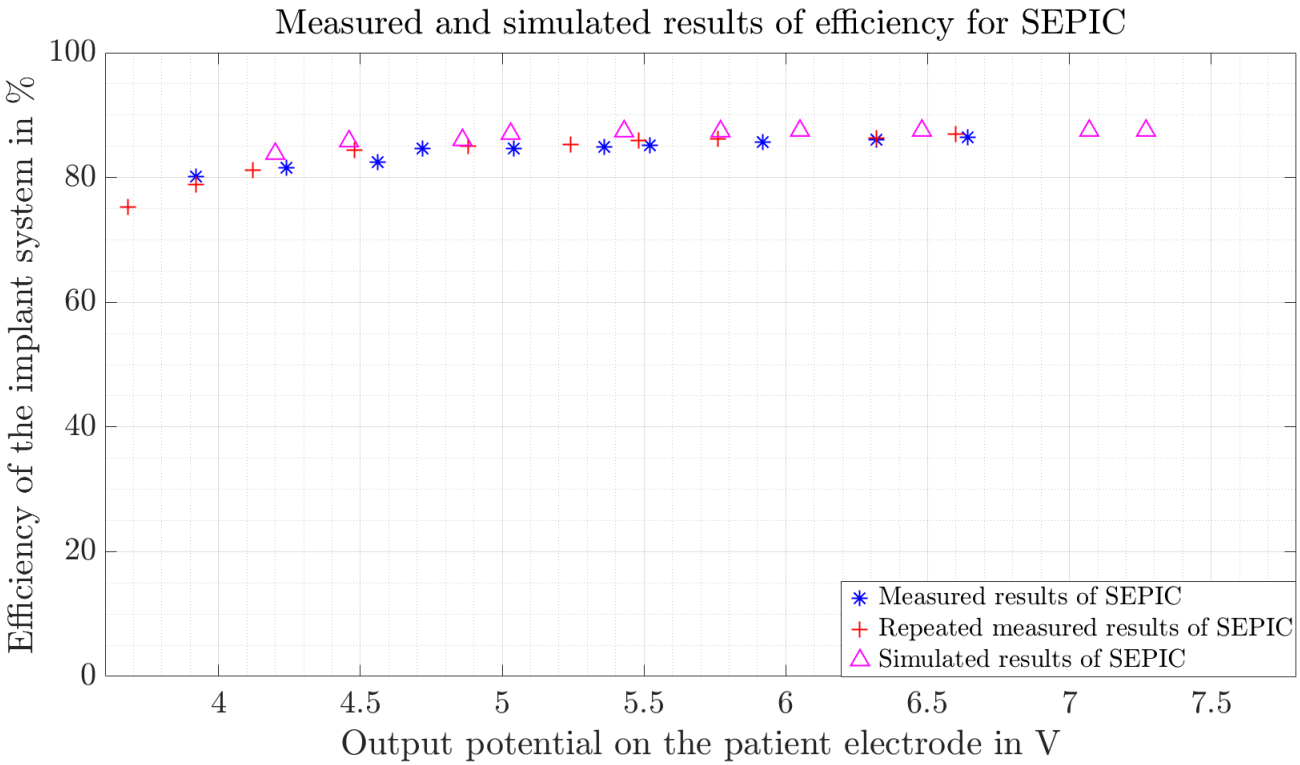

Fig. 6. Efficiency plots of initial measurement, repeated measurement and comparing it with simulated measurement.

Table I: Error in SEPIC's each initial and repeated measured results

Simulated Efficiency (%)	Initial Measured Efficiency (%)	Repeated Measured Efficiency (%)	Initial Measurements (% error)	Repeated Measurements (% error)
83.8	80.1	75.2	4.6	10.9
85.8	81.5	78.9	5.2	8.4
86.0	82.5	81.2	4.2	5.8
87.0	84.6	84.4	2.8	3.0
87.4	84.7	85.0	3.1	2.8
87.4	84.9	85.3	2.9	2.4
87.5	85.2	85.9	2.7	1.8
87.5	85.7	86.2	2.0	1.4
87.5	86.1	86.3	1.7	1.4
87.5	86.4	86.9	1.2	0.7

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