Supercapacitor Assisted Low Dropout Regulators (SCALDO) with Reduced Switches: A New Approach to High Efficiency VRM Designs

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***Abstract*- Supercapacitor assisted low dropout (SCALDO) regulator is a new approach to develop high efficiency DC-DC converters with supercapacitors used for energy recovery. One limitation in these topologies is that in some configurations a large number of low-speed switches are required. If the SCALDO technique is adapted to build voltage regulator modules (VRM), it is necessary to reduce number of switches combined with a high current capable LDO. A new topology-variation with less number of switches can be achieved by reconfiguring the original SCALDO and adding an extra LDO to the circuit. The paper presents a summary of some preliminary work, and experimental results for a 2.5V proof of concept-prototype.**

Keywords—VRM, Efficiency, Supercapacitors, Low dropout regulators

I. INTRODUCTION

VRM or processor power module (PPM) is a power supply unit that provides appropriate voltage and current to a processor in a computer system. In high performance computing platforms, processors consume a large amount of power. To power processors in mobile devices, a battery pack is used. In such situations high efficiency VRMs are used where the processor could command these power supplies to vary DC output voltage and achieve the best energy conversion efficiency while providing optimum DC voltage rails required for the processor modules. A consortium of computer manufacturing companies including Hewlett-Packard and Intel have developed recommendations such as Advanced Configuration and Power Interface Specification (ACPI) to encourage implementing innovative and cost effective computer power management systems while highlighting the processing power required for a computer platform [1].

A VRM usually is a step-down converter with several important characteristics:

- High current output capability achieved via parallel operation of multiple step-down converters
- Maintain very-low output voltage tolerance over full ambient temperature range and high current slew rates
- Highly efficient voltage conversion
- Processor commanded fast responding output voltage adjustment capability

For example, according to Intel design guidelines-11.1, in Xeon 5500 platforms, VRMs are required to support 150A peak current at any output voltage ranging from 0.5-1.6V. The specific output voltage is set according to the voltage identification (VID) code provided by the processor. A stringent output voltage tolerance should be maintained within a 30mV band across the full load line [2].

The demand for VRMs is stimulated by the trends of hi-tech end-user applications, such as smartphones, laptops, etc. Many portable products expected to have longer run-time and better end-to-end efficiencies that require multiple DC rails. These products are powered using point of load (POL) techniques where multiple regulator stages will be used. Some of these regulators can be high slew rate capable low dropout (LDO) regulators [3-5].

The SCALDO regulator is a new extra-low frequency topology [6-7] where a supercapacitor (SC) is used as a lossless voltage-dropper. This technique considerably increases the end-to-end efficiency by reducing power dissipation in the series pass-element of a linear regulator such as a LDO [8]. In a typical 12-5V SCALDO configuration, an efficiency multiplication factor of 2 can be achieved by using four low-speed switches with one SC [8, 9]. For example, a conventional 12-5V linear regulator with the best possible end-to-end efficiency of 42% can theoretically be increased to 84%. This is by assuming that the control circuits consume negligible power, and ideal capacitors and switches are available [10, 11]. Allowing secondary losses in the capacitor-ESR and the low-speed switches, previously built prototypes have achieved practical efficiencies over 80% [12]. Publications [12, 13] indicate that efficiency improvement factors of 1.33, 2 or 3 could be achieved for common converter configurations such as 5-3.3V, 12-5V, and 5-1.5V respectively.

In a recent publication [14], the SCALDO technique is compared with well-known charge pump techniques [15, 16], where the significant differences are highlighted. The key

differences between the two techniques are compared in Table I. More details are available in [14].

TABLE I
A COMPARISON SUMMARY OF SWITCHED CAPACITOR CONVERTERS AND THE SCALDO TECHNIQUE [source: 14]

Switched capacitor (charge pump) technique	**SCALDO technique**
Basically a high frequency switching technique for voltage conversion.	A modified version of a linear regulator with an enormous capacitor in series path as a lossless voltage dropper. (capacitor and the switches do not convert the voltage)
Practically used to boost or invert a DC voltage.	Always a step-down configuration
Capacitors used are in the range of few nano-farads to few tens of micro-farads.	Enormously large capacitors are used.
Circuit design starts with an oscillator supplying a fixed switching frequency.	Operating frequency varies with the load current. Switch operation is based on the case of a maximum/ minimum voltage detected across the input of the LDO.
Switching frequency is in the range of 10s to few 100 kHz	Very low frequency (10Hz to few 100Hz) used for capacitor energy recovery and reuse.
Load regulation is not precise and requires a another voltage regulator (linear/low drop out type) for precise output voltage	Load always sees the precise output of a linear/low drop out regulator
In one part of the cycle capacitor comes in parallel to unregulated supply.	Capacitor never comes parallel to the input unregulated supply.
Technique is suitable only for very low load currents	Technique is applicable to very large load currents. (High current capable LDO is required)
Significant dynamic losses in switches.	Negligible dynamic losses in switches.
Theoretically a voltage conversion factor applies to a given configuration	Theoretically an efficiency multiplication factor is defined for a given configuration

New generations of SCs have (i) capacitance values in the range from 0.1F to over 3000F (ii) very low ESR in the range of fractional mΩ to few 100 mΩ (iii) high charging and discharging current capabilities. By using SCs with high current capable LDOs a very high current SCALDO configuration can be developed. Discrete transistors can be used to develop high current LDOs, or IC versions for medium currents.

Section II describes the basic concept of the SCALDO technique and the basis to develop a modified configuration suitable for linear VRM, utilizing lower switch-count based SCALDO configurations. Section III details three possible topologies with reduced switches. A proof of concept circuit and experimental results are discussed in Section IV. Practical issues of presently built reduced-switch SCALDO (RS-SCALDO) prototype and suggestions to address those issues are described in Section V.

II. BASIS FOR REDUCED SWITCH-COUNT BASED SCALDO TECHNIQUE

A: Basic SCALDO technique versus the reduced switch SCALDO

A supercapacitor energy circulation based efficiency improvement was discussed in [6-14]. Fig. 1 indicates the simplest case with four switches of SCALDO configurations applicable to a 12-5V converter. A pre-charged SC is connected between a LDO regulator and the unregulated power supply. SC is charged by the input current of LDO until it reaches the minimum input voltage $V_{in,min}$ required for regulation. Then the excess charge in SC is released to the LDO and the circuit returns to series configuration.

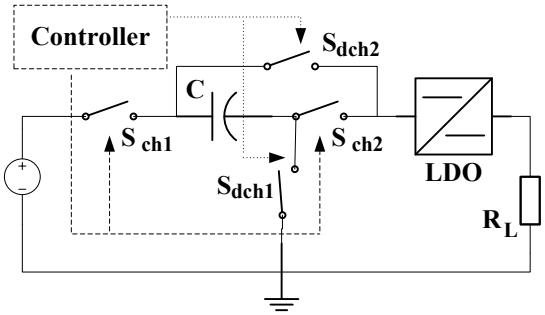


Fig. 1. Basic SCALDO topology with four switches applicable to a case such as a 12 -5V converter

The technique can be generalized for two different configurations where several SCs are placed in series and then discharged in parallel to the LDO, or vice versa, where overall efficiency can be expressed as:

$$\eta = (1+k)\frac{V_{reg}}{V_s} \tag{1}$$

(1+*k*), the efficiency improvement factor depends on the number of SCs *n*, needed for a given converter configuration. For a case in Fig. 1 regulator, using a single SC, where k=1, the end-to-end efficiency will be given as;

$$\eta = 2\frac{V_{reg}}{V_s} \tag{2}$$

More details are in [8-14].

With V_{reg} and V_s where the regulated output voltage and unregulated DC supply voltage respectively, k can be defined for following two different scenarios.

$k=n$ for a case where $V_s>(1+n)V_{in,min}$ (3a)

and

$k=1/n$ for $V_s>(1+1/n)V_{in,min}$ (3b)

By suitably configuring the SC array and the input-output voltage combination, a very high theoretical end-to-end efficiency can be achieved. However, depending on the input-output voltage combination, number of switches can be large (i.e. $3n$ +1). This may be considered as a negative

aspect, when a high current SCALDO version is to be developed.

In order to reduce the number of switches in a basic SCALDO configuration, following strategy was considered:

- Develop a LDO with a suitable control circuit, where the series pass-element in a LDO stage driven into an open circuit while the other LDO is configured to regulate the output voltage
- Suitably replace additional switches by utilizing multiple LDO stages with a common output terminal

This new approach is compared with the basic SCALDO configuration with a case of four switches around one SC. The equivalent four-switch case in Fig. 1 may be achieved by only two switches and two LDOs as in Fig. 2. Since this configuration reduces number of switches in the charging and/or discharging paths, ON resistance (of the power switch) related losses are also reduced. This also allows us to connect two LDOs in parallel.

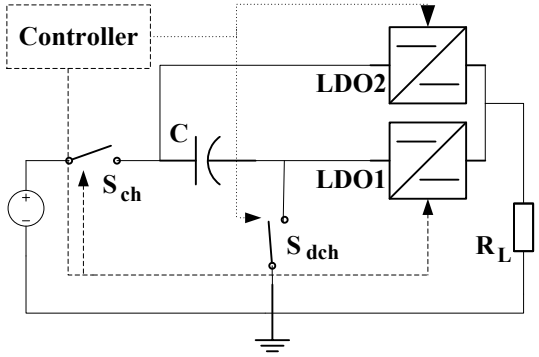


Fig. 2. Reduced-Switch SCALDO topology with two switches

In Fig. 2, LDO1 comes in series with the S_{ch} while S_{dch} is open, charging SC until input voltage for the LDO1 reaches its minimum required value for regulation. Once this condition is reached, LDO1 is driven into a disconnected state, and the two switches are reversed. At this time the LDO2 switches ON, and the SC releases excess energy into LDO2. In effect this modified topology allows us to build a more cost effective circuit configuration and also opens up a possibility to parallel LDO-stages to get a high output current capability. Alternatively current capability of LDO can be increased by adding parallel MOSFETs in the pass-element.

First scenario in (3a) applies to a situation where several SCs are placed in series with the LDO stage, and later discharged into the LDO in parallel, where the general topology and two states of operation is shown in Fig. 3. This configuration applies to a case where input voltage is at least 2 times larger than the minimum input voltage required by LDO to maintain output regulation. As shown in Fig. 3, charging requires 2*n* number of switches to assemble the SCs and LDO, and *n*+1 number of switches to discharge. It is possible to reduce the total number of switches to 2*n* in the Fig. 3 SCALDO configuration by following the above switch reduction strategy in designing a new RS-SCALDO as shown in Fig. 4.

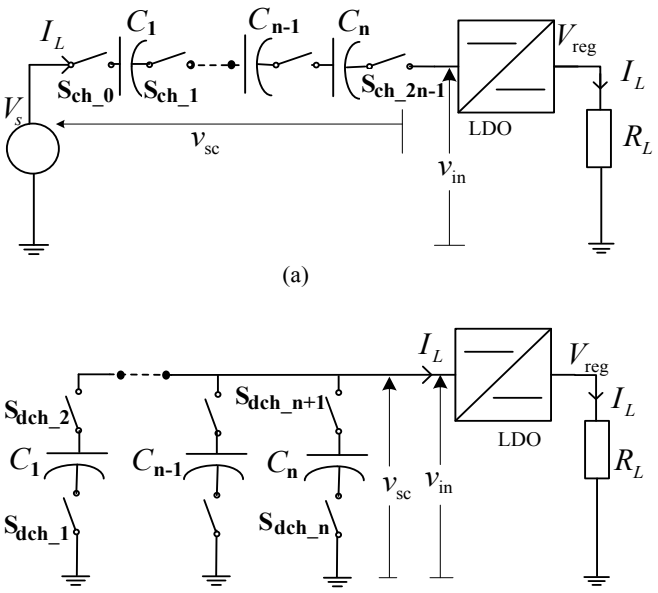


Fig. 3. SCALDO switching configurations for a case where $V_s>(1+n)V_{in,min}$ (a)charging mode and (b) discharging mode

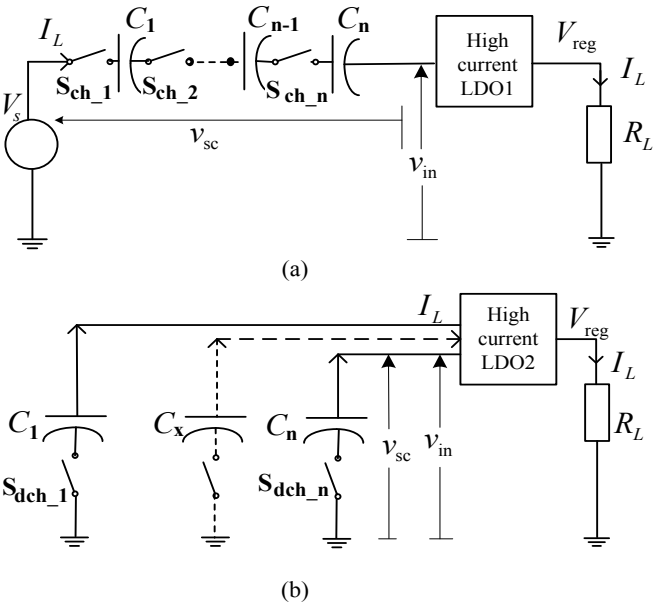


Fig. 4. RS-SCALDO switching configuration for a case where $V_s>(1+n)V_{in,min}$ (a) charging mode and (b) discharging mode

The second scenario in (3b) applies to a case where unregulated input voltage is slightly higher than the minimum input voltage required by the LDO as depicted in Fig. 5. In all figures of SCALDO and RS-SCALDO in this paper, S_{ch} switches are closed and S_{dch} are opened while charging SC; and vice versa in discharging cycle. The RS-SCALDO version in Fig. 6 can reduce *n*+1 number of switches from similar SCALDO of case $V_s>(1+1/n)V_{in,min}$ by following the switch reduction strategy.

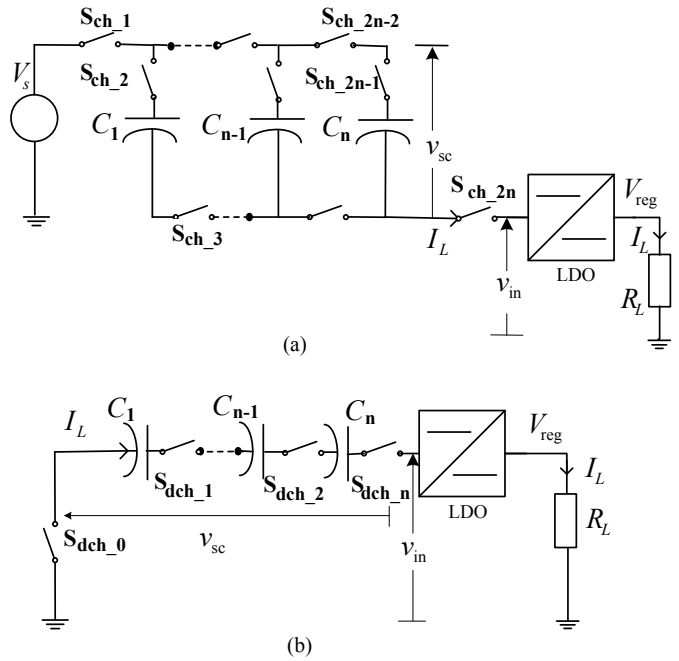


Fig. 5. SCALDO switching configurations for a case where power supply voltage $V_s>(1+1/n)V_{in,min}$ (a) charging mode, and (b) discharging mode

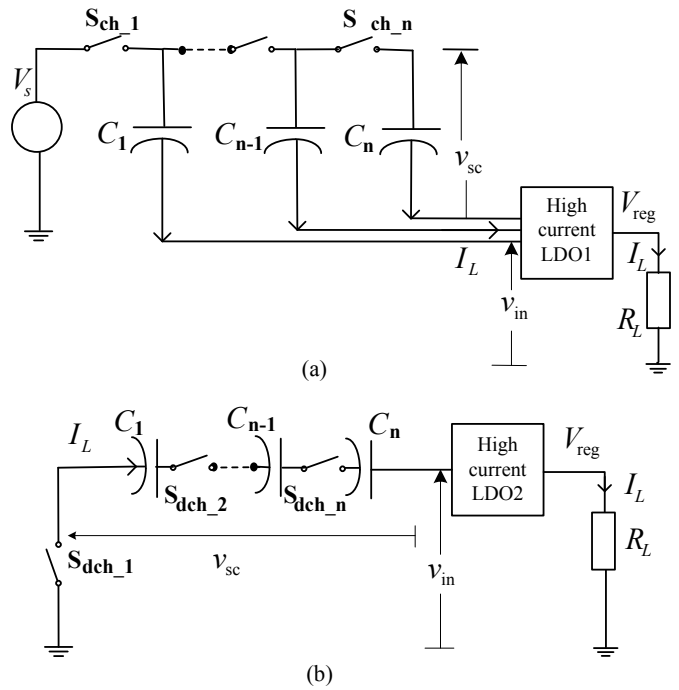


Fig. 6. RS-SCALDO switching configurations for a case where power supply voltage $V_s>(1+1/n)V_{in,min}$ (a) charging mode, and (b) discharging mode

B: Losses

As per (2), which is derived from (1), in the simplest case where only one SC is used states that the basic linear regulator efficiency is getting doubled, encouraging us to use the technique in high current versions. However, losses incurred in a case like this is mainly due to the following:

i. *Equivalent Series Resistance (ESR) related losses in the SC*- This can be minimized by selecting very low ESR type SCs. For SCs of values below 100F, ESR is in the range of 30 to 200 mΩ. But for higher value SCs ESR can be from 0.3 to 10 mΩ.

ii. *Switch losses*- In general, switches implemented with MOSFETs will have their R_{ON} contributing to the losses in a major way. Based on the possible configurations, in both charging and discharging configurations, total resistances in the connection path is a series combination of R_{ON} and the effect of ESR values of each SC (r_s). However compared to the situation of high frequency switch-mode power supplies, this is only a matter of static loss. If a designer selects SCs with very low ESR values, the combined static losses will be at an affordable level to achieve significant end-to-end efficiency.

iii. *Losses due to paralleling two capacitors*: In a SCALDO technique, SC comes in parallel to LDO during the discharging phase. A buffer capacitor C_B may be required at the input of the LDO stage to help in load current continuity during the transition from series to parallel modes. If so, certain losses will be incurred when the two capacitors (with slightly different voltages) come into parallel. However, if C_B is much smaller compared to SC value, the loss will be considerably small.

iv. *Control circuit losses*: By developing a low power circuit we can keep these controller losses at an affordable value so that the ultimate efficiency does not deviate too much from the theoretical efficiency.

In both these SCALDO and RS-SCALDO topologies, above four loss components come in addition to the unavoidable loss in series-pass element in a LDO regulator. However, if the LDO stage can be designed with very low voltage difference between input and the output, this contribution is already accounted in (1). Also it is important to emphasize the fact that commonly incurred dynamic losses in switches and any diode losses etc. are not significant in this technique, since switching occurs at significantly low frequency, usually from fractional hertz to few tens of hertz.

Assuming that the switches and capacitors are identical; ESR and ON resistance related losses in Fig. 3 can be calculated by (4) and (5) respectively in charging and discharging cycles of the SCALDO. Equations (6) and (7) can be used to calculate respective losses in a RS-SCALDO in Fig. 4.

$$I_L^2.\ (2nR_{ON} + nr_s) \tag{4}$$

$$I_L^2.\ [(n+1)R_{ON} + nr_s]/n \tag{5}$$

$$I_L^2.n\ (R_{ON} + r_s) \tag{6}$$

$$I_L^2 . (R_{ON} + r_s) \quad (7)$$

Approximate loss when paralleling two capacitors,

$$\approx 1/2\ C_B\ (V_S - V_B)^2 \quad (8)$$

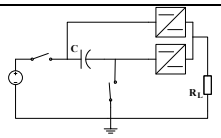
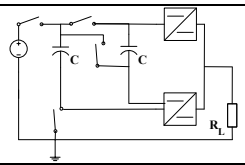
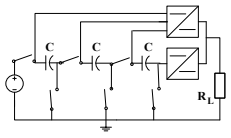
Where, V_B is the buffer capacitor voltage at the LDO input when paralleling.

III. Three Basic SCALDO Technique With Reduced Switches

Given the above summary on significant losses in SCALDO technique (more details in [10,11]), the new reduced-switch approach shown in Fig. 2 is configured to use half the number of switches, and two LDO stages, allowing us to apply in VRM. In previous publications [7, 12, 13], practically useful configurations of SCALDO were discussed. Table II compares RS-SCALDO topologies with three basic cases of SCALDO configurations in terms of switches required.

In practice, both SCALDO and RS-SCALDO techniques require switches without body diodes. In addition, a RS-SCALDO configuration also requires LDOs without body diode (which could exist in the series pass-element). This is due to the fact that in some phases of the operation, body diodes can create a path to prematurely discharge SCs or, the body diode can form a short circuit path to output rail. This complication can be avoided in an IC implementation, since body diode can be removed during the fabrication process. Therefore, in high current VRM implementations with discrete components, we should develop switches and LDOs with this restriction in mind.

TABLE II
Summary of Three Basic Configurations of RE-SCALDO Technique

SCALDO Configuration	RS-SCALDO Topology	No. switches in SCALDO (3n+1)	No. switches in RS-SCALDO (2n)
12-5V		4	2
5-1.5V		7	4
5-3.3V		10	6

*n -number of SCs required [7-13]

IV. Experimental Results

In order to prove the concept of RS-SCALDO configuration applicable to a radically new VRM design approach, a 2.5V, 300mA converter was built to work from an input voltage of 7.6V nominal. Some commonly available ADP1706 LDO ICs from Analog Devices and two series connected CAP-XX SCs (1.8F, 2.75V) were used to build the circuit together with two PVN012A solid state relays from International Rectifier. Additionally two diodes were used at the output end of the LDO as in Fig. 7. That was to avoid the possibility of SC discharging or the load getting grounded via body diode present in LDO shown in Fig. 8. Controller used was a PIC16F684 microcontroller with a multiplex switch at LDO input voltage sensing points.

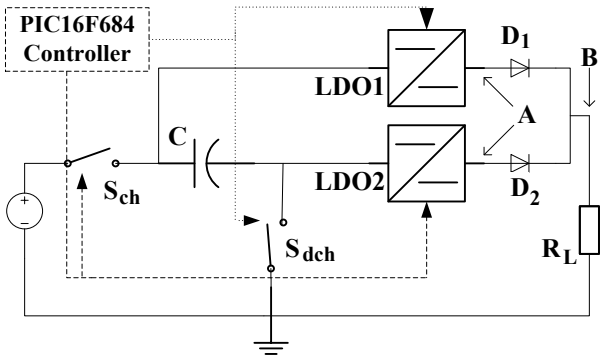


Fig. 7.Simplified diagram of experimental circuit with two diodes to avoid body-diode effect

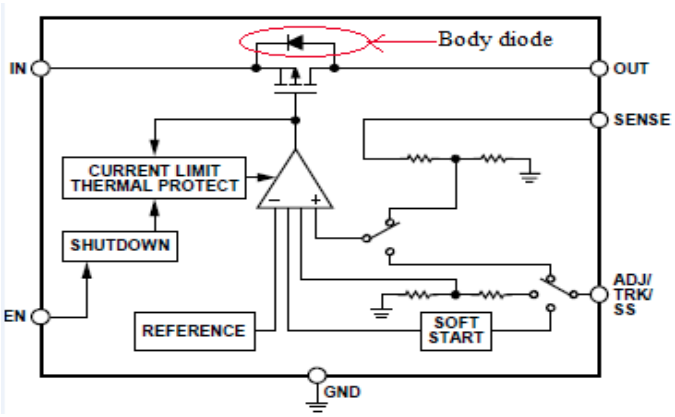


Fig. 8. Internal block diagram of ADP1706 LDO *[source: 17]*

This 7.6-2.5V, 300mA regulator was built to prove the feasibility of new RS-SCALDO technique. A PIC controller commands the two switches and LDOs while monitoring the input voltage at each LDO input. The monitored output at SC, LDO and point B are illustrated by the wave forms in Fig. 9. Graph in Fig. 10 shows the efficiency at LDO output as well as at the load. The results proved that approximately twice the theoretical efficiency of conventional linear regulator could be achieved as expected.

It is important to indicate that in a discrete implementation of this kind as in Fig. 7, the diodes D_1 and D_2 are used simply to avoid body-diode present in series pass element of the LDO ICs used. Those diodes at the output will not be required in an IC implementation or in a discrete version with nMOSFETs of RS-SCALDO as discussed earlier.

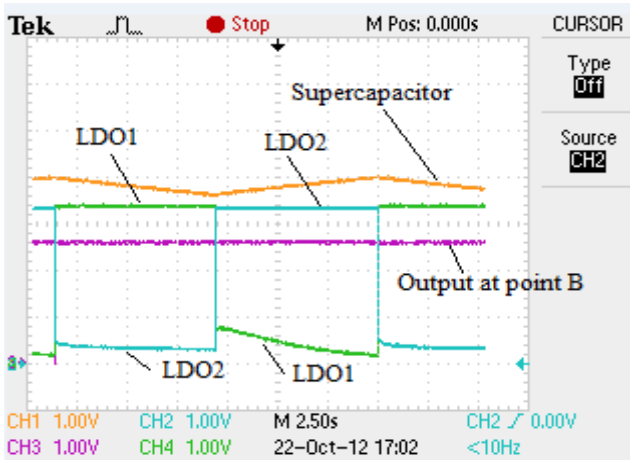


Fig. 9. Waveforms at the output of point A (LDO1, LDO2), SC charging and discharging, output at point B

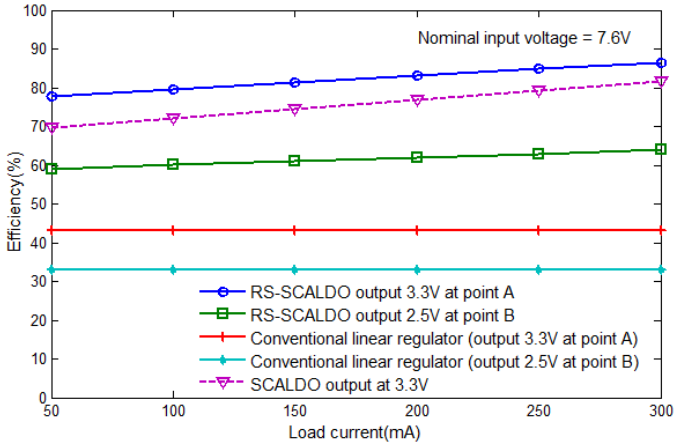


Fig. 10. Load current (mA) vs. efficiency (%) for the RS-SCALDO circuit.

IV. FUTURE WORK

Above experimental details indicate that the RS-SCALDO technique can be further developed into high output current versions suitable for VRMs based on the following approach:

a) Develop suitable linear regulator modules with low -dropout voltage and high current capability.
b) Develop suitable switch configurations to avoid a discharge path created by the body diode
c) In developing the LDO stages required, maintain the need to parallel them at output to achieve high total current.
d) Develop low power control stage, to minimize the overall losses.

CONCLUSION

In this paper a modified version of SCALDO technique which can be used for VRM development is discussed, indicating its validity to develop high current VRM systems. Paper also presents a summary of losses to be considered in the design, in addition to a discussion on the required design approaches for the circuit elements in adopting the patented SCALDO technique in a form of a reduced-switch version. Further work is in progress.

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